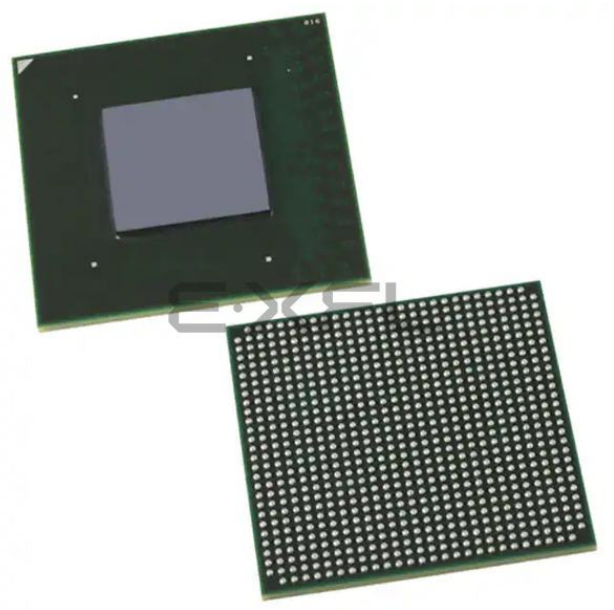
Intel - EP2AGX125EF29C4N Datasheet



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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Obsolete
Number of LABs/CLBs	4964
Number of Logic Elements/Cells	118143
Total RAM Bits	8315904
Number of I/O	372
Number of Gates	-
Voltage - Supply	0.87V ~ 0.93V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	780-BBGA, FCBGA
Supplier Device Package	780-FBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep2agx125ef29c4n

Table 1–2. Absolute Maximum Ratings for Arria II GZ Devices (Part 2 of 2)

Symbol	Description	Minimum	Maximum	Unit
V_{CCA_L}	Supplies transceiver high voltage power (left side)	-0.5	3.75	V
V_{CCA_R}	Supplies transceiver high voltage power (right side)	-0.5	3.75	V
V_{CCHIP_L}	Supplies transceiver HIP digital power (left side)	-0.5	1.35	V
V_{CCR_L}	Supplies receiver power (left side)	-0.5	1.35	V
V_{CCR_R}	Supplies receiver power (right side)	-0.5	1.35	V
V_{CCT_L}	Supplies transmitter power (left side)	-0.5	1.35	V
V_{CCT_R}	Supplies transmitter power (right side)	-0.5	1.35	V
V_{CCL_GXBLn} *(1)*	Supplies power to the transceiver PMA TX, PMA RX, and clocking (left side)	-0.5	1.35	V
V_{CCL_GXBRn} *(1)*	Supplies power to the transceiver PMA TX, PMA RX, and clocking (right side)	-0.5	1.35	V
V_{CCH_GXBLn} *(1)*	Supplies power to the transceiver PMA output (TX) buffer (left side)	-0.5	1.8	V
V_{CCH_GXBRn} *(1)*	Supplies power to the transceiver PMA output (TX) buffer (right side)	-0.5	1.8	V
T_J	Operating junction temperature	-55	125	°C
T_{STG}	Storage temperature (no bias)	-65	150	°C

Note to Table 1–2:

(1) n = 0, 1, or 2.

Maximum Allowed Overshoot and Undershoot Voltage

During transitions, input signals may overshoot to the voltage shown in Table 1–3 and undershoot to –2.0 V for magnitude of currents less than 100 mA and periods shorter than 20 ns.

Table 1–3 lists the Arria II GX and GZ maximum allowed input overshoot voltage and the duration of the overshoot voltage as a percentage over the device lifetime. The maximum allowed overshoot duration is specified as a percentage of high-time over the lifetime of the device. A DC signal is equivalent to 100% duty cycle. For example, a signal that overshoots to 4.3 V can only be at 4.3 V for 5.41% over the lifetime of the device; for a device lifetime of 10 years, this amounts to 5.41/10ths of a year.

Table 1–17 lists the pin capacitance for Arria II GZ devices.

Table 1–17. Pin Capacitance for Arria II GZ Devices

Symbol	Description	Typical	Unit
C_{IOTB}	Input capacitance on the top and bottom I/O pins	4	pF
C_{IOLR}	Input capacitance on the left and right I/O pins	4	pF
C_{CLKTB}	Input capacitance on the top and bottom non-dedicated clock input pins	4	pF
C_{CLKLR}	Input capacitance on the left and right non-dedicated clock input pins	4	pF
C_{OUTFB}	Input capacitance on the dual-purpose clock output and feedback pins	5	pF
C_{CLK1}, C_{CLK3}, C_{CLK8}, and C_{CLK10}	Input capacitance for dedicated clock input pins	2	pF

Internal Weak Pull-Up and Weak Pull-Down Resistors

Table 1–18 lists the weak pull-up and pull-down resistor values for Arria II GX devices.

Table 1–18. Internal Weak Pull-up and Weak Pull-Down Resistors for Arria II GX Devices *(Note 1)*

Symbol	Description	Conditions	Min	Typ	Max	Unit
R_{PU}	Value of I/O pin pull-up resistor before and during configuration, as well as user mode if the programmable pull-up resistor option is enabled.	V_{CCIO} = 3.3 V ±5% *(2)*	7	25	41	kΩ
		V_{CCIO} = 3.0 V ±5% *(2)*	7	28	47	kΩ
		V_{CCIO} = 2.5 V ±5% *(2)*	8	35	61	kΩ
		V_{CCIO} = 1.8 V ±5% *(2)*	10	57	108	kΩ
		V_{CCIO} = 1.5 V ±5% *(2)*	13	82	163	kΩ
		V_{CCIO} = 1.2 V ±5% *(2)*	19	143	351	kΩ
R_{PD}	Value of TCK pin pull-down resistor	V_{CCIO} = 3.3 V ±5%	6	19	29	kΩ
		V_{CCIO} = 3.0 V ±5%	6	22	32	kΩ
		V_{CCIO} = 2.5 V ±5%	6	25	42	kΩ
		V_{CCIO} = 1.8 V ±5%	7	35	70	kΩ
		V_{CCIO} = 1.5 V ±5%	8	50	112	kΩ

Notes to Table 1–18:

(1) All I/O pins have an option to enable weak pull-up except configuration, test, and JTAG pins. The weak pull-down feature is only available for JTAG TCK.

(2) Pin pull-up resistance values may be lower if an external source drives the pin higher than V_{CCIO}.

Table 1–23. Single-Ended I/O Standards for Arria II GZ Devices (Part 2 of 2)

I/O Standard	V_{CCIO} (V)			V_{IL} (V)		V_{IH} (V)		V_{OL} (V)	V_{OH} (V)	I_{OL} (mA)	I_{OH} (mA)
	Min	Typ	Max	Min	Max	Min	Max	Max	Min		
1.2 V	1.14	1.2	1.26	-0.3	0.35 × V_{CCIO}	0.65 × V_{CCIO}	V_{CCIO} + 0.3	0.25 × V_{CCIO}	0.75 × V_{CCIO}	2	-2
3.0-V PCI	2.85	3	3.15	—	0.3 × V_{CCIO}	0.5 × V_{CCIO}	3.6	0.1 × V_{CCIO}	0.9 × V_{CCIO}	1.5	-0.5
3.0-V PCI-X	2.85	3	3.15	—	0.35 × V_{CCIO}	0.5 × V_{CCIO}	—	0.1 × V_{CCIO}	0.9 × V_{CCIO}	1.5	-0.5

Table 1–24 lists the single-ended SSTL and HSTL I/O reference voltage specifications for Arria II GX devices.

Table 1–24. Single-Ended SSTL and HSTL I/O Reference Voltage Specifications for Arria II GX Devices

I/O Standard	V_{CCIO} (V)			V_{REF} (V)			V_{TT} (V)		
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max
SSTL-2 Class I, II	2.375	2.5	2.625	0.49 × V_{CCIO}	0.5 × V_{CCIO}	0.51 × V_{CCIO}	V_{REF} - 0.04	V_{REF}	V_{REF} + 0.04
SSTL-18 Class I, II	1.71	1.8	1.89	0.833	0.9	0.969	V_{REF} - 0.04	V_{REF}	V_{REF} + 0.04
SSTL-15 Class I, II	1.425	1.5	1.575	0.47 × V_{CCIO}	0.5 × V_{CCIO}	0.53 × V_{CCIO}	0.47 × V_{CCIO}	0.5 × V_{CCIO}	0.53 × V_{CCIO}
HSTL-18 Class I, II	1.71	1.8	1.89	0.85	0.9	0.95	0.85	0.9	0.95
HSTL-15 Class I, II	1.425	1.5	1.575	0.71	0.75	0.79	0.71	0.75	0.79
HSTL-12 Class I, II	1.14	1.2	1.26	0.48 × V_{CCIO}	0.5 × V_{CCIO}	0.52 × V_{CCIO}	—	V_{CCIO}/2	—

Table 1–25 lists the single-ended SSTL and HSTL I/O reference voltage specifications for Arria II GZ devices.

Table 1–25. Single-Ended SSTL and HSTL I/O Reference Voltage Specifications for Arria II GZ Devices

I/O Standard	V_{CCIO} (V)			V_{REF} (V)			V_{TT} (V)		
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max
SSTL-2 Class I, II	2.375	2.5	2.625	0.49 × V_{CCIO}	0.5 × V_{CCIO}	0.51 × V_{CCIO}	V_{REF} - 0.04	V_{REF}	V_{REF} + 0.04
SSTL-18 Class I, II	1.71	1.8	1.89	0.833	0.9	0.969	V_{REF} - 0.04	V_{REF}	V_{REF} + 0.04
SSTL-15 Class I, II	1.425	1.5	1.575	0.47 × V_{CCIO}	0.5 × V_{CCIO}	0.53 × V_{CCIO}	0.47 × V_{CCIO}	V_{REF}	0.53 × V_{CCIO}
HSTL-18 Class I, II	1.71	1.8	1.89	0.85	0.9	0.95	—	V_{CCIO}/2	—
HSTL-15 Class I, II	1.425	1.5	1.575	0.68	0.75	0.9	—	V_{CCIO}/2	—
HSTL-12 Class I, II	1.14	1.2	1.26	0.47 × V_{CCIO}	0.5 × V_{CCIO}	0.53 × V_{CCIO}	—	V_{CCIO}/2	—

Table 1–30 lists the HSTL I/O standards for Arria II GX devices.

Table 1–30. Differential HSTL I/O Standards for Arria II GX Devices

I/O Standard	V_{CCIO} (V)			$V_{DIF(DC)}$ (V)		$V_{X(AC)}$ (V)			$V_{CM(DC)}$ (V)			$V_{DIF(AC)}$ (V)	
	Min	Typ	Max	Min	Max	Min	Typ	Max	Min	Typ	Max	Min	Max
HSTL-18 Class I	1.71	1.8	1.89	0.2	—	0.85	—	0.95	0.88	—	0.95	0.4	—
HSTL-15 Class I, II	1.425	1.5	1.575	0.2	—	0.71	—	0.79	0.71	—	0.79	0.4	—
HSTL-12 Class I, II	1.14	1.2	1.26	0.16	—	—	0.5 × V_{CCIO}	—	0.48 × V_{CCIO}	0.5 × V_{CCIO}	0.52 × V_{CCIO}	0.3	—

Table 1–31 lists the HSTL I/O standards for Arria II GZ devices.

Table 1–31. Differential HSTL I/O Standards for Arria II GZ Devices

I/O Standard	V_{CCIO} (V)			$V_{DIF(DC)}$ (V)		$V_{X(AC)}$ (V)			$V_{CM(DC)}$ (V)			$V_{DIF(AC)}$ (V)	
	Min	Typ	Max	Min	Max	Min	Typ	Max	Min	Typ	Max	Min	Max
HSTL-18 Class I	1.71	1.8	1.89	0.2	—	0.78	—	1.12	0.78	—	1.12	0.4	—
HSTL-15 Class I, II	1.425	1.5	1.575	0.2	—	0.68	—	0.9	0.68	—	0.9	0.4	—
HSTL-12 Class I, II	1.14	1.2	1.26	0.16	V_{CCIO} + 0.3	—	0.5 × V_{CCIO}	—	0.4 × V_{CCIO}	0.5 × V_{CCIO}	0.6 × V_{CCIO}	0.3	V_{CCIO} + 0.48

Table 1–32 lists the differential I/O standard specifications for Arria II GX devices.

Table 1–32. Differential I/O Standard Specifications for Arria II GX Devices *(Note 1)*

I/O Standard	V_{CCIO} (V)			V_{ID} (mV)			V_{ICM} (V) *(2)*		V_{OD} (V) *(3)*			V_{OCM} (V)		
	Min	Typ	Max	Min	Cond.	Max	Min	Max	Min	Typ	Max	Min	Typ	Max
2.5 V LVDS	2.375	2.5	2.625	100	V_{CM} = 1.25 V	—	0.05	1.80	0.247	—	0.6	1.125	1.25	1.375
RSDS *(4)*	2.375	2.5	2.625	—	—	—	—	—	0.1	0.2	0.6	0.5	1.2	1.4
Mini-LVDS *(4)*	2.375	2.5	2.625	—	—	—	—	—	0.25	—	0.6	1	1.2	1.4
LVPECL *(5)*	2.375	2.5	2.625	300	—	—	0.6	1.8	—	—	—	—	—	—
BLVDS *(6)*	2.375	2.5	2.625	100	—	—	—	—	—	—	—	—	—	—

Notes to Table 1–32:

(1) The 1.5 V PCML transceiver I/O standard specifications are described in "Transceiver Performance Specifications" on page 1–21.

(2) V_{IN} range: 0 <= V_{IN} <= 1.85 V.

(3) R_L range: 90 <= RL <= 110 Ω.

(4) The RSDS and mini-LVDS I/O standards are only supported for differential outputs.

(5) The LVPECL input standard is supported at the dedicated clock input pins (GCLK) only.

(6) There are no fixed V_{ICM}, V_{OD}, and V_{OCM} specifications for BLVDS. These specifications depend on the system topology.

Table 1–33 lists the differential I/O standard specifications for Arria II GZ devices.

Table 1–33. Differential I/O Standard Specifications for Arria II GZ Devices *(Note 1)*

I/O Standard *(2)*	V_{CCIO} (V)			V_{ID} (mV)			$V_{ICM(DC)}$ (V)		V_{OD} (V) *(3)*			V_{OCM} (V) *(3)*		
	Min	Typ	Max	Min	Cond.	Max	Min	Max	Min	Typ	Max	Min	Typ	Max
2.5 V LVDS (HIO)	2.375	2.5	2.625	100	V_{CM} = 1.25 V	—	0.05	1.8	0.247	—	0.6	1.125	1.25	1.375
2.5 V LVDS (VIO)	2.375	2.5	2.625	100	V_{CM} = 1.25 V	—	0.05	1.8	0.247	—	0.6	1	1.25	1.5
RSDS (HIO)	2.375	2.5	2.625	100	V_{CM} = 1.25 V	—	0.3	1.4	0.1	0.2	0.6	0.5	1.2	1.4
RSDS (VIO)	2.375	2.5	2.625	100	V_{CM} = 1.25 V	—	0.3	1.4	0.1	0.2	0.6	0.5	1.2	1.5
Mini-LVDS (HIO)	2.375	2.5	2.625	200	—	600	0.4	1.325	0.25	—	0.6	1	1.2	1.4
Mini-LVDS (VIO)	2.375	2.5	2.625	200	—	600	0.4	1.325	0.25	—	0.6	1	1.2	1.5
LVPECL	2.375	2.5	2.625	300	—	—	0.6	1.8	—	—	—	—	—	—
BLVDS *(4)*	2.375	2.5	2.625	100	—	—	—	—	—	—	—	—	—	—

Notes to Table 1–33:

(1) 1.4-V/1.5-V PCML transceiver I/O standard specifications are described in "Transceiver Performance Specifications" on page 1–21.
(2) Vertical I/O (VIO) is top and bottom I/Os; horizontal I/O (HIO) is left and right I/Os.
(3) R_L range: $90 \leq RL \leq 110\ \Omega$.
(4) There are no fixed V_{ICM}, V_{OD}, and V_{OCM} specifications for BLVDS. These specifications depend on the system topology.

Power Consumption for the Arria II Device Family

Altera offers two ways to estimate power for a design:

- Using the Microsoft Excel-based Early Power Estimator
- Using the Quartus® II PowerPlay Power Analyzer feature

The interactive Microsoft Excel-based Early Power Estimator is typically used prior to designing the FPGA in order to get a magnitude estimate of the device power. The Quartus II PowerPlay Power Analyzer provides better quality estimates based on the specifics of the design after place-and-route is complete. The PowerPlay Power Analyzer can apply a combination of user-entered, simulation-derived, and estimated signal activities which, when combined with detailed circuit models, can yield very accurate power estimates.

For more information about power estimation tools, refer to the *PowerPlay Early Power Estimator User Guide* and the *PowerPlay Power Analysis* chapter in volume 3 of the *Quartus II Handbook*.

Table 1–40. Transceiver Block Jitter Specifications for Arria II GX Devices *(Note 1)* (Part 2 of 10)

Symbol/ Description	Conditions	I3			C4			C5, I5			C6			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Jitter tolerance at 2488.32 Mbps	Jitter frequency = 0.06 KHz Pattern = PRBS15	> 15			> 15			> 15			> 15			UI
	Jitter frequency = 100 KHZ Pattern = PRBS15	> 1.5			> 1.5			> 1.5			> 1.5			UI
	Jitter frequency = 1 MHz Pattern = PRBS15	> 0.15			> 0.15			> 0.15			> 0.15			UI
	Jitter frequency = 10 MHz Pattern = PRBS15	> 0.15			> 0.15			> 0.15			> 0.15			UI
XAUI Transmit Jitter Generation *(3)*														
Total jitter at 3.125 Gbps	Pattern = CJPAT	—	—	0.3	—	—	0.3	—	—	0.3	—	—	0.3	UI
Deterministic jitter at 3.125 Gbps	Pattern = CJPAT	—	—	0.17	—	—	0.17	—	—	0.17	—	—	0.17	UI
XAUI Receiver Jitter Tolerance *(3)*														
Total jitter	—	> 0.65			> 0.65			> 0.65			> 0.65			UI
Deterministic jitter	—	> 0.37			> 0.37			> 0.37			> 0.37			UI
Peak-to-peak jitter	Jitter frequency = 22.1 KHz	> 8.5			> 8.5			> 8.5			> 8.5			UI
Peak-to-peak jitter	Jitter frequency = 1.875 MHz	> 0.1			> 0.1			> 0.1			> 0.1			UI
Peak-to-peak jitter	Jitter frequency = 20 MHz	> 0.1			> 0.1			> 0.1			> 0.1			UI
PCIe Transmit Jitter Generation *(4)*														
Total jitter at 2.5 Gbps (Gen1)	Compliance pattern	—	—	0.25	—	—	0.25	—	—	0.25	—	—	0.25	UI

Table 1–40. Transceiver Block Jitter Specifications for Arria II GX Devices *(Note 1)* (Part 3 of 10)

Symbol/ Description	Conditions	I3			C4			C5, I5			C6			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
PCIe Receiver Jitter Tolerance *(4)*														
Total jitter at 2.5 Gbps (Gen1)	Compliance pattern	> 0.6			> 0.6			> 0.6			> 0.6			UI
PCIe (Gen 1) Electrical Idle Detect Threshold *(9)*														
VRX-IDLE-DETDIFF (p-p)	Compliance pattern	65	—	175	65	—	175	65	—	175	65	—	175	mV
Serial RapidIO® (SRIO) Transmit Jitter Generation *(5)*														
Deterministic jitter (peak-to-peak)	Data Rate = 1.25, 2.5, 3.125 Gbps Pattern = CJPAT	—	—	0.17	—	—	0.17	—	—	0.17	—	—	0.17	UI
Total jitter (peak-to-peak)	Data Rate = 1.25, 2.5, 3.125 Gbps Pattern = CJPAT	—	—	0.35	—	—	0.35	—	—	0.35	—	—	0.35	UI
SRIO Receiver Jitter Tolerance *(5)*														
Deterministic jitter tolerance (peak-to-peak)	Data Rate = 1.25, 2.5, 3.125 Gbps Pattern = CJPAT	> 0.37			> 0.37			> 0.37			> 0.37			UI
Combined deterministic and random jitter tolerance (peak-to-peak)	Data Rate = 1.25, 2.5, 3.125 Gbps Pattern = CJPAT	> 0.55			> 0.55			> 0.55			> 0.55			UI
Sinusoidal jitter tolerance (peak-to-peak)	Jitter frequency = 22.1 KHz Data rate = 1.25, 2.5, 3.125 Gbps Pattern = CJPAT	> 8.5			> 8.5			> 8.5			> 8.5			UI
	Jitter frequency = 1.875 MHz Data rate = 1.25, 2.5, 3.125 Gbps Pattern = CJPAT	> 0.1			> 0.1			> 0.1			> 0.1			UI
	Jitter frequency = 20 MHz Data rate = 1.25, 2.5, 3.125 Gbps Pattern = CJPAT	> 0.1			> 0.1			> 0.1			> 0.1			UI
GIGE Transmit Jitter Generation *(6)*														
Deterministic jitter (peak-to-peak)	Pattern = CRPAT	—	—	0.14	—	—	0.14	—	—	0.14	—	—	0.14	UI

Table 1–41. Transceiver Block Jitter Specifications for Arria II GZ Devices *(Note 1)*, *(2)* (Part 4 of 7)

Symbol/ Description	Conditions	–C3 and –I3			–C4 and –I4			Unit
		Min	Typ	Max	Min	Typ	Max	
GIGE Receiver Jitter Tolerance *(11)*								
Deterministic jitter tolerance (peak-to-peak)	Pattern = CJPAT	> 0.4			> 0.4			UI
Combined deterministic and random jitter tolerance (peak-to-peak)	Pattern = CJPAT	> 0.66			> 0.66			UI
HiGig Transmit Jitter Generation								
Deterministic jitter (peak-to-peak)	Data rate = 3.75 Gbps Pattern = CJPAT	—	—	0.17	—	—	—	UI
Total jitter (peak-to-peak)	Data rate = 3.75 Gbps Pattern = CJPAT	—	—	0.35	—	—	—	UI
HiGig Receiver Jitter Tolerance								
Deterministic jitter tolerance (peak-to-peak)	Data rate = 3.75 Gbps Pattern = CJPAT	> 0.37			—	—	—	UI
Combined deterministic and random jitter tolerance (peak-to-peak)	Data rate = 3.75 Gbps Pattern = CJPAT	> 0.65			—	—	—	UI
Sinusoidal jitter tolerance (peak-to-peak)	Jitter frequency = 22.1 KHz Data rate = 3.75 Gbps Pattern = CJPAT	> 8.5			—	—	—	UI
	Jitter frequency = 22.1 KHz Data rate = 3.75 Gbps Pattern = CJPAT	> 0.1			—	—	—	UI
	Jitter frequency = 22.1 KHz Data rate = 3.75 Gbps Pattern = CJPAT	> 0.1			—	—	—	UI
(OIF) CEI Transmitter Jitter Generation								
Total jitter (peak-to-peak)	Data rate = 6.375 Gbps Pattern = PRBS15 BER = 10^{-12}	—	—	0.3	—	—	0.3	UI
(OIF) CEI Receiver Jitter Tolerance								
Deterministic jitter tolerance (peak-to-peak)	Data rate = 6.375 Gbps Pattern = PRBS31 BER = 10^{-12}	> 0.675			—	—	—	UI
Combined deterministic and random jitter tolerance (peak-to-peak)	Data rate = 6.375 Gbps Pattern = PRBS31 BER = 10^{-12}	> 0.988			—	—	—	UI

Table 1–41. Transceiver Block Jitter Specifications for Arria II GZ Devices *(Note 1)*, *(2)* **(Part 6 of 7)**

Symbol/ Description	Conditions	–C3 and –I3			–C4 and –I4			Unit
		Min	Typ	Max	Min	Typ	Max	
Deterministic jitter at 3.0 Gbps (G2)	Pattern = CJPAT	—	—	0.35	—	—	0.35	UI
Total jitter at 6.0 Gbps (G3)	Pattern = CJPAT	—	—	0.25	—	—	0.25	UI
Random jitter at 6.0 Gbps (G3)	Pattern = CJPAT	—	—	0.15	—	—	0.15	UI
SAS Receiver Jitter Tolerance *(13)*								
Total jitter tolerance at 1.5 Gbps (G1)	Pattern = CJPAT	—	—	0.65	—	—	0.65	UI
Deterministic jitter tolerance at 1.5 Gbps (G1)	Pattern = CJPAT	—	—	0.35	—	—	0.35	UI
Sinusoidal jitter tolerance at 1.5 Gbps (G1)	Jitter frequency = 900 KHz to 5 MHz Pattern = CJTPAT BER = 1E-12	> 0.1			> 0.1			UI
CPRI Transmit Jitter Generation *(14)*								
Total jitter	E.6.HV, E.12.HV Pattern = CJPAT	—	—	0.279	—	—	0.279	UI
	E.6.LV, E.12.LV, E.24.LV, E.30.LV Pattern = CJPAT	—	—	0.35	—	—	0.35	UI
Deterministic jitter	E.6.HV, E.12.HV Pattern = CJPAT	—	—	0.14	—	—	0.14	UI
	E.6.LV, E.12.LV, E.24.LV, E.30.LV Pattern = CJPAT	—	—	0.17	—	—	0.17	UI
CPRI Receiver Jitter Tolerance *(14)*								
Total jitter tolerance	E.6.HV, E.12.HV Pattern = CJPAT	> 0.66			> 0.66			UI
Deterministic jitter tolerance	E.6.HV, E.12.HV Pattern = CJPAT	> 0.4			> 0.4			UI
Total jitter tolerance	E.6.LV, E.12.LV, E.24.LV, E.30.LV Pattern = CJPAT	> 0.65			> 0.65			UI
Deterministic jitter tolerance	E.6.LV, E.12.LV, E.24.LV, E.30.LV Pattern = CJPAT	> 0.37			> 0.37			UI
Combined deterministic and random jitter tolerance	E.6.LV, E.12.LV, E.24.LV, E.30.LV Pattern = CJPAT	> 0.55			> 0.55			UI
OBSAI Transmit Jitter Generation *(15)*								
Total jitter at 768 Mbps, 1536 Mbps, and 3072 Mbps	REFCLK = 153.6 MHz Pattern CJPAT	—	—	0.35	—	—	0.35	UI
Deterministic jitter at 768 MBps, 1536 Mbps, and 3072 Mbps	REFCLK = 153.6 MHz Pattern CJPAT	—	—	0.17	—	—	0.17	UI

Core Performance Specifications for the Arria II Device Family

This section describes the clock tree, phase-locked loop (PLL), digital signal processing (DSP), embedded memory, configuration, and JTAG specifications for Arria II GX and GZ devices.

Clock Tree Specifications

Table 1–42 lists the clock tree specifications for Arria II GX devices.

Table 1–42. Clock Tree Performance for Arria II GX Devices

Clock Network	Performance			Unit
	I3, C4	C5,I5	C6	
GCLK and RCLK	500	500	400	MHz
PCLK	420	350	280	MHz

Table 1–43 lists the clock tree specifications for Arria II GZ devices.

Table 1–43. Clock Tree Performance for Arria II GZ Devices

Clock Network	Performance		Unit
	–C3 and –I3	–C4 and –I4	
GCLK and RCLK	700	500	MHz
PCLK	500	450	MHz

PLL Specifications

Table 1–44 lists the PLL specifications for Arria II GX devices.

Table 1–44. PLL Specifications for Arria II GX Devices (Part 1 of 3)

Symbol	Description	Min	Typ	Max	Unit
f_{IN}	Input clock frequency (from clock input pins residing in right/top/bottom banks) (–4 Speed Grade)	5	—	670 *(1)*	MHz
	Input clock frequency (from clock input pins residing in right/top/bottom banks) (–5 Speed Grade)	5	—	622 *(1)*	MHz
	Input clock frequency (from clock input pins residing in right/top/bottom banks) (–6 Speed Grade)	5	—	500 *(1)*	MHz
f_{INPFD}	Input frequency to the PFD	5	—	325	MHz
f_{VCO}	PLL VCO operating Range *(2)*	600	—	1,400	MHz
f_{INDUTY}	Input clock duty cycle	40	—	60	%
$f_{EINDUTY}$	External feedback clock input duty cycle	40	—	60	%
t_{INCCJ} *(3)*, *(4)*	Input clock cycle-to-cycle jitter (Frequency ≥ 100 MHz)	—	—	0.15	UI (p–p)
	Input clock cycle-to-cycle jitter (Frequency ≤ 100 MHz)	—	—	±750	ps (p–p)

Table 1–45. PLL Specifications for Arria II GZ Devices (Part 2 of 2)

Symbol	Parameter	Min	Typ	Max	Unit
t_{DLOCK}	Time required to lock dynamically (after switchover or reconfiguring any non-post-scale counters/delays)	—	—	1	ms
f_{CLBW}	PLL closed-loop low bandwidth	—	0.3	—	MHz
	PLL closed-loop medium bandwidth	—	1.5	—	MHz
	PLL closed-loop high bandwidth *(7)*	—	4	—	MHz
t_{PLL_PSERR}	Accuracy of PLL phase shift	—	—	±50	ps
t_{ARESET}	Minimum pulse width on the `areset` signal	10	—	—	ns
t_{INCCJ} *(3)*, *(4)*	Input clock cycle to cycle jitter ($F_{REF} \geq 100$ MHz)	—	—	0.15	UI (p-p)
	Input clock cycle to cycle jitter ($F_{REF} < 100$ MHz)	—	—	±750	ps (p-p)
t_{OUTPJ_DC} *(5)*	Period Jitter for dedicated clock output ($F_{OUT} \geq 100$ MHz)	—	—	175	ps (p-p)
	Period Jitter for dedicated clock output ($F_{OUT} < 100$ MHz)	—	—	17.5	mUI (p-p)
t_{OUTCCJ_DC} *(5)*	Cycle to Cycle Jitter for dedicated clock output ($F_{OUT} \geq 100$ MHz)	—	—	175	ps (p-p)
	Cycle to Cycle Jitter for dedicated clock output ($F_{OUT} < 100$ MHz)	—	—	17.5	mUI (p-p)
t_{OUTPJ_IO} *(5)*, *(8)*	Period Jitter for clock output on regular I/O ($F_{OUT} \geq 100$ MHz)	—	—	600	ps (p-p)
	Period Jitter for clock output on regular I/O ($F_{OUT} < 100$ MHz)	—	—	60	mUI (p-p)
t_{OUTCCJ_IO} *(5)*, *(8)*	Cycle to Cycle Jitter for clock output on regular I/O ($F_{OUT} \geq 100$ MHz)	—	—	600	ps (p-p)
	Cycle to Cycle Jitter for clock output on regular I/O ($F_{OUT} < 100$ MHz)	—	—	60	mUI (p-p)
$t_{CASC\_OUTPJ\_DC}$ *(5)*, *(6)*	Period Jitter for dedicated clock output in cascaded PLLs ($F_{OUT} \geq 100$MHz)	—	—	250	ps (p-p)
	Period Jitter for dedicated clock output in cascaded PLLs ($F_{OUT} < 100$MHz)	—	—	25	mUI (p-p)
f_{DRIFT}	Frequency drift after PFDENA is disabled for duration of 100 us	—	—	±10	%

Notes to Table 1–45:

(1) This specification is limited in the Quartus II software by the I/O maximum frequency. The maximum I/O frequency is different for each I/O standard.

(2) This specification is limited by the lower of the two: I/O F_{MAX} or F_{OUT} of the PLL.

(3) A high input jitter directly affects the PLL output jitter. To have low PLL output clock jitter, you must provide a clean clock source that is less than 120 ps.

(4) F_{REF} is fIN/N when N = 1.

(5) Peak-to-peak jitter with a probability level of 10^{-12} (14 sigma, 99.99999999974404% confidence level). The output jitter specification applies to the intrinsic jitter of the PLL, when an input jitter of 30 ps is applied. The external memory interface clock output jitter specifications use a different measurement method and are available in Table 1–64 on page 1–71.

(6) The cascaded PLL specification is only applicable with the following condition:
a. Upstream PLL: 0.59 Mhz ≤ Upstream PLL BW < 1 MHz
b. Downstream PLL: Downstream PLL BW > 2 MHz

(7) High bandwidth PLL settings are not supported in external feedback mode.

(8) External memory interface clock output jitter specifications use a different measurement method, which is available in Table 1–63 on page 1–71.

Table 1–47. DSP Block Performance Specifications for Arria II GZ Devices *(Note 1)* (Part 2 of 2)

Mode	Resources Used	Performance		Unit
	Number of Multipliers	–3	–4	
Double mode	1	440	380	MHz

Notes to Table 1–47:

(1) Maximum is for fully pipelined block with **Round** and **Saturation** disabled.

(2) Maximum for loopback input registers disabled, **Round** and **Saturation** disabled, and pipeline and output registers enabled.

Embedded Memory Block Specifications

Table 1–48 lists the embedded memory block specifications for Arria II GX devices.

Table 1–48. Embedded Memory Block Performance Specifications for Arria II GX Devices

Memory	Mode	Resources Used		Performance				Unit
		ALUTs	Embedded Memory	I3	C4	C5,I5	C6	
Memory Logic Array Block (MLAB)	Single port 64 × 10	0	1	450	500	450	378	MHz
	Simple dual-port 32 × 20 single clock	0	1	270	500	450	378	MHz
	Simple dual-port 64 × 10 single clock	0	1	428	500	450	378	MHz
M9K Block	Single-port 256 × 36	0	1	360	400	360	310	MHz
	Single-port 256 × 36, with the **read-during-write** option set to **Old Data**	0	1	250	280	250	210	MHz
	Simple dual-port 256 × 36 single CLK	0	1	360	400	360	310	MHz
	Single-port 256 × 36 single CLK, with the **read-during-write** option set to **Old Data**	0	1	250	280	250	210	MHz
	True dual port 512 × 18 single CLK	0	1	360	400	360	310	MHz
	True dual-port 512 × 18 single CLK, with the **read-during-write** option set to **Old Data**	0	1	250	280	250	210	MHz
	Min Pulse Width (clock high time)	—	—	900	850	950	1130	ps
	Min Pulse Width (clock low time)	—	—	730	690	770	920	ps

Table 1–49 lists the embedded memory block specifications for Arria II GZ devices.

Table 1–49. Embedded Memory Block Performance Specifications for Arria II GZ Devices *(Note 1)*

Memory	Mode	Resources Used		Performance				Unit
		ALUTs	TriMatrix Memory	C3	I3	C4	I4	
MLAB *(2)*	Single port 64 × 10	0	1	500	500	450	450	MHz
	Simple dual-port 32 × 20	0	1	500	500	450	450	MHz
	Simple dual-port 64 × 10	0	1	500	500	450	450	MHz
	ROM 64 × 10	0	1	500	500	450	450	MHz
	ROM 32 × 20	0	1	500	500	450	450	MHz
M9K Block *(2)*	Single-port 256 × 36	0	1	540	540	475	475	MHz
	Simple dual-port 256 × 36	0	1	490	490	420	420	MHz
	Simple dual-port 256 × 36, with the read-during-write option set to **Old Data**	0	1	340	340	300	300	MHz
	True dual port 512 × 18	0	1	430	430	370	370	MHz
	True dual-port 512 × 18, with the read-during-write option set to **Old Data**	0	1	335	335	290	290	MHz
	ROM 1 Port	0	1	540	540	475	475	MHz
	ROM 2 Port	0	1	540	540	475	475	MHz
	Min Pulse Width (clock high time)	—	—	800	800	850	850	ps
	Min Pulse Width (clock low time)	—	—	625	625	690	690	ps
M144K Block *(2)*	Single-port 2K × 72	0	1	440	400	380	350	MHz
	Simple dual-port 2K × 72	0	1	435	375	385	325	MHz
	Simple dual-port 2K × 72, with the read-during-write option set to **Old Data**	0	1	240	225	205	200	MHz
	Simple dual-port 2K × 64 (with ECC)	0	1	300	295	255	250	MHz
	True dual-port 4K × 36	0	1	375	350	330	310	MHz
	True dual-port 4K × 36, with the read-during-write option set to **Old Data**	0	1	230	225	205	200	MHz
	ROM 1 Port	0	1	500	450	435	420	MHz
	ROM 2 Port	0	1	465	425	400	400	MHz
	Min Pulse Width (clock high time)	—	—	755	860	860	950	ps
	Min Pulse Width (clock low time)	—	—	625	690	690	690	ps

Notes to Table 1–48:

(1) To achieve the maximum memory block performance, use a memory block clock that comes through global clock routing from an on-chip PLL set to 50% output duty cycle. Use the Quartus II software to report timing for this and other memory block clocking schemes.

(2) When you use the error detection CRC feature, there is no degradation in F_{MAX}.

Table 1–53. High-Speed I/O Specifications for Arria II GX Devices (Part 3 of 4)

Symbol	Conditions	I3		C4		C5,I5		C6		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{TX_JITTER} *(4)*	True LVDS with dedicated SERDES (data rate 600–1,250 Mbps)	—	175	—	175	—	225	—	300	ps
	True LVDS with dedicated SERDES (data rate < 600 Mbps)	—	0.105	—	0.105	—	0.135	—	0.18	UI
	True LVDS and emulated LVDS_E_3R with logic elements as SERDES (data rate 600 – 945 Mbps)	—	260	—	260	—	300	—	350	ps
	True LVDS and emulated LVDS_E_3R with logic elements as SERDES (data rate < 600 Mbps)	—	0.16	—	0.16	—	0.18	—	0.21	UI
t_{TX_DCD}	True LVDS and emulated LVDS_E_3R	45	55	45	55	45	55	45	55	%
t_{RISE} and t_{FALL}	True LVDS and emulated LVDS_E_3R	—	200	—	200	—	225	—	250	ps
TCCS	True LVDS *(5)*	—	150	—	150	—	175	—	200	ps
	Emulated LVDS_E_3R	—	200	—	200	—	250	—	300	ps
Receiver *(6)*										
True differential I/O standards - $f_{HSDRDPA}$ (data rate)	SERDES factor J = 3 to 10	150	1250	150	1250	150	1050	150	840	Mbps

Figure 1–6 shows the LVDS soft-CDR/DPA sinusoidal jitter tolerance specification for Arria II GZ devices at 1.25 Gbps data rate.

Figure 1–6. LVDS Soft-CDR/DPA Sinusoidal Jitter Tolerance Specification for Arria II GZ Devices at a 1.25 Gbps Data Rate

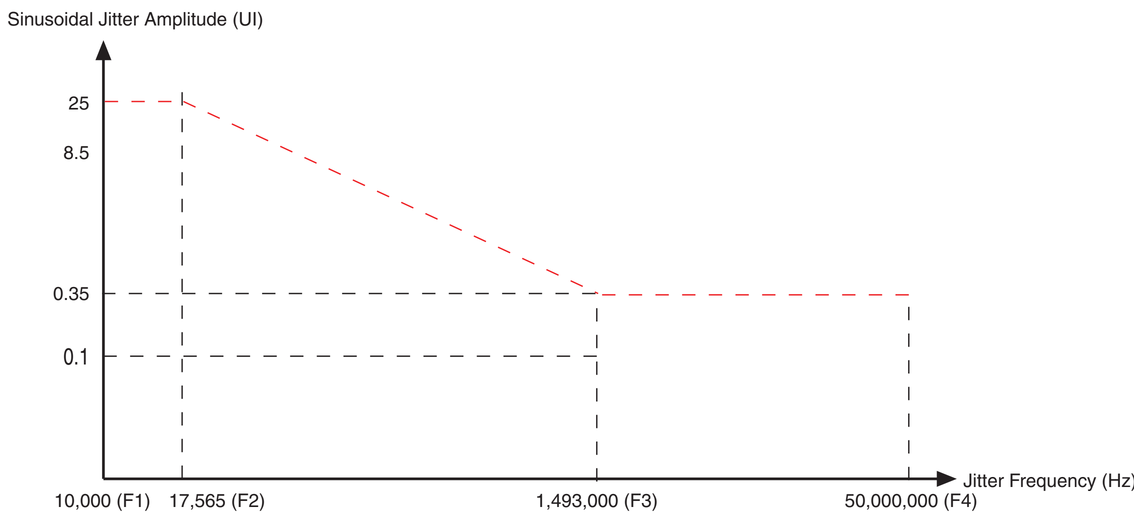


Table 1–56 lists the LVDS soft-CDR/DPA sinusoidal jitter tolerance specification for Arria II GZ devices at 1.25 Gbps data rate.

Table 1–56. LVDS Soft-CDR/DPA Sinusoidal Jitter Mask Values for Arria II GZ Devices at 1.25 Gbps Data Rate

Jitter Frequency (Hz)		Sinusoidal Jitter (UI)
F1	10,000	25.000
F2	17,565	25.000
F3	1,493,000	0.350
F4	50,000,000	0.350

External Memory Interface Specifications

For the maximum clock rate supported for Arria II GX and GZ device family, refer to the External Memory Interface Spec Estimator page on the Altera website.

Table 1–57 lists the external memory interface specifications for Arria II GX devices.

Table 1–57. External Memory Interface Specifications for Arria II GX Devices (Part 1 of 2)

Frequency Mode	Frequency Range (MHz)			Resolution (°)	DQS Delay Buffer Mode (1)	Number of Delay Chains
	C4	I3, C5, I5	C6			
0	90-140	90-130	90-110	22.5	Low	16
1	110-180	110-170	110-150	30	Low	12
2	140-220	140-210	140-180	36	Low	10
3	170-270	170-260	170-220	45	Low	8
4	220-340	220-310	220-270	30	High	12

Table 1–60 lists the DQS phase shift error for Arria II GX devices.

Table 1–60. DQS Phase Shift Error Specification for DLL-Delayed Clock (t_{DQS_PSERR}) for Arria II GX Devices *(Note 1)*

Number of DQS Delay Buffer	C4	I3, C5, I5	C6	Unit
1	26	30	36	ps
2	52	60	72	ps
3	78	90	108	ps
4	104	120	144	ps

Note to Table 1–60:

(1) This error specification is the absolute maximum and minimum error. For example, skew on three DQS delay buffers in a C4 speed grade is ± 78 ps or ± 39 ps.

Table 1–61 lists the DQS phase shift error for Arria II GZ devices.

Table 1–61. DQS Phase Shift Error Specification for DLL-Delayed Clock (t_{DQS_PSERR}) for Arria II GZ Devices *(Note 1)*

Number of DQS Delay Buffer	–3	–4	Unit
1	28	30	ps
2	56	60	ps
3	84	90	ps
4	112	120	ps

Note to Table 1–61:

(1) This error specification is the absolute maximum and minimum error. For example, skew on three DQS delay buffers in a 3 speed grade is ± 84 ps or ± 42 ps.

Table 1–62 lists the memory output clock jitter specifications for Arria II GX devices.

Table 1–62. Memory Output Clock Jitter Specification for Arria II GX Devices *(Note 1)*, *(2)*, *(3)*

Parameter	Clock Network	Symbol	–4		–5		–6		Unit
			Min	Max	Min	Max	Min	Max	
Clock period jitter	Global	$t_{JIT(per)}$	-100	100	-125	125	-125	125	ps
Cycle-to-cycle period jitter	Global	$t_{JIT(cc)}$	-200	200	-250	250	-250	250	ps
Duty cycle jitter	Global	$t_{JIT(duty)}$	-100	100	-125	125	-125	125	ps

Notes to Table 1–62:

(1) The memory output clock jitter measurements are for 200 consecutive clock cycles, as specified in the JEDEC DDR2/DDR3 SDRAM standard.

(2) The clock jitter specification applies to memory output clock pins generated using DDIO circuits clocked by a PLL output routed on a global clock network.

(3) The memory output clock jitter stated in Table 1–62 is applicable when an input jitter of 30 ps is applied.

IOE Programmable Delay

Table 1–66 lists the delay associated with each supported IOE programmable delay chain for Arria II GX devices.

Table 1–66. IOE Programmable Delay for Arria II GX Devices

Parameter	Available Settings *(1)*	Minimum Offset *(2)*	Maximum Offset								Unit
			Fast Model			Slow Model					
			I3	C4	I5	I3	C4	C5	I5	C6	
Output enable pin delay	7	0	0.413	0.442	0.413	0.814	0.713	0.796	0.801	0.873	ns
Delay from output register to output pin	7	0	0.339	0.362	0.339	0.671	0.585	0.654	0.661	0.722	ns
Input delay from pin to internal cell	52	0	1.494	1.607	1.494	2.895	2.520	2.733	2.775	2.944	ns
Input delay from pin to input register	52	0	1.493	1.607	1.493	2.896	2.503	2.732	2.774	2.944	ns
DQS bus to input register delay	4	0	0.074	0.076	0.074	0.140	0.124	0.147	0.147	0.167	ns

Notes to Table 1–66:

(1) The available setting for every delay chain starts with zero and ends with the specified maximum number of settings.

(2) The minimum offset represented in the table does not include intrinsic delay.

Table 1–67 lists the IOE programmable delay settings for Arria II GZ devices.

Table 1–67. IOE Programmable Delay for Arria II GZ Devices

Parameter	Available Settings *(1)*	Minimum Offset *(2)*	Maximum Offset						Unit
			Fast Model		Slow Model				
			Industrial	Commercial	C3	I3	C4	I4	
D1	15	0	0.462	0.505	0.795	0.801	0.857	0.864	ns
D2	7	0	0.234	0.232	0.372	0.371	0.407	0.405	ns
D3	7	0	1.700	1.769	2.927	2.948	3.157	3.178	ns
D4	15	0	0.508	0.554	0.882	0.889	0.952	0.959	ns
D5	15	0	0.472	0.500	0.799	0.817	0.875	0.882	ns
D6	6	0	0.186	0.195	0.319	0.321	0.345	0.347	ns

Notes to Table 1–67:

(1) You can set this value in the Quartus II software by selecting **D1**, **D2**, **D3**, **D4**, **D5**, and **D6** in the **Assignment Name** column.

(2) Minimum offset does not include the intrinsic delay.

I/O Timing

Altera offers two ways to determine I/O timing:

- Using the Microsoft Excel-based I/O Timing.
- Using the Quartus II Timing Analyzer.

The Microsoft Excel-based I/O Timing provides pin timing performance for each device density and speed grade. The data is typically used prior to designing the FPGA to get an estimate of the timing budget as part of the link timing analysis. The Quartus II timing analyzer provides a more accurate and precise I/O timing data based on the specifics of the design after place-and-route is complete.

The Microsoft Excel-based I/O Timing spreadsheet is downloadable from the Literature: Arria II Devices web page.

Glossary

Table 1–68 lists the glossary for this chapter.

Table 1–68. Glossary (Part 1 of 4)

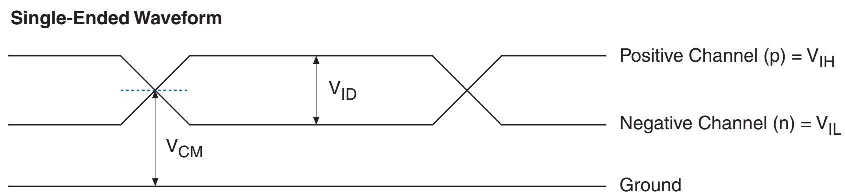
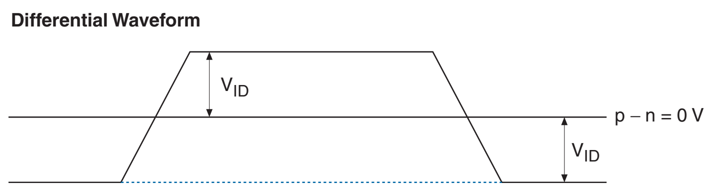
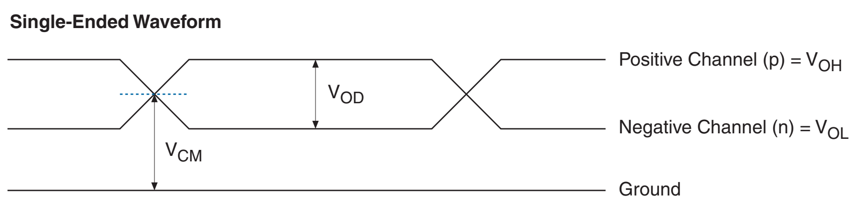
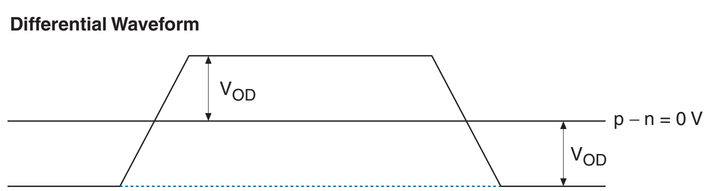
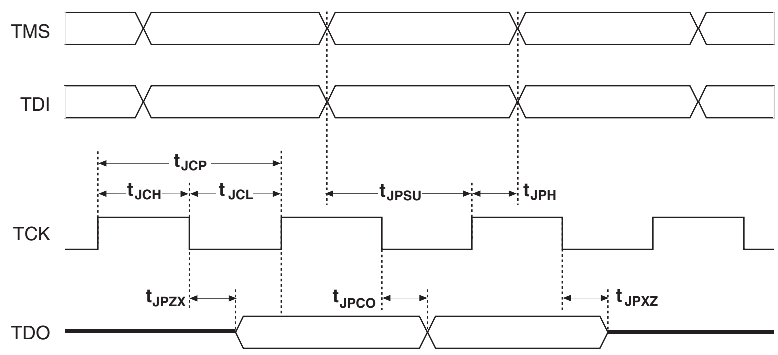
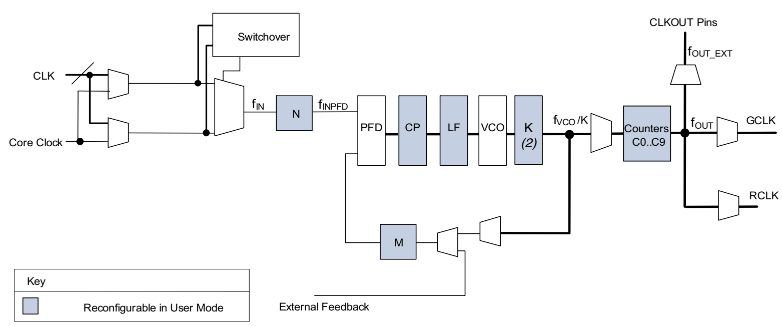
Letter	Subject	Definitions
A, B, C, D	Differential I/O Standards	*Receiver Input Waveforms*   *Transmitter Output Waveforms*  
E, F	f_{HSCLK}	Left/Right PLL input clock frequency.
	f_{HSDR}	High-speed I/O block: Maximum/minimum LVDS data transfer rate (f_{HSDR} = 1/TUI), non-DPA.
	$f_{HSDRDPA}$	High-speed I/O block: Maximum/minimum LVDS data transfer rate ($f_{HSDRDPA}$ = 1/TUI), DPA.

Table 1–68. Glossary (Part 2 of 4)

Letter	Subject	Definitions
G, H, I, J	J	High-speed I/O block: Deserialization factor (width of parallel data bus).
	JTAG Timing Specifications	JTAG Timing Specifications: 
K, L, M, N, O, P	PLL Specifications	PLL Specification parameters: **Diagram of PLL Specifications** ***(1)***  **Notes:** (1) CoreClock can only be fed by dedicated clock input pins or PLL outputs. (2) This is the VCO post-scale counter K.
Q, R	R_L	Receiver differential input discrete resistor (external to the Arria II device).