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Details

Product Status	Obsolete
Number of LABs/CLBs	4964
Number of Logic Elements/Cells	118143
Total RAM Bits	8315904
Number of I/O	372
Number of Gates	-
Voltage - Supply	0.87V ~ 0.93V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	780-BBGA, FCBGA
Supplier Device Package	780-FBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep2agx125ef29i3

Table 1-17 lists the pin capacitance for Arria II GZ devices.

Table 1-17. Pin Capacitance for Arria II GZ Devices

Symbol	Description	Typical	Unit
C_{IOTB}	Input capacitance on the top and bottom I/O pins	4	pF
C_{IOLR}	Input capacitance on the left and right I/O pins	4	pF
C_{CLKTB}	Input capacitance on the top and bottom non-dedicated clock input pins	4	pF
C_{CLKLR}	Input capacitance on the left and right non-dedicated clock input pins	4	pF
C_{OUTFB}	Input capacitance on the dual-purpose clock output and feedback pins	5	pF
C_{CLK1} , C_{CLK3} , C_{CLK8} , and C_{CLK10}	Input capacitance for dedicated clock input pins	2	pF

Internal Weak Pull-Up and Weak Pull-Down Resistors

Table 1-18 lists the weak pull-up and pull-down resistor values for Arria II GX devices.

Table 1-18. Internal Weak Pull-up and Weak Pull-Down Resistors for Arria II GX Devices (Note 1)

Symbol	Description	Conditions	Min	Typ	Max	Unit
R_{PU}	Value of I/O pin pull-up resistor before and during configuration, as well as user mode if the programmable pull-up resistor option is enabled.	$V_{CCIO} = 3.3 \text{ V} \pm 5\%$ (2)	7	25	41	k Ω
		$V_{CCIO} = 3.0 \text{ V} \pm 5\%$ (2)	7	28	47	k Ω
		$V_{CCIO} = 2.5 \text{ V} \pm 5\%$ (2)	8	35	61	k Ω
		$V_{CCIO} = 1.8 \text{ V} \pm 5\%$ (2)	10	57	108	k Ω
		$V_{CCIO} = 1.5 \text{ V} \pm 5\%$ (2)	13	82	163	k Ω
		$V_{CCIO} = 1.2 \text{ V} \pm 5\%$ (2)	19	143	351	k Ω
R_{PD}	Value of TCK pin pull-down resistor	$V_{CCIO} = 3.3 \text{ V} \pm 5\%$	6	19	29	k Ω
		$V_{CCIO} = 3.0 \text{ V} \pm 5\%$	6	22	32	k Ω
		$V_{CCIO} = 2.5 \text{ V} \pm 5\%$	6	25	42	k Ω
		$V_{CCIO} = 1.8 \text{ V} \pm 5\%$	7	35	70	k Ω
		$V_{CCIO} = 1.5 \text{ V} \pm 5\%$	8	50	112	k Ω

Notes to Table 1-18:

- (1) All I/O pins have an option to enable weak pull-up except configuration, test, and JTAG pins. The weak pull-down feature is only available for JTAG TCK.
- (2) Pin pull-up resistance values may be lower if an external source drives the pin higher than V_{CCIO} .

I/O Standard Specifications

Table 1-22 through Table 1-35 list input voltage (V_{IH} and V_{IL}), output voltage (V_{OH} and V_{OL}), and current drive characteristics (I_{OH} and I_{OL}) for various I/O standards supported by the Arria II device family. They also show the Arria II device family I/O standard specifications. V_{OL} and V_{OH} values are valid at the corresponding I_{OH} and I_{OL} , respectively.



For an explanation of terms used in Table 1-22 through Table 1-35, refer to “Glossary” on page 1-74.

Table 1-22 lists the single-ended I/O standards for Arria II GX devices.

Table 1-22. Single-Ended I/O Standards for Arria II GX Devices

I/O Standard	V_{CCIO} (V)			V_{IL} (V)		V_{IH} (V)		V_{OL} (V)	V_{OH} (V)	I_{OL} (mA)	I_{OH} (mA)
	Min	Typ	Max	Min	Max	Min	Max	Max	Min		
3.3 V LVTTTL	3.135	3.3	3.465	-0.3	0.8	1.7	3.6	0.45	2.4	4	-4
3.3 V LVCMOS	3.135	3.3	3.465	-0.3	0.8	1.7	3.6	0.2	$V_{CCIO} - 0.2$	2	-2
3.0 V LVTTTL	2.85	3	3.15	-0.3	0.8	1.7	$V_{CCIO} + 0.3$	0.45	2.4	4	-4
3.0 V LVCMOS	2.85	3	3.15	-0.3	0.8	1.7	$V_{CCIO} + 0.3$	0.2	$V_{CCIO} - 0.2$	0.1	-0.1
2.5 V LVCMOS	2.375	2.5	2.625	-0.3	0.7	1.7	$V_{CCIO} + 0.3$	0.4	2	1	-1
1.8 V LVCMOS	1.71	1.8	1.89	-0.3	$0.35 \times V_{CCIO}$	$0.65 \times V_{CCIO}$	$V_{CCIO} + 0.3$	0.45	$V_{CCIO} - 0.45$	2	-2
1.5 V LVCMOS	1.425	1.5	1.575	-0.3	$0.35 \times V_{CCIO}$	$0.65 \times V_{CCIO}$	$V_{CCIO} + 0.3$	$0.25 \times V_{CCIO}$	$0.75 \times V_{CCIO}$	2	-2
1.2 V LVCMOS	1.14	1.2	1.26	-0.3	$0.35 \times V_{CCIO}$	$0.65 \times V_{CCIO}$	$V_{CCIO} + 0.3$	$0.25 \times V_{CCIO}$	$0.75 \times V_{CCIO}$	2	-2
3.0-V PCI	2.85	3	3.15	—	$0.3 \times V_{CCIO}$	$0.5 \times V_{CCIO}$	$V_{CCIO} + 0.3$	$0.1 \times V_{CCIO}$	$0.9 \times V_{CCIO}$	1.5	-0.5
3.0-V PCI-X	2.85	3	3.15	—	$0.35 \times V_{CCIO}$	$0.5 \times V_{CCIO}$	$V_{CCIO} + 0.3$	$0.1 \times V_{CCIO}$	$0.9 \times V_{CCIO}$	1.5	-0.5

Table 1-23 lists the single-ended I/O standards for Arria II GZ devices.

Table 1-23. Single-Ended I/O Standards for Arria II GZ Devices (Part 1 of 2)

I/O Standard	V_{CCIO} (V)			V_{IL} (V)		V_{IH} (V)		V_{OL} (V)	V_{OH} (V)	I_{OL} (mA)	I_{OH} (mA)
	Min	Typ	Max	Min	Max	Min	Max	Max	Min		
LVTTTL	2.85	3	3.15	-0.3	0.8	1.7	3.6	0.4	2.4	2	-2
LVCMOS	2.85	3	3.15	-0.3	0.8	1.7	3.6	0.2	$V_{CCIO} - 0.2$	0.1	-0.1
2.5 V	2.375	2.5	2.625	-0.3	0.7	1.7	3.6	0.4	2	1	-1
1.8 V	1.71	1.8	1.89	-0.3	$0.35 \times V_{CCIO}$	$0.65 \times V_{CCIO}$	$V_{CCIO} + 0.3$	0.45	$V_{CCIO} - 0.45$	2	-2
1.5 V	1.425	1.5	1.575	-0.3	$0.35 \times V_{CCIO}$	$0.65 \times V_{CCIO}$	$V_{CCIO} + 0.3$	$0.25 \times V_{CCIO}$	$0.75 \times V_{CCIO}$	2	-2

Table 1–23. Single-Ended I/O Standards for Arria II GZ Devices (Part 2 of 2)

I/O Standard	V_{CCIO} (V)			V_{IL} (V)		V_{IH} (V)		V_{OL} (V)	V_{OH} (V)	I_{OL} (mA)	I_{OH} (mA)
	Min	Typ	Max	Min	Max	Min	Max	Max	Min		
1.2 V	1.14	1.2	1.26	-0.3	$0.35 \times V_{CCIO}$	$0.65 \times V_{CCIO}$	$V_{CCIO} + 0.3$	$0.25 \times V_{CCIO}$	$0.75 \times V_{CCIO}$	2	-2
3.0-V PCI	2.85	3	3.15	—	$0.3 \times V_{CCIO}$	$0.5 \times V_{CCIO}$	3.6	$0.1 \times V_{CCIO}$	$0.9 \times V_{CCIO}$	1.5	-0.5
3.0-V PCI-X	2.85	3	3.15	—	$0.35 \times V_{CCIO}$	$0.5 \times V_{CCIO}$	—	$0.1 \times V_{CCIO}$	$0.9 \times V_{CCIO}$	1.5	-0.5

Table 1–24 lists the single-ended SSTL and HSTL I/O reference voltage specifications for Arria II GX devices.

Table 1–24. Single-Ended SSTL and HSTL I/O Reference Voltage Specifications for Arria II GX Devices

I/O Standard	V_{CCIO} (V)			V_{REF} (V)			V_{TT} (V)		
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max
SSTL-2 Class I, II	2.375	2.5	2.625	$0.49 \times V_{CCIO}$	$0.5 \times V_{CCIO}$	$0.51 \times V_{CCIO}$	$V_{REF} - 0.04$	V_{REF}	$V_{REF} + 0.04$
SSTL-18 Class I, II	1.71	1.8	1.89	0.833	0.9	0.969	$V_{REF} - 0.04$	V_{REF}	$V_{REF} + 0.04$
SSTL-15 Class I, II	1.425	1.5	1.575	$0.47 \times V_{CCIO}$	$0.5 \times V_{CCIO}$	$0.53 \times V_{CCIO}$	$0.47 \times V_{CCIO}$	$0.5 \times V_{CCIO}$	$0.53 \times V_{CCIO}$
HSTL-18 Class I, II	1.71	1.8	1.89	0.85	0.9	0.95	0.85	0.9	0.95
HSTL-15 Class I, II	1.425	1.5	1.575	0.71	0.75	0.79	0.71	0.75	0.79
HSTL-12 Class I, II	1.14	1.2	1.26	$0.48 \times V_{CCIO}$	$0.5 \times V_{CCIO}$	$0.52 \times V_{CCIO}$	—	$V_{CCIO}/2$	—

Table 1–25 lists the single-ended SSTL and HSTL I/O reference voltage specifications for Arria II GZ devices.

Table 1–25. Single-Ended SSTL and HSTL I/O Reference Voltage Specifications for Arria II GZ Devices

I/O Standard	V_{CCIO} (V)			V_{REF} (V)			V_{TT} (V)		
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max
SSTL-2 Class I, II	2.375	2.5	2.625	$0.49 \times V_{CCIO}$	$0.5 \times V_{CCIO}$	$0.51 \times V_{CCIO}$	$V_{REF} - 0.04$	V_{REF}	$V_{REF} + 0.04$
SSTL-18 Class I, II	1.71	1.8	1.89	0.833	0.9	0.969	$V_{REF} - 0.04$	V_{REF}	$V_{REF} + 0.04$
SSTL-15 Class I, II	1.425	1.5	1.575	$0.47 \times V_{CCIO}$	$0.5 \times V_{CCIO}$	$0.53 \times V_{CCIO}$	$0.47 \times V_{CCIO}$	V_{REF}	$0.53 \times V_{CCIO}$
HSTL-18 Class I, II	1.71	1.8	1.89	0.85	0.9	0.95	—	$V_{CCIO}/2$	—
HSTL-15 Class I, II	1.425	1.5	1.575	0.68	0.75	0.9	—	$V_{CCIO}/2$	—
HSTL-12 Class I, II	1.14	1.2	1.26	$0.47 \times V_{CCIO}$	$0.5 \times V_{CCIO}$	$0.53 \times V_{CCIO}$	—	$V_{CCIO}/2$	—

Table 1-30 lists the HSTL I/O standards for Arria II GX devices.

Table 1-30. Differential HSTL I/O Standards for Arria II GX Devices

I/O Standard	V _{CCIO} (V)			V _{DIF(DC)} (V)		V _{X(AC)} (V)			V _{CM(DC)} (V)			V _{DIF(AC)} (V)	
	Min	Typ	Max	Min	Max	Min	Typ	Max	Min	Typ	Max	Min	Max
HSTL-18 Class I	1.71	1.8	1.89	0.2	—	0.85	—	0.95	0.88	—	0.95	0.4	—
HSTL-15 Class I, II	1.425	1.5	1.575	0.2	—	0.71	—	0.79	0.71	—	0.79	0.4	—
HSTL-12 Class I, II	1.14	1.2	1.26	0.16	—	—	0.5 × V _{CCIO}	—	0.48 × V _{CCIO}	0.5 × V _{CCIO}	0.52 × V _{CCIO}	0.3	—

Table 1-31 lists the HSTL I/O standards for Arria II GZ devices.

Table 1-31. Differential HSTL I/O Standards for Arria II GZ Devices

I/O Standard	V _{CCIO} (V)			V _{DIF(DC)} (V)		V _{X(AC)} (V)			V _{CM(DC)} (V)			V _{DIF(AC)} (V)	
	Min	Typ	Max	Min	Max	Min	Typ	Max	Min	Typ	Max	Min	Max
HSTL-18 Class I	1.71	1.8	1.89	0.2	—	0.78	—	1.12	0.78	—	1.12	0.4	—
HSTL-15 Class I, II	1.425	1.5	1.575	0.2	—	0.68	—	0.9	0.68	—	0.9	0.4	—
HSTL-12 Class I, II	1.14	1.2	1.26	0.16	V _{CCIO} + 0.3	—	0.5 × V _{CCIO}	—	0.4 × V _{CCIO}	0.5 × V _{CCIO}	0.6 × V _{CCIO}	0.3	V _{CCIO} + 0.48

Table 1-32 lists the differential I/O standard specifications for Arria II GX devices.

Table 1-32. Differential I/O Standard Specifications for Arria II GX Devices (Note 1)

I/O Standard	V _{CCIO} (V)			V _{ID} (mV)			V _{ICM} (V) (2)		V _{OD} (V) (3)			V _{OCM} (V)		
	Min	Typ	Max	Min	Cond.	Max	Min	Max	Min	Typ	Max	Min	Typ	Max
2.5 V LVDS	2.375	2.5	2.625	100	V _{CM} = 1.25 V	—	0.05	1.80	0.247	—	0.6	1.125	1.25	1.375
RSDS (4)	2.375	2.5	2.625	—	—	—	—	—	0.1	0.2	0.6	0.5	1.2	1.4
Mini-LVDS (4)	2.375	2.5	2.625	—	—	—	—	—	0.25	—	0.6	1	1.2	1.4
LVPECL (5)	2.375	2.5	2.625	300	—	—	0.6	1.8	—	—	—	—	—	—
BLVDS (6)	2.375	2.5	2.625	100	—	—	—	—	—	—	—	—	—	—

Notes to Table 1-32:

- (1) The 1.5 V PCML transceiver I/O standard specifications are described in “Transceiver Performance Specifications” on page 1-21.
- (2) V_{IN} range: 0 ≤ V_{IN} ≤ 1.85 V.
- (3) R_L range: 90 ≤ R_L ≤ 110 Ω.
- (4) The RSDS and mini-LVDS I/O standards are only supported for differential outputs.
- (5) The LVPECL input standard is supported at the dedicated clock input pins (GCLK) only.
- (6) There are no fixed V_{ICM}, V_{OD}, and V_{OCM} specifications for BLVDS. These specifications depend on the system topology.

Table 1–34. Transceiver Specifications for Arria II GX Devices (Note 1) (Part 2 of 7)

Symbol/ Description	Condition	I3			C4			C5 and I5			C6			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Spread-spectrum downspread	PCIe	—	0 to –0.5%	—	—	0 to –0.5%	—	—	0 to –0.5%	—	—	0 to –0.5%	—	—
On-chip termination resistors	—	—	100	—	—	100	—	—	100	—	—	100	—	Ω
V _{ICM} (AC coupled)	—	1100 ± 5%			1100 ± 5%			1100 ± 5%			1100 ± 5%			mV
V _{ICM} (DC coupled)	HCSL I/O standard for PCIe reference clock	250	—	550	250	—	550	250	—	550	250	—	550	mV
Transmitter REFCLK Phase Noise	10 Hz	—	—	-50	—	—	-50	—	—	-50	—	—	-50	dBc/Hz
	100 Hz	—	—	-80	—	—	-80	—	—	-80	—	—	-80	dBc/Hz
	1 KHz	—	—	-110	—	—	-110	—	—	-110	—	—	-110	dBc/Hz
	10 KHz	—	—	-120	—	—	-120	—	—	-120	—	—	-120	dBc/Hz
	100 KHz	—	—	-120	—	—	-120	—	—	-120	—	—	-120	dBc/Hz
	≥ 1 MHz	—	—	-130	—	—	-130	—	—	-130	—	—	-130	dBc/Hz
Transmitter REFCLK Phase Jitter (rms) for 100 MHz REFCLK (3)	10 KHz to 20 MHz	—	—	3	—	—	3	—	—	3	—	—	3	ps
R _{ref}	—	—	2000 ± 1%	—	—	2000 ± 1%	—	—	2000 ± 1%	—	—	2000 ± 1%	—	Ω
Transceiver Clocks														
Calibration block clock frequency (cal_blk_clk)	—	10	—	125	10	—	125	10	—	125	10	—	125	MHz

Table 1–34. Transceiver Specifications for Arria II GX Devices (Note 1) (Part 5 of 7)

Symbol/ Description	Condition	I3			C4			C5 and I5			C6			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
LTD lock time (11)	—	0	100	4000	0	100	4000	0	100	4000	0	100	4000	ns
Data lock time from rx_ freqlocked (12)	—	—	—	4000	—	—	4000	—	—	4000	—	—	4000	ns
Programmable DC gain	DC Gain Setting = 0	—	0	—	—	0	—	—	0	—	—	0	—	dB
	DC Gain Setting = 1	—	3	—	—	3	—	—	3	—	—	3	—	dB
	DC Gain Setting = 2	—	6	—	—	6	—	—	6	—	—	6	—	dB
Transmitter														
Supported I/O Standards	1.5-V PCML													
Data rate	—	600	—	6375	600	—	3750	600	—	3750	600	—	3125	Mbps
V _{OCM}	0.65 V setting	—	650	—	—	650	—	—	650	—	—	650	—	mV
Differential on-chip termination resistors	100-Ω setting	—	100	—	—	100	—	—	100	—	—	100	—	Ω
Return loss differential mode	PCIe	50 MHz to 1.25 GHz: –10dB												
	XAUI	312 MHz to 625 MHz: –10dB 625 MHz to 3.125 GHz: –10dB/decade slope												
Return loss common mode	PCIe	50 MHz to 1.25 GHz: –6dB												
Rise time (2)	—	50	—	200	50	—	200	50	—	200	50	—	200	ps
Fall time	—	50	—	200	50	—	200	50	—	200	50	—	200	ps

Table 1–34. Transceiver Specifications for Arria II GX Devices (Note 1) (Part 6 of 7)

Symbol/ Description	Condition	I3			C4			C5 and I5			C6			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Intra-differential pair skew	—	—	—	15	—	—	15	—	—	15	—	—	15	ps
Intra-transceiver block skew	PCIe ×4	—	—	120	—	—	120	—	—	120	—	—	120	ps
Inter-transceiver block skew	PCIe ×8	—	—	300	—	—	300	—	—	300	—	—	300	ps
CMU PLL0 and CMU PLL1														
CMU PLL lock time from CMUPLL_reset deassertion	—	—	—	100	—	—	100	—	—	100	—	—	100	μs
PLD-Transceiver Interface														
Interface speed	—	25	—	320	25	—	240	25	—	240	25	—	200	MHz

Table 1–34. Transceiver Specifications for Arria II GX Devices (Note 1) (Part 7 of 7)

Symbol/ Description	Condition	I3			C4			C5 and I5			C6			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Digital reset pulse width	—	Minimum is 2 parallel clock cycles												

Notes to Table 1–34:

- (1) For AC-coupled links, the on-chip biasing circuit is switched off before and during configuration. Ensure that input specifications are not violated during this period.
- (2) The rise/fall time is specified from 20% to 80%.
- (3) To calculate the REFCLK rms phase jitter requirement at reference clock frequencies other than 100 MHz, use the following formula:
REFCLK rms phase jitter at f (MHz) = REFCLK rms phase jitter at 100 MHz * 100/f.
- (4) The minimum `reconfig_clk` frequency is 2.5 MHz if the transceiver channel is configured in **Transmitter only** mode. The minimum `reconfig_clk` frequency is 37.5 MHz if the transceiver channel is configured in **Receiver only** or **Receiver and Transmitter** mode. For more information, refer to [AN 558: Implementing Dynamic Reconfiguration in Arria II Devices](#).
- (5) If your design uses more than one dynamic reconfiguration controller instances (`altgx_reconfig`) to control the transceiver channels (`altgx`) physically located on the same side of the device, and if you use different `reconfig_clk` sources for these `altgx_reconfig` instances, the delta time between any two of these `reconfig_clk` sources becoming stable must not exceed the maximum specification listed.
- (6) The device cannot tolerate prolonged operation at this absolute maximum.
- (7) You must use the 1.1-V RX V_{ICM} setting if the input serial data standard is LVDS and the link is DC-coupled.
- (8) The rate matcher supports only up to ± 300 parts per million (ppm).
- (9) Time taken to `rx_pll_locked` goes high from `rx_analogreset` de-assertion. Refer to [Figure 1–1](#).
- (10) The time in which the CDR must be kept in lock-to-reference mode after `rx_pll_locked` goes high and before `rx_locktodata` is asserted in manual mode. Refer to [Figure 1–1](#).
- (11) The time taken to recover valid data after the `rx_locktodata` signal is asserted in manual mode. Refer to [Figure 1–1](#).
- (12) The time taken to recover valid data after the `rx_freqlocked` signal goes high in automatic mode. Refer to [Figure 1–2](#).
- (13) To support data rates lower than the minimum specification through oversampling, use the CDR in LTR mode only.

Table 1–35 lists the transceiver specifications for Arria II GZ devices.

Table 1–35. Transceiver Specifications for Arria II GZ Devices (Part 1 of 5)

Symbol/ Description	Conditions	–C3 and –I3 (1)			–C4 and –I4			Unit
		Min	Typ	Max	Min	Typ	Max	
Reference Clock								
Supported I/O Standards	1.2-V PCML, 1.5-V PCML, 2.5-V PCML, Differential LVPECL, LVDS, and HCSL							
Input frequency from REFCLK input pins	—	50	—	697	50	—	637.5	MHz
Phase frequency detector (CMU PLL and receiver CDR)	—	50	—	325	50	—	325	MHz
Absolute V _{MAX} for a REFCLK pin	—	—	—	1.6	—	—	1.6	V
Operational V _{MAX} for a REFCLK pin	—	—	—	1.5	—	—	1.5	V
Absolute V _{MIN} for a REFCLK pin	—	-0.4	—	—	-0.4	—	—	V
Rise/fall time (2)	—	—	—	0.2	—	—	0.2	UI
Duty cycle	—	45	—	55	45	—	55	%
Peak-to-peak differential input voltage	—	200	—	1600	200	—	1600	mV
Spread-spectrum modulating clock frequency	PCIe	30	—	33	30	—	33	kHz
Spread-spectrum downspread	PCIe	—	0 to -0.5%	—	—	0 to -0.5%	—	—
On-chip termination resistors	—	—	100	—	—	100	—	Ω
V _{ICM} (AC coupled)	—	1100 ± 10%			1100 ± 10%			mV
V _{ICM} (DC coupled)	HCSL I/O standard for PCIe reference clock	250	—	550	250	—	550	mV
Transmitter REFCLK Phase Noise	10 Hz	—	—	-50	—	—	-50	dBc/Hz
	100 Hz	—	—	-80	—	—	-80	dBc/Hz
	1 KHz	—	—	-110	—	—	-110	dBc/Hz
	10 KHz	—	—	-120	—	—	-120	dBc/Hz
	100 KHz	—	—	-120	—	—	-120	dBc/Hz
	≥ 1 MHz	—	—	-130	—	—	-130	dBc/Hz
Transmitter REFCLK Phase Jitter (rms) for 100 MHz REFCLK (3)	10 KHz to 20 MHz	—	—	3	—	—	3	ps
R _{REF}	—	—	2000 ± 1%	—	—	2000 ± 1%	—	Ω

Table 1–39 lists typical transmitter pre-emphasis levels for Arria II GZ devices (in dB) for the first post tap under the following conditions (low-frequency data pattern [five 1s and five 0s] at 6.25 Gbps). The levels listed in Table 1–39 are a representation of possible pre-emphasis levels under the specified conditions only and that the pre-emphasis levels may change with data pattern and data rate.



To predict the pre-emphasis level for your specific data rate and pattern, run simulations using the [Arria II HSSI HSPICE](#) models.

Table 1–39. Transmitter Pre-Emphasis Levels for Arria II GZ Devices (Part 1 of 2)

Pre-Emphasis 1st Post-Tap Setting	V _{DD} Setting							
	0	1	2	3	4	5	6	7
0	0	0	0	0	0	0	0	0
1	N/A	0.7	0	0	0	0	0	0
2	N/A	1	0.3	0	0	0	0	0
3	N/A	1.5	0.6	0	0	0	0	0
4	N/A	2	0.7	0.3	0	0	0	0
5	N/A	2.7	1.2	0.5	0.3	0	0	0
6	N/A	3.1	1.3	0.8	0.5	0.2	0	0
7	N/A	3.7	1.8	1.1	0.7	0.4	0.2	0
8	N/A	4.2	2.1	1.3	0.9	0.6	0.3	0
9	N/A	4.9	2.4	1.6	1.2	0.8	0.5	0.2
10	N/A	5.4	2.8	1.9	1.4	1	0.7	0.3
11	N/A	6	3.2	2.2	1.7	1.2	0.9	0.4
12	N/A	6.8	3.5	2.6	1.9	1.4	1.1	0.6
13	N/A	7.5	3.8	2.8	2.1	1.6	1.2	0.6
14	N/A	8.1	4.2	3.1	2.3	1.7	1.3	0.7
15	N/A	8.8	4.5	3.4	2.6	1.9	1.5	0.8
16	N/A	N/A	4.9	3.7	2.9	2.2	1.7	0.9
17	N/A	N/A	5.3	4	3.1	2.4	1.8	1.1
18	N/A	N/A	5.7	4.4	3.4	2.6	2	1.2
19	N/A	N/A	6.1	4.7	3.6	2.8	2.2	1.4
20	N/A	N/A	6.6	5.1	4	3.1	2.4	1.5
21	N/A	N/A	7	5.4	4.3	3.3	2.7	1.7
22	N/A	N/A	8	6.1	4.8	3.8	3	2
23	N/A	N/A	9	6.8	5.4	4.3	3.4	2.3
24	N/A	N/A	10	7.6	6	4.8	3.9	2.6
25	N/A	N/A	11.4	8.4	6.8	5.4	4.4	3
26	N/A	N/A	12.6	9.4	7.4	5.9	4.9	3.3
27	N/A	N/A	N/A	10.3	8.1	6.4	5.3	3.6
28	N/A	N/A	N/A	11.3	8.8	7.1	5.8	4

Table 1–40. Transceiver Block Jitter Specifications for Arria II GX Devices (Note 1) (Part 4 of 10)

Symbol/ Description	Conditions	I3			C4			C5, I5			C6			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Total jitter (peak-to-peak)	Pattern = CRPAT	—	—	0.27 9	—	—	0.279	—	—	0.279	—	—	0.279	UI
GIGE Receiver Jitter Tolerance (6)														
Deterministic jitter tolerance (peak-to-peak)	Pattern = CJPAT	> 0.4			> 0.4			> 0.4			> 0.4			UI
Combined deterministic and random jitter tolerance (peak-to-peak)	Pattern = CJPAT	> 0.66			> 0.66			> 0.66			> 0.66			UI
HiGig Transmit Jitter Generation (7)														
Deterministic jitter (peak-to-peak)	Data rate = 3.75 Gbps Pattern = CJPAT	—	—	0.17	—	—	0.17	—	—	—	—	—	—	UI
Total jitter (peak-to-peak)	Data rate = 3.75 Gbps Pattern = CJPAT	—	—	0.35	—	—	0.35	—	—	—	—	—	—	UI
HiGig Receiver Jitter Tolerance (7)														
Deterministic jitter tolerance (peak-to-peak)	Data rate = 3.75 Gbps Pattern = CJPAT	> 0.37			> 0.37			—	—	—	—	—	—	UI
Combined deterministic and random jitter tolerance (peak-to-peak)	Data rate = 3.75 Gbps Pattern = CJPAT	> 0.65			> 0.65			—	—	—	—	—	—	UI
Sinusoidal jitter tolerance (peak-to-peak)	Jitter frequency = 22.1 KHz Data rate = 3.75 Gbps Pattern = CJPAT	> 8.5			> 8.5			—	—	—	—	—	—	UI
	Jitter frequency = 1.875MHz Data rate = 3.75 Gbps Pattern = CJPAT	> 0.1			> 0.1			—	—	—	—	—	—	UI
	Jitter frequency = 20 MHz Data rate = 3.75 Gbps Pattern = CJPAT	> 0.1			> 0.1			—	—	—	—	—	—	UI

Table 1-40. Transceiver Block Jitter Specifications for Arria II GX Devices (Note 1) (Part 7 of 10)

Symbol/ Description	Conditions	I3			C4			C5, I5			C6			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
SSC modulation deviation at 1.5 Gbps (G1)	Compliance pattern	5700			5700			5700			5700			ppm
RX differential skew at 1.5 Gbps (G1)	Compliance pattern	80			80			80			80			ps
RX AC common mode voltage at 1.5 Gbps (G1)	Compliance pattern	150			150			150			150			mV
Total jitter tolerance at 3.0 Gbps (G2)	Compliance pattern	> 0.65			> 0.65			> 0.65			> 0.65			UI
Deterministic jitter tolerance at 3.0 Gbps (G2)	Compliance pattern	> 0.35			> 0.35			> 0.35			> 0.35			UI
SSC modulation frequency at 3.0 Gbps (G2)	Compliance pattern	33			33			33			33			kHz
SSC modulation deviation at 3.0 Gbps (G2)	Compliance pattern	5700			5700			5700			5700			ppm
RX differential skew at 3.0 Gbps (G2)	Compliance pattern	75			75			75			75			ps
RX AC common mode voltage at 3.0 Gbps (G2)	Compliance pattern	150			150			150			150			mV
Total jitter tolerance at 6.0 Gbps (G3)	Compliance pattern	> 0.60			> 0.60			> 0.60			> 0.60			UI
Random jitter tolerance at 6.0 Gbps (G3)	Compliance pattern	> 0.18			> 0.18			> 0.18			> 0.18			UI
SSC modulation frequency at 6.0 Gbps (G3)	Compliance pattern	33			33			33			33			kHz
SSC modulation deviation at 6.0 Gbps (G3)	Compliance pattern	5700			5700			5700			5700			ppm
RX differential skew at 6.0 Gbps (G3)	Compliance pattern	30			30			30			30			ps
RX AC common mode voltage at 6.0 Gbps (G3)	Compliance pattern	100			100			100			100			mV

Table 1–41. Transceiver Block Jitter Specifications for Arria II GZ Devices (Note 1), (2) (Part 5 of 7)

Symbol/ Description	Conditions	–C3 and –I3			–C4 and –I4			Unit
		Min	Typ	Max	Min	Typ	Max	
Sinusoidal jitter tolerance (peak-to-peak)	Jitter Frequency = 38.2 KHz Data rate = 6.375 Gbps Pattern = PRBS31 BER = 10 ⁻¹²	> 0.5			—	—	—	UI
	Jitter Frequency = 3.82 MHz Data rate = 6.375 Gbps Pattern = PRBS31 BER = 10 ⁻¹²	> 0.05			—	—	—	UI
	Jitter Frequency = 20 MHz Data rate = 6.375 Gbps Pattern = PRBS31 BER = 10 ⁻¹²	> 0.05			—	—	—	UI
SDI Transmitter Jitter Generation (12)								
Alignment jitter (peak-to-peak)	Data rate = 1.485 Gbps (HD) Pattern = color bar Low-frequency roll-off = 100 KHz	0.2	—	—	0.2	—	—	UI
	Data rate = 2.97 Gbps (3G) Pattern = color bar Low-frequency roll-off = 100 KHz	0.3	—	—	0.3	—	—	UI
SDI Receiver Jitter Tolerance (12)								
Sinusoidal jitter tolerance (peak-to-peak)	Jitter frequency = 15 KHz Data rate = 2.97 Gbps (3G) Pattern = single line scramble color bar	> 2			> 2			UI
	Jitter frequency = 100 KHz Data rate = 2.97 Gbps (3G) Pattern = single line scramble color bar	> 0.3			> 0.3			UI
	Jitter frequency = 148.5 MHz Data rate = 2.97 Gbps (3G) Pattern = single line scramble color bar	> 0.3			> 0.3			UI
Sinusoidal jitter tolerance (peak-to-peak)	Jitter frequency = 20 KHz Data rate = 1.485 Gbps (HD) pattern = 75% color bar	> 1			> 1			UI
	Jitter frequency = 100 KHz Data rate = 1.485 Gbps (HD) Pattern = 75% color bar	> 0.2			> 0.2			UI
	Jitter frequency = 148.5 MHz Data rate = 1.485 Gbps (HD) Pattern = 75% color bar	> 0.2			> 0.2			UI
SAS Transmit Jitter Generation (13)								
Total jitter at 1.5 Gbps (G1)	Pattern = CJPAT	—	—	0.55	—	—	0.55	UI
Deterministic jitter at 1.5 Gbps (G1)	Pattern = CJPAT	—	—	0.35	—	—	0.35	UI
Total jitter at 3.0 Gbps (G2)	Pattern = CJPAT	—	—	0.55	—	—	0.55	UI

Table 1–41. Transceiver Block Jitter Specifications for Arria II GZ Devices (Note 1), (2) (Part 7 of 7)

Symbol/ Description	Conditions	–C3 and –I3			–C4 and –I4			Unit
		Min	Typ	Max	Min	Typ	Max	
OBSAI Receiver Jitter Tolerance (15)								
Deterministic jitter tolerance at 768 Mbps, 1536 Mbps, and 3072 Mbps	Pattern = CJPAT	> 0.37			> 0.37			UI
Combined deterministic and random jitter tolerance at 768 Mbps, 1536 Mbps, and 3072 Mbps	Pattern = CJPAT	> 0.55			> 0.55			UI
Sinusoidal jitter tolerance at 768 Mbps	Jitter frequency = 5.4 KHz Pattern = CJPAT	> 8.5			> 8.5			UI
	Jitter frequency = 460 MHz to 20 MHz Pattern = CJPAT	> 0.1			> 0.1			UI
Sinusoidal jitter tolerance at 1536 Mbps	Jitter frequency = 10.9 KHz Pattern = CJPAT	> 8.5			> 8.5			UI
	Jitter frequency = 921.6 MHz to 20 MHz Pattern = CJPAT	> 0.1			> 0.1			UI
Sinusoidal jitter tolerance at 3072 Mbps	Jitter frequency = 21.8 KHz Pattern = CJPAT	> 8.5			> 8.5			UI
	Jitter frequency = 1843.2 MHz to 20 MHz Pattern = CJPAT	> 0.1			> 0.1			UI

Notes to Table 1–41:

- (1) Dedicated `refclk` pins were used to drive the input reference clocks.
- (2) The jitter numbers are valid for the stated conditions only.
- (3) The jitter numbers for SONET/SDH are compliant to the GR-253-CORE Issue 3 Specification.
- (4) The jitter numbers for Fibre Channel are compliant to the FC-P1-4 Specification revision 6.10.
- (5) The Fibre Channel transmitter jitter generation numbers are compliant to the specification at the δ_T inter operability point.
- (6) The Fibre Channel receiver jitter tolerance numbers are compliant to the specification at the δ_R interpretability point.
- (7) The jitter numbers for XAUI are compliant to the IEEE802.3ae-2002 Specification.
- (8) The jitter numbers for PCIe are compliant to the PCIe Base Specification 2.0.
- (9) Arria II GZ PCIe receivers are compliant to this specification provided the $V_{TX-CM-DC-ACTIVEIDLE-DELTA}$ of the upstream transmitter is less than 50 mV.
- (10) The jitter numbers for SRIO are compliant to the RapidIO Specification 1.3.
- (11) The jitter numbers for GIGE are compliant to the IEEE802.3-2002 Specification.
- (12) The HD-SDI and 3G-SDI jitter numbers are compliant to the SMPTE292M and SMPTE424M Specifications.
- (13) The jitter numbers for Serial Attached SCSI (SAS) are compliant to the SAS-2.1 Specification.
- (14) The jitter numbers for CPRI are compliant to the CPRI Specification V3.0.
- (15) The jitter numbers for OBSAI are compliant to the OBSAI RP3 Specification V4.1.

Core Performance Specifications for the Arria II Device Family

This section describes the clock tree, phase-locked loop (PLL), digital signal processing (DSP), embedded memory, configuration, and JTAG specifications for Arria II GX and GZ devices.

Clock Tree Specifications

Table 1-42 lists the clock tree specifications for Arria II GX devices.

Table 1-42. Clock Tree Performance for Arria II GX Devices

Clock Network	Performance			Unit
	I3, C4	C5,I5	C6	
GCLK and RCLK	500	500	400	MHz
PCLK	420	350	280	MHz

Table 1-43 lists the clock tree specifications for Arria II GZ devices.

Table 1-43. Clock Tree Performance for Arria II GZ Devices

Clock Network	Performance		Unit
	-C3 and -I3	-C4 and -I4	
GCLK and RCLK	700	500	MHz
PCLK	500	450	MHz

PLL Specifications

Table 1-44 lists the PLL specifications for Arria II GX devices.

Table 1-44. PLL Specifications for Arria II GX Devices (Part 1 of 3)

Symbol	Description	Min	Typ	Max	Unit
f_{IN}	Input clock frequency (from clock input pins residing in right/top/bottom banks) (-4 Speed Grade)	5	—	670 (1)	MHz
	Input clock frequency (from clock input pins residing in right/top/bottom banks) (-5 Speed Grade)	5	—	622 (1)	MHz
	Input clock frequency (from clock input pins residing in right/top/bottom banks) (-6 Speed Grade)	5	—	500 (1)	MHz
f_{INPFD}	Input frequency to the PFD	5	—	325	MHz
f_{VCO}	PLL VCO operating Range (2)	600	—	1,400	MHz
f_{INDUTY}	Input clock duty cycle	40	—	60	%
$f_{EINDUTY}$	External feedback clock input duty cycle	40	—	60	%
t_{INCCJ} (3), (4)	Input clock cycle-to-cycle jitter (Frequency ≥ 100 MHz)	—	—	0.15	UI (p-p)
	Input clock cycle-to-cycle jitter (Frequency ≤ 100 MHz)	—	—	± 750	ps (p-p)

DSP Block Specifications

Table 1-46 lists the DSP block performance specifications for Arria II GX devices.

Table 1-46. DSP Block Performance Specifications for Arria II GX Devices (Note 1)

Mode	Resources Used	Performance				Unit
	Number of Multipliers	C4	I3	C5,I5	C6	
9 × 9-bit multiplier	1	380	310	300	250	MHz
12 × 12-bit multiplier	1	380	310	300	250	MHz
18 × 18-bit multiplier	1	380	310	300	250	MHz
36 × 36-bit multiplier	1	350	270	270	220	MHz
18 × 36-bit high-precision multiplier adder mode	1	350	270	270	220	MHz
18 × 18-bit multiply accumulator	4	380	310	300	250	MHz
18 × 18-bit multiply adder	4	380	310	300	250	MHz
18 × 18-bit multiply adder-signed full precision	2	380	310	300	250	MHz
18 × 18-bit multiply adder with loopback (2)	2	275	220	220	180	MHz
36-bit shift (32-bit data)	1	350	270	270	220	MHz
Double mode	1	350	270	270	220	MHz

Notes to Table 1-46:

- (1) Maximum is for a fully-pipelined block with **Round** and **Saturation** disabled.
- (2) Maximum is for loopback input registers disabled, **Round** and **Saturation** disabled, pipeline and output registers enabled.

Table 1-47 lists the DSP block performance specifications for Arria II GZ devices.

Table 1-47. DSP Block Performance Specifications for Arria II GZ Devices (Note 1) (Part 1 of 2)

Mode	Resources Used	Performance		Unit
	Number of Multipliers	-3	-4	
9 × 9-bit multiplier	1	460	400	MHz
12 × 12-bit multiplier	1	500	440	MHz
18 × 18-bit multiplier	1	550	480	MHz
36 × 36-bit multiplier	1	440	380	MHz
18 × 18-bit multiply accumulator	4	440	380	MHz
18 × 18-bit multiply adder	4	470	410	MHz
18 × 18-bit multiply adder-signed full precision	2	450	390	MHz
18 × 18-bit multiply adder with loopback (2)	2	350	310	MHz
36-bit shift (32-bit data)	1	440	380	MHz

Configuration

Table 1–50 lists the configuration mode specifications for Arria II GX and GZ devices.

Table 1–50. Configuration Mode Specifications for Arria II Devices

Programming Mode	DCLK Frequency			Unit
	Min	Typ	Max	
Passive serial	—	—	125	MHz
Fast passive parallel	—	—	125	MHz
Fast active serial (fast clock)	17	26	40	MHz
Fast active serial (slow clock)	8.5	13	20	MHz
Remote update only in fast AS mode	—	—	10	MHz

JTAG Specifications

Table 1–51 lists the JTAG timing parameters and values for Arria II GX and GZ devices.

Table 1–51. JTAG Timing Parameters and Values for Arria II Devices

Symbol	Description	Min	Max	Unit
t_{JCP}	TCK clock period	30	—	ns
t_{JCH}	TCK clock high time	14	—	ns
t_{JCL}	TCK clock low time	14	—	ns
$t_{JPSU(TDI)}$	TDI JTAG port setup time	1	—	ns
$t_{JPSU(TMS)}$	TMS JTAG port setup time	3	—	ns
t_{JPH}	JTAG port hold time	5	—	ns
t_{JPCO}	JTAG port clock to output	—	11	ns
t_{JPZX}	JTAG port high impedance to valid output	—	14	ns
t_{JPXZ}	JTAG port valid output to high impedance	—	14	ns

Chip-Wide Reset (Dev_CLRn) Specifications

Table 1–52 lists the specifications for the chip-wide reset (Dev_CLRn) for Arria II GX and GZ devices.

Table 1–52. Chip-Wide Reset (Dev_CLRn) Specifications for Arria II Devices

Description	Min	Typ	Max	Unit
Dev_CLRn	500	—	—	μ s

Figure 1-6 shows the LVDS soft-CDR/DPA sinusoidal jitter tolerance specification for Arria II GZ devices at 1.25 Gbps data rate.

Figure 1-6. LVDS Soft-CDR/DPA Sinusoidal Jitter Tolerance Specification for Arria II GZ Devices at a 1.25 Gbps Data Rate

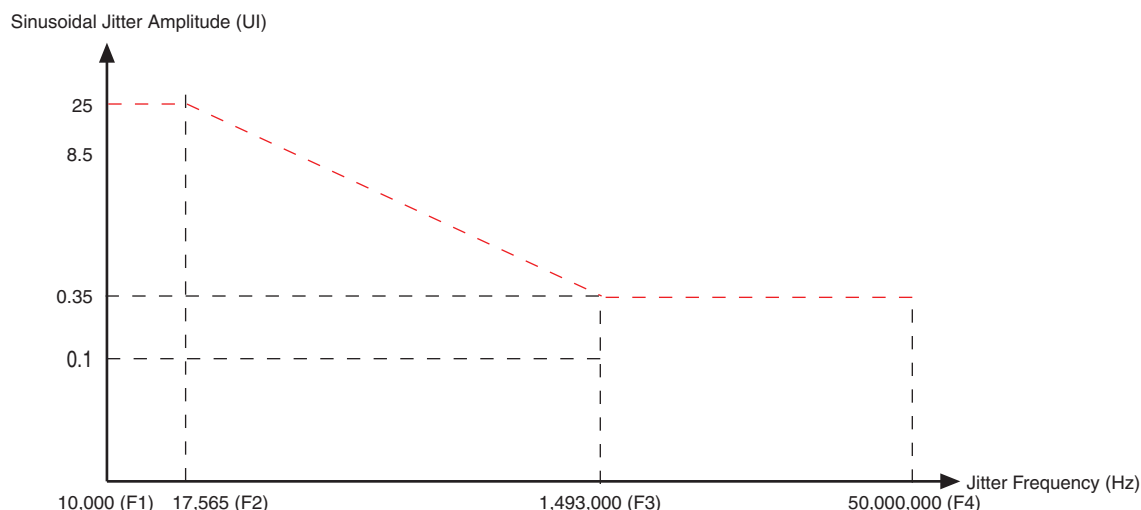


Table 1-56 lists the LVDS soft-CDR/DPA sinusoidal jitter tolerance specification for Arria II GZ devices at 1.25 Gbps data rate.

Table 1-56. LVDS Soft-CDR/DPA Sinusoidal Jitter Mask Values for Arria II GZ Devices at 1.25 Gbps Data Rate

Jitter Frequency (Hz)		Sinusoidal Jitter (UI)
F1	10,000	25.000
F2	17,565	25.000
F3	1,493,000	0.350
F4	50,000,000	0.350

External Memory Interface Specifications

 For the maximum clock rate supported for Arria II GX and GZ device family, refer to the [External Memory Interface Spec Estimator](#) page on the Altera website.

Table 1-57 lists the external memory interface specifications for Arria II GX devices.

Table 1-57. External Memory Interface Specifications for Arria II GX Devices (Part 1 of 2)

Frequency Mode	Frequency Range (MHz)			Resolution (°)	DQS Delay Buffer Mode ⁽¹⁾	Number of Delay Chains
	C4	I3, C5, I5	C6			
0	90-140	90-130	90-110	22.5	Low	16
1	110-180	110-170	110-150	30	Low	12
2	140-220	140-210	140-180	36	Low	10
3	170-270	170-260	170-220	45	Low	8
4	220-340	220-310	220-270	30	High	12

Table 1-57. External Memory Interface Specifications for Arria II GX Devices (Part 2 of 2)

Frequency Mode	Frequency Range (MHz)			Resolution (°)	DQS Delay Buffer Mode (1)	Number of Delay Chains
	C4	I3, C5, I5	C6			
5	270-410	270-380	270-320	36	High	10
6	320-450	320-410	320-370	45	High	8

Note to Table 1-57:

(1) Low indicates a 6-bit DQS delay setting; high indicates a 5-bit DQS delay setting.

Table 1-58 lists the DLL frequency range specifications for Arria II GZ devices.

Table 1-58. DLL Frequency Range Specifications for Arria II GZ Devices

Frequency Mode	Frequency Range (MHz)		Available Phase Shift	DQS Delay Buffer Mode (1)	Number of Delay Chains
	-3	-4			
0	90-130	90-120	22.5°, 45°, 67.5°, 90°	Low	16
1	120-170	120-160	30°, 60°, 90°, 120°	Low	12
2	150-210	150-200	36°, 72°, 108°, 144°	Low	10
3	180-260	180-240	45°, 90°, 135°, 180°	Low	8
4	240-320	240-290	30°, 60°, 90°, 120°	High	12
5	290-380	290-360	36°, 72°, 108°, 144°	High	10
6	360-450	360-450	45°, 90°, 135°, 180°	High	8
7	470-630	470-590	60°, 120°, 180°, 240°	High	6

Note to Table 1-58:

(1) Low indicates a 6-bit DQS delay setting; high indicates a 5-bit DQS delay setting.

Table 1-59 lists the DQS phase offset delay per stage for Arria II GX devices.

Table 1-59. DQS Phase Offset Delay Per Setting for Arria II GX Devices (Note 1), (2), (3)

Speed Grade	Min	Max	Unit
C4	7.0	13.0	ps
I3, C5, I5	7.0	15.0	ps
C6	8.5	18.0	ps

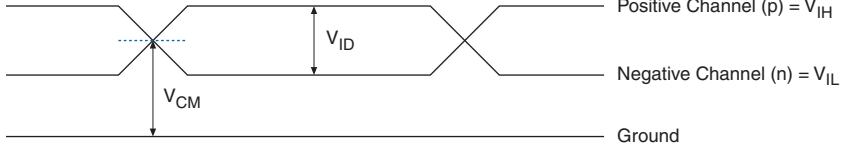
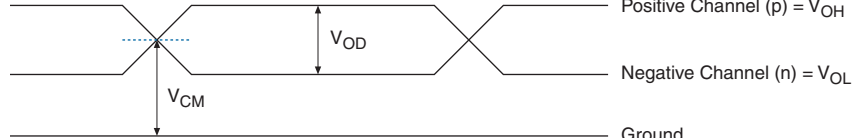
Notes to Table 1-59:

- (1) The valid settings for phase offset are -64 to +63 for frequency modes 0 to 3 and -32 to +31 for frequency modes 4 to 5.
- (2) The typical value equals the average of the minimum and maximum values.
- (3) The delay settings are linear.

Glossary

Table 1-68 lists the glossary for this chapter.

Table 1-68. Glossary (Part 1 of 4)

Letter	Subject	Definitions
A, B, C, D	Differential I/O Standards	<i>Receiver Input Waveforms</i> Single-Ended Waveform  Positive Channel (p) = V_{IH} Negative Channel (n) = V_{IL} Ground Differential Waveform  <i>Transmitter Output Waveforms</i> Single-Ended Waveform  Positive Channel (p) = V_{OH} Negative Channel (n) = V_{OL} Ground Differential Waveform 
E, F	f_{HSCLK}	Left/Right PLL input clock frequency.
	f_{HSDR}	High-speed I/O block: Maximum/minimum LVDS data transfer rate ($f_{HSDR} = 1/TUI$), non-DPA.
	f_{HSRDPA}	High-speed I/O block: Maximum/minimum LVDS data transfer rate ($f_{HSRDPA} = 1/TUI$), DPA.