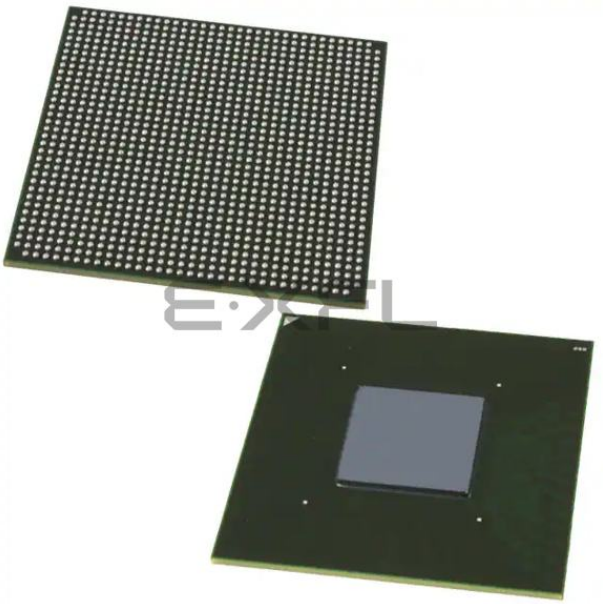

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The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	4964
Number of Logic Elements/Cells	118143
Total RAM Bits	8315904
Number of I/O	452
Number of Gates	-
Voltage - Supply	0.87V ~ 0.93V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1152-BBGA, FCBGA
Supplier Device Package	1152-FBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep2agx125ef35c5

CAUTION

Conditions beyond those listed in Table 1–1 and Table 1–2 may cause permanent damage to the device. Additionally, device operation at the absolute maximum ratings for extended periods of time may have adverse effects on the device.

Table 1–1 lists the absolute maximum ratings for Arria II GX devices.

Table 1–1. Absolute Maximum Ratings for Arria II GX Devices

Symbol	Description	Minimum	Maximum	Unit
V_{CC}	Supplies power to the core, periphery, I/O registers, PCI Express® (PIPE) (PCIe) HIP block, and transceiver PCS	–0.5	1.35	V
V_{CCCB}	Supplies power for the configuration RAM bits	–0.5	1.8	V
V_{CCBAT}	Battery back-up power supply for design security volatile key register	–0.5	3.75	V
V_{CCPD}	Supplies power to the I/O pre-drivers, differential input buffers, and MSEL circuitry	–0.5	3.75	V
V_{CCIO}	Supplies power to the I/O banks	–0.5	3.9	V
V_{CCD_PLL}	Supplies power to the digital portions of the PLL	–0.5	1.35	V
V_{CCA_PLL}	Supplies power to the analog portions of the PLL and device-wide power management circuitry	–0.5	3.75	V
V_I	DC input voltage	–0.5	4.0	V
I_{OUT}	DC output current, per pin	–25	40	mA
V_{CCA}	Supplies power to the transceiver PMA regulator	—	3.75	V
V_{CCL_GXB}	Supplies power to the transceiver PMA TX, PMA RX, and clocking	—	1.21	V
V_{CCH_GXB}	Supplies power to the transceiver PMA output (TX) buffer	—	1.8	V
T_J	Operating junction temperature	–55	125	°C
T_{STG}	Storage temperature (no bias)	–65	150	°C

Table 1–2 lists the absolute maximum ratings for Arria II GZ devices.

Table 1–2. Absolute Maximum Ratings for Arria II GZ Devices (Part 1 of 2)

Symbol	Description	Minimum	Maximum	Unit
V_{CC}	Supplies power to the core, periphery, I/O registers, PCIe HIP block, and transceiver PCS	-0.5	1.35	V
V_{CCCB}	Power supply to the configuration RAM bits	-0.5	1.8	V
V_{CCPGM}	Supplies power to the configuration pins	-0.5	3.75	V
V_{CCAUX}	Auxiliary supply	-0.5	3.75	V
V_{CCBAT}	Supplies battery back-up power for design security volatile key register	-0.5	3.75	V
V_{CCPD}	Supplies power to the I/O pre-drivers, differential input buffers, and MSEL circuitry	-0.5	3.75	V
V_{CCIO}	Supplies power to the I/O banks	-0.5	3.9	V
V_{CC_CLKIN}	Supplies power to the differential clock input	-0.5	3.75	V
V_{CCD_PLL}	Supplies power to the digital portions of the PLL	-0.5	1.35	V
V_{CCA_PLL}	Supplies power to the analog portions of the PLL and device-wide power management circuitry	-0.5	3.75	V
V_I	DC input voltage	-0.5	4.0	V
I_{OUT}	DC output current, per pin	-25	40	mA

Recommended Operating Conditions

This section lists the functional operation limits for AC and DC parameters for Arria II GX and GZ devices. All supplies are required to monotonically reach their full-rail values without plateaus within t_{RAMP}.

Table 1–5 lists the recommended operating conditions for Arria II GX devices.

Table 1–5. Recommended Operating Conditions for Arria II GX Devices *(Note 1)* (Part 1 of 2)

Symbol	Description	Condition	Minimum	Typical	Maximum	Unit
V_{CC}	Supplies power to the core, periphery, I/O registers, PCIe HIP block, and transceiver PCS	—	0.87	0.90	0.93	V
V_{CCCB}	Supplies power to the configuration RAM bits	—	1.425	1.50	1.575	V
V_{CCBAT} *(2)*	Battery back-up power supply for design security volatile key registers	—	1.2	—	3.3	V
V_{CCPD} *(3)*	Supplies power to the I/O pre-drivers, differential input buffers, and MSEL circuitry	—	3.135	3.3	3.465	V
		—	2.85	3.0	3.15	V
		—	2.375	2.5	2.625	V
V_{CCIO}	Supplies power to the I/O banks *(4)*	—	3.135	3.3	3.465	V
		—	2.85	3.0	3.15	V
		—	2.375	2.5	2.625	V
		—	1.71	1.8	1.89	V
		—	1.425	1.5	1.575	V
		—	1.14	1.2	1.26	V
V_{CCD_PLL}	Supplies power to the digital portions of the PLL	—	0.87	0.90	0.93	V
V_{CCA_PLL}	Supplies power to the analog portions of the PLL and device-wide power management circuitry	—	2.375	2.5	2.625	V
V_I	DC Input voltage	—	–0.5	—	3.6	V
V_O	Output voltage	—	0	—	V_{CCIO}	V
V_{CCA}	Supplies power to the transceiver PMA regulator	—	2.375	2.5	2.625	V
V_{CCL_GXB}	Supplies power to the transceiver PMA TX, PMA RX, and clocking	—	1.045	1.1	1.155	V
V_{CCH_GXB}	Supplies power to the transceiver PMA output (TX) buffer	—	1.425	1.5	1.575	V
T_J	Operating junction temperature	Commercial	0	—	85	°C
		Industrial	–40	—	100	°C

Table 1–30 lists the HSTL I/O standards for Arria II GX devices.

Table 1–30. Differential HSTL I/O Standards for Arria II GX Devices

I/O Standard	V_{CCIO} (V)			$V_{DIF(DC)}$ (V)		$V_{X(AC)}$ (V)			$V_{CM(DC)}$ (V)			$V_{DIF(AC)}$ (V)	
	Min	Typ	Max	Min	Max	Min	Typ	Max	Min	Typ	Max	Min	Max
HSTL-18 Class I	1.71	1.8	1.89	0.2	—	0.85	—	0.95	0.88	—	0.95	0.4	—
HSTL-15 Class I, II	1.425	1.5	1.575	0.2	—	0.71	—	0.79	0.71	—	0.79	0.4	—
HSTL-12 Class I, II	1.14	1.2	1.26	0.16	—	—	0.5 × V_{CCIO}	—	0.48 × V_{CCIO}	0.5 × V_{CCIO}	0.52 × V_{CCIO}	0.3	—

Table 1–31 lists the HSTL I/O standards for Arria II GZ devices.

Table 1–31. Differential HSTL I/O Standards for Arria II GZ Devices

I/O Standard	V_{CCIO} (V)			$V_{DIF(DC)}$ (V)		$V_{X(AC)}$ (V)			$V_{CM(DC)}$ (V)			$V_{DIF(AC)}$ (V)	
	Min	Typ	Max	Min	Max	Min	Typ	Max	Min	Typ	Max	Min	Max
HSTL-18 Class I	1.71	1.8	1.89	0.2	—	0.78	—	1.12	0.78	—	1.12	0.4	—
HSTL-15 Class I, II	1.425	1.5	1.575	0.2	—	0.68	—	0.9	0.68	—	0.9	0.4	—
HSTL-12 Class I, II	1.14	1.2	1.26	0.16	V_{CCIO} + 0.3	—	0.5 × V_{CCIO}	—	0.4 × V_{CCIO}	0.5 × V_{CCIO}	0.6 × V_{CCIO}	0.3	V_{CCIO} + 0.48

Table 1–32 lists the differential I/O standard specifications for Arria II GX devices.

Table 1–32. Differential I/O Standard Specifications for Arria II GX Devices *(Note 1)*

I/O Standard	V_{CCIO} (V)			V_{ID} (mV)			V_{ICM} (V) *(2)*		V_{OD} (V) *(3)*			V_{OCM} (V)		
	Min	Typ	Max	Min	Cond.	Max	Min	Max	Min	Typ	Max	Min	Typ	Max
2.5 V LVDS	2.375	2.5	2.625	100	V_{CM} = 1.25 V	—	0.05	1.80	0.247	—	0.6	1.125	1.25	1.375
RSDS *(4)*	2.375	2.5	2.625	—	—	—	—	—	0.1	0.2	0.6	0.5	1.2	1.4
Mini-LVDS *(4)*	2.375	2.5	2.625	—	—	—	—	—	0.25	—	0.6	1	1.2	1.4
LVPECL *(5)*	2.375	2.5	2.625	300	—	—	0.6	1.8	—	—	—	—	—	—
BLVDS *(6)*	2.375	2.5	2.625	100	—	—	—	—	—	—	—	—	—	—

Notes to Table 1–32:

(1) The 1.5 V PCML transceiver I/O standard specifications are described in "Transceiver Performance Specifications" on page 1–21.
(2) V_{IN} range: 0 <= V_{IN} <= 1.85 V.
(3) R_L range: 90 <= RL <= 110 Ω.
(4) The RSDS and mini-LVDS I/O standards are only supported for differential outputs.
(5) The LVPECL input standard is supported at the dedicated clock input pins (GCLK) only.
(6) There are no fixed V_{ICM}, V_{OD}, and V_{OCM} specifications for BLVDS. These specifications depend on the system topology.

Table 1–34. Transceiver Specifications for Arria II GX Devices *(Note 1)* (Part 4 of 7)

Symbol/ Description	Condition	I3			C4			C5 and I5			C6			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Minimum peak-to-peak differential input voltage V_{ID} (diff p-p)	—	100	—	—	100	—	—	100	—	—	100	—	—	mV
V_{ICM}	V_{ICM} = 0.82 V setting	—	820	—	—	820	—	—	820	—	—	820	—	mV
	V_{ICM} =1.1 V setting *(7)*	—	1100	—	—	1100	—	—	1100	—	—	1100	—	mV
Differential on-chip termination resistors	100–Ω setting	—	100	—	—	100	—	—	100	—	—	100	—	Ω
Return loss differential mode	PCIe				50 MHz to 1.25 GHz: –10dB									
	XAUI				100 MHz to 2.5 GHz: –10dB									
Return loss common mode	PCIe				50 MHz to 1.25 GHz: –6dB									
	XAUI				100 MHz to 2.5 GHz: –6dB									
Programmable PPM detector *(8)*	—	± 62.5, 100, 125, 200, 250, 300, 500, 1000												ppm
Run length	—	—	80	—	—	80	—	—	80	—	—	80	—	UI
Programmable equalization	—	—	—	7	—	—	7	—	—	7	—	—	7	dB
Signal detect/loss threshold	PCIe Mode	65	—	175	65	—	175	65	—	175	65	—	175	mV
CDR LTR time *(9)*	—	—	—	75	—	—	75	—	—	75	—	—	75	µs
CDR minimum T1b *(10)*	—	15	—	—	15	—		15	—	—	15	—	—	µs

Table 1–34. Transceiver Specifications for Arria II GX Devices *(Note 1)* (Part 6 of 7)

Symbol/ Description	Condition	I3			C4			C5 and I5			C6			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Intra-differential pair skew	—	—	—	15	—	—	15	—	—	15	—	—	15	ps
Intra-transceiver block skew	PCIe ×4	—	—	120	—	—	120	—	—	120	—	—	120	ps
Inter-transceiver block skew	PCIe ×8	—	—	300	—	—	300	—	—	300	—	—	300	ps
CMU PLL0 and CMU PLL1														
CMU PLL lock time from `CMUPLL_reset` deassertion	—	—	—	100	—	—	100	—	—	100	—	—	100	µs
PLD-Transceiver Interface														
Interface speed	—	25	—	320	25	—	240	25	—	240	25	—	200	MHz

Table 1–35. Transceiver Specifications for Arria II GZ Devices (Part 5 of 5)

Symbol/ Description	Conditions	–C3 and –I3 *(1)*			–C4 and –I4			Unit
		Min	Typ	Max	Min	Typ	Max	
-3 dB Bandwidth	PCIe Gen1	2.5 - 3.5						MHz
	PCIe Gen2	6 - 8						MHz
	(OIF) CEI PHY at 4.976 Gbps	7 - 11						MHz
	(OIF) CEI PHY at 6.375 Gbps	5 - 10						MHz
	XAUI	2 - 4						MHz
	SRIO 1.25 Gbps	3 - 5.5						MHz
	SRIO 2.5 Gbps	3 - 5.5						MHz
	SRIO 3.125 Gbps	2 - 4						MHz
	GIGE	2.5 - 4.5						MHz
	SONET OC12	1.5 - 2.5						MHz
	SONET OC48	3.5 - 6						MHz
Transceiver-FPGA Fabric Interface								
Interface speed	—	25	—	325	25	—	250	MHz
Digital reset pulse width	—	Minimum is two parallel clock cycles						—

Notes to Table 1–35:

(1) The 3x speed grade is the fastest speed grade offered in the following Arria II GZ devices: EP2AGZ225, EP2AGZ300, and EP2AGZ350.

(2) The rise and fall time transition is specified from 20% to 80%.

(3) To calculate the REFCLK rms phase jitter requirement at reference clock frequencies other than 100 MHz, use the following formula: REFCLK rms phase jitter at f (MHz) = REFCLK rms phase jitter at 100 MHz * 100/f.

(4) The minimum `reconfig_clk` frequency is 2.5 MHz if the transceiver channel is configured in **Transmitter only** mode. The minimum `reconfig_clk` frequency is 37.5 MHz if the transceiver channel is configured in **Receiver only** or **Receiver and Transmitter** mode.

(5) If your design uses more than one dynamic reconfiguration controller (`altgx_reconfig`) instances to control the transceiver (`altgx`) channels physically located on the same side of the device AND if you use different `reconfig_clk` sources for these `altgx_reconfig` instances, the delta time between any two of these `reconfig_clk` sources becoming stable must not exceed the maximum specification listed.

(6) The device cannot tolerate prolonged operation at this absolute maximum.

(7) You must use the 1.1-V RX V_{ICM} setting if the input serial data standard is LVDS.

(8) The differential eye opening specification at the receiver input pins assumes that Receiver Equalization is disabled. If you enable Receiver Equalization, the receiver circuitry can tolerate a lower minimum eye opening, depending on the equalization level. Use H-Spice simulation to derive the minimum eye opening requirement with Receiver Equalization enabled.

(9) The rate matcher supports only up to ± 300 ppm.

(10) Time taken to `rx_pll_locked` goes high from `rx_analogreset` de-assertion. Refer to Figure 1–1 on page 1–33.

(11) Time for which the CDR must be kept in lock-to-reference mode after `rx_pll_locked` goes high and before `rx_locktodata` is asserted in manual mode. Refer to Figure 1–1 on page 1–33.

(12) Time taken to recover valid data after the `rx_locktodata` signal is asserted in manual mode. Refer to Figure 1–1 on page 1–33.

(13) Time taken to recover valid data after the `rx_freqlocked` signal goes high in automatic mode. Refer to Figure 1–2 on page 1–33.

(14) A GPLL may be required to meet the PMA-FPGA fabric interface timing above certain data rates. For more information, refer to the *Transceiver Clocking for Arria II Devices* chapter.

(15) The Quartus II software automatically selects the appropriate slew rate depending on the configured data rate or functional mode.

(16) To support data rates lower than the minimum specification through oversampling, use the CDR in LTR mode only.

Table 1–40. Transceiver Block Jitter Specifications for Arria II GX Devices *(Note 1)* (Part 2 of 10)

Symbol/ Description	Conditions	I3			C4			C5, I5			C6			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Jitter tolerance at 2488.32 Mbps	Jitter frequency = 0.06 KHz Pattern = PRBS15		> 15			> 15			> 15			> 15		UI
	Jitter frequency = 100 KHZ Pattern = PRBS15		> 1.5			> 1.5			> 1.5			> 1.5		UI
	Jitter frequency = 1 MHz Pattern = PRBS15		> 0.15			> 0.15			> 0.15			> 0.15		UI
	Jitter frequency = 10 MHz Pattern = PRBS15		> 0.15			> 0.15			> 0.15			> 0.15		UI
XAUI Transmit Jitter Generation *(3)*														
Total jitter at 3.125 Gbps	Pattern = CJPAT	—	—	0.3	—	—	0.3	—	—	0.3	—	—	0.3	UI
Deterministic jitter at 3.125 Gbps	Pattern = CJPAT	—	—	0.17	—	—	0.17	—	—	0.17	—	—	0.17	UI
XAUI Receiver Jitter Tolerance *(3)*														
Total jitter	—		> 0.65			> 0.65			> 0.65			> 0.65		UI
Deterministic jitter	—		> 0.37			> 0.37			> 0.37			> 0.37		UI
Peak-to-peak jitter	Jitter frequency = 22.1 KHz		> 8.5			> 8.5			> 8.5			> 8.5		UI
Peak-to-peak jitter	Jitter frequency = 1.875 MHz		> 0.1			> 0.1			> 0.1			> 0.1		UI
Peak-to-peak jitter	Jitter frequency = 20 MHz		> 0.1			> 0.1			> 0.1			> 0.1		UI
PCIe Transmit Jitter Generation *(4)*														
Total jitter at 2.5 Gbps (Gen1)	Compliance pattern	—	—	0.25	—	—	0.25	—	—	0.25	—	—	0.25	UI

Table 1–40. Transceiver Block Jitter Specifications for Arria II GX Devices *(Note 1)* (Part 4 of 10)

Symbol/ Description	Conditions	I3			C4			C5, I5			C6			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Total jitter (peak-to-peak)	Pattern = CRPAT	—	—	0.279	—	—	0.279	—	—	0.279	—	—	0.279	UI
GIGE Receiver Jitter Tolerance *(6)*														
Deterministic jitter tolerance (peak-to-peak)	Pattern = CJPAT	> 0.4			> 0.4			> 0.4			> 0.4			UI
Combined deterministic and random jitter tolerance (peak-to-peak)	Pattern = CJPAT	> 0.66			> 0.66			> 0.66			> 0.66			UI
HiGig Transmit Jitter Generation *(7)*														
Deterministic jitter (peak-to-peak)	Data rate = 3.75 Gbps Pattern = CJPAT	—	—	0.17	—	—	0.17	—	—	—	—	—	—	UI
Total jitter (peak-to-peak)	Data rate = 3.75 Gbps Pattern = CJPAT	—	—	0.35	—	—	0.35	—	—	—	—	—	—	UI
HiGig Receiver Jitter Tolerance *(7)*														
Deterministic jitter tolerance (peak-to-peak)	Data rate = 3.75 Gbps Pattern = CJPAT	> 0.37			> 0.37			—	—	—	—	—	—	UI
Combined deterministic and random jitter tolerance (peak-to-peak)	Data rate = 3.75 Gbps Pattern = CJPAT	> 0.65			> 0.65			—	—	—	—	—	—	UI
Sinusoidal jitter tolerance (peak-to-peak)	Jitter frequency = 22.1 KHz Data rate = 3.75 Gbps Pattern = CJPAT	> 8.5			> 8.5			—	—	—	—	—	—	UI
	Jitter frequency = 1.875MHz Data rate = 3.75 Gbps Pattern = CJPAT	> 0.1			> 0.1			—	—	—	—	—	—	UI
	Jitter frequency = 20 MHz Data rate = 3.75 Gbps Pattern = CJPAT	> 0.1			> 0.1			—	—	—	—	—	—	UI

Table 1–41. Transceiver Block Jitter Specifications for Arria II GZ Devices *(Note 1)*, *(2)* (Part 3 of 7)

Symbol/ Description	Conditions	–C3 and –I3			–C4 and –I4			Unit
		Min	Typ	Max	Min	Typ	Max	
Peak-to-peak jitter	Jitter frequency = 22.1 KHz		> 8.5			> 8.5		UI
Peak-to-peak jitter	Jitter frequency = 1.875 MHz		> 0.1			> 0.1		UI
Peak-to-peak jitter	Jitter frequency = 20 MHz		> 0.1			> 0.1		UI
PCIe Transmit Jitter Generation *(8)*								
Total jitter at 2.5 Gbps (Gen1)—x1, x4, and x8	Compliance pattern	—	—	0.25	—	—	0.25	UI
Total jitter at 5 Gbps (Gen2)—x1, x4, and x8	Compliance pattern	—	—	0.25	—	—	—	UI
PCIe Receiver Jitter Tolerance *(8)*								
Total jitter at 2.5 Gbps (Gen1)	Compliance pattern		> 0.6			> 0.6		UI
Total jitter at 5 Gbps (Gen2)	Compliance pattern		Not supported			Not supported		UI
PCIe (Gen 1) Electrical Idle Detect Threshold								
$V_{RX-IDLE-DETDIFFp-p}$ *(9)*	Compliance pattern	65	—	175	65	—	175	UI
SRIO Transmit Jitter Generation *(10)*								
Deterministic jitter (peak-to-peak)	Data rate = 1.25, 2.5, 3.125 Gbps Pattern = CJPAT	—	—	0.17	—	—	0.17	UI
Total jitter (peak-to-peak)	Data rate = 1.25, 2.5, 3.125 Gbps Pattern = CJPAT	—	—	0.35	—	—	0.35	UI
SRIO Receiver Jitter Tolerance *(10)*								
Deterministic jitter tolerance (peak-to-peak)	Data rate = 1.25, 2.5, 3.125 Gbps Pattern = CJPAT		> 0.37			> 0.37		UI
Combined deterministic and random jitter tolerance (peak-to-peak)	Data rate = 1.25, 2.5, 3.125 Gbps Pattern = CJPAT		> 0.55			> 0.55		UI
Sinusoidal jitter tolerance (peak-to-peak)	Jitter frequency = 22.1 KHz Data rate = 1.25, 2.5, 3.125 Gbps Pattern = CJPAT		> 8.5			> 8.5		UI
	Jitter frequency = 1.875 MHz Data rate = 1.25, 2.5, 3.125 Gbps Pattern = CJPAT		> 0.1			> 0.1		UI
	Jitter frequency = 20 MHz Data rate = 1.25, 2.5, 3.125 Gbps Pattern = CJPAT		> 0.1			> 0.1		UI
GIGE Transmit Jitter Generation *(11)*								
Deterministic jitter (peak-to-peak)	Pattern = CRPAT	—	—	0.14	—	—	0.14	UI
Total jitter (peak-to-peak)	Pattern = CRPAT	—	—	0.279	—	—	0.279	UI

Table 1–41. Transceiver Block Jitter Specifications for Arria II GZ Devices *(Note 1)*, *(2)* (Part 4 of 7)

Symbol/ Description	Conditions	–C3 and –I3			–C4 and –I4			Unit
		Min	Typ	Max	Min	Typ	Max	
GIGE Receiver Jitter Tolerance *(11)*								
Deterministic jitter tolerance (peak-to-peak)	Pattern = CJPAT		> 0.4			> 0.4		UI
Combined deterministic and random jitter tolerance (peak-to-peak)	Pattern = CJPAT		> 0.66			> 0.66		UI
HiGig Transmit Jitter Generation								
Deterministic jitter (peak-to-peak)	Data rate = 3.75 Gbps Pattern = CJPAT	—	—	0.17	—	—	—	UI
Total jitter (peak-to-peak)	Data rate = 3.75 Gbps Pattern = CJPAT	—	—	0.35	—	—	—	UI
HiGig Receiver Jitter Tolerance								
Deterministic jitter tolerance (peak-to-peak)	Data rate = 3.75 Gbps Pattern = CJPAT		> 0.37		—	—	—	UI
Combined deterministic and random jitter tolerance (peak-to-peak)	Data rate = 3.75 Gbps Pattern = CJPAT		> 0.65		—	—	—	UI
Sinusoidal jitter tolerance (peak-to-peak)	Jitter frequency = 22.1 KHz Data rate = 3.75 Gbps Pattern = CJPAT		> 8.5		—	—	—	UI
	Jitter frequency = 22.1 KHz Data rate = 3.75 Gbps Pattern = CJPAT		> 0.1		—	—	—	UI
	Jitter frequency = 22.1 KHz Data rate = 3.75 Gbps Pattern = CJPAT		> 0.1		—	—	—	UI
(OIF) CEI Transmitter Jitter Generation								
Total jitter (peak-to-peak)	Data rate = 6.375 Gbps Pattern = PRBS15 BER = 10^{-12}	—	—	0.3	—	—	0.3	UI
(OIF) CEI Receiver Jitter Tolerance								
Deterministic jitter tolerance (peak-to-peak)	Data rate = 6.375 Gbps Pattern = PRBS31 BER = 10^{-12}		> 0.675		—	—	—	UI
Combined deterministic and random jitter tolerance (peak-to-peak)	Data rate = 6.375 Gbps Pattern = PRBS31 BER = 10^{-12}		> 0.988		—	—	—	UI

Core Performance Specifications for the Arria II Device Family

This section describes the clock tree, phase-locked loop (PLL), digital signal processing (DSP), embedded memory, configuration, and JTAG specifications for Arria II GX and GZ devices.

Clock Tree Specifications

Table 1–42 lists the clock tree specifications for Arria II GX devices.

Table 1–42. Clock Tree Performance for Arria II GX Devices

Clock Network	Performance			Unit
	I3, C4	C5,I5	C6	
GCLK and RCLK	500	500	400	MHz
PCLK	420	350	280	MHz

Table 1–43 lists the clock tree specifications for Arria II GZ devices.

Table 1–43. Clock Tree Performance for Arria II GZ Devices

Clock Network	Performance		Unit
	–C3 and –I3	–C4 and –I4	
GCLK and RCLK	700	500	MHz
PCLK	500	450	MHz

PLL Specifications

Table 1–44 lists the PLL specifications for Arria II GX devices.

Table 1–44. PLL Specifications for Arria II GX Devices (Part 1 of 3)

Symbol	Description	Min	Typ	Max	Unit
f_{IN}	Input clock frequency (from clock input pins residing in right/top/bottom banks) (–4 Speed Grade)	5	—	670 *(1)*	MHz
	Input clock frequency (from clock input pins residing in right/top/bottom banks) (–5 Speed Grade)	5	—	622 *(1)*	MHz
	Input clock frequency (from clock input pins residing in right/top/bottom banks) (–6 Speed Grade)	5	—	500 *(1)*	MHz
f_{INPFD}	Input frequency to the PFD	5	—	325	MHz
f_{VCO}	PLL VCO operating Range *(2)*	600	—	1,400	MHz
f_{INDUTY}	Input clock duty cycle	40	—	60	%
$f_{EINDUTY}$	External feedback clock input duty cycle	40	—	60	%
t_{INCCJ} *(3)*, *(4)*	Input clock cycle-to-cycle jitter (Frequency ≥ 100 MHz)	—	—	0.15	UI (p–p)
	Input clock cycle-to-cycle jitter (Frequency ≤ 100 MHz)	—	—	±750	ps (p–p)

Table 1–44. PLL Specifications for Arria II GX Devices (Part 3 of 3)

Symbol	Description	Min	Typ	Max	Unit
$t_{CASC\_OUTJITTER\_PERIOD\_DEDCLK}$ *(6), (7)*	Period Jitter for dedicated clock output in cascaded PLLs (FOUT ≥ 100 MHz)	—	—	425	ps (p-p)
	Period Jitter for dedicated clock output in cascaded PLLs (FOUT ≤ 100 MHz)	—	—	42.5	mUI (p-p)

Notes to Table 1–44:

(1) f_{IN} is limited by the I/O f_{MAX}.

(2) The VCO frequency reported by the Quartus II software in the PLL summary section of the compilation report takes into consideration the VCO post-scale counter K value. Therefore, if the counter K has a value of 2, the frequency reported can be lower than the f_{VCO} specification.

(3) A high-input jitter directly affects the PLL output jitter. To have low PLL output clock jitter, you must provide a clean-clock source, which is less than 200 ps.

(4) F_{REF} is fIN/N when N = 1.

(5) This specification is limited by the lower of the two: I/O f_{MAX} or f_{OUT} of the PLL.

(6) Peak-to-peak jitter with a probability level of 10^{-12} (14 sigma, 99.99999999974404% confidence level). The output jitter specification applies to the intrinsic jitter of the PLL, when an input jitter of 30 ps is applied. The external memory interface clock output jitter specifications use a different measurement method and are available in Table 1–62 on page 1–70.

(7) The cascaded PLL specification is only applicable with the following condition:
a. Upstream PLL: 0.59 Mhz ≤ Upstream PLL BW < 1 MHz
b. Downstream PLL: Downstream PLL BW > 2 MHz

Table 1–45 lists the PLL specifications for Arria II GZ devices when operating in both the commercial junction temperature range (0° to 85°C) and the industrial junction temperature range (-40° to 100°C).

Table 1–45. PLL Specifications for Arria II GZ Devices (Part 1 of 2)

Symbol	Parameter	Min	Typ	Max	Unit
f_{IN}	Input clock frequency (–3 speed grade)	5	—	717 *(1)*	MHz
	Input clock frequency (–4 speed grade)	5	—	717 *(1)*	MHz
f_{INPFD}	Input frequency to the PFD	5	—	325	MHz
f_{VCO}	PLL VCO operating range (–3 speed grade)	600	—	1,300	MHz
	PLL VCO operating range (–4 speed grade)	600	—	1,300	MHz
$t_{EINDUTY}$	Input clock or external feedback clock input duty cycle	40	—	60	%
f_{OUT}	Output frequency for internal global or regional clock (–3 speed grade)	—	—	700 *(2)*	MHz
	Output frequency for internal global or regional clock (–4 speed grade)	—	—	500 *(2)*	MHz
f_{OUT_EXT}	Output frequency for external clock output (–3 speed grade)	—	—	717 *(2)*	MHz
	Output frequency for external clock output (–4 speed grade)	—	—	717 *(2)*	MHz
$t_{OUTDUTY}$	Duty cycle for external clock output (when set to 50%)	45	50	55	%
t_{FCOMP}	External feedback clock compensation time	—	—	10	ns
$t_{CONFIGPLL}$	Time required to reconfigure scan chain	—	3.5	—	scanclk cycles
$t_{CONFIGPHASE}$	Time required to reconfigure phase shift	—	1	—	scanclk cycles
$f_{SCANCLK}$	scanclk frequency	—	—	100	MHz
t_{LOCK}	Time required to lock from end-of-device configuration or de-assertion of areset	—	—	1	ms

Table 1–45. PLL Specifications for Arria II GZ Devices (Part 2 of 2)

Symbol	Parameter	Min	Typ	Max	Unit
t_{DLOCK}	Time required to lock dynamically (after switchover or reconfiguring any non-post-scale counters/delays)	—	—	1	ms
f_{CLBW}	PLL closed-loop low bandwidth	—	0.3	—	MHz
	PLL closed-loop medium bandwidth	—	1.5	—	MHz
	PLL closed-loop high bandwidth *(7)*	—	4	—	MHz
t_{PLL_PSERR}	Accuracy of PLL phase shift	—	—	±50	ps
t_{ARESET}	Minimum pulse width on the `areset` signal	10	—	—	ns
t_{INCCJ} *(3)*, *(4)*	Input clock cycle to cycle jitter ($F_{REF} \geq 100$ MHz)	—	—	0.15	UI (p-p)
	Input clock cycle to cycle jitter ($F_{REF} < 100$ MHz)	—	—	±750	ps (p-p)
t_{OUTPJ_DC} *(5)*	Period Jitter for dedicated clock output ($F_{OUT} \geq 100$ MHz)	—	—	175	ps (p-p)
	Period Jitter for dedicated clock output ($F_{OUT} < 100$ MHz)	—	—	17.5	mUI (p-p)
t_{OUTCCJ_DC} *(5)*	Cycle to Cycle Jitter for dedicated clock output ($F_{OUT} \geq 100$ MHz)	—	—	175	ps (p-p)
	Cycle to Cycle Jitter for dedicated clock output ($F_{OUT} < 100$ MHz)	—	—	17.5	mUI (p-p)
t_{OUTPJ_IO} *(5)*, *(8)*	Period Jitter for clock output on regular I/O ($F_{OUT} \geq 100$ MHz)	—	—	600	ps (p-p)
	Period Jitter for clock output on regular I/O ($F_{OUT} < 100$ MHz)	—	—	60	mUI (p-p)
t_{OUTCCJ_IO} *(5)*, *(8)*	Cycle to Cycle Jitter for clock output on regular I/O ($F_{OUT} \geq 100$ MHz)	—	—	600	ps (p-p)
	Cycle to Cycle Jitter for clock output on regular I/O ($F_{OUT} < 100$ MHz)	—	—	60	mUI (p-p)
$t_{CASC\_OUTPJ\_DC}$ *(5)*, *(6)*	Period Jitter for dedicated clock output in cascaded PLLs ($F_{OUT} \geq 100$MHz)	—	—	250	ps (p-p)
	Period Jitter for dedicated clock output in cascaded PLLs ($F_{OUT} < 100$MHz)	—	—	25	mUI (p-p)
f_{DRIFT}	Frequency drift after PFDENA is disabled for duration of 100 us	—	—	±10	%

Notes to Table 1–45:

(1) This specification is limited in the Quartus II software by the I/O maximum frequency. The maximum I/O frequency is different for each I/O standard.

(2) This specification is limited by the lower of the two: I/O F_{MAX} or F_{OUT} of the PLL.

(3) A high input jitter directly affects the PLL output jitter. To have low PLL output clock jitter, you must provide a clean clock source that is less than 120 ps.

(4) F_{REF} is fIN/N when N = 1.

(5) Peak-to-peak jitter with a probability level of 10^{-12} (14 sigma, 99.99999999974404% confidence level). The output jitter specification applies to the intrinsic jitter of the PLL, when an input jitter of 30 ps is applied. The external memory interface clock output jitter specifications use a different measurement method and are available in Table 1–64 on page 1–71.

(6) The cascaded PLL specification is only applicable with the following condition:
a. Upstream PLL: 0.59 Mhz ≤ Upstream PLL BW < 1 MHz
b. Downstream PLL: Downstream PLL BW > 2 MHz

(7) High bandwidth PLL settings are not supported in external feedback mode.

(8) External memory interface clock output jitter specifications use a different measurement method, which is available in Table 1–63 on page 1–71.

Configuration

Table 1–50 lists the configuration mode specifications for Arria II GX and GZ devices.

Table 1–50. Configuration Mode Specifications for Arria II Devices

Programming Mode	DCLK Frequency			Unit
	Min	Typ	Max	
Passive serial	—	—	125	MHz
Fast passive parallel	—	—	125	MHz
Fast active serial (fast clock)	17	26	40	MHz
Fast active serial (slow clock)	8.5	13	20	MHz
Remote update only in fast AS mode	—	—	10	MHz

JTAG Specifications

Table 1–51 lists the JTAG timing parameters and values for Arria II GX and GZ devices.

Table 1–51. JTAG Timing Parameters and Values for Arria II Devices

Symbol	Description	Min	Max	Unit
t_{JCP}	TCK clock period	30	—	ns
t_{JCH}	TCK clock high time	14	—	ns
t_{JCL}	TCK clock low time	14	—	ns
$t_{JPSU\ (TDI)}$	TDI JTAG port setup time	1	—	ns
$t_{JPSU\ (TMS)}$	TMS JTAG port setup time	3	—	ns
t_{JPH}	JTAG port hold time	5	—	ns
t_{JPCO}	JTAG port clock to output	—	11	ns
t_{JPZX}	JTAG port high impedance to valid output	—	14	ns
t_{JPXZ}	JTAG port valid output to high impedance	—	14	ns

Chip-Wide Reset (Dev_CLRn) Specifications

Table 1–52 lists the specifications for the chip-wide reset (Dev_CLRn) for Arria II GX and GZ devices.

Table 1–52. Chip-Wide Reset (Dev_CLRn) Specifications for Arria II Devices

Description	Min	Typ	Max	Unit
Dev_CLRn	500	—	—	µs

Table 1–53. High-Speed I/O Specifications for Arria II GX Devices (Part 3 of 4)

Symbol	Conditions	I3		C4		C5,I5		C6		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{TX_JITTER} *(4)*	True LVDS with dedicated SERDES (data rate 600–1,250 Mbps)	—	175	—	175	—	225	—	300	ps
	True LVDS with dedicated SERDES (data rate < 600 Mbps)	—	0.105	—	0.105	—	0.135	—	0.18	UI
	True LVDS and emulated LVDS_E_3R with logic elements as SERDES (data rate 600 – 945 Mbps)	—	260	—	260	—	300	—	350	ps
	True LVDS and emulated LVDS_E_3R with logic elements as SERDES (data rate < 600 Mbps)	—	0.16	—	0.16	—	0.18	—	0.21	UI
t_{TX_DCD}	True LVDS and emulated LVDS_E_3R	45	55	45	55	45	55	45	55	%
t_{RISE} and t_{FALL}	True LVDS and emulated LVDS_E_3R	—	200	—	200	—	225	—	250	ps
TCCS	True LVDS *(5)*	—	150	—	150	—	175	—	200	ps
	Emulated LVDS_E_3R	—	200	—	200	—	250	—	300	ps
Receiver ***(6)***										
True differential I/O standards - $f_{HSDRDPA}$ (data rate)	SERDES factor J = 3 to 10	150	1250	150	1250	150	1050	150	840	Mbps

Table 1–54. High-Speed I/O Specifications for Arria II GZ Devices *(Note 1), (2), (10)* (Part 2 of 3)

Symbol	Conditions	C3, I3			C4, I4			Unit
		Min	Typ	Max	Min	Typ	Max	
f_{HSCLK_OUT} (output clock frequency)	—	5	—	717 *(7)*	5	—	717 *(7)*	MHz
Transmitter								
f_{HSDR} (true LVDS output data rate)	SERDES factor, J = 3 to 10 (using dedicated SERDES) *(8)*	*(4)*	—	1250	*(4)*	—	1250	Mbps
	SERDES factor J = 2, (using DDR registers)	*(4)*	—	*(5)*	*(4)*	—	*(5)*	Mbps
	SERDES factor J = 1, (uses an SDR register)	*(4)*	—	*(5)*	*(4)*	—	*(5)*	Mbps
f_{HSDR} (emulated LVDS_E_3R output data rate) *(5)*	SERDES factor J = 4 to 10	*(4)*	—	1152	*(4)*	—	800	Mbps
f_{HSDR} (emulated LVDS_E_1R output data rate)		*(4)*	—	200	*(4)*	—	200	Mbps
$t_{x\ Jitter}$	Total jitter for data rate, 600 Mbps to 1.6 Gbps	—	—	160	—	—	160	ps
	Total jitter for data rate, < 600 Mbps	—	—	0.1	—	—	0.1	UI
$t_{x\ Jitter}$ - emulated differential I/O standards with three external output resistor network	Total jitter for data rate, 600 Mbps to 1.25 Gbps	—	—	300	—	—	325	ps
	Total jitter for data rate < 600 Mbps	—	—	0.2	—	—	0.25	UI
$t_{x\ Jitter}$ - emulated differential I/O standards with one external output resistor network	—	—	—	0.15	—	—	0.15	UI
t_{DUTY}	TX output clock duty cycle for both True and emulated differential I/O standards	45	50	55	45	50	55	%

Table 1–55. DPA Lock Time Specifications for Arria II Devices *(Note 1)*, *(2)*, *(3)*

Standard	Training Pattern	Number of Data Transitions in One Repetition of the Training Pattern	Number of Repetitions per 256 Data Transitions *(4)*	Maximum
SPI-4	00000000001111111111	2	128	640 data transitions
Parallel Rapid I/O	00001111	2	128	640 data transitions
	10010000	4	64	640 data transitions
Miscellaneous	10101010	8	32	640 data transitions
	01010101	8	32	640 data transitions

Notes to Table 1–55:

(1) The DPA lock time is for one channel.
(2) One data transition is defined as a 0-to-1 or 1-to-0 transition.
(3) The DPA lock time stated in the table applies to both commercial and industrial grade.
(4) This is the number of repetitions for the stated training pattern to achieve the 256 data transitions.

Figure 1–5 shows the LVDS soft-CDR/DPA sinusoidal jitter tolerance specification for Arria II GZ devices at a data rate less than 1.25 Gbps and all the Arria II GX devices.

Figure 1–5. LVDS Soft-CDR/DPA Sinusoidal Jitter Tolerance Specification for All Arria II GX Devices and for Arria II GZ Devices at a Data Rate less than 1.25 Gbps

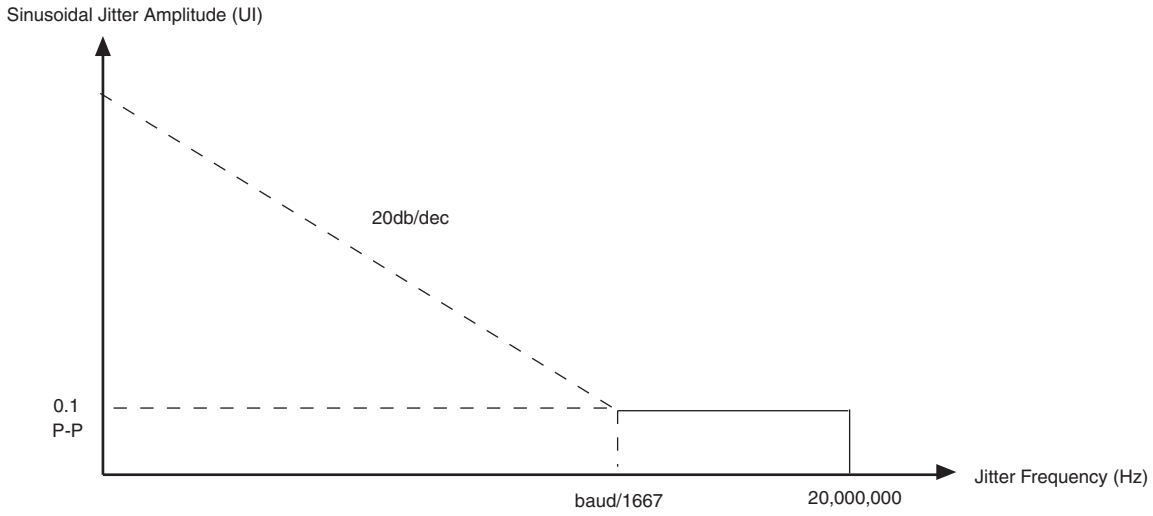


Table 1–60 lists the DQS phase shift error for Arria II GX devices.

Table 1–60. DQS Phase Shift Error Specification for DLL-Delayed Clock (t_{DQS_PSERR}) for Arria II GX Devices *(Note 1)*

Number of DQS Delay Buffer	C4	I3, C5, I5	C6	Unit
1	26	30	36	ps
2	52	60	72	ps
3	78	90	108	ps
4	104	120	144	ps

Note to Table 1–60:

(1) This error specification is the absolute maximum and minimum error. For example, skew on three DQS delay buffers in a C4 speed grade is ± 78 ps or ± 39 ps.

Table 1–61 lists the DQS phase shift error for Arria II GZ devices.

Table 1–61. DQS Phase Shift Error Specification for DLL-Delayed Clock (t_{DQS_PSERR}) for Arria II GZ Devices *(Note 1)*

Number of DQS Delay Buffer	–3	–4	Unit
1	28	30	ps
2	56	60	ps
3	84	90	ps
4	112	120	ps

Note to Table 1–61:

(1) This error specification is the absolute maximum and minimum error. For example, skew on three DQS delay buffers in a 3 speed grade is ± 84 ps or ± 42 ps.

Table 1–62 lists the memory output clock jitter specifications for Arria II GX devices.

Table 1–62. Memory Output Clock Jitter Specification for Arria II GX Devices *(Note 1)*, *(2)*, *(3)*

Parameter	Clock Network	Symbol	–4		–5		–6		Unit
			Min	Max	Min	Max	Min	Max	
Clock period jitter	Global	$t_{JIT(per)}$	-100	100	-125	125	-125	125	ps
Cycle-to-cycle period jitter	Global	$t_{JIT(cc)}$	-200	200	-250	250	-250	250	ps
Duty cycle jitter	Global	$t_{JIT(duty)}$	-100	100	-125	125	-125	125	ps

Notes to Table 1–62:

(1) The memory output clock jitter measurements are for 200 consecutive clock cycles, as specified in the JEDEC DDR2/DDR3 SDRAM standard.

(2) The clock jitter specification applies to memory output clock pins generated using DDIO circuits clocked by a PLL output routed on a global clock network.

(3) The memory output clock jitter stated in Table 1–62 is applicable when an input jitter of 30 ps is applied.

I/O Timing

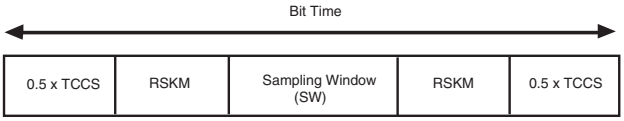
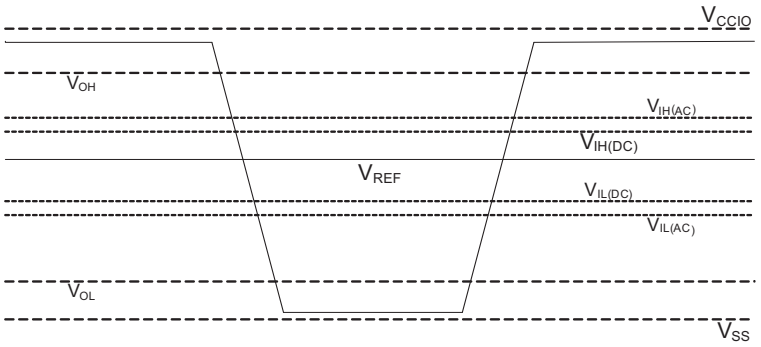
Altera offers two ways to determine I/O timing:

- Using the Microsoft Excel-based I/O Timing.
- Using the Quartus II Timing Analyzer.

The Microsoft Excel-based I/O Timing provides pin timing performance for each device density and speed grade. The data is typically used prior to designing the FPGA to get an estimate of the timing budget as part of the link timing analysis. The Quartus II timing analyzer provides a more accurate and precise I/O timing data based on the specifics of the design after place-and-route is complete.

The Microsoft Excel-based I/O Timing spreadsheet is downloadable from the Literature: Arria II Devices web page.

Table 1–68. Glossary (Part 3 of 4)

Letter	Subject	Definitions
S	**SW (sampling window)**	The period of time during which the data must be valid in order to capture it correctly. The setup and hold times determine the ideal strobe position within the sampling window: *Timing Diagram* 
	Single-ended Voltage Referenced I/O Standard	The JEDEC standard for SSTL and HSTL I/O standards define both the AC and DC input signal values. The AC values indicate the voltage levels at which the receiver must meet its timing specifications. The DC values indicate the voltage levels at which the final logic state of the receiver is unambiguously defined. After the receiver input has crossed the AC value, the receiver changes to the new logic state. The new logic state is then maintained as long as the input stays beyond the AC threshold. This approach is intended to provide predictable receiver timing in the presence of input waveform ringing: *Single-Ended Voltage Referenced I/O Standard* 
T	t_C	High-speed receiver and transmitter input and output clock period.
	TCCS (channel-to-channel-skew)	The timing difference between the fastest and slowest output edges, including t_{CO} variation and clock skew, across channels driven by the same PLL. The clock is included in the TCCS measurement (refer to the *Timing Diagram* figure under **S** in this table).
	t_{DUTY}	High-speed I/O block: Duty cycle on the high-speed transmitter output clock.
		Timing Unit Interval (TUI) The timing budget allowed for skew, propagation delays, and data sampling window. (TUI = 1/(Receiver Input Clock Frequency Multiplication Factor) = t_C/w)
	t_{FALL}	Signal high-to-low transition time (80-20%)
	t_{INCCJ}	Cycle-to-cycle jitter tolerance on the PLL clock input.
	t_{OUTPJ_IO}	Period jitter on the general purpose I/O driven by a PLL.
	t_{OUTPJ_DC}	Period jitter on the dedicated clock output driven by a PLL.
	t_{RISE}	Signal low-to-high transition time (20-80%).