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Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	7612
Number of Logic Elements/Cells	181165
Total RAM Bits	10177536
Number of I/O	372
Number of Gates	-
Voltage - Supply	0.87V ~ 0.93V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	780-BBGA, FCBGA
Supplier Device Package	780-FBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep2agx190ef29c4

Table 1-11. OCT With and Without Calibration Specification for Arria II GX Device I/Os (Note 1) (Part 2 of 2)

Symbol	Description	Conditions (V)	Calibration Accuracy		Unit
			Commercial	Industrial	
50- Ω R_S 3.0, 2.5, 1.8, 1.5, 1.2	50- Ω series OCT with calibration	$V_{CCIO} = 3.0, 2.5,$ 1.8, 1.5, 1.2	± 10	± 10	%
100- Ω R_D 2.5	100- Ω differential OCT without calibration	$V_{CCIO} = 2.5$	± 30	± 30	%

Note to Table 1-11:

(1) OCT with calibration accuracy is valid at the time of calibration only.

Table 1-12 lists the OCT termination calibration accuracy specifications for Arria II GZ devices.

Table 1-12. OCT with Calibration Accuracy Specifications for Arria II GZ Devices (Note 1)

Symbol	Description	Conditions (V)	Calibration Accuracy			Unit
			C2	C3,I3	C4,I4	
25- Ω R_S 3.0, 2.5, 1.8, 1.5, 1.2 (2)	25- Ω series OCT with calibration	$V_{CCIO} = 3.0, 2.5,$ 1.8, 1.5, 1.2	± 8	± 8	± 8	%
50- Ω R_S 3.0, 2.5, 1.8, 1.5, 1.2	50- Ω internal series OCT with calibration	$V_{CCIO} = 3.0, 2.5,$ 1.8, 1.5, 1.2	± 8	± 8	± 8	%
50- Ω R_T 2.5, 1.8, 1.5, 1.2	50- Ω internal parallel OCT with calibration	$V_{CCIO} = 2.5, 1.8,$ 1.5, 1.2	± 10	± 10	± 10	%
20- Ω , 40- Ω , and 60- Ω R_S 3.0, 2.5, 1.8, 1.5, 1.2 (3)	20- Ω , 40- Ω and 60- Ω R_S expanded range for internal series OCT with calibration	$V_{CCIO} = 3.0, 2.5,$ 1.8, 1.5, 1.2	± 10	± 10	± 10	%
25- Ω $R_{S_left_shift}$ 3.0, 2.5, 1.8, 1.5, 1.2	25- Ω $R_{S_left_shift}$ internal left shift series OCT with calibration	$V_{CCIO} = 3.0, 2.5,$ 1.8, 1.5, 1.2	± 10	± 10	± 10	%

Notes to Table 1-12:

- (1) OCT calibration accuracy is valid at the time of calibration only.
 (2) 25- Ω R_S is not supported for 1.5 V and 1.2 V in Row I/O.
 (3) 20- Ω R_S is not supported for 1.5 V and 1.2 V in Row I/O.

The calibration accuracy for calibrated series and parallel OCTs are applicable at the moment of calibration. When process, voltage, and temperature (PVT) conditions change after calibration, the tolerance may change.

Table 1-13 lists the Arria II GZ OCT without calibration resistance tolerance to PVT changes.

Table 1-13. OCT Without Calibration Resistance Tolerance Specifications for Arria II GZ Devices

Symbol	Description	Conditions (V)	Resistance Tolerance		Unit
			C3,I3	C4,I4	
25-Ω R _S 3.0 and 2.5	25-Ω internal series OCT without calibration	V _{CCIO} = 3.0, 2.5	± 40	± 40	%
25-Ω R _S 1.8 and 1.5	25-Ω internal series OCT without calibration	V _{CCIO} = 1.8, 1.5	± 40	± 40	%
25-Ω R _S 1.2	25-Ω internal series OCT without calibration	V _{CCIO} = 1.2	± 50	± 50	%
50-Ω R _S 3.0 and 2.5	50-Ω internal series OCT without calibration	V _{CCIO} = 3.0, 2.5	± 40	± 40	%
50-Ω R _S 1.8 and 1.5	50-Ω internal series OCT without calibration	V _{CCIO} = 1.8, 1.5	± 40	± 40	%
50-Ω R _S 1.2	50-Ω internal series OCT without calibration	V _{CCIO} = 1.2	± 50	± 50	%
100-Ω R _D 2.5	100-Ω internal differential OCT	V _{CCIO} = 2.5	± 25	± 25	%

OCT calibration is automatically performed at power up for OCT-enabled I/Os. When voltage and temperature conditions change after calibration, the resistance may change. Use Equation 1-1 and Table 1-14 to determine the OCT variation when voltage and temperature vary after power-up calibration for Arria II GX and GZ devices.

Equation 1-1. OCT Variation (Note 1)

$$R_{OCT} = R_{SCAL} \left(1 + \left\langle \frac{dR}{dT} \times \Delta T \right\rangle \pm \left\langle \frac{dR}{dV} \times \Delta V \right\rangle \right)$$

Notes to Equation 1-1:

- (1) R_{OCT} value calculated from Equation 1-1 shows the range of OCT resistance with the variation of temperature and V_{CCIO}.

Table 1–34. Transceiver Specifications for Arria II GX Devices (Note 1) (Part 3 of 7)

Symbol/ Description	Condition	I3			C4			C5 and I5			C6			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
fixedclk clock frequency	PCIe Receiver Detect	—	125	—	—	125	—	—	125	—	—	125	—	MHz
reconfig_clk clock frequency	Dynamic reconfig. clock frequency	2.5/ 37.5 (4)	—	50	2.5/ 37.5 (4)	—	50	2.5/ 37.5 (4)	—	50	2.5/ 37.5 (4)	—	50	MHz
Delta time between reconfig_clks (5)	—	—	—	2	—	—	2	—	—	2	—	—	2	ms
Transceiver block minimum power-down pulse width	—	—	1	—	—	1	—	—	1	—	—	1	—	μs
Receiver														
Supported I/O Standards	1.4-V PCML, 1.5-V PCML, 2.5-V PCML, 2.5-V PCML, LVPECL, and LVDS													
Data rate (13)	—	600	—	6375	600	—	3750	600	—	3750	600	—	3125	Mbps
Absolute V _{MAX} for a receiver pin (6)	—	—	—	1.5	—	—	1.5	—	—	1.5	—	—	1.5	V
Absolute V _{MIN} for a receiver pin	—	-0.4	—	—	-0.4	—	—	-0.4	—	—	-0.4	—	—	V
Maximum peak-to-peak differential input voltage V _{ID} (diff p-p)	V _{ICM} = 0.82 V setting	—	—	2.7	—	—	2.7	—	—	2.7	—	—	2.7	V
	V _{ICM} = 1.1 V setting (7)	—	—	1.6	—	—	1.6	—	—	1.6	—	—	1.6	V

Table 1–34. Transceiver Specifications for Arria II GX Devices (Note 1) (Part 6 of 7)

Symbol/ Description	Condition	I3			C4			C5 and I5			C6			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Intra-differential pair skew	—	—	—	15	—	—	15	—	—	15	—	—	15	ps
Intra-transceiver block skew	PCIe ×4	—	—	120	—	—	120	—	—	120	—	—	120	ps
Inter-transceiver block skew	PCIe ×8	—	—	300	—	—	300	—	—	300	—	—	300	ps
CMU PLL0 and CMU PLL1														
CMU PLL lock time from CMUPLL_reset deassertion	—	—	—	100	—	—	100	—	—	100	—	—	100	μs
PLD-Transceiver Interface														
Interface speed	—	25	—	320	25	—	240	25	—	240	25	—	200	MHz

Table 1–34. Transceiver Specifications for Arria II GX Devices (Note 1) (Part 7 of 7)

Symbol/ Description	Condition	I3			C4			C5 and I5			C6			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Digital reset pulse width	—	Minimum is 2 parallel clock cycles												

Notes to Table 1–34:

- (1) For AC-coupled links, the on-chip biasing circuit is switched off before and during configuration. Ensure that input specifications are not violated during this period.
- (2) The rise/fall time is specified from 20% to 80%.
- (3) To calculate the REFCLK rms phase jitter requirement at reference clock frequencies other than 100 MHz, use the following formula:
REFCLK rms phase jitter at f (MHz) = REFCLK rms phase jitter at 100 MHz * 100/f.
- (4) The minimum `reconfig_clk` frequency is 2.5 MHz if the transceiver channel is configured in **Transmitter only** mode. The minimum `reconfig_clk` frequency is 37.5 MHz if the transceiver channel is configured in **Receiver only** or **Receiver and Transmitter** mode. For more information, refer to [AN 558: Implementing Dynamic Reconfiguration in Arria II Devices](#).
- (5) If your design uses more than one dynamic reconfiguration controller instances (`altgx_reconfig`) to control the transceiver channels (`altgx`) physically located on the same side of the device, and if you use different `reconfig_clk` sources for these `altgx_reconfig` instances, the delta time between any two of these `reconfig_clk` sources becoming stable must not exceed the maximum specification listed.
- (6) The device cannot tolerate prolonged operation at this absolute maximum.
- (7) You must use the 1.1-V RX V_{ICM} setting if the input serial data standard is LVDS and the link is DC-coupled.
- (8) The rate matcher supports only up to ± 300 parts per million (ppm).
- (9) Time taken to `rx_pll_locked` goes high from `rx_analogreset` de-assertion. Refer to [Figure 1–1](#).
- (10) The time in which the CDR must be kept in lock-to-reference mode after `rx_pll_locked` goes high and before `rx_locktodata` is asserted in manual mode. Refer to [Figure 1–1](#).
- (11) The time taken to recover valid data after the `rx_locktodata` signal is asserted in manual mode. Refer to [Figure 1–1](#).
- (12) The time taken to recover valid data after the `rx_freqlocked` signal goes high in automatic mode. Refer to [Figure 1–2](#).
- (13) To support data rates lower than the minimum specification through oversampling, use the CDR in LTR mode only.

Table 1-35. Transceiver Specifications for Arria II GZ Devices (Part 2 of 5)

Symbol/ Description	Conditions	–C3 and –I3 (1)			–C4 and –I4			Unit
		Min	Typ	Max	Min	Typ	Max	
Transceiver Clocks								
Calibration block clock frequency (cal_blk_clk)	—	10	—	125	10	—	125	MHz
fixedclk clock frequency	PCIe Receiver Detect	—	125	—	—	125	—	MHz
reconfig_clk clock frequency	Dynamic reconfiguration clock frequency	2.5/ 37.5 (4)	—	50	2.5/ 37.5 (4)	—	50	MHz
Delta time between reconfig_clks (5)	—	—	—	2	—	—	2	ms
Transceiver block minimum power-down (gxb_powerdown) pulse width	—	1	—	—	1	—	—	µs
Receiver								
Supported I/O Standards	1.4-V PCML, 1.5-V PCML, 2.5-V PCML, LVPECL, and LVDS							
Data rate (16)	—	600	—	6375	600	—	3750	Mbps
Absolute V _{MAX} for a receiver pin (6)	—	—	—	1.6	—	—	1.6	V
Operational V _{MAX} for a receiver pin	—	—	—	1.5	—	—	1.5	V
Absolute V _{MIN} for a receiver pin	—	-0.4	—	—	-0.4	—	—	V
Maximum peak-to-peak differential input voltage V _{ID} (diff p-p) before device configuration	—	—	—	1.6	—	—	1.6	V
Maximum peak-to-peak differential input voltage V _{ID} (diff p-p) after device configuration	V _{ICM} = 0.82 V setting	—	—	2.7	—	—	2.7	V
	V _{ICM} = 1.1 V setting (7)	—	—	1.6	—	—	1.6	V
Minimum differential eye opening at receiver serial input pins (8)	Data Rate = 600 Mbps to 5 Gbps Equalization = 0 DC gain = 0 dB	100	—	—	165	—	—	mV
	Data Rate > 5 Gbps Equalization = 0 DC gain = 0 dB	165	—	—	165	—	—	mV
V _{ICM}	V _{ICM} = 0.82 V setting	820 ± 10%			820 ± 10%			mV
	V _{ICM} = 1.1 V setting (7)	1100 ± 10%			1100 ± 10%			mV

Table 1–39. Transmitter Pre-Emphasis Levels for Arria II GZ Devices (Part 2 of 2)

Pre-Emphasis 1st Post-Tap Setting	V _{DD} Setting							
	0	1	2	3	4	5	6	7
29	N/A	N/A	N/A	12.5	9.6	7.7	6.3	4.3
30	N/A	N/A	N/A	N/A	11.4	9	7.4	N/A
31	N/A	N/A	N/A	N/A	12.9	10	8.2	N/A

Table 1–40 lists the transceiver jitter specifications for all supported protocols for Arria II GX devices.

Table 1–40. Transceiver Block Jitter Specifications for Arria II GX Devices (Note 1) (Part 1 of 10)

Symbol/ Description	Conditions	I3			C4			C5, I5			C6			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
SONET/SDH Transmit Jitter Generation (2)														
Peak-to-peak jitter at 622.08 Mbps	Pattern = PRBS15	—	—	0.1	—	—	0.1	—	—	0.1	—	—	0.1	UI
RMS jitter at 622.08 Mbps	Pattern = PRBS15	—	—	0.01	—	—	0.01	—	—	0.01	—	—	0.01	UI
Peak-to-peak jitter at 2488.32 Mbps	Pattern = PRBS15	—	—	0.1	—	—	0.1	—	—	0.1	—	—	0.1	UI
RMS jitter at 2488.32 Mbps	Pattern = PRBS15	—	—	0.01	—	—	0.01	—	—	0.01	—	—	0.01	UI
SONET/SDH Receiver Jitter Tolerance (2)														
Jitter tolerance at 622.08 Mbps	Jitter frequency = 0.03 KHz Pattern = PRBS15	> 15			> 15			> 15			> 15			UI
	Jitter frequency = 25 KHZ Pattern = PRBS15	> 1.5			> 1.5			> 1.5			> 1.5			UI
	Jitter frequency = 250 KHz Pattern = PRBS15	> 0.15			> 0.15			> 0.15			> 0.15			UI

Table 1–40. Transceiver Block Jitter Specifications for Arria II GX Devices (Note 1) (Part 3 of 10)

Symbol/ Description	Conditions	I3			C4			C5, I5			C6			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
PCIe Receiver Jitter Tolerance (4)														
Total jitter at 2.5 Gbps (Gen1)	Compliance pattern	> 0.6			> 0.6			> 0.6			> 0.6			UI
PCIe (Gen 1) Electrical Idle Detect Threshold (9)														
VRX-IDLE-DETDIFF (p-p)	Compliance pattern	65	—	175	65	—	175	65	—	175	65	—	175	mV
Serial RapidIO® (SRIO) Transmit Jitter Generation (5)														
Deterministic jitter (peak-to-peak)	Data Rate = 1.25, 2.5, 3.125 Gbps Pattern = CJPAT	—	—	0.17	—	—	0.17	—	—	0.17	—	—	0.17	UI
Total jitter (peak-to-peak)	Data Rate = 1.25, 2.5, 3.125 Gbps Pattern = CJPAT	—	—	0.35	—	—	0.35	—	—	0.35	—	—	0.35	UI
SRIO Receiver Jitter Tolerance (5)														
Deterministic jitter tolerance (peak-to-peak)	Data Rate = 1.25, 2.5, 3.125 Gbps Pattern = CJPAT	> 0.37			> 0.37			> 0.37			> 0.37			UI
Combined deterministic and random jitter tolerance (peak-to-peak)	Data Rate = 1.25, 2.5, 3.125 Gbps Pattern = CJPAT	> 0.55			> 0.55			> 0.55			> 0.55			UI
Sinusoidal jitter tolerance (peak-to-peak)	Jitter frequency = 22.1 KHz Data rate = 1.25, 2.5, 3.125 Gbps Pattern = CJPAT	> 8.5			> 8.5			> 8.5			> 8.5			UI
	Jitter frequency = 1.875 MHz Data rate = 1.25, 2.5, 3.125 Gbps Pattern = CJPAT	> 0.1			> 0.1			> 0.1			> 0.1			UI
	Jitter frequency = 20 MHz Data rate = 1.25, 2.5, 3.125 Gbps Pattern = CJPAT	> 0.1			> 0.1			> 0.1			> 0.1			UI
GIGE Transmit Jitter Generation (6)														
Deterministic jitter (peak-to-peak)	Pattern = CRPAT	—	—	0.14	—	—	0.14	—	—	0.14	—	—	0.14	UI

Table 1-40. Transceiver Block Jitter Specifications for Arria II GX Devices (Note 1) (Part 8 of 10)

Symbol/ Description	Conditions	I3			C4			C5, I5			C6			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
CPRI Transmit Jitter Generation (11)														
Total jitter	E.6.HV, E.12.HV Pattern = CJPAT	—	—	0.27 9	—	—	0.279	—	—	0.279	—	—	0.279	UI
	E.6.LV, E.12.LV, E.24.LV, E.30.LV Pattern = CJTPAT	—	—	0.35	—	—	0.35	—	—	0.35	—	—	0.35	UI
Deterministic jitter	E.6.HV, E.12.HV Pattern = CJPAT	—	—	0.14	—	—	0.14	—	—	0.14	—	—	0.14	UI
	E.6.LV, E.12.LV, E.24.LV, E.30.LV Pattern = CJTPAT	—	—	0.17	—	—	0.17	—	—	0.17	—	—	0.17	UI
CPRI Receiver Jitter Tolerance (11)														
Total jitter tolerance	E.6.HV, E.12.HV Pattern = CJPAT	> 0.66			> 0.66			> 0.66			> 0.66			UI
Deterministic jitter tolerance	E.6.HV, E.12.HV Pattern = CJPAT	> 0.4			> 0.4			> 0.4			> 0.4			UI
Total jitter tolerance	E.6.LV, E.12.LV, E.24.LV, E.30.LV Pattern = CJTPAT	> 0.65			> 0.65			> 0.65			> 0.65			UI
	E.60.LV Pattern = PRBS31	> 0.6			—			—			—			UI
Deterministic jitter tolerance	E.6.LV, E.12.LV, E.24.LV, E.30.LV Pattern = CJTPAT	> 0.37			> 0.37			> 0.37			> 0.37			UI
	E.60.LV Pattern = PRBS31	> 0.45			—			—			—			UI
Combined deterministic and random jitter tolerance	E.6.LV, E.12.LV, E.24.LV, E.30.LV Pattern = CJTPAT	> 0.55			> 0.55			> 0.55			> 0.55			UI
OBSAI Transmit Jitter Generation (12)														
Total jitter at 768 Mbps, 1536 Mbps, and 3072 Mbps	REFCLK = 153.6 MHz Pattern = CJPAT	—	—	0.35	—	—	0.35	—	—	0.35	—	—	0.35	UI
Deterministic jitter at 768 Mbps, 1536 Mbps, and 3072 Mbps	REFCLK = 153.6 MHz Pattern = CJPAT	—	—	0.17	—	—	0.17	—	—	0.17	—	—	0.17	UI

Table 1-40. Transceiver Block Jitter Specifications for Arria II GX Devices (Note 1) (Part 9 of 10)

Symbol/ Description	Conditions	I3			C4			C5, I5			C6			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
OBSAI Receiver Jitter Tolerance (12)														
Deterministic jitter tolerance at 768 Mbps, 1536 Mbps, and 3072 Mbps	Pattern = CJPAT	> 0.37			> 0.37			> 0.37			> 0.37			UI
Combined deterministic and random jitter tolerance at 768 Mbps, 1536 Mbps, and 3072 Mbps	Pattern = CJPAT	> 0.55			> 0.55			> 0.55			> 0.55			UI
Sinusoidal jitter tolerance at 768 Mbps	Jitter frequency = 5.4 KHz Pattern = CJPAT	> 8.5			> 8.5			> 8.5			> 8.5			UI
	Jitter frequency = 460.8 KHz to 20 MHz Pattern = CJPAT	> 0.1			> 0.1			> 0.1			> 0.1			UI
Sinusoidal jitter tolerance at 1536 Mbps	Jitter frequency = 10.9 KHz Pattern = CJPAT	> 8.5			> 8.5			> 8.5			> 8.5			UI
	Jitter frequency = 921.6 KHz to 20 MHz Pattern = CJPAT	> 0.1			> 0.1			> 0.1			> 0.1			UI

Table 1–41. Transceiver Block Jitter Specifications for Arria II GZ Devices (Note 1), (2) (Part 5 of 7)

Symbol/ Description	Conditions	–C3 and –I3			–C4 and –I4			Unit
		Min	Typ	Max	Min	Typ	Max	
Sinusoidal jitter tolerance (peak-to-peak)	Jitter Frequency = 38.2 KHz Data rate = 6.375 Gbps Pattern = PRBS31 BER = 10 ⁻¹²	> 0.5			—	—	—	UI
	Jitter Frequency = 3.82 MHz Data rate = 6.375 Gbps Pattern = PRBS31 BER = 10 ⁻¹²	> 0.05			—	—	—	UI
	Jitter Frequency = 20 MHz Data rate = 6.375 Gbps Pattern = PRBS31 BER = 10 ⁻¹²	> 0.05			—	—	—	UI
SDI Transmitter Jitter Generation (12)								
Alignment jitter (peak-to-peak)	Data rate = 1.485 Gbps (HD) Pattern = color bar Low-frequency roll-off = 100 KHz	0.2	—	—	0.2	—	—	UI
	Data rate = 2.97 Gbps (3G) Pattern = color bar Low-frequency roll-off = 100 KHz	0.3	—	—	0.3	—	—	UI
SDI Receiver Jitter Tolerance (12)								
Sinusoidal jitter tolerance (peak-to-peak)	Jitter frequency = 15 KHz Data rate = 2.97 Gbps (3G) Pattern = single line scramble color bar	> 2			> 2			UI
	Jitter frequency = 100 KHz Data rate = 2.97 Gbps (3G) Pattern = single line scramble color bar	> 0.3			> 0.3			UI
	Jitter frequency = 148.5 MHz Data rate = 2.97 Gbps (3G) Pattern = single line scramble color bar	> 0.3			> 0.3			UI
Sinusoidal jitter tolerance (peak-to-peak)	Jitter frequency = 20 KHz Data rate = 1.485 Gbps (HD) pattern = 75% color bar	> 1			> 1			UI
	Jitter frequency = 100 KHz Data rate = 1.485 Gbps (HD) Pattern = 75% color bar	> 0.2			> 0.2			UI
	Jitter frequency = 148.5 MHz Data rate = 1.485 Gbps (HD) Pattern = 75% color bar	> 0.2			> 0.2			UI
SAS Transmit Jitter Generation (13)								
Total jitter at 1.5 Gbps (G1)	Pattern = CJPAT	—	—	0.55	—	—	0.55	UI
Deterministic jitter at 1.5 Gbps (G1)	Pattern = CJPAT	—	—	0.35	—	—	0.35	UI
Total jitter at 3.0 Gbps (G2)	Pattern = CJPAT	—	—	0.55	—	—	0.55	UI

Core Performance Specifications for the Arria II Device Family

This section describes the clock tree, phase-locked loop (PLL), digital signal processing (DSP), embedded memory, configuration, and JTAG specifications for Arria II GX and GZ devices.

Clock Tree Specifications

Table 1-42 lists the clock tree specifications for Arria II GX devices.

Table 1-42. Clock Tree Performance for Arria II GX Devices

Clock Network	Performance			Unit
	I3, C4	C5,I5	C6	
GCLK and RCLK	500	500	400	MHz
PCLK	420	350	280	MHz

Table 1-43 lists the clock tree specifications for Arria II GZ devices.

Table 1-43. Clock Tree Performance for Arria II GZ Devices

Clock Network	Performance		Unit
	-C3 and -I3	-C4 and -I4	
GCLK and RCLK	700	500	MHz
PCLK	500	450	MHz

PLL Specifications

Table 1-44 lists the PLL specifications for Arria II GX devices.

Table 1-44. PLL Specifications for Arria II GX Devices (Part 1 of 3)

Symbol	Description	Min	Typ	Max	Unit
f_{IN}	Input clock frequency (from clock input pins residing in right/top/bottom banks) (-4 Speed Grade)	5	—	670 (1)	MHz
	Input clock frequency (from clock input pins residing in right/top/bottom banks) (-5 Speed Grade)	5	—	622 (1)	MHz
	Input clock frequency (from clock input pins residing in right/top/bottom banks) (-6 Speed Grade)	5	—	500 (1)	MHz
f_{INPFD}	Input frequency to the PFD	5	—	325	MHz
f_{VCO}	PLL VCO operating Range (2)	600	—	1,400	MHz
f_{INDUTY}	Input clock duty cycle	40	—	60	%
$f_{EINDUTY}$	External feedback clock input duty cycle	40	—	60	%
t_{INCCJ} (3), (4)	Input clock cycle-to-cycle jitter (Frequency ≥ 100 MHz)	—	—	0.15	UI (p-p)
	Input clock cycle-to-cycle jitter (Frequency ≤ 100 MHz)	—	—	± 750	ps (p-p)

Table 1–44. PLL Specifications for Arria II GX Devices (Part 2 of 3)

Symbol	Description	Min	Typ	Max	Unit
f_{OUT}	Output frequency for internal global or regional clock (–4 Speed Grade)	—	—	500	MHz
	Output frequency for internal global or regional clock (–5 Speed Grade)	—	—	500	MHz
	Output frequency for internal global or regional clock (–6 Speed Grade)	—	—	400	MHz
f_{OUT_EXT}	Output frequency for external clock output (–4 Speed Grade)	—	—	670 (5)	MHz
	Output frequency for external clock output (–5 Speed Grade)	—	—	622 (5)	MHz
	Output frequency for external clock output (–6 Speed Grade)	—	—	500 (5)	MHz
$t_{OUTDUTY}$	Duty cycle for external clock output (when set to 50%)	45	50	55	%
t_{OUTPJ_DC}	Dedicated clock output period jitter ($f_{OUT} \geq 100$ MHz)	—	—	300	ps (p–p)
	Dedicated clock output period jitter ($f_{OUT} < 100$ MHz)	—	—	30	mUI (p–p)
t_{OUTCCJ_DC}	Dedicated clock output cycle-to-cycle jitter ($f_{OUT} \geq 100$ MHz)	—	—	300	ps (p–p)
	Dedicated clock output cycle-to-cycle jitter ($f_{OUT} < 100$ MHz)	—	—	30	mUI (p–p)
f_{OUTPJ_IO}	Regular I/O clock output period jitter ($f_{OUT} \geq 100$ MHz)	—	—	650	ps (p–p)
	Regular I/O clock output period jitter ($f_{OUT} < 100$ MHz)	—	—	65	mUI (p–p)
f_{OUTCCJ_IO}	Regular I/O clock output cycle-to-cycle jitter ($f_{OUT} \geq 100$ MHz)	—	—	650	ps (p–p)
	Regular I/O clock output cycle-to-cycle jitter ($f_{OUT} < 100$ MHz)	—	—	65	mUI (p–p)
$t_{CONFIGPLL}$	Time required to reconfigure PLL scan chains	—	3.5	—	SCANCLK cycles
$t_{CONFIGPHASE}$	Time required to reconfigure phase shift	—	1	—	SCANCLK cycles
$f_{SCANCLK}$	SCANCLK frequency	—	—	100	MHz
t_{LOCK}	Time required to lock from end of device configuration	—	—	1	ms
t_{DLOCK}	Time required to lock dynamically (after switchover or reconfiguring any non-post-scale counters/delays)	—	—	1	ms
$f_{CL\ BW}$	PLL closed-loop low bandwidth	—	0.3	—	MHz
	PLL closed-loop medium bandwidth	—	1.5	—	MHz
	PLL closed-loop high bandwidth	—	4	—	MHz
t_{PLL_PSERR}	Accuracy of PLL phase shift	—	—	±50	ps
t_{ARESET}	Minimum pulse width on areset signal	10	—	—	ns

Table 1-45. PLL Specifications for Arria II GZ Devices (Part 2 of 2)

Symbol	Parameter	Min	Typ	Max	Unit
t_{DLOCK}	Time required to lock dynamically (after switchover or reconfiguring any non-post-scale counters/delays)	—	—	1	ms
f_{CLBW}	PLL closed-loop low bandwidth	—	0.3	—	MHz
	PLL closed-loop medium bandwidth	—	1.5	—	MHz
	PLL closed-loop high bandwidth (7)	—	4	—	MHz
$t_{\text{PLL_PSERR}}$	Accuracy of PLL phase shift	—	—	±50	ps
t_{ARESET}	Minimum pulse width on the areset signal	10	—	—	ns
t_{INCCJ} (3), (4)	Input clock cycle to cycle jitter ($F_{\text{REF}} \geq 100$ MHz)	—	—	0.15	UI (p-p)
	Input clock cycle to cycle jitter ($F_{\text{REF}} < 100$ MHz)	—	—	±750	ps (p-p)
$t_{\text{OUTPJ_DC}}$ (5)	Period Jitter for dedicated clock output ($F_{\text{OUT}} \geq 100$ MHz)	—	—	175	ps (p-p)
	Period Jitter for dedicated clock output ($F_{\text{OUT}} < 100$ MHz)	—	—	17.5	mUI (p-p)
$t_{\text{OUTCCJ_DC}}$ (5)	Cycle to Cycle Jitter for dedicated clock output ($F_{\text{OUT}} \geq 100$ MHz)	—	—	175	ps (p-p)
	Cycle to Cycle Jitter for dedicated clock output ($F_{\text{OUT}} < 100$ MHz)	—	—	17.5	mUI (p-p)
$t_{\text{OUTPJ_IO}}$ (5), (8)	Period Jitter for clock output on regular I/O ($F_{\text{OUT}} \geq 100$ MHz)	—	—	600	ps (p-p)
	Period Jitter for clock output on regular I/O ($F_{\text{OUT}} < 100$ MHz)	—	—	60	mUI (p-p)
$t_{\text{OUTCCJ_IO}}$ (5), (8)	Cycle to Cycle Jitter for clock output on regular I/O ($F_{\text{OUT}} \geq 100$ MHz)	—	—	600	ps (p-p)
	Cycle to Cycle Jitter for clock output on regular I/O ($F_{\text{OUT}} < 100$ MHz)	—	—	60	mUI (p-p)
$t_{\text{CASC_OUTPJ_DC}}$ (5), (6)	Period Jitter for dedicated clock output in cascaded PLLs ($F_{\text{OUT}} \geq 100$ MHz)	—	—	250	ps (p-p)
	Period Jitter for dedicated clock output in cascaded PLLs ($F_{\text{OUT}} < 100$ MHz)	—	—	25	mUI (p-p)
f_{DRIFT}	Frequency drift after PFDENA is disabled for duration of 100 μ s	—	—	±10	%

Notes to Table 1-45:

- (1) This specification is limited in the Quartus II software by the I/O maximum frequency. The maximum I/O frequency is different for each I/O standard.
- (2) This specification is limited by the lower of the two: I/O F_{MAX} or F_{OUT} of the PLL.
- (3) A high input jitter directly affects the PLL output jitter. To have low PLL output clock jitter, you must provide a clean clock source that is less than 120 ps.
- (4) F_{REF} is f_{IN}/N when $N = 1$.
- (5) Peak-to-peak jitter with a probability level of 10^{-12} (14 sigma, 99.9999999974404% confidence level). The output jitter specification applies to the intrinsic jitter of the PLL, when an input jitter of 30 ps is applied. The external memory interface clock output jitter specifications use a different measurement method and are available in [Table 1-64 on page 1-71](#).
- (6) The cascaded PLL specification is only applicable with the following condition:
 - a. Upstream PLL: $0.59 \text{ MHz} \leq \text{Upstream PLL BW} < 1 \text{ MHz}$
 - b. Downstream PLL: $\text{Downstream PLL BW} > 2 \text{ MHz}$
- (7) High bandwidth PLL settings are not supported in external feedback mode.
- (8) External memory interface clock output jitter specifications use a different measurement method, which is available in [Table 1-63 on page 1-71](#).

DSP Block Specifications

Table 1-46 lists the DSP block performance specifications for Arria II GX devices.

Table 1-46. DSP Block Performance Specifications for Arria II GX Devices (Note 1)

Mode	Resources Used	Performance				Unit
	Number of Multipliers	C4	I3	C5,I5	C6	
9 × 9-bit multiplier	1	380	310	300	250	MHz
12 × 12-bit multiplier	1	380	310	300	250	MHz
18 × 18-bit multiplier	1	380	310	300	250	MHz
36 × 36-bit multiplier	1	350	270	270	220	MHz
18 × 36-bit high-precision multiplier adder mode	1	350	270	270	220	MHz
18 × 18-bit multiply accumulator	4	380	310	300	250	MHz
18 × 18-bit multiply adder	4	380	310	300	250	MHz
18 × 18-bit multiply adder-signed full precision	2	380	310	300	250	MHz
18 × 18-bit multiply adder with loopback (2)	2	275	220	220	180	MHz
36-bit shift (32-bit data)	1	350	270	270	220	MHz
Double mode	1	350	270	270	220	MHz

Notes to Table 1-46:

- (1) Maximum is for a fully-pipelined block with **Round** and **Saturation** disabled.
- (2) Maximum is for loopback input registers disabled, **Round** and **Saturation** disabled, pipeline and output registers enabled.

Table 1-47 lists the DSP block performance specifications for Arria II GZ devices.

Table 1-47. DSP Block Performance Specifications for Arria II GZ Devices (Note 1) (Part 1 of 2)

Mode	Resources Used	Performance		Unit
	Number of Multipliers	-3	-4	
9 × 9-bit multiplier	1	460	400	MHz
12 × 12-bit multiplier	1	500	440	MHz
18 × 18-bit multiplier	1	550	480	MHz
36 × 36-bit multiplier	1	440	380	MHz
18 × 18-bit multiply accumulator	4	440	380	MHz
18 × 18-bit multiply adder	4	470	410	MHz
18 × 18-bit multiply adder-signed full precision	2	450	390	MHz
18 × 18-bit multiply adder with loopback (2)	2	350	310	MHz
36-bit shift (32-bit data)	1	440	380	MHz

Configuration

Table 1–50 lists the configuration mode specifications for Arria II GX and GZ devices.

Table 1–50. Configuration Mode Specifications for Arria II Devices

Programming Mode	DCLK Frequency			Unit
	Min	Typ	Max	
Passive serial	—	—	125	MHz
Fast passive parallel	—	—	125	MHz
Fast active serial (fast clock)	17	26	40	MHz
Fast active serial (slow clock)	8.5	13	20	MHz
Remote update only in fast AS mode	—	—	10	MHz

JTAG Specifications

Table 1–51 lists the JTAG timing parameters and values for Arria II GX and GZ devices.

Table 1–51. JTAG Timing Parameters and Values for Arria II Devices

Symbol	Description	Min	Max	Unit
t_{JCP}	TCK clock period	30	—	ns
t_{JCH}	TCK clock high time	14	—	ns
t_{JCL}	TCK clock low time	14	—	ns
$t_{JPSU(TDI)}$	TDI JTAG port setup time	1	—	ns
$t_{JPSU(TMS)}$	TMS JTAG port setup time	3	—	ns
t_{JPH}	JTAG port hold time	5	—	ns
t_{JPCO}	JTAG port clock to output	—	11	ns
t_{JPZX}	JTAG port high impedance to valid output	—	14	ns
t_{JPXZ}	JTAG port valid output to high impedance	—	14	ns

Chip-Wide Reset (Dev_CLRn) Specifications

Table 1–52 lists the specifications for the chip-wide reset (Dev_CLRn) for Arria II GX and GZ devices.

Table 1–52. Chip-Wide Reset (Dev_CLRn) Specifications for Arria II Devices

Description	Min	Typ	Max	Unit
Dev_CLRn	500	—	—	μs

Table 1–53. High-Speed I/O Specifications for Arria II GX Devices (Part 4 of 4)

Symbol	Conditions	I3		C4		C5,I5		C6		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
f_{HSDR} (data rate)	SERDES factor J = 3 to 10	(3)	945 (7)	(3)	945 (7)	(3)	740 (7)	(3)	640 (7)	Mbps
	SERDES factor J = 2 (using DDR registers)	(3)	(7)	(3)	(7)	(3)	(7)	(3)	(7)	Mbps
	SERDES factor J = 1 (using SDR registers)	(3)	(7)	(3)	(7)	(3)	(7)	(3)	(7)	Mbps
Soft-CDR PPM tolerance	Soft-CDR mode	—	300	—	300	—	300	—	300	±PPM
DPA run length	DPA mode	—	10,000	—	10,000	—	10,000	—	10,000	UI
Sampling window (SW)	Non-DPA mode (5)	—	300	—	300	—	350	—	400	ps

Notes to Table 1–53:

- (1) $f_{\text{HCLK_IN}} = f_{\text{HSDR}} / W$. Use W to determine the supported selection of input reference clock frequencies for the desired data rate.
- (2) Applicable for interfacing with DPA receivers only. For interfacing with non-DPA receivers, you must calculate the leftover timing margin in the receiver by performing link timing closure analysis. For Arria II GX transmitter to Arria II GX non-DPA receiver, the maximum supported data rate is 945 Mbps. For data rates above 840 Mbps, perform PCB trace compensation by adjusting the PCB trace length for LVDS channels to improve channel-to-channel skews.
- (3) The minimum and maximum specification depends on the clock source (for example, PLL and clock pin) and the clock routing resource you use (global, regional, or local). The I/O differential buffer and input register do not have a minimum toggle rate.
- (4) The specification is only applicable under the influence of core noise.
- (5) Applicable for true LVDS using dedicated SERDES only.
- (6) Dedicated SERDES and DPA features are only available on the right banks.
- (7) You must calculate the leftover timing margin in the receiver by performing link timing closure analysis. You must consider the board skew margin, transmitter channel-to-channel skew, and the receiver sampling margin to determine the leftover timing margin.

Table 1–54 lists the high-speed I/O timing for Arria II GZ devices.

Table 1–54. High-Speed I/O Specifications for Arria II GZ Devices (Note 1), (2), (10) (Part 1 of 3)

Symbol	Conditions	C3, I3			C4, I4			Unit
		Min	Typ	Max	Min	Typ	Max	
Clock								
f _{HCLK_in} (input clock frequency) true differential I/O standards	Clock boost factor W = 1 to 40 (3)	5	—	717	5	—	717	MHz
f _{HCLK_in} (input clock frequency) single ended I/O standards (9)	Clock boost factor W = 1 to 40 (3)	5	—	717	5	—	717	MHz
f _{HCLK_in} (input clock frequency) single ended I/O standards (10)	Clock boost factor W = 1 to 40 (3)	5	—	420	5	—	420	MHz

Table 1-54. High-Speed I/O Specifications for Arria II GZ Devices (Note 1), (2), (10) (Part 2 of 3)

Symbol	Conditions	C3, I3			C4, I4			Unit
		Min	Typ	Max	Min	Typ	Max	
$f_{\text{HCLK_OUT}}$ (output clock frequency)	—	5	—	717 (7)	5	—	717 (7)	MHz
Transmitter								
f_{HSDR} (true LVDS output data rate)	SERDES factor, J = 3 to 10 (using dedicated SERDES) (8)	(4)	—	1250	(4)	—	1250	Mbps
	SERDES factor J = 2, (using DDR registers)	(4)	—	(5)	(4)	—	(5)	Mbps
	SERDES factor J = 1, (uses an SDR register)	(4)	—	(5)	(4)	—	(5)	Mbps
f_{HSDR} (emulated LVDS_E_3R output data rate) (5)	SERDES factor J = 4 to 10	(4)	—	1152	(4)	—	800	Mbps
f_{HSDR} (emulated LVDS_E_1R output data rate)		(4)	—	200	(4)	—	200	Mbps
$t_{\text{x Jitter}}$	Total jitter for data rate, 600 Mbps to 1.6 Gbps	—	—	160	—	—	160	ps
	Total jitter for data rate, < 600 Mbps	—	—	0.1	—	—	0.1	UI
$t_{\text{x Jitter}}$ - emulated differential I/O standards with three external output resistor network	Total jitter for data rate, 600 Mbps to 1.25 Gbps	—	—	300	—	—	325	ps
	Total jitter for data rate < 600 Mbps	—	—	0.2	—	—	0.25	UI
$t_{\text{x Jitter}}$ - emulated differential I/O standards with one external output resistor network	—	—	—	0.15	—	—	0.15	UI
t_{DUTY}	TX output clock duty cycle for both True and emulated differential I/O standards	45	50	55	45	50	55	%

Table 1-57. External Memory Interface Specifications for Arria II GX Devices (Part 2 of 2)

Frequency Mode	Frequency Range (MHz)			Resolution (°)	DQS Delay Buffer Mode (1)	Number of Delay Chains
	C4	I3, C5, I5	C6			
5	270-410	270-380	270-320	36	High	10
6	320-450	320-410	320-370	45	High	8

Note to Table 1-57:

(1) Low indicates a 6-bit DQS delay setting; high indicates a 5-bit DQS delay setting.

Table 1-58 lists the DLL frequency range specifications for Arria II GZ devices.

Table 1-58. DLL Frequency Range Specifications for Arria II GZ Devices

Frequency Mode	Frequency Range (MHz)		Available Phase Shift	DQS Delay Buffer Mode (1)	Number of Delay Chains
	-3	-4			
0	90-130	90-120	22.5°, 45°, 67.5°, 90°	Low	16
1	120-170	120-160	30°, 60°, 90°, 120°	Low	12
2	150-210	150-200	36°, 72°, 108°, 144°	Low	10
3	180-260	180-240	45°, 90°, 135°, 180°	Low	8
4	240-320	240-290	30°, 60°, 90°, 120°	High	12
5	290-380	290-360	36°, 72°, 108°, 144°	High	10
6	360-450	360-450	45°, 90°, 135°, 180°	High	8
7	470-630	470-590	60°, 120°, 180°, 240°	High	6

Note to Table 1-58:

(1) Low indicates a 6-bit DQS delay setting; high indicates a 5-bit DQS delay setting.

Table 1-59 lists the DQS phase offset delay per stage for Arria II GX devices.

Table 1-59. DQS Phase Offset Delay Per Setting for Arria II GX Devices (Note 1), (2), (3)

Speed Grade	Min	Max	Unit
C4	7.0	13.0	ps
I3, C5, I5	7.0	15.0	ps
C6	8.5	18.0	ps

Notes to Table 1-59:

- (1) The valid settings for phase offset are -64 to +63 for frequency modes 0 to 3 and -32 to +31 for frequency modes 4 to 5.
- (2) The typical value equals the average of the minimum and maximum values.
- (3) The delay settings are linear.

Table 1–60 lists the DQS phase shift error for Arria II GX devices.

Table 1–60. DQS Phase Shift Error Specification for DLL-Delayed Clock (t_{DQS_PSERR}) for Arria II GX Devices (Note 1)

Number of DQS Delay Buffer	C4	I3, C5, I5	C6	Unit
1	26	30	36	ps
2	52	60	72	ps
3	78	90	108	ps
4	104	120	144	ps

Note to Table 1–60:

- (1) This error specification is the absolute maximum and minimum error. For example, skew on three DQS delay buffers in a C4 speed grade is ± 78 ps or ± 39 ps.

Table 1–61 lists the DQS phase shift error for Arria II GZ devices.

Table 1–61. DQS Phase Shift Error Specification for DLL-Delayed Clock (t_{DQS_PSERR}) for Arria II GZ Devices (Note 1)

Number of DQS Delay Buffer	–3	–4	Unit
1	28	30	ps
2	56	60	ps
3	84	90	ps
4	112	120	ps

Note to Table 1–61:

- (1) This error specification is the absolute maximum and minimum error. For example, skew on three DQS delay buffers in a 3 speed grade is ± 84 ps or ± 42 ps.

Table 1–62 lists the memory output clock jitter specifications for Arria II GX devices.

Table 1–62. Memory Output Clock Jitter Specification for Arria II GX Devices (Note 1), (2), (3)

Parameter	Clock Network	Symbol	–4		–5		–6		Unit
			Min	Max	Min	Max	Min	Max	
Clock period jitter	Global	$t_{JIT(per)}$	-100	100	-125	125	-125	125	ps
Cycle-to-cycle period jitter	Global	$t_{JIT(cc)}$	-200	200	-250	250	-250	250	ps
Duty cycle jitter	Global	$t_{JIT(duty)}$	-100	100	-125	125	-125	125	ps

Notes to Table 1–62:

- (1) The memory output clock jitter measurements are for 200 consecutive clock cycles, as specified in the JEDEC DDR2/DDR3 SDRAM standard.
- (2) The clock jitter specification applies to memory output clock pins generated using DDIO circuits clocked by a PLL output routed on a global clock network.
- (3) The memory output clock jitter stated in Table 1–62 is applicable when an input jitter of 30 ps is applied.