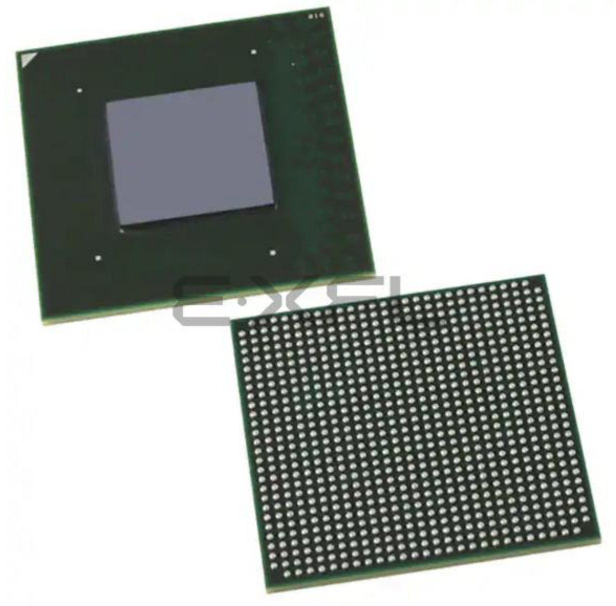
# Intel - EP2AGX190EF29C4N Datasheet



**Welcome to** **E-XFL.COM**

## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

| **Details** | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | 7612 |
| Number of Logic Elements/Cells | 181165 |
| Total RAM Bits | 10177536 |
| Number of I/O | 372 |
| Number of Gates | - |
| Voltage - Supply | 0.87V ~ 0.93V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 85°C (TJ) |
| Package / Case | 780-BBGA, FCBGA |
| Supplier Device Package | 780-FBGA (29x29) |
| Purchase URL | https://www.e-xfl.com/product-detail/intel/ep2agx190ef29c4n |

**Table 1–5. Recommended Operating Conditions for Arria II GX Devices *(Note 1)* (Part 2 of 2)**

| Symbol | Description | Condition | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|---|
| $t_{RAMP}$ | Power Supply Ramp time | Normal POR | 0.05 | — | 100 | ms |
| | | Fast POR | 0.05 | — | 4 | ms |

**Notes to Table 1–5:**

(1) For more information about supply pin connections, refer to the *Arria II Device Family Pin Connection Guidelines*.

(2) Altera recommends a 3.0-V nominal battery voltage when connecting $V_{CCBAT}$ to a battery for volatile key backup. If you do not use the volatile security key, you may connect the $V_{CCBAT}$ to either GND or a 3.0-V power supply.

(3) $V_{CCPD}$ must be 2.5-V for I/O banks with 2.5-V and lower $V_{CCIO}$, 3.0-V for 3.0-V $V_{CCIO}$, and 3.3-V for 3.3-V $V_{CCIO}$.

(4) $V_{CCIO}$ for 3C and 8C I/O banks where the configuration pins reside only supports 3.3-, 3.0-, 2.5-, or 1.8-V voltage levels.

Table 1–6 lists the recommended operating conditions for Arria II GZ devices.

**Table 1–6. Recommended Operating Conditions for Arria II GZ Devices *(Note 6)* (Part 1 of 2)**

| Symbol | Description | Condition | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Core voltage and periphery circuitry power supply | — | 0.87 | 0.90 | 0.93 | V |
| $V_{CCCB}$ | Supplies power for the configuration RAM bits | — | 1.45 | 1.50 | 1.55 | V |
| $V_{CCAUX}$ | Auxiliary supply | — | 2.375 | 2.5 | 2.625 | V |
| $V_{CCPD}$ *(2)* | I/O pre-driver (3.0 V) power supply | — | 2.85 | 3.0 | 3.15 | V |
| | I/O pre-driver (2.5 V) power supply | — | 2.375 | 2.5 | 2.625 | V |
| $V_{CCIO}$ | I/O buffers (3.0 V) power supply | — | 2.85 | 3.0 | 3.15 | V |
| | I/O buffers (2.5 V) power supply | — | 2.375 | 2.5 | 2.625 | V |
| | I/O buffers (1.8 V) power supply | — | 1.71 | 1.8 | 1.89 | V |
| | I/O buffers (1.5 V) power supply | — | 1.425 | 1.5 | 1.575 | V |
| | I/O buffers (1.2 V) power supply | — | 1.14 | 1.2 | 1.26 | V |
| $V_{CCPGM}$ | Configuration pins (3.0 V) power supply | — | 2.85 | 3.0 | 3.15 | V |
| | Configuration pins (2.5 V) power supply | — | 2.375 | 2.5 | 2.625 | V |
| | Configuration pins (1.8 V) power supply | — | 1.71 | 1.8 | 1.89 | V |
| $V_{CCA\_PLL}$ | PLL analog voltage regulator power supply | — | 2.375 | 2.5 | 2.625 | V |
| $V_{CCD\_PLL}$ | PLL digital voltage regulator power supply | — | 0.87 | 0.90 | 0.93 | V |
| $V_{CC\_CLKIN}$ | Differential clock input power supply | — | 2.375 | 2.5 | 2.625 | V |
| $V_{CCBAT}$ *(1)* | Battery back-up power supply (For design security volatile key register) | — | 1.2 | — | 3.3 | V |
| $V_I$ | DC input voltage | — | –0.5 | — | 3.6 | V |
| $V_O$ | Output voltage | — | 0 | — | $V_{CCIO}$ | V |
| $V_{CCA\_L}$ | Transceiver high voltage power (left side) | — | 2.85/2.375 | 3.0/2.5 *(4)* | 3.15/2.625 | V |
| $V_{CCA\_R}$ | Transceiver high voltage power (right side) | — | | | | |
| $V_{CCHIP\_L}$ | Transceiver HIP digital power (left side) | — | 0.87 | 0.9 | 0.93 | V |
| $V_{CCR\_L}$ | Receiver power (left side) | — | 1.05 | 1.1 | 1.15 | V |
| $V_{CCR\_R}$ | Receiver power (right side) | — | 1.05 | 1.1 | 1.15 | V |
| $V_{CCT\_L}$ | Transmitter power (left side) | — | 1.05 | 1.1 | 1.15 | V |
| $V_{CCT\_R}$ | Transmitter power (right side) | — | 1.05 | 1.1 | 1.15 | V |

**Table 1–6. Recommended Operating Conditions for Arria II GZ Devices** *(Note 6)* **(Part 2 of 2)**

| Symbol | Description | Condition | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|---|
| $V_{CCL\_GXBLn}$ (3) | Transceiver clock power (left side) | — | 1.05 | 1.1 | 1.15 | V |
| $V_{CCL\_GXBRn}$ (3) | Transceiver clock power (right side) | — | 1.05 | 1.1 | 1.15 | V |
| $V_{CCH\_GXBLn}$ (3) | Transmitter output buffer power (left side) | — | 1.33/1.425 | 1.4/1.5 (5) | 1.575 | V |
| $V_{CCH\_GXBRn}$ (3) | Transmitter output buffer power (right side) | — | | | | |
| $T_J$ | Operating junction temperature | Commercial | 0 | — | 85 | °C |
| | | Industrial | –40 | — | 100 | °C |
| $t_{RAMP}$ | Power supply ramp time | Normal POR (PORSEL=0) | 0.05 | — | 100 | ms |
| | | Fast POR (PORSEL=1) | 0.05 | — | 4 | ms |

**Notes to Table 1–6:**

(1) Altera recommends a 3.0-V nominal battery voltage when connecting $V_{CCBAT}$ to a battery for volatile key backup. If you do not use the volatile security key, you may connect the $V_{CCBAT}$ to either GND or a 3.0-V power supply.

(2) $V_{CCPD}$ must be 2.5 V when $V_{CCIO}$ is 2.5, 1.8, 1.5, or 1.2 V. $V_{CCPD}$ must be 3.0 V when $V_{CCIO}$ is 3.0 V.

(3) n = 0, 1, or 2.

(4) $V_{CCA\_L/R}$ must be connected to a 3.0-V supply if the clock multiplier unit (CMU) phase-locked loop (PLL), receiver clock data recovery (CDR), or both, are configured at a base data rate > 4.25 Gbps. For data rates up to 4.25 Gbps, you can connect $V_{CCA\_L/R}$ to either 3.0 V or 2.5 V.

(5) $V_{CCH\_GXBL/R}$ must be connected to a 1.4-V supply if the transmitter channel data rate is > 6.5 Gbps. For data rates up to 6.5 Gbps, you can connect $V_{CCH\_GXBL/R}$ to either 1.4 V or 1.5 V.

(6) Transceiver power supplies do not have power-on-reset (POR) circuitry. After initial power-up, violating the transceiver power supply operating conditions could lead to unpredictable link behavior.

## DC Characteristics

This section lists the supply current, I/O pin leakage current, on-chip termination (OCT) accuracy and variation, input pin capacitance, internal weak pull-up and pull-down resistance, hot socketing, and Schmitt trigger input specifications.

### Supply Current

Standby current is the current the device draws after the device is configured with no inputs or outputs toggling and no activity in the device. Because these currents vary largely with the resources used, use the Microsoft Excel-based Early Power Estimator (EPE) to get supply current estimates for your design.

For more information about power estimation tools, refer to the *PowerPlay Early Power Estimator User Guide* and the *PowerPlay Power Analysis* chapter.

Table 1–10 lists the bus hold specifications for Arria II GZ devices.

**Table 1–10. Bus Hold Parameters for Arria II GZ Devices**

| Parameter | Symbol | Cond. | $V_{CCIO}$ (V) | | | | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 1.2 | | 1.5 | | 1.8 | | 2.5 | | 3.0 | | |
| | | | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | |
| Bus-hold Low sustaining current | $I_{SUSL}$ | $V_{IN} > V_{IL}$ (max.) | 22.5 | — | 25.0 | — | 30.0 | — | 50.0 | — | 70.0 | — | µA |
| Bus-hold High sustaining current | $I_{SUSH}$ | $V_{IN} < V_{IH}$ (min.) | -22.5 | — | -25.0 | — | -30.0 | — | -50.0 | — | -70.0 | — | µA |
| Bus-hold Low overdrive current | $I_{ODL}$ | $0V < V_{IN} < V_{CCIO}$ | — | 120 | — | 160 | — | 200 | — | 300 | — | 500 | µA |
| Bus-hold High overdrive current | $I_{ODH}$ | $0V < V_{IN} < V_{CCIO}$ | — | -120 | — | -160 | — | -200 | — | -300 | — | -500 | µA |
| Bus-hold trip point | $V_{TRIP}$ | — | 0.45 | 0.95 | 0.50 | 1.00 | 0.68 | 1.07 | 0.70 | 1.70 | 0.80 | 2.00 | V |

### OCT Specifications

Table 1–11 lists the Arria II GX device and differential OCT with and without calibration accuracy.

**Table 1–11. OCT With and Without Calibration Specification for Arria II GX Device I/Os *(Note 1)* (Part 1 of 2)**

| Symbol | Description | Conditions (V) | Calibration Accuracy | | Unit |
|---|---|---|---|---|---|
| | | | Commercial | Industrial | |
| 25-Ω $R_S$ 3.0, 2.5 | 25-Ω series OCT without calibration | $V_{CCIO}$ = 3.0, 2.5 | ± 30 | ± 40 | % |
| 50-Ω $R_S$ 3.0, 2.5 | 50-Ω series OCT without calibration | $V_{CCIO}$ = 3.0, 2.5 | ± 30 | ± 40 | % |
| 25-Ω $R_S$ 1.8 | 25-Ω series OCT without calibration | $V_{CCIO}$ = 1.8 | ± 40 | ± 50 | % |
| 50-Ω $R_S$ 1.8 | 50-Ω series OCT without calibration | $V_{CCIO}$ = 1.8 | ± 40 | ± 50 | % |
| 25-Ω $R_S$ 1.5, 1.2 | 25-Ω series OCT without calibration | $V_{CCIO}$ = 1.5, 1.2 | ± 50 | ± 50 | % |
| 50-Ω $R_S$ 1.5, 1.2 | 50-Ω series OCT without calibration | $V_{CCIO}$ = 1.5, 1.2 | ± 50 | ± 50 | % |
| 25-Ω $R_S$ 3.0, 2.5, 1.8, 1.5, 1.2 | 25-Ω series OCT with calibration | $V_{CCIO}$ = 3.0, 2.5, 1.8, 1.5, 1.2 | ± 10 | ± 10 | % |

Table 1–19 lists the weak pull-up resistor values for Arria II GZ devices.

**Table 1–19. Internal Weak Pull-Up Resistor for Arria II GZ Devices** *(Note 1)*, *(2)*

| Symbol | Description | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $R_{PU}$ | Value of the I/O pin pull-up resistor before and during configuration, as well as user mode if the programmable pull-up resistor option is enabled. | $V_{CCIO}$ = 3.0 V ±5% *(3)* | — | 25 | — | kΩ |
| | | $V_{CCIO}$ = 2.5 V ±5% *(3)* | — | 25 | — | kΩ |
| | | $V_{CCIO}$ = 1.8 V ±5% *(3)* | — | 25 | — | kΩ |
| | | $V_{CCIO}$ = 1.5 V ±5% *(3)* | — | 25 | — | kΩ |
| | | $V_{CCIO}$ = 1.2 V ±5% *(3)* | — | 25 | — | kΩ |

**Notes to Table 1–19:**

(1) All I/O pins have an option to enable weak pull-up except configuration, test, and JTAG pins.

(2) The internal weak pull-down feature is only available for the JTAG `TCK` pin. The typical value for this internal weak pull-down resistor is approximately 25 kΩ .

(3) Pin pull-up resistance values may be lower if an external source drives the pin higher than $V_{CCIO}$.

### Hot Socketing

Table 1–20 lists the hot-socketing specification for Arria II GX and GZ devices.

**Table 1–20. Hot Socketing Specifications for Arria II Devices**

| Symbol | Description | Maximum |
|---|---|---|
| $I_{IIOPIN(DC)}$ | DC current per I/O pin | 300 μA |
| $I_{IOPIN(AC)}$ | AC current per I/O pin | 8 mA *(1)* |
| $I_{XCVRTX(DC)}$ | DC current per transceiver TX pin | 100 mA |
| $I_{XCVRRX(DC)}$ | DC current per transceiver RX pin | 50 mA |

**Note to Table 1–20:**

(1) The I/O ramp rate is 10 ns or more. For ramp rates faster than 10 ns, $|I_{IOPIN}|$ = C dv/dt, in which “C” is I/O pin capacitance and “dv/dt” is slew rate.

## Schmitt Trigger Input

The Arria II GX device supports Schmitt trigger input on the `TDI`, `TMS`, `TCK`, `nSTATUS`, `nCONFIG`, `nCE`, `CONF_DONE`, and `DCLK` pins. A Schmitt trigger feature introduces hysteresis to the input signal for improved noise immunity, especially for signals with slow edge rates.

Table 1–21 lists the hysteresis specifications across the supported $V_{CCIO}$ range for Schmitt trigger inputs in Arria II GX devices.

**Table 1–21. Schmitt Trigger Input Hysteresis Specifications for Arria II GX Devices**

| Symbol | Description | Condition (V) | Minimum | Unit |
|---|---|---|---|---|
| $V_{Schmitt}$ | Hysteresis for Schmitt trigger input | $V_{CCIO}$ = 3.3 | 220 | mV |
| | | $V_{CCIO}$ = 2.5 | 180 | mV |
| | | $V_{CCIO}$ = 1.8 | 110 | mV |
| | | $V_{CCIO}$ = 1.5 | 70 | mV |

Table 1–33 lists the differential I/O standard specifications for Arria II GZ devices.

**Table 1–33. Differential I/O Standard Specifications for Arria II GZ Devices** *(Note 1)*

| I/O Standard *(2)* | $V_{CCIO}$ (V) | | | $V_{ID}$ (mV) | | | $V_{ICM(DC)}$ (V) | | $V_{OD}$ (V) *(3)* | | | $V_{OCM}$ (V) *(3)* | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | **Min** | **Typ** | **Max** | **Min** | **Cond.** | **Max** | **Min** | **Max** | **Min** | **Typ** | **Max** | **Min** | **Typ** | **Max** |
| 2.5 V LVDS (HIO) | 2.375 | 2.5 | 2.625 | 100 | $V_{CM}$ = 1.25 V | — | 0.05 | 1.8 | 0.247 | — | 0.6 | 1.125 | 1.25 | 1.375 |
| 2.5 V LVDS (VIO) | 2.375 | 2.5 | 2.625 | 100 | $V_{CM}$ = 1.25 V | — | 0.05 | 1.8 | 0.247 | — | 0.6 | 1 | 1.25 | 1.5 |
| RSDS (HIO) | 2.375 | 2.5 | 2.625 | 100 | $V_{CM}$ = 1.25 V | — | 0.3 | 1.4 | 0.1 | 0.2 | 0.6 | 0.5 | 1.2 | 1.4 |
| RSDS (VIO) | 2.375 | 2.5 | 2.625 | 100 | $V_{CM}$ = 1.25 V | — | 0.3 | 1.4 | 0.1 | 0.2 | 0.6 | 0.5 | 1.2 | 1.5 |
| Mini-LVDS (HIO) | 2.375 | 2.5 | 2.625 | 200 | — | 600 | 0.4 | 1.325 | 0.25 | — | 0.6 | 1 | 1.2 | 1.4 |
| Mini-LVDS (VIO) | 2.375 | 2.5 | 2.625 | 200 | — | 600 | 0.4 | 1.325 | 0.25 | — | 0.6 | 1 | 1.2 | 1.5 |
| LVPECL | 2.375 | 2.5 | 2.625 | 300 | — | — | 0.6 | 1.8 | — | — | — | — | — | — |
| BLVDS *(4)* | 2.375 | 2.5 | 2.625 | 100 | — | — | — | — | — | — | — | — | — | — |

**Notes to Table 1–33:**

(1) 1.4-V/1.5-V PCML transceiver I/O standard specifications are described in "Transceiver Performance Specifications" on page 1–21.

(2) Vertical I/O (VIO) is top and bottom I/Os; horizontal I/O (HIO) is left and right I/Os.

(3) $R_L$ range: $90 \leq RL \leq 110\ \Omega$.

(4) There are no fixed $V_{ICM}$, $V_{OD}$, and $V_{OCM}$ specifications for BLVDS. These specifications depend on the system topology.

## Power Consumption for the Arria II Device Family

Altera offers two ways to estimate power for a design:

- Using the Microsoft Excel-based Early Power Estimator
- Using the Quartus® II PowerPlay Power Analyzer feature

The interactive Microsoft Excel-based Early Power Estimator is typically used prior to designing the FPGA in order to get a magnitude estimate of the device power. The Quartus II PowerPlay Power Analyzer provides better quality estimates based on the specifics of the design after place-and-route is complete. The PowerPlay Power Analyzer can apply a combination of user-entered, simulation-derived, and estimated signal activities which, when combined with detailed circuit models, can yield very accurate power estimates.

For more information about power estimation tools, refer to the *PowerPlay Early Power Estimator User Guide* and the *PowerPlay Power Analysis* chapter in volume 3 of the *Quartus II Handbook.*

**Table 1–34. Transceiver Specifications for Arria II GX Devices** *(Note 1)* **(Part 2 of 7)**

| Symbol/ Description | Condition | I3 | | | C4 | | | C5 and I5 | | | C6 | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Spread-spectrum downspread | PCIe | — | 0 to –0.5% | — | — | 0 to –0.5% | — | — | 0 to –0.5% | — | — | 0 to –0.5% | — | — |
| On-chip termination resistors | — | — | 100 | — | — | 100 | — | — | 100 | — | — | 100 | — | Ω |
| $V_{ICM}$ (AC coupled) | — | 1100 ± 5% | | | 1100 ± 5% | | | 1100 ± 5% | | | 1100 ± 5% | | | mV |
| $V_{ICM}$ (DC coupled) | HCSL I/O standard for PCIe reference clock | 250 | — | 550 | 250 | — | 550 | 250 | — | 550 | 250 | — | 550 | mV |
| Transmitter REFCLK Phase Noise | 10 Hz | — | — | -50 | — | — | -50 | — | — | -50 | — | — | -50 | dBc/Hz |
| | 100 Hz | — | — | -80 | — | — | -80 | — | — | -80 | — | — | -80 | dBc/Hz |
| | 1 KHz | — | — | -110 | — | — | -110 | — | — | -110 | — | — | -110 | dBc/Hz |
| | 10 KHz | — | — | -120 | — | — | -120 | — | — | -120 | — | — | -120 | dBc/Hz |
| | 100 KHz | — | — | -120 | — | — | -120 | — | — | -120 | — | — | -120 | dBc/Hz |
| | ≥ 1 MHz | — | — | -130 | — | — | -130 | — | — | -130 | — | — | -130 | dBc/Hz |
| Transmitter REFCLK Phase Jitter (rms) for 100 MHz REFCLK *(3)* | 10 KHz to 20 MHz | — | — | 3 | — | — | 3 | — | — | 3 | — | — | 3 | ps |
| $R_{ref}$ | — | — | 2000 ± 1% | — | — | 2000 ± 1% | — | — | 2000 ± 1% | — | — | 2000 ± 1% | — | Ω |
| **Transceiver Clocks** | | | | | | | | | | | | | | |
| Calibration block clock frequency (`cal_blk_clk`) | — | 10 | — | 125 | 10 | — | 125 | 10 | — | 125 | 10 | — | 125 | MHz |

**Table 1–34. Transceiver Specifications for Arria II GX Devices** *(Note 1)* **(Part 4 of 7)**

| Symbol/ Description | Condition | I3 | | | C4 | | | C5 and I5 | | | C6 | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Minimum peak-to-peak differential input voltage $V_{ID}$ (diff p-p) | — | 100 | — | — | 100 | — | — | 100 | — | — | 100 | — | — | mV |
| $V_{ICM}$ | $V_{ICM}$ = 0.82 V setting | — | 820 | — | — | 820 | — | — | 820 | — | — | 820 | — | mV |
| | $V_{ICM}$ =1.1 V setting *(7)* | — | 1100 | — | — | 1100 | — | — | 1100 | — | — | 1100 | — | mV |
| Differential on-chip termination resistors | 100–Ω setting | — | 100 | — | — | 100 | — | — | 100 | — | — | 100 | — | Ω |
| Return loss differential mode | PCIe | | | | 50 MHz to 1.25 GHz: –10dB | | | | | | | | | |
| | XAUI | | | | 100 MHz to 2.5 GHz: –10dB | | | | | | | | | |
| Return loss common mode | PCIe | | | | 50 MHz to 1.25 GHz: –6dB | | | | | | | | | |
| | XAUI | | | | 100 MHz to 2.5 GHz: –6dB | | | | | | | | | |
| Programmable PPM detector *(8)* | — | ± 62.5, 100, 125, 200,<br>250, 300, 500, 1000 | | | | | | | | | | | | ppm |
| Run length | — | — | 80 | — | — | 80 | — | — | 80 | — | — | 80 | — | UI |
| Programmable equalization | — | — | — | 7 | — | — | 7 | — | — | 7 | — | — | 7 | dB |
| Signal detect/loss threshold | PCIe Mode | 65 | — | 175 | 65 | — | 175 | 65 | — | 175 | 65 | — | 175 | mV |
| CDR LTR time *(9)* | — | — | — | 75 | — | — | 75 | — | — | 75 | — | — | 75 | µs |
| CDR minimum T1b *(10)* | — | 15 | — | — | 15 | — | | 15 | — | — | 15 | — | — | µs |

### Table 1–34. Transceiver Specifications for Arria II GX Devices *(Note 1)* (Part 7 of 7)

| Symbol/ Description | Condition | I3 | | | C4 | | | C5 and I5 | | | C6 | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Digital reset pulse width | — | Minimum is 2 parallel clock cycles | | | | | | | | | | | | |

**Notes to Table 1–34:**

(1) For AC-coupled links, the on-chip biasing circuit is switched off before and during configuration. Ensure that input specifications are not violated during this period.

(2) The rise/fall time is specified from 20% to 80%.

(3) To calculate the REFCLK rms phase jitter requirement at reference clock frequencies other than 100 MHz, use the following formula:
REFCLK rms phase jitter at f (MHz) = REFCLK rms phase jitter at 100 MHz * 100/f.

(4) The minimum `reconfig_clk` frequency is 2.5 MHz if the transceiver channel is configured in **Transmitter only** mode. The minimum `reconfig_clk` frequency is 37.5 MHz if the transceiver channel is configured in **Receiver only** or **Receiver and Transmitter** mode. For more information, refer to *AN 558: Implementing Dynamic Reconfiguration in Arria II Devices*.

(5) If your design uses more than one dynamic reconfiguration controller instances (`altgx_reconfig`) to control the transceiver channels (`altgx`) physically located on the same side of the device, and if you use different `reconfig_clk` sources for these `altgx_reconfig` instances, the delta time between any two of these `reconfig_clk` sources becoming stable must not exceed the maximum specification listed.

(6) The device cannot tolerate prolonged operation at this absolute maximum.

(7) You must use the 1.1-V RX $V_{ICM}$ setting if the input serial data standard is LVDS and the link is DC-coupled.

(8) The rate matcher supports only up to ±300 parts per million (ppm).

(9) Time taken to `rx_pll_locked` goes high from `rx_analogreset` de-assertion. Refer to Figure 1–1.

(10) The time in which the CDR must be kept in lock-to-reference mode after `rx_pll_locked` goes high and before `rx_locktodata` is asserted in manual mode. Refer to Figure 1–1.

(11) The time taken to recover valid data after the `rx_locktodata` signal is asserted in manual mode. Refer to Figure 1–1.

(12) The time taken to recover valid data after the `rx_freqlocked` signal goes high in automatic mode. Refer to Figure 1–2.

(13) To support data rates lower than the minimum specification through oversampling, use the CDR in LTR mode only.

Table 1–35 lists the transceiver specifications for Arria II GZ devices.

**Table 1–35. Transceiver Specifications for Arria II GZ Devices (Part 1 of 5)**

| Symbol/ Description | Conditions | –C3 and –I3 *(1)* | | | –C4 and –I4 | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| **Reference Clock** | | | | | | | | |
| Supported I/O Standards | 1.2-V PCML, 1.5-V PCML, 2.5-V PCML, Differential LVPECL, LVDS, and HCSL | | | | | | | |
| Input frequency from `REFCLK` input pins | — | 50 | — | 697 | 50 | — | 637.5 | MHz |
| Phase frequency detector (CMU PLL and receiver CDR) | — | 50 | — | 325 | 50 | — | 325 | MHz |
| Absolute $V_{MAX}$ for a `REFCLK` pin | — | — | — | 1.6 | — | — | 1.6 | V |
| Operational $V_{MAX}$ for a `REFCLK` pin | — | — | — | 1.5 | — | — | 1.5 | V |
| Absolute $V_{MIN}$ for a `REFCLK` pin | — | -0.4 | — | — | -0.4 | — | — | V |
| Rise/fall time *(2)* | — | — | — | 0.2 | — | — | 0.2 | UI |
| Duty cycle | — | 45 | — | 55 | 45 | — | 55 | % |
| Peak-to-peak differential input voltage | — | 200 | — | 1600 | 200 | — | 1600 | mV |
| Spread-spectrum modulating clock frequency | PCIe | 30 | — | 33 | 30 | — | 33 | kHz |
| Spread-spectrum downspread | PCIe | — | 0 to -0.5% | — | — | 0 to -0.5% | — | — |
| On-chip termination resistors | — | — | 100 | — | — | 100 | — | Ω |
| $V_{ICM}$ (AC coupled) | — | 1100 ± 10% | | | 1100 ± 10% | | | mV |
| $V_{ICM}$ (DC coupled) | HCSL I/O standard for PCIe reference clock | 250 | — | 550 | 250 | — | 550 | mV |
| Transmitter REFCLK Phase Noise | 10 Hz | — | — | -50 | — | — | -50 | dBc/Hz |
| | 100 Hz | — | — | -80 | — | — | -80 | dBc/Hz |
| | 1 KHz | — | — | -110 | — | — | -110 | dBc/Hz |
| | 10 KHz | — | — | -120 | — | — | -120 | dBc/Hz |
| | 100 KHz | — | — | -120 | — | — | -120 | dBc/Hz |
| | ≥ 1 MHz | — | — | -130 | — | — | -130 | dBc/Hz |
| Transmitter REFCLK Phase Jitter (rms) for 100 MHz REFCLK *(3)* | 10 KHz to 20 MHz | — | — | 3 | — | — | 3 | ps |
| $R_{REF}$ | — | — | 2000 ± 1% | — | — | 2000 ± 1% | — | Ω |

Figure 1–1 shows the lock time parameters in manual mode.

☞ LTD = lock-to-data. LTR = lock-to-reference.

**Figure 1–1. Lock Time Parameters for Manual Mode**

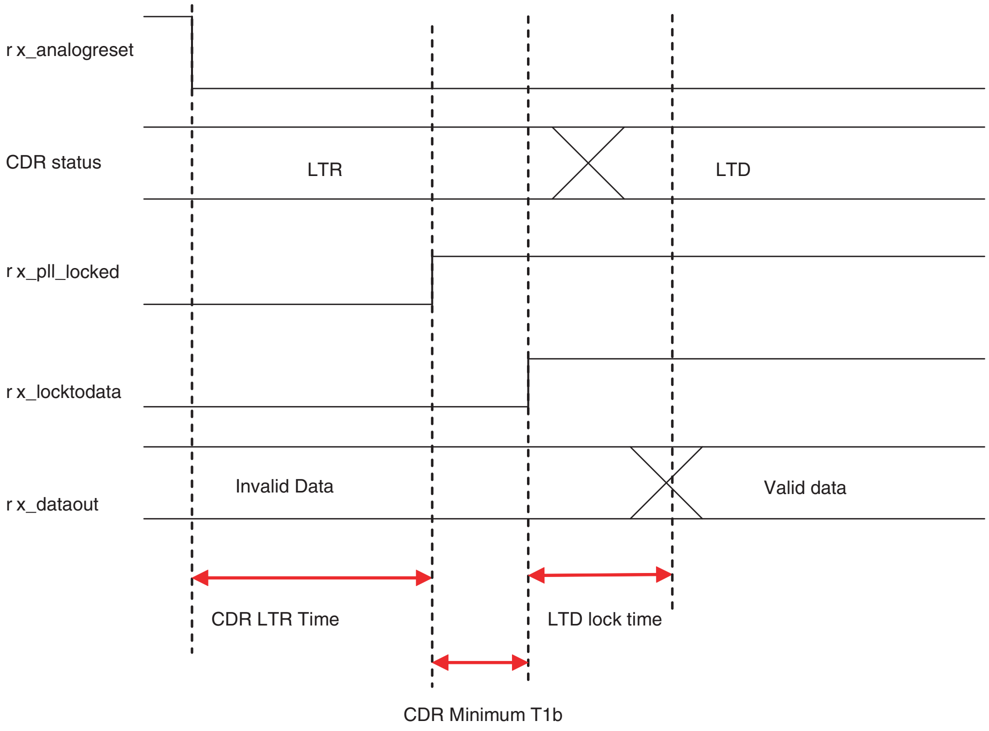


Figure 1–2 shows the lock time parameters in automatic mode.

**Figure 1–2. Lock Time Parameters for Automatic Mode**

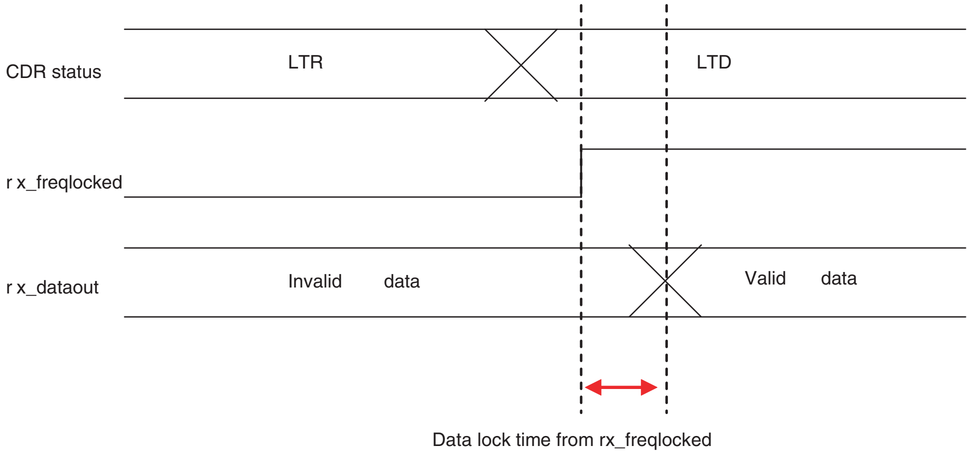


Figure 1–3 shows the differential receiver input waveform.

**Figure 1–3. Receiver Input Waveform**

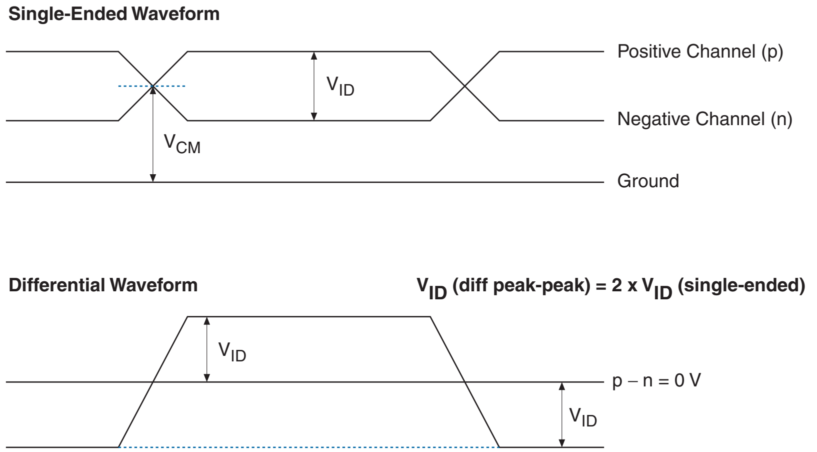


Figure 1–4 shows the transmitter output waveform.

**Figure 1–4. Transmitter Output Waveform**

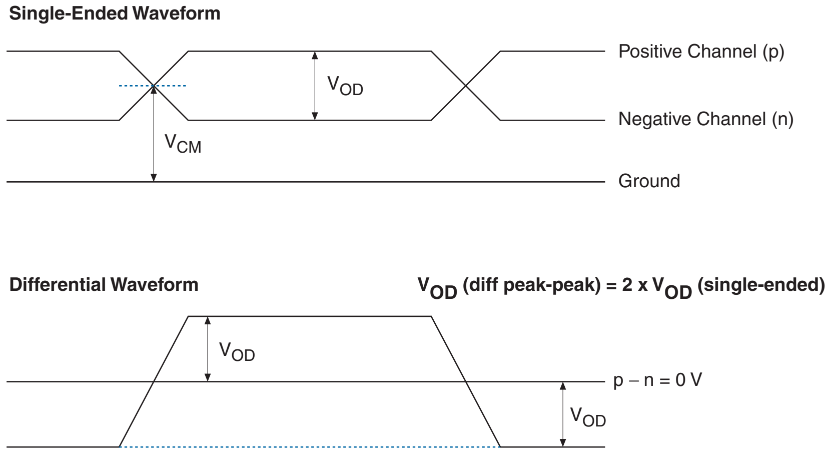


Table 1–36 lists the typical $V_{OD}$ for TX term that equals 85 Ω for Arria II GZ devices.

**Table 1–36. Typical $V_{OD}$ Setting, TX Term = 85 Ω for Arria II GZ Devices**

| Symbol | $V_{OD}$ Setting (mV) | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| $V_{OD}$ differential peak-to-peak Typical (mV) | 170 ± 20% | 340 ± 20% | 510 ± 20% | 595 ± 20% | 680 ± 20% | 765 ± 20% | 850 ± 20% | 1020± 20% |

**Table 1–40. Transceiver Block Jitter Specifications for Arria II GX Devices** ***(Note 1)*** **(Part 6 of 10)**

| Symbol/ Description | Conditions | I3 | | | C4 | | | C5, I5 | | | C6 | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Sinusoidal jitter tolerance (peak-to-peak) | Jitter frequency = 20 KHz<br>Data rate = 1.485 Gbps (HD) Pattern = 75% color bar | > 1 | | | > 1 | | | > 1 | | | > 1 | | | UI |
| | Jitter frequency = 100 KHz Data rate = 1.485 Gbps (HD) Pattern = 75% color bar | > 0.2 | | | > 0.2 | | | > 0.2 | | | > 0.2 | | | UI |
| | Jitter frequency = 148.5 MHz<br>Data rate = 1.485 Gbps (HD) Pattern =75% color bar | > 0.2 | | | > 0.2 | | | > 0.2 | | | > 0.2 | | | UI |
| **SATA Transmit Jitter Generation** *(10)* | | | | | | | | | | | | | | |
| Total jitter at 1.5 Gbps (G1) | Compliance pattern | — | — | 0.55 | — | — | 0.55 | — | — | 0.55 | — | — | 0.55 | UI |
| Deterministic jitter at 1.5 Gbps (G1) | Compliance pattern | — | — | 0.35 | — | — | 0.35 | — | — | 0.35 | — | — | 0.35 | UI |
| Total jitter at 3.0 Gbps (G2) | Compliance pattern | — | — | 0.55 | — | — | 0.55 | — | — | 0.55 | — | — | 0.55 | UI |
| Deterministic jitter at 3.0 Gbps (G2) | Compliance pattern | — | — | 0.35 | — | — | 0.35 | — | — | 0.35 | — | — | 0.35 | UI |
| Total jitter at 6.0 Gbps (G3) | Compliance pattern | — | — | 0.52 | — | — | — | — | — | — | — | — | — | UI |
| Random jitter at 6.0 Gbps (G3) | Compliance pattern | — | — | 0.18 | — | — | — | — | — | — | — | — | — | UI |
| **SATA Receiver Jitter Tolerance** *(10)* | | | | | | | | | | | | | | |
| Total jitter tolerance at 1.5 Gbps (G1) | Compliance pattern | > 0.65 | | | > 0.65 | | | > 0.65 | | | > 0.65 | | | UI |
| Deterministic jitter tolerance at 1.5 Gbps (G1) | Compliance pattern | > 0.35 | | | > 0.35 | | | > 0.35 | | | > 0.35 | | | UI |
| SSC modulation frequency at 1.5 Gbps (G1) | Compliance pattern | 33 | | | 33 | | | 33 | | | 33 | | | kHz |

**Table 1–41. Transceiver Block Jitter Specifications for Arria II GZ Devices** *(Note 1)*, *(2)* **(Part 3 of 7)**

| **Symbol/ Description** | **Conditions** | **–C3 and –I3** | | | **–C4 and –I4** | | | **Unit** |
|---|---|---|---|---|---|---|---|---|
| | | **Min** | **Typ** | **Max** | **Min** | **Typ** | **Max** | |
| Peak-to-peak jitter | Jitter frequency = 22.1 KHz | > 8.5 | | | > 8.5 | | | UI |
| Peak-to-peak jitter | Jitter frequency = 1.875 MHz | > 0.1 | | | > 0.1 | | | UI |
| Peak-to-peak jitter | Jitter frequency = 20 MHz | > 0.1 | | | > 0.1 | | | UI |
| **PCIe Transmit Jitter Generation** *(8)* | | | | | | | | |
| Total jitter at 2.5 Gbps (Gen1)—x1, x4, and x8 | Compliance pattern | — | — | 0.25 | — | — | 0.25 | UI |
| Total jitter at 5 Gbps (Gen2)—x1, x4, and x8 | Compliance pattern | — | — | 0.25 | — | — | — | UI |
| **PCIe Receiver Jitter Tolerance** *(8)* | | | | | | | | |
| Total jitter at 2.5 Gbps (Gen1) | Compliance pattern | > 0.6 | | | > 0.6 | | | UI |
| Total jitter at 5 Gbps (Gen2) | Compliance pattern | Not supported | | | Not supported | | | UI |
| **PCIe (Gen 1) Electrical Idle Detect Threshold** | | | | | | | | |
| $V_{RX\text{-}IDLE\text{-}DETDIFFp\text{-}p}$ *(9)* | Compliance pattern | 65 | — | 175 | 65 | — | 175 | UI |
| **SRIO Transmit Jitter Generation** *(10)* | | | | | | | | |
| Deterministic jitter (peak-to-peak) | Data rate = 1.25, 2.5, 3.125 Gbps<br>Pattern = CJPAT | — | — | 0.17 | — | — | 0.17 | UI |
| Total jitter (peak-to-peak) | Data rate = 1.25, 2.5, 3.125 Gbps<br>Pattern = CJPAT | — | — | 0.35 | — | — | 0.35 | UI |
| **SRIO Receiver Jitter Tolerance** *(10)* | | | | | | | | |
| Deterministic jitter tolerance (peak-to-peak) | Data rate = 1.25, 2.5, 3.125 Gbps<br>Pattern = CJPAT | > 0.37 | | | > 0.37 | | | UI |
| Combined deterministic and random jitter tolerance (peak-to-peak) | Data rate = 1.25, 2.5, 3.125 Gbps<br>Pattern = CJPAT | > 0.55 | | | > 0.55 | | | UI |
| Sinusoidal jitter tolerance (peak-to-peak) | Jitter frequency = 22.1 KHz<br>Data rate = 1.25, 2.5, 3.125 Gbps<br>Pattern = CJPAT | > 8.5 | | | > 8.5 | | | UI |
| | Jitter frequency = 1.875 MHz<br>Data rate = 1.25, 2.5, 3.125 Gbps<br>Pattern = CJPAT | > 0.1 | | | > 0.1 | | | UI |
| | Jitter frequency = 20 MHz<br>Data rate = 1.25, 2.5, 3.125 Gbps<br>Pattern = CJPAT | > 0.1 | | | > 0.1 | | | UI |
| **GIGE Transmit Jitter Generation** *(11)* | | | | | | | | |
| Deterministic jitter (peak-to-peak) | Pattern = CRPAT | — | — | 0.14 | — | — | 0.14 | UI |
| Total jitter (peak-to-peak) | Pattern = CRPAT | — | — | 0.279 | — | — | 0.279 | UI |

**Table 1–44. PLL Specifications for Arria II GX Devices (Part 2 of 3)**

| Symbol | Description | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $f_{OUT}$ | Output frequency for internal global or regional clock (–4 Speed Grade) | — | — | 500 | MHz |
| | Output frequency for internal global or regional clock (–5 Speed Grade) | — | — | 500 | MHz |
| | Output frequency for internal global or regional clock (–6 Speed Grade) | — | — | 400 | MHz |
| $f_{OUT\_EXT}$ | Output frequency for external clock output (–4 Speed Grade) | — | — | 670 *(5)* | MHz |
| | Output frequency for external clock output (–5 Speed Grade) | — | — | 622 *(5)* | MHz |
| | Output frequency for external clock output (–6 Speed Grade) | — | — | 500 *(5)* | MHz |
| $t_{OUTDUTY}$ | Duty cycle for external clock output (when set to 50%) | 45 | 50 | 55 | % |
| $t_{OUTPJ\_DC}$ | Dedicated clock output period jitter ($f_{OUT} \geq 100$ MHz) | — | — | 300 | ps (p–p) |
| | Dedicated clock output period jitter ($f_{OUT} < 100$ MHz) | — | — | 30 | mUI (p–p) |
| $t_{OUTCCJ\_DC}$ | Dedicated clock output cycle-to-cycle jitter ($f_{OUT} \geq 100$ MHz) | — | — | 300 | ps (p–p) |
| | Dedicated clock output cycle-to-cycle jitter ($f_{OUT} < 100$ MHz) | — | — | 30 | mUI (p–p) |
| $f_{OUTPJ\_IO}$ | Regular I/O clock output period jitter ($f_{OUT} \geq 100$ MHz) | — | — | 650 | ps (p–p) |
| | Regular I/O clock output period jitter ($f_{OUT} < 100$ MHz) | — | — | 65 | mUI (p–p) |
| $f_{OUTCCJ\_IO}$ | Regular I/O clock output cycle-to-cycle jitter ($f_{OUT} \geq 100$ MHz) | — | — | 650 | ps (p–p) |
| | Regular I/O clock output cycle-to-cycle jitter ($f_{OUT} < 100$ MHz) | — | — | 65 | mUI (p–p) |
| $t_{CONFIGPLL}$ | Time required to reconfigure PLL scan chains | — | 3.5 | — | SCANCLK cycles |
| $t_{CONFIGPHASE}$ | Time required to reconfigure phase shift | — | 1 | — | SCANCLK cycles |
| $f_{SCANCLK}$ | SCANCLK frequency | — | — | 100 | MHz |
| $t_{LOCK}$ | Time required to lock from end of device configuration | — | — | 1 | ms |
| $t_{DLOCK}$ | Time required to lock dynamically (after switchover or reconfiguring any non-post-scale counters/delays) | — | — | 1 | ms |
| $f_{CL\ B\ W}$ | PLL closed-loop low bandwidth | — | 0.3 | — | MHz |
| | PLL closed-loop medium bandwidth | — | 1.5 | — | MHz |
| | PLL closed-loop high bandwidth | — | 4 | — | MHz |
| $t_{PLL\_PSERR}$ | Accuracy of PLL phase shift | — | — | ±50 | ps |
| $t_{ARESET}$ | Minimum pulse width on `areset` signal | 10 | — | — | ns |

**Table 1–44. PLL Specifications for Arria II GX Devices (Part 3 of 3)**

| Symbol | Description | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $t_{CASC\_OUTJITTER\_PERIOD\_DEDCLK}$ *(6)*, *(7)* | Period Jitter for dedicated clock output in cascaded PLLs (FOUT ≥ 100 MHz) | — | — | 425 | ps (p-p) |
| | Period Jitter for dedicated clock output in cascaded PLLs (FOUT ≤ 100 MHz) | — | — | 42.5 | mUI (p-p) |

**Notes to Table 1–44:**

(1) $f_{IN}$ is limited by the I/O $f_{MAX}$.

(2) The VCO frequency reported by the Quartus II software in the PLL summary section of the compilation report takes into consideration the VCO post-scale counter K value. Therefore, if the counter K has a value of 2, the frequency reported can be lower than the $f_{VCO}$ specification.

(3) A high-input jitter directly affects the PLL output jitter. To have low PLL output clock jitter, you must provide a clean-clock source, which is less than 200 ps.

(4) $F_{REF}$ is fIN/N when N = 1.

(5) This specification is limited by the lower of the two: I/O $f_{MAX}$ or $f_{OUT}$ of the PLL.

(6) Peak-to-peak jitter with a probability level of $10^{-12}$ (14 sigma, 99.99999999974404% confidence level). The output jitter specification applies to the intrinsic jitter of the PLL, when an input jitter of 30 ps is applied. The external memory interface clock output jitter specifications use a different measurement method and are available in Table 1–62 on page 1–70.

(7) The cascaded PLL specification is only applicable with the following condition:
a. Upstream PLL: 0.59 Mhz ≤ Upstream PLL BW < 1 MHz
b. Downstream PLL: Downstream PLL BW > 2 MHz

Table 1–45 lists the PLL specifications for Arria II GZ devices when operating in both the commercial junction temperature range (0° to 85°C) and the industrial junction temperature range (-40° to 100°C).

**Table 1–45. PLL Specifications for Arria II GZ Devices (Part 1 of 2)**

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $f_{IN}$ | Input clock frequency (–3 speed grade) | 5 | — | 717 *(1)* | MHz |
| | Input clock frequency (–4 speed grade) | 5 | — | 717 *(1)* | MHz |
| $f_{INPFD}$ | Input frequency to the PFD | 5 | — | 325 | MHz |
| $f_{VCO}$ | PLL VCO operating range (–3 speed grade) | 600 | — | 1,300 | MHz |
| | PLL VCO operating range (–4 speed grade) | 600 | — | 1,300 | MHz |
| $t_{EINDUTY}$ | Input clock or external feedback clock input duty cycle | 40 | — | 60 | % |
| $f_{OUT}$ | Output frequency for internal global or regional clock (–3 speed grade) | — | — | 700 *(2)* | MHz |
| | Output frequency for internal global or regional clock (–4 speed grade) | — | — | 500 *(2)* | MHz |
| $f_{OUT\_EXT}$ | Output frequency for external clock output (–3 speed grade) | — | — | 717 *(2)* | MHz |
| | Output frequency for external clock output (–4 speed grade) | — | — | 717 *(2)* | MHz |
| $t_{OUTDUTY}$ | Duty cycle for external clock output (when set to 50%) | 45 | 50 | 55 | % |
| $t_{FCOMP}$ | External feedback clock compensation time | — | — | 10 | ns |
| $t_{CONFIGPLL}$ | Time required to reconfigure scan chain | — | 3.5 | — | scanclk cycles |
| $t_{CONFIGPHASE}$ | Time required to reconfigure phase shift | — | 1 | — | scanclk cycles |
| $f_{SCANCLK}$ | scanclk frequency | — | — | 100 | MHz |
| $t_{LOCK}$ | Time required to lock from end-of-device configuration or de-assertion of areset | — | — | 1 | ms |

Table 1–49 lists the embedded memory block specifications for Arria II GZ devices.

**Table 1–49. Embedded Memory Block Performance Specifications for Arria II GZ Devices** *(Note 1)*

| Memory | Mode | Resources Used | | Performance | | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | ALUTs | TriMatrix Memory | C3 | I3 | C4 | I4 | |
| MLAB *(2)* | Single port 64 × 10 | 0 | 1 | 500 | 500 | 450 | 450 | MHz |
| | Simple dual-port 32 × 20 | 0 | 1 | 500 | 500 | 450 | 450 | MHz |
| | Simple dual-port 64 × 10 | 0 | 1 | 500 | 500 | 450 | 450 | MHz |
| | ROM 64 × 10 | 0 | 1 | 500 | 500 | 450 | 450 | MHz |
| | ROM 32 × 20 | 0 | 1 | 500 | 500 | 450 | 450 | MHz |
| M9K Block *(2)* | Single-port 256 × 36 | 0 | 1 | 540 | 540 | 475 | 475 | MHz |
| | Simple dual-port 256 × 36 | 0 | 1 | 490 | 490 | 420 | 420 | MHz |
| | Simple dual-port 256 × 36, with the read-during-write option set to **Old Data** | 0 | 1 | 340 | 340 | 300 | 300 | MHz |
| | True dual port 512 × 18 | 0 | 1 | 430 | 430 | 370 | 370 | MHz |
| | True dual-port 512 × 18, with the read-during-write option set to **Old Data** | 0 | 1 | 335 | 335 | 290 | 290 | MHz |
| | ROM 1 Port | 0 | 1 | 540 | 540 | 475 | 475 | MHz |
| | ROM 2 Port | 0 | 1 | 540 | 540 | 475 | 475 | MHz |
| | Min Pulse Width (clock high time) | — | — | 800 | 800 | 850 | 850 | ps |
| | Min Pulse Width (clock low time) | — | — | 625 | 625 | 690 | 690 | ps |
| M144K Block *(2)* | Single-port 2K × 72 | 0 | 1 | 440 | 400 | 380 | 350 | MHz |
| | Simple dual-port 2K × 72 | 0 | 1 | 435 | 375 | 385 | 325 | MHz |
| | Simple dual-port 2K × 72, with the read-during-write option set to **Old Data** | 0 | 1 | 240 | 225 | 205 | 200 | MHz |
| | Simple dual-port 2K × 64 (with ECC) | 0 | 1 | 300 | 295 | 255 | 250 | MHz |
| | True dual-port 4K × 36 | 0 | 1 | 375 | 350 | 330 | 310 | MHz |
| | True dual-port 4K × 36, with the read-during-write option set to **Old Data** | 0 | 1 | 230 | 225 | 205 | 200 | MHz |
| | ROM 1 Port | 0 | 1 | 500 | 450 | 435 | 420 | MHz |
| | ROM 2 Port | 0 | 1 | 465 | 425 | 400 | 400 | MHz |
| | Min Pulse Width (clock high time) | — | — | 755 | 860 | 860 | 950 | ps |
| | Min Pulse Width (clock low time) | — | — | 625 | 690 | 690 | 690 | ps |

**Notes to Table 1–48:**

(1) To achieve the maximum memory block performance, use a memory block clock that comes through global clock routing from an on-chip PLL set to 50% output duty cycle. Use the Quartus II software to report timing for this and other memory block clocking schemes.

(2) When you use the error detection CRC feature, there is no degradation in $F_{MAX}$.

**Table 1–53. High-Speed I/O Specifications for Arria II GX Devices (Part 3 of 4)**

| Symbol | Conditions | I3 | | C4 | | C5,I5 | | C6 | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| $t_{TX\_JITTER}$ *(4)* | True LVDS with dedicated SERDES (data rate 600–1,250 Mbps) | — | 175 | — | 175 | — | 225 | — | 300 | ps |
| | True LVDS with dedicated SERDES (data rate < 600 Mbps) | — | 0.105 | — | 0.105 | — | 0.135 | — | 0.18 | UI |
| | True LVDS and emulated LVDS_E_3R with logic elements as SERDES (data rate 600 – 945 Mbps) | — | 260 | — | 260 | — | 300 | — | 350 | ps |
| | True LVDS and emulated LVDS_E_3R with logic elements as SERDES (data rate < 600 Mbps) | — | 0.16 | — | 0.16 | — | 0.18 | — | 0.21 | UI |
| $t_{TX\_DCD}$ | True LVDS and emulated LVDS_E_3R | 45 | 55 | 45 | 55 | 45 | 55 | 45 | 55 | % |
| $t_{RISE}$ and $t_{FALL}$ | True LVDS and emulated LVDS_E_3R | — | 200 | — | 200 | — | 225 | — | 250 | ps |
| TCCS | True LVDS *(5)* | — | 150 | — | 150 | — | 175 | — | 200 | ps |
| | Emulated LVDS_E_3R | — | 200 | — | 200 | — | 250 | — | 300 | ps |
| **Receiver** *(6)* | | | | | | | | | | |
| True differential I/O standards - $f_{HSDRDPA}$ (data rate) | SERDES factor J = 3 to 10 | 150 | 1250 | 150 | 1250 | 150 | 1050 | 150 | 840 | Mbps |

**Table 1–54. High-Speed I/O Specifications for Arria II GZ Devices** *(Note 1), (2), (10)* **(Part 3 of 3)**

| Symbol | Conditions | C3, I3 | | | C4, I4 | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| $t_{RISE}$ & $t_{FALL}$ | True differential I/O standards | — | — | 200 | — | — | 200 | ps |
| | Emulated differential I/O standards with three external output resistor networks | — | — | 250 | — | — | 300 | ps |
| | Emulated differential I/O standards with one external output resistor | — | — | 500 | — | — | 500 | ps |
| TCCS | True LVDS | — | — | 100 | — | — | 100 | ps |
| | Emulated LVDS_E_3R | — | — | 250 | — | — | 250 | ps |
| **Receiver** | | | | | | | | |
| True differential I/O standards - $f_{HSDRDPA}$ (data rate) | SERDES factor J = 3 to 10 | 150 | — | 1250 | 150 | — | 1250 | Mbps |
| $f_{HSDR}$ (data rate) | SERDES factor J = 3 to 10 | *(4)* | — | *(6)* | *(4)* | — | *(6)* | Mbps |
| | SERDES factor J = 2, uses DDR registers | *(4)* | — | *(5)* | *(4)* | — | *(5)* | Mbps |
| | SERDES factor J = 1, uses an SDR register | *(4)* | — | *(5)* | *(4)* | — | *(5)* | Mbps |
| DPA run length | DPA mode | — | — | 10000 | — | — | 10000 | UI |
| Soft-CDR PPM tolerance | Soft-CDR mode | — | — | 300 | — | — | 300 | ± PPM |
| Sampling Window (SW) | Non-DPA mode | — | — | 300 | — | — | 300 | ps |

**Notes to Table 1–54:**

(1) When J = 3 to 10, use the SERDES block.

(2) When J = 1 or 2, bypass the SERDES block.

(3) Clock Boost Factor (W) is the ratio between input data rate to the input clock rate.

(4) The minimum specification depends on the clock source (for example, the PLL and clock pin) and the clock routing resource (global, regional, or local) that you use. The I/O differential buffer and input register do not have a minimum toggle rate.

(5) You must calculate the leftover timing margin in the receiver by performing link timing closure analysis. You must consider the board skew margin, transmitter channel-to-channel skew, and receiver sampling margin to determine leftover timing margin.

(6) You can estimate the achievable maximum data rate for non-DPA mode by performing link timing closure analysis. You must consider the board skew margin, transmitter delay margin, and the receiver sampling margin to determine the maximum data rate supported.

(7) This is achieved by using the LVDS and DPA clock network.

(8) If the receiver with DPA enabled and transmitter are using shared PLLs, the minimum data rate is 150 Mbps.

(9) This only applies to DPA and soft-CDR modes.

(10) This only applies to LVDS source synchronous mode.

Table 1–55 lists DPA lock time specifications for Arria II GX and GZ devices.

**Table 1–57. External Memory Interface Specifications for Arria II GX Devices (Part 2 of 2)**

| Frequency Mode | Frequency Range (MHz) | | | Resolution (°) | DQS Delay Buffer Mode *(1)* | Number of Delay Chains |
|---|---|---|---|---|---|---|
| | C4 | I3, C5, I5 | C6 | | | |
| 5 | 270-410 | 270-380 | 270-320 | 36 | High | 10 |
| 6 | 320-450 | 320-410 | 320-370 | 45 | High | 8 |

**Note to Table 1–57:**

(1) Low indicates a 6-bit DQS delay setting; high indicates a 5-bit DQS delay setting.

Table 1–58 lists the DLL frequency range specifications for Arria II GZ devices.

**Table 1–58. DLL Frequency Range Specifications for Arria II GZ Devices**

| Frequency Mode | Frequency Range (MHz) | | Available Phase Shift | DQS Delay Buffer Mode *(1)* | Number of Delay Chains |
|---|---|---|---|---|---|
| | –3 | –4 | | | |
| 0 | 90-130 | 90-120 | 22.5°, 45°, 67.5°, 90° | Low | 16 |
| 1 | 120-170 | 120-160 | 30°, 60°, 90°, 120° | Low | 12 |
| 2 | 150-210 | 150-200 | 36°, 72°, 108°, 144° | Low | 10 |
| 3 | 180-260 | 180-240 | 45°, 90°,135°, 180° | Low | 8 |
| 4 | 240-320 | 240-290 | 30°, 60°, 90°, 120° | High | 12 |
| 5 | 290-380 | 290-360 | 36°, 72°, 108°, 144° | High | 10 |
| 6 | 360-450 | 360-450 | 45°, 90°, 135°, 180° | High | 8 |
| 7 | 470-630 | 470-590 | 60°, 120°, 180°, 240° | High | 6 |

**Note to Table 1–58:**

(1) Low indicates a 6-bit DQS delay setting; high indicates a 5-bit DQS delay setting.

Table 1–59 lists the DQS phase offset delay per stage for Arria II GX devices.

**Table 1–59. DQS Phase Offset Delay Per Setting for Arria II GX Devices *(Note 1)*, *(2)*, *(3)***

| Speed Grade | Min | Max | Unit |
|---|---|---|---|
| C4 | 7.0 | 13.0 | ps |
| I3, C5, I5 | 7.0 | 15.0 | ps |
| C6 | 8.5 | 18.0 | ps |

**Notes to Table 1–59:**

(1) The valid settings for phase offset are -64 to +63 for frequency modes 0 to 3 and -32 to +31 for frequency modes 4 to 5.

(2) The typical value equals the average of the minimum and maximum values.

(3) The delay settings are linear.

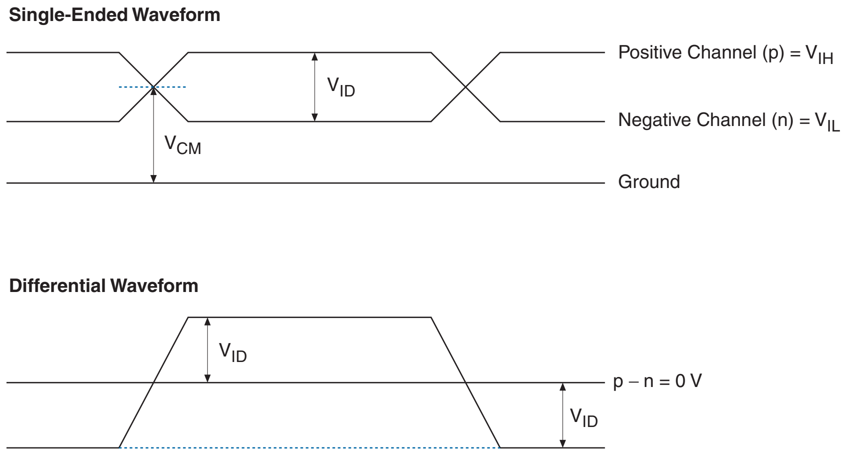
# Glossary

Table 1–68 lists the glossary for this chapter.

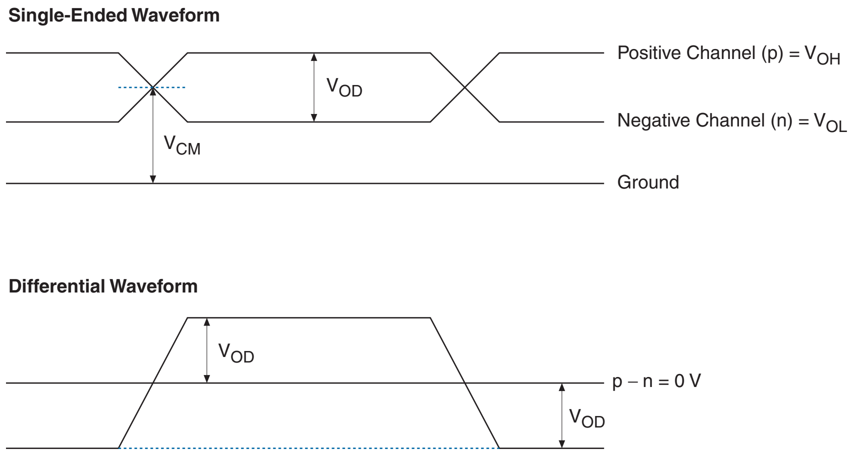
**Table 1–68. Glossary (Part 1 of 4)**

<table>
<tr><th>Letter</th><th>Subject</th><th>Definitions</th></tr>
<tr><td>A,<br>B,<br>C,<br>D</td><td>Differential I/O Standards</td><td>

*Receiver Input Waveforms*



*Transmitter Output Waveforms*



</td></tr>
<tr><td rowspan="3">E,<br>F</td><td>$f_{HSCLK}$</td><td>Left/Right PLL input clock frequency.</td></tr>
<tr><td>$f_{HSDR}$</td><td>High-speed I/O block: Maximum/minimum LVDS data transfer rate ($f_{HSDR}$ = 1/TUI), non-DPA.</td></tr>
<tr><td>$f_{HSDRDPA}$</td><td>High-speed I/O block: Maximum/minimum LVDS data transfer rate ($f_{HSDRDPA}$ = 1/TUI), DPA.</td></tr>
</table>