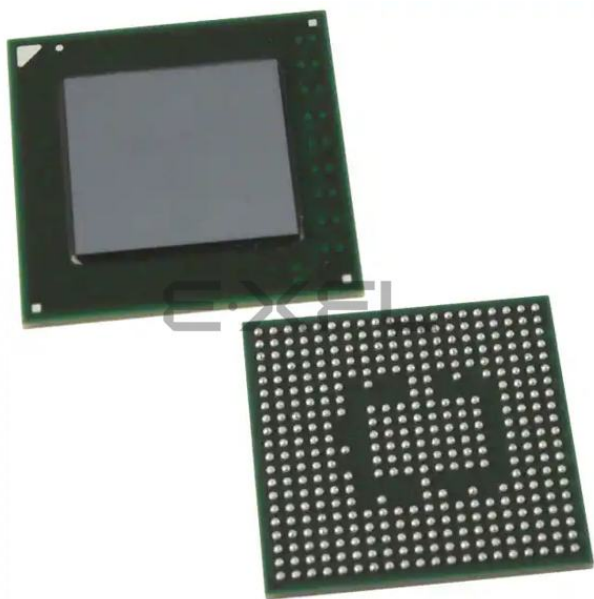




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Details

Product Status	Obsolete
Number of LABs/CLBs	1805
Number of Logic Elements/Cells	42959
Total RAM Bits	3517440
Number of I/O	156
Number of Gates	-
Voltage - Supply	0.87V ~ 0.93V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	358-LFBGA, FCBGA
Supplier Device Package	358-UBGA, FCBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep2agx45cu17i3n

Table 1–3. Maximum Allowed Overshoot During Transitions for Arria II Devices

Symbol	Description	Condition (V)	Overshoot Duration as % of High Time	Unit
V_I (AC)	AC Input Voltage	4.0	100.000	%
		4.05	79.330	%
		4.1	46.270	%
		4.15	27.030	%
		4.2	15.800	%
		4.25	9.240	%
		4.3	5.410	%
		4.35	3.160	%
		4.4	1.850	%
		4.45	1.080	%
		4.5	0.630	%
		4.55	0.370	%
		4.6	0.220	%

Maximum Allowed I/O Operating Frequency

Table 1–4 lists the maximum allowed I/O operating frequency for Arria II GX I/Os using the specified I/O standards to ensure device reliability.

Table 1–4. Maximum Allowed I/O Operating Frequency for Arria II GX Devices

I/O Standard	I/O Frequency (MHz)
HSTL-18 and HSTL-15	333
SSTL -15	400
SSTL-18	333
2.5-V LVCMOS	260
3.3-V and 3.0-V LVTTTL	250
3.3-V, 3.0-V, 1.8-V, and 1.5-V LVCMOS	
PCI and PCI-X	
SSTL-2	
1.2-V LVCMOS HSTL-12	200

Recommended Operating Conditions

This section lists the functional operation limits for AC and DC parameters for Arria II GX and GZ devices. All supplies are required to monotonically reach their full-rail values without plateaus within t_{RAMP} .

Table 1–5 lists the recommended operating conditions for Arria II GX devices.

Table 1–5. Recommended Operating Conditions for Arria II GX Devices (Note 1) (Part 1 of 2)

Symbol	Description	Condition	Minimum	Typical	Maximum	Unit
V_{CC}	Supplies power to the core, periphery, I/O registers, PCIe HIP block, and transceiver PCS	—	0.87	0.90	0.93	V
V_{CCCB}	Supplies power to the configuration RAM bits	—	1.425	1.50	1.575	V
V_{CCBAT} (2)	Battery back-up power supply for design security volatile key registers	—	1.2	—	3.3	V
V_{CCPD} (3)	Supplies power to the I/O pre-drivers, differential input buffers, and MSEL circuitry	—	3.135	3.3	3.465	V
		—	2.85	3.0	3.15	V
		—	2.375	2.5	2.625	V
V_{CCIO}	Supplies power to the I/O banks (4)	—	3.135	3.3	3.465	V
		—	2.85	3.0	3.15	V
		—	2.375	2.5	2.625	V
		—	1.71	1.8	1.89	V
		—	1.425	1.5	1.575	V
		—	1.14	1.2	1.26	V
V_{CCD_PLL}	Supplies power to the digital portions of the PLL	—	0.87	0.90	0.93	V
V_{CCA_PLL}	Supplies power to the analog portions of the PLL and device-wide power management circuitry	—	2.375	2.5	2.625	V
V_I	DC Input voltage	—	–0.5	—	3.6	V
V_O	Output voltage	—	0	—	V_{CCIO}	V
V_{CCA}	Supplies power to the transceiver PMA regulator	—	2.375	2.5	2.625	V
V_{CCL_GXB}	Supplies power to the transceiver PMA TX, PMA RX, and clocking	—	1.045	1.1	1.155	V
V_{CCH_GXB}	Supplies power to the transceiver PMA output (TX) buffer	—	1.425	1.5	1.575	V
T_J	Operating junction temperature	Commercial	0	—	85	°C
		Industrial	–40	—	100	°C

The calibration accuracy for calibrated series and parallel OCTs are applicable at the moment of calibration. When process, voltage, and temperature (PVT) conditions change after calibration, the tolerance may change.

Table 1-13 lists the Arria II GZ OCT without calibration resistance tolerance to PVT changes.

Table 1-13. OCT Without Calibration Resistance Tolerance Specifications for Arria II GZ Devices

Symbol	Description	Conditions (V)	Resistance Tolerance		Unit
			C3,I3	C4,I4	
25-Ω R _S 3.0 and 2.5	25-Ω internal series OCT without calibration	V _{CCIO} = 3.0, 2.5	± 40	± 40	%
25-Ω R _S 1.8 and 1.5	25-Ω internal series OCT without calibration	V _{CCIO} = 1.8, 1.5	± 40	± 40	%
25-Ω R _S 1.2	25-Ω internal series OCT without calibration	V _{CCIO} = 1.2	± 50	± 50	%
50-Ω R _S 3.0 and 2.5	50-Ω internal series OCT without calibration	V _{CCIO} = 3.0, 2.5	± 40	± 40	%
50-Ω R _S 1.8 and 1.5	50-Ω internal series OCT without calibration	V _{CCIO} = 1.8, 1.5	± 40	± 40	%
50-Ω R _S 1.2	50-Ω internal series OCT without calibration	V _{CCIO} = 1.2	± 50	± 50	%
100-Ω R _D 2.5	100-Ω internal differential OCT	V _{CCIO} = 2.5	± 25	± 25	%

OCT calibration is automatically performed at power up for OCT-enabled I/Os. When voltage and temperature conditions change after calibration, the resistance may change. Use Equation 1-1 and Table 1-14 to determine the OCT variation when voltage and temperature vary after power-up calibration for Arria II GX and GZ devices.

Equation 1-1. OCT Variation (Note 1)

$$R_{OCT} = R_{SCAL} \left(1 + \left\langle \frac{dR}{dT} \times \Delta T \right\rangle \pm \left\langle \frac{dR}{dV} \times \Delta V \right\rangle \right)$$

Notes to Equation 1-1:

- (1) R_{OCT} value calculated from Equation 1-1 shows the range of OCT resistance with the variation of temperature and V_{CCIO}.

Use the following with Equation 1-1:

- R_{SCAL} is the OCT resistance value at power up.
- ΔT is the variation of temperature with respect to the temperature at power up.
- ΔV is the variation of voltage with respect to the V_{CCIO} at power up.
- dR/dT is the percentage change of R_{SCAL} with temperature.
- dR/dV is the percentage change of R_{SCAL} with voltage.

Table 1-14 lists the OCT variation with temperature and voltage after power-up calibration for Arria II GX devices.

Table 1-14. OCT Variation after Power-up Calibration for Arria II GX Devices

Nominal Voltage V_{CCIO} (V)	dR/dT (%/°C)	dR/dV (%/mV)
3.0	0.262	0.035
2.5	0.234	0.039
1.8	0.219	0.086
1.5	0.199	0.136
1.2	0.161	0.288

Table 1-15 lists the OCT variation with temperature and voltage after power-up calibration for Arria II GZ devices.

Table 1-15. OCT Variation after Power-Up Calibration for Arria II GZ Devices (Note 1)

Nominal Voltage, V_{CCIO} (V)	dR/dT (%/°C)	dR/dV (%/mV)
3.0	0.189	0.0297
2.5	0.208	0.0344
1.8	0.266	0.0499
1.5	0.273	0.0744
1.2	0.317	0.1241

Note to Table 1-15:

(1) Valid for V_{CCIO} range of $\pm 5\%$ and temperature range of 0° to 85°C.

Pin Capacitance

Table 1-16 lists the pin capacitance for Arria II GX devices.

Table 1-16. Pin Capacitance for Arria II GX Devices

Symbol	Description	Typical	Unit
C_{IO}	Input capacitance on I/O pins, dual-purpose pins (differential I/O, clock, R_{up} , R_{dn}), and dedicated clock input pins	7	pF

Table 1-30 lists the HSTL I/O standards for Arria II GX devices.

Table 1-30. Differential HSTL I/O Standards for Arria II GX Devices

I/O Standard	V _{CCIO} (V)			V _{DIF(DC)} (V)		V _{X(AC)} (V)			V _{CM(DC)} (V)			V _{DIF(AC)} (V)	
	Min	Typ	Max	Min	Max	Min	Typ	Max	Min	Typ	Max	Min	Max
HSTL-18 Class I	1.71	1.8	1.89	0.2	—	0.85	—	0.95	0.88	—	0.95	0.4	—
HSTL-15 Class I, II	1.425	1.5	1.575	0.2	—	0.71	—	0.79	0.71	—	0.79	0.4	—
HSTL-12 Class I, II	1.14	1.2	1.26	0.16	—	—	0.5 × V _{CCIO}	—	0.48 × V _{CCIO}	0.5 × V _{CCIO}	0.52 × V _{CCIO}	0.3	—

Table 1-31 lists the HSTL I/O standards for Arria II GZ devices.

Table 1-31. Differential HSTL I/O Standards for Arria II GZ Devices

I/O Standard	V _{CCIO} (V)			V _{DIF(DC)} (V)		V _{X(AC)} (V)			V _{CM(DC)} (V)			V _{DIF(AC)} (V)	
	Min	Typ	Max	Min	Max	Min	Typ	Max	Min	Typ	Max	Min	Max
HSTL-18 Class I	1.71	1.8	1.89	0.2	—	0.78	—	1.12	0.78	—	1.12	0.4	—
HSTL-15 Class I, II	1.425	1.5	1.575	0.2	—	0.68	—	0.9	0.68	—	0.9	0.4	—
HSTL-12 Class I, II	1.14	1.2	1.26	0.16	V _{CCIO} + 0.3	—	0.5 × V _{CCIO}	—	0.4 × V _{CCIO}	0.5 × V _{CCIO}	0.6 × V _{CCIO}	0.3	V _{CCIO} + 0.48

Table 1-32 lists the differential I/O standard specifications for Arria II GX devices.

Table 1-32. Differential I/O Standard Specifications for Arria II GX Devices (Note 1)

I/O Standard	V _{CCIO} (V)			V _{ID} (mV)			V _{ICM} (V) (2)		V _{OD} (V) (3)			V _{OCM} (V)		
	Min	Typ	Max	Min	Cond.	Max	Min	Max	Min	Typ	Max	Min	Typ	Max
2.5 V LVDS	2.375	2.5	2.625	100	V _{CM} = 1.25 V	—	0.05	1.80	0.247	—	0.6	1.125	1.25	1.375
RSDS (4)	2.375	2.5	2.625	—	—	—	—	—	0.1	0.2	0.6	0.5	1.2	1.4
Mini-LVDS (4)	2.375	2.5	2.625	—	—	—	—	—	0.25	—	0.6	1	1.2	1.4
LVPECL (5)	2.375	2.5	2.625	300	—	—	0.6	1.8	—	—	—	—	—	—
BLVDS (6)	2.375	2.5	2.625	100	—	—	—	—	—	—	—	—	—	—

Notes to Table 1-32:

- (1) The 1.5 V PCML transceiver I/O standard specifications are described in “Transceiver Performance Specifications” on page 1-21.
- (2) V_{IN} range: 0 ≤ V_{IN} ≤ 1.85 V.
- (3) R_L range: 90 ≤ R_L ≤ 110 Ω.
- (4) The RSDS and mini-LVDS I/O standards are only supported for differential outputs.
- (5) The LVPECL input standard is supported at the dedicated clock input pins (GCLK) only.
- (6) There are no fixed V_{ICM}, V_{OD}, and V_{OCM} specifications for BLVDS. These specifications depend on the system topology.

Table 1–34. Transceiver Specifications for Arria II GX Devices (Note 1) (Part 5 of 7)

Symbol/ Description	Condition	I3			C4			C5 and I5			C6			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
LTD lock time (11)	—	0	100	4000	0	100	4000	0	100	4000	0	100	4000	ns
Data lock time from rx_ freqlocked (12)	—	—	—	4000	—	—	4000	—	—	4000	—	—	4000	ns
Programmable DC gain	DC Gain Setting = 0	—	0	—	—	0	—	—	0	—	—	0	—	dB
	DC Gain Setting = 1	—	3	—	—	3	—	—	3	—	—	3	—	dB
	DC Gain Setting = 2	—	6	—	—	6	—	—	6	—	—	6	—	dB
Transmitter														
Supported I/O Standards	1.5-V PCML													
Data rate	—	600	—	6375	600	—	3750	600	—	3750	600	—	3125	Mbps
V _{OCM}	0.65 V setting	—	650	—	—	650	—	—	650	—	—	650	—	mV
Differential on-chip termination resistors	100-Ω setting	—	100	—	—	100	—	—	100	—	—	100	—	Ω
Return loss differential mode	PCIe	50 MHz to 1.25 GHz: –10dB												
	XAUI	312 MHz to 625 MHz: –10dB 625 MHz to 3.125 GHz: –10dB/decade slope												
Return loss common mode	PCIe	50 MHz to 1.25 GHz: –6dB												
Rise time (2)	—	50	—	200	50	—	200	50	—	200	50	—	200	ps
Fall time	—	50	—	200	50	—	200	50	—	200	50	—	200	ps

Table 1–34. Transceiver Specifications for Arria II GX Devices (Note 1) (Part 6 of 7)

Symbol/ Description	Condition	I3			C4			C5 and I5			C6			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Intra-differential pair skew	—	—	—	15	—	—	15	—	—	15	—	—	15	ps
Intra-transceiver block skew	PCIe x4	—	—	120	—	—	120	—	—	120	—	—	120	ps
Inter-transceiver block skew	PCIe x8	—	—	300	—	—	300	—	—	300	—	—	300	ps
CMU PLL0 and CMU PLL1														
CMU PLL lock time from CMUPLL_reset deassertion	—	—	—	100	—	—	100	—	—	100	—	—	100	μs
PLD-Transceiver Interface														
Interface speed	—	25	—	320	25	—	240	25	—	240	25	—	200	MHz

Table 1–34. Transceiver Specifications for Arria II GX Devices (Note 1) (Part 7 of 7)

Symbol/ Description	Condition	I3			C4			C5 and I5			C6			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Digital reset pulse width	—	Minimum is 2 parallel clock cycles												

Notes to Table 1–34:

- (1) For AC-coupled links, the on-chip biasing circuit is switched off before and during configuration. Ensure that input specifications are not violated during this period.
- (2) The rise/fall time is specified from 20% to 80%.
- (3) To calculate the REFCLK rms phase jitter requirement at reference clock frequencies other than 100 MHz, use the following formula:
REFCLK rms phase jitter at f (MHz) = REFCLK rms phase jitter at 100 MHz * 100/f.
- (4) The minimum `reconfig_clk` frequency is 2.5 MHz if the transceiver channel is configured in **Transmitter only** mode. The minimum `reconfig_clk` frequency is 37.5 MHz if the transceiver channel is configured in **Receiver only** or **Receiver and Transmitter** mode. For more information, refer to [AN 558: Implementing Dynamic Reconfiguration in Arria II Devices](#).
- (5) If your design uses more than one dynamic reconfiguration controller instances (`altgx_reconfig`) to control the transceiver channels (`altgx`) physically located on the same side of the device, and if you use different `reconfig_clk` sources for these `altgx_reconfig` instances, the delta time between any two of these `reconfig_clk` sources becoming stable must not exceed the maximum specification listed.
- (6) The device cannot tolerate prolonged operation at this absolute maximum.
- (7) You must use the 1.1-V RX V_{ICM} setting if the input serial data standard is LVDS and the link is DC-coupled.
- (8) The rate matcher supports only up to ± 300 parts per million (ppm).
- (9) Time taken to `rx_pll_locked` goes high from `rx_analogreset` de-assertion. Refer to [Figure 1–1](#).
- (10) The time in which the CDR must be kept in lock-to-reference mode after `rx_pll_locked` goes high and before `rx_locktodata` is asserted in manual mode. Refer to [Figure 1–1](#).
- (11) The time taken to recover valid data after the `rx_locktodata` signal is asserted in manual mode. Refer to [Figure 1–1](#).
- (12) The time taken to recover valid data after the `rx_freqlocked` signal goes high in automatic mode. Refer to [Figure 1–2](#).
- (13) To support data rates lower than the minimum specification through oversampling, use the CDR in LTR mode only.

Table 1–35. Transceiver Specifications for Arria II GZ Devices (Part 3 of 5)

Symbol/ Description	Conditions	–C3 and –I3 (1)			–C4 and –I4			Unit
		Min	Typ	Max	Min	Typ	Max	
Receiver DC Coupling Support	—	For more information about receiver DC coupling support, refer to the “DC-Coupled Links” section in the <i>Transceiver Architecture for Arria II Devices</i> chapter.						
Differential on-chip termination resistors	85–Ω setting	85 ± 20%			85 ± 20%			Ω
	100–Ω setting	100 ± 20%			100 ± 20%			Ω
	120–Ω setting	120 ± 20%			120 ± 20%			Ω
	150–Ω setting	150 ± 20%			150 ± 20%			Ω
Differential and common mode return loss	PCIe (Gen 1 and Gen 2), XAUI, HiGig+, CEI SR/LR, SRIO SR/LR, CPRI LV/HV, OBSAI, SATA	Compliant						—
Programmable PPM detector (9)	—	± 62.5, 100, 125, 200, 250, 300, 500, 1,000						ppm
Run length	—	—	—	200	—	—	200	UI
Programmable equalization	—	—	—	16	—	—	16	dB
t _{LTR} (10)	—	—	—	75	—	—	75	μs
t _{LTR_LTD_Manual} (11)	—	15	—	—	15	—	—	μs
t _{LTD_Manual} (12)	—	—	—	4000	—	—	4000	ns
t _{LTD_Auto} (13)	—	—	—	4000	—	—	4000	ns
Receiver CDR 3 dB Bandwidth in lock-to-data (LTD) mode	PCIe Gen1	2.0 - 3.5						MHz
	PCIe Gen2	40 - 65						MHz
	(OIF) CEI PHY at 6.375 Gbps	20 - 35						MHz
	XAUI	10 - 18						MHz
	SRIO 1.25 Gbps	10 - 18						MHz
	SRIO 2.5 Gbps	10 - 18						MHz
	SRIO 3.125 Gbps	6 - 10						MHz
	GIGE	6 - 10						MHz
	SONET OC12	3 - 6						MHz
	SONET OC48	14 - 19						MHz
Receiver buffer and CDR offset cancellation time (per channel)	—	—	—	17000	—	—	17000	recon fig_ clk cycles
Programmable DC gain	DC Gain Setting = 0	—	0	—	—	0	—	dB
	DC Gain Setting = 1	—	3	—	—	3	—	dB
	DC Gain Setting = 2	—	6	—	—	6	—	dB

Figure 1-1 shows the lock time parameters in manual mode.

 LTD = lock-to-data. LTR = lock-to-reference.

Figure 1-1. Lock Time Parameters for Manual Mode

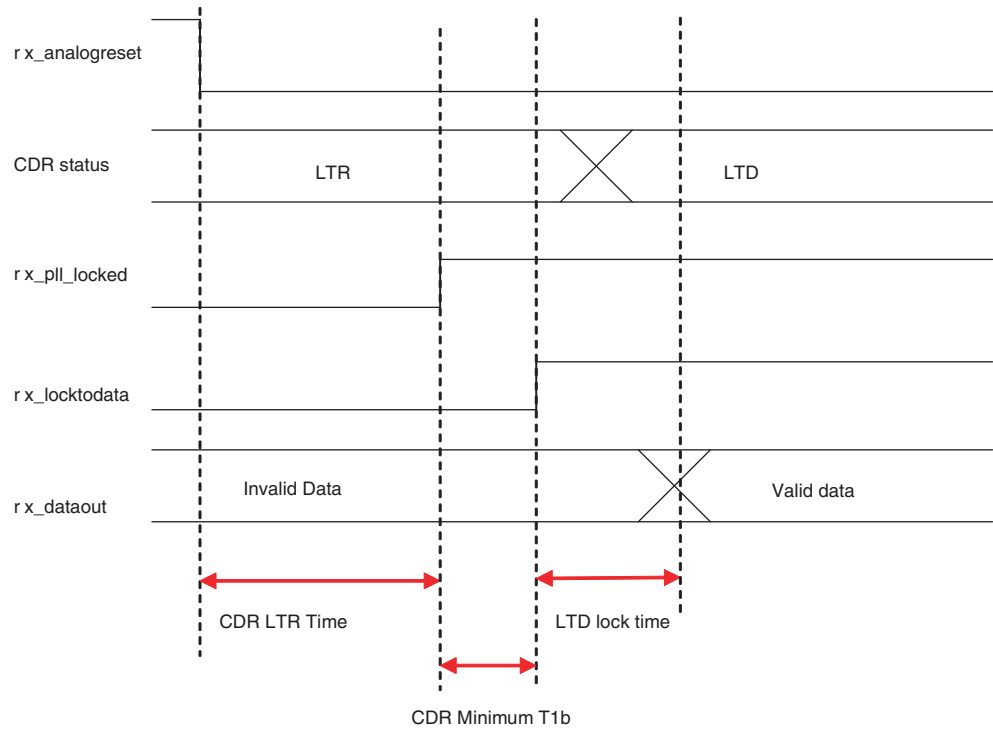


Figure 1-2 shows the lock time parameters in automatic mode.

Figure 1-2. Lock Time Parameters for Automatic Mode

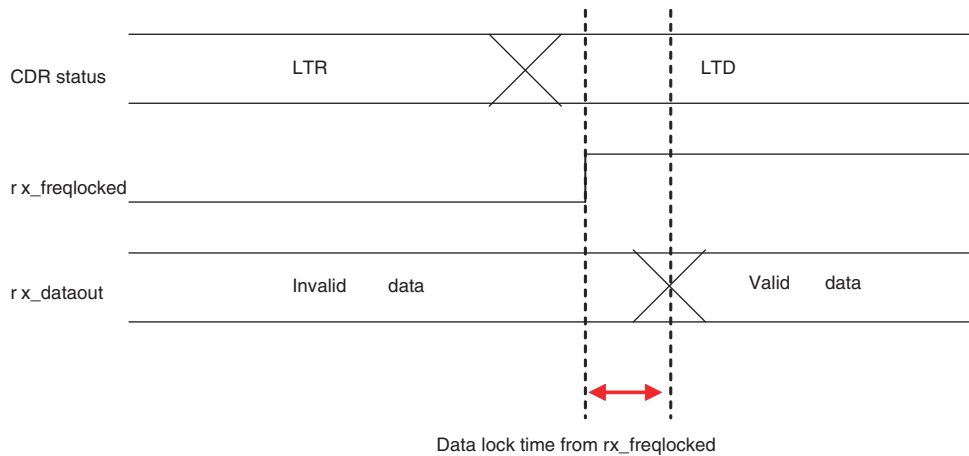


Table 1–39 lists typical transmitter pre-emphasis levels for Arria II GZ devices (in dB) for the first post tap under the following conditions (low-frequency data pattern [five 1s and five 0s] at 6.25 Gbps). The levels listed in Table 1–39 are a representation of possible pre-emphasis levels under the specified conditions only and that the pre-emphasis levels may change with data pattern and data rate.



To predict the pre-emphasis level for your specific data rate and pattern, run simulations using the [Arria II HSSI HSPICE](#) models.

Table 1–39. Transmitter Pre-Emphasis Levels for Arria II GZ Devices (Part 1 of 2)

Pre-Emphasis 1st Post-Tap Setting	V _{DD} Setting							
	0	1	2	3	4	5	6	7
0	0	0	0	0	0	0	0	0
1	N/A	0.7	0	0	0	0	0	0
2	N/A	1	0.3	0	0	0	0	0
3	N/A	1.5	0.6	0	0	0	0	0
4	N/A	2	0.7	0.3	0	0	0	0
5	N/A	2.7	1.2	0.5	0.3	0	0	0
6	N/A	3.1	1.3	0.8	0.5	0.2	0	0
7	N/A	3.7	1.8	1.1	0.7	0.4	0.2	0
8	N/A	4.2	2.1	1.3	0.9	0.6	0.3	0
9	N/A	4.9	2.4	1.6	1.2	0.8	0.5	0.2
10	N/A	5.4	2.8	1.9	1.4	1	0.7	0.3
11	N/A	6	3.2	2.2	1.7	1.2	0.9	0.4
12	N/A	6.8	3.5	2.6	1.9	1.4	1.1	0.6
13	N/A	7.5	3.8	2.8	2.1	1.6	1.2	0.6
14	N/A	8.1	4.2	3.1	2.3	1.7	1.3	0.7
15	N/A	8.8	4.5	3.4	2.6	1.9	1.5	0.8
16	N/A	N/A	4.9	3.7	2.9	2.2	1.7	0.9
17	N/A	N/A	5.3	4	3.1	2.4	1.8	1.1
18	N/A	N/A	5.7	4.4	3.4	2.6	2	1.2
19	N/A	N/A	6.1	4.7	3.6	2.8	2.2	1.4
20	N/A	N/A	6.6	5.1	4	3.1	2.4	1.5
21	N/A	N/A	7	5.4	4.3	3.3	2.7	1.7
22	N/A	N/A	8	6.1	4.8	3.8	3	2
23	N/A	N/A	9	6.8	5.4	4.3	3.4	2.3
24	N/A	N/A	10	7.6	6	4.8	3.9	2.6
25	N/A	N/A	11.4	8.4	6.8	5.4	4.4	3
26	N/A	N/A	12.6	9.4	7.4	5.9	4.9	3.3
27	N/A	N/A	N/A	10.3	8.1	6.4	5.3	3.6
28	N/A	N/A	N/A	11.3	8.8	7.1	5.8	4

Table 1–39. Transmitter Pre-Emphasis Levels for Arria II GZ Devices (Part 2 of 2)

Pre-Emphasis 1st Post-Tap Setting	V _{DD} Setting							
	0	1	2	3	4	5	6	7
29	N/A	N/A	N/A	12.5	9.6	7.7	6.3	4.3
30	N/A	N/A	N/A	N/A	11.4	9	7.4	N/A
31	N/A	N/A	N/A	N/A	12.9	10	8.2	N/A

Table 1–40 lists the transceiver jitter specifications for all supported protocols for Arria II GX devices.

Table 1–40. Transceiver Block Jitter Specifications for Arria II GX Devices (Note 1) (Part 1 of 10)

Symbol/ Description	Conditions	I3			C4			C5, I5			C6			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
SONET/SDH Transmit Jitter Generation (2)														
Peak-to-peak jitter at 622.08 Mbps	Pattern = PRBS15	—	—	0.1	—	—	0.1	—	—	0.1	—	—	0.1	UI
RMS jitter at 622.08 Mbps	Pattern = PRBS15	—	—	0.01	—	—	0.01	—	—	0.01	—	—	0.01	UI
Peak-to-peak jitter at 2488.32 Mbps	Pattern = PRBS15	—	—	0.1	—	—	0.1	—	—	0.1	—	—	0.1	UI
RMS jitter at 2488.32 Mbps	Pattern = PRBS15	—	—	0.01	—	—	0.01	—	—	0.01	—	—	0.01	UI
SONET/SDH Receiver Jitter Tolerance (2)														
Jitter tolerance at 622.08 Mbps	Jitter frequency = 0.03 KHz Pattern = PRBS15	> 15			> 15			> 15			> 15			UI
	Jitter frequency = 25 KHZ Pattern = PRBS15	> 1.5			> 1.5			> 1.5			> 1.5			UI
	Jitter frequency = 250 KHz Pattern = PRBS15	> 0.15			> 0.15			> 0.15			> 0.15			UI

Table 1–40. Transceiver Block Jitter Specifications for Arria II GX Devices (Note 1) (Part 4 of 10)

Symbol/ Description	Conditions	I3			C4			C5, I5			C6			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Total jitter (peak-to-peak)	Pattern = CRPAT	—	—	0.27 9	—	—	0.279	—	—	0.279	—	—	0.279	UI
GIGE Receiver Jitter Tolerance (6)														
Deterministic jitter tolerance (peak-to-peak)	Pattern = CJPAT	> 0.4			> 0.4			> 0.4			> 0.4			UI
Combined deterministic and random jitter tolerance (peak-to-peak)	Pattern = CJPAT	> 0.66			> 0.66			> 0.66			> 0.66			UI
HiGig Transmit Jitter Generation (7)														
Deterministic jitter (peak-to-peak)	Data rate = 3.75 Gbps Pattern = CJPAT	—	—	0.17	—	—	0.17	—	—	—	—	—	—	UI
Total jitter (peak-to-peak)	Data rate = 3.75 Gbps Pattern = CJPAT	—	—	0.35	—	—	0.35	—	—	—	—	—	—	UI
HiGig Receiver Jitter Tolerance (7)														
Deterministic jitter tolerance (peak-to-peak)	Data rate = 3.75 Gbps Pattern = CJPAT	> 0.37			> 0.37			—	—	—	—	—	—	UI
Combined deterministic and random jitter tolerance (peak-to-peak)	Data rate = 3.75 Gbps Pattern = CJPAT	> 0.65			> 0.65			—	—	—	—	—	—	UI
Sinusoidal jitter tolerance (peak-to-peak)	Jitter frequency = 22.1 KHz Data rate = 3.75 Gbps Pattern = CJPAT	> 8.5			> 8.5			—	—	—	—	—	—	UI
	Jitter frequency = 1.875MHz Data rate = 3.75 Gbps Pattern = CJPAT	> 0.1			> 0.1			—	—	—	—	—	—	UI
	Jitter frequency = 20 MHz Data rate = 3.75 Gbps Pattern = CJPAT	> 0.1			> 0.1			—	—	—	—	—	—	UI

Table 1–40. Transceiver Block Jitter Specifications for Arria II GX Devices (Note 1) (Part 7 of 10)

Symbol/ Description	Conditions	I3			C4			C5, I5			C6			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
SSC modulation deviation at 1.5 Gbps (G1)	Compliance pattern	5700			5700			5700			5700			ppm
RX differential skew at 1.5 Gbps (G1)	Compliance pattern	80			80			80			80			ps
RX AC common mode voltage at 1.5 Gbps (G1)	Compliance pattern	150			150			150			150			mV
Total jitter tolerance at 3.0 Gbps (G2)	Compliance pattern	> 0.65			> 0.65			> 0.65			> 0.65			UI
Deterministic jitter tolerance at 3.0 Gbps (G2)	Compliance pattern	> 0.35			> 0.35			> 0.35			> 0.35			UI
SSC modulation frequency at 3.0 Gbps (G2)	Compliance pattern	33			33			33			33			kHz
SSC modulation deviation at 3.0 Gbps (G2)	Compliance pattern	5700			5700			5700			5700			ppm
RX differential skew at 3.0 Gbps (G2)	Compliance pattern	75			75			75			75			ps
RX AC common mode voltage at 3.0 Gbps (G2)	Compliance pattern	150			150			150			150			mV
Total jitter tolerance at 6.0 Gbps (G3)	Compliance pattern	> 0.60			> 0.60			> 0.60			> 0.60			UI
Random jitter tolerance at 6.0 Gbps (G3)	Compliance pattern	> 0.18			> 0.18			> 0.18			> 0.18			UI
SSC modulation frequency at 6.0 Gbps (G3)	Compliance pattern	33			33			33			33			kHz
SSC modulation deviation at 6.0 Gbps (G3)	Compliance pattern	5700			5700			5700			5700			ppm
RX differential skew at 6.0 Gbps (G3)	Compliance pattern	30			30			30			30			ps
RX AC common mode voltage at 6.0 Gbps (G3)	Compliance pattern	100			100			100			100			mV

Table 1-40. Transceiver Block Jitter Specifications for Arria II GX Devices (Note 1) (Part 9 of 10)

Symbol/ Description	Conditions	I3			C4			C5, I5			C6			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
OBSAI Receiver Jitter Tolerance (12)														
Deterministic jitter tolerance at 768 Mbps, 1536 Mbps, and 3072 Mbps	Pattern = CJPAT	> 0.37			> 0.37			> 0.37			> 0.37			UI
Combined deterministic and random jitter tolerance at 768 Mbps, 1536 Mbps, and 3072 Mbps	Pattern = CJPAT	> 0.55			> 0.55			> 0.55			> 0.55			UI
Sinusoidal jitter tolerance at 768 Mbps	Jitter frequency = 5.4 KHz Pattern = CJPAT	> 8.5			> 8.5			> 8.5			> 8.5			UI
	Jitter frequency = 460.8 KHz to 20 MHz Pattern = CJPAT	> 0.1			> 0.1			> 0.1			> 0.1			UI
Sinusoidal jitter tolerance at 1536 Mbps	Jitter frequency = 10.9 KHz Pattern = CJPAT	> 8.5			> 8.5			> 8.5			> 8.5			UI
	Jitter frequency = 921.6 KHz to 20 MHz Pattern = CJPAT	> 0.1			> 0.1			> 0.1			> 0.1			UI

Table 1-41. Transceiver Block Jitter Specifications for Arria II GZ Devices (Note 1), (2) (Part 4 of 7)

Symbol/ Description	Conditions	–C3 and –I3			–C4 and –I4			Unit
		Min	Typ	Max	Min	Typ	Max	
GIGE Receiver Jitter Tolerance (11)								
Deterministic jitter tolerance (peak-to-peak)	Pattern = CJPAT	> 0.4			> 0.4			UI
Combined deterministic and random jitter tolerance (peak-to-peak)	Pattern = CJPAT	> 0.66			> 0.66			UI
HiGig Transmit Jitter Generation								
Deterministic jitter (peak-to-peak)	Data rate = 3.75 Gbps Pattern = CJPAT	—	—	0.17	—	—	—	UI
Total jitter (peak-to-peak)	Data rate = 3.75 Gbps Pattern = CJPAT	—	—	0.35	—	—	—	UI
HiGig Receiver Jitter Tolerance								
Deterministic jitter tolerance (peak-to-peak)	Data rate = 3.75 Gbps Pattern = CJPAT	> 0.37			—	—	—	UI
Combined deterministic and random jitter tolerance (peak-to-peak)	Data rate = 3.75 Gbps Pattern = CJPAT	> 0.65			—	—	—	UI
Sinusoidal jitter tolerance (peak-to-peak)	Jitter frequency = 22.1 KHz Data rate = 3.75 Gbps Pattern = CJPAT	> 8.5			—	—	—	UI
	Jitter frequency = 22.1 KHz Data rate = 3.75 Gbps Pattern = CJPAT	> 0.1			—	—	—	UI
	Jitter frequency = 22.1 KHz Data rate = 3.75 Gbps Pattern = CJPAT	> 0.1			—	—	—	UI
(OIF) CEI Transmitter Jitter Generation								
Total jitter (peak-to-peak)	Data rate = 6.375 Gbps Pattern = PRBS15 BER = 10 ⁻¹²	—	—	0.3	—	—	0.3	UI
(OIF) CEI Receiver Jitter Tolerance								
Deterministic jitter tolerance (peak-to-peak)	Data rate = 6.375 Gbps Pattern = PRBS31 BER = 10 ⁻¹²	> 0.675			—	—	—	UI
Combined deterministic and random jitter tolerance (peak-to-peak)	Data rate = 6.375 Gbps Pattern = PRBS31 BER = 10 ⁻¹²	> 0.988			—	—	—	UI

Table 1–41. Transceiver Block Jitter Specifications for Arria II GZ Devices (Note 1), (2) (Part 6 of 7)

Symbol/ Description	Conditions	–C3 and –I3			–C4 and –I4			Unit
		Min	Typ	Max	Min	Typ	Max	
Deterministic jitter at 3.0 Gbps (G2)	Pattern = CJPAT	—	—	0.35	—	—	0.35	UI
Total jitter at 6.0 Gbps (G3)	Pattern = CJPAT	—	—	0.25	—	—	0.25	UI
Random jitter at 6.0 Gbps (G3)	Pattern = CJPAT	—	—	0.15	—	—	0.15	UI
SAS Receiver Jitter Tolerance (13)								
Total jitter tolerance at 1.5 Gbps (G1)	Pattern = CJPAT	—	—	0.65	—	—	0.65	UI
Deterministic jitter tolerance at 1.5 Gbps (G1)	Pattern = CJPAT	—	—	0.35	—	—	0.35	UI
Sinusoidal jitter tolerance at 1.5 Gbps (G1)	Jitter frequency = 900 KHz to 5 MHz Pattern = CJTPAT BER = 1E-12	> 0.1			> 0.1			UI
CPRI Transmit Jitter Generation (14)								
Total jitter	E.6.HV, E.12.HV Pattern = CJPAT	—	—	0.279	—	—	0.279	UI
	E.6.LV, E.12.LV, E.24.LV, E.30.LV Pattern = CJPAT	—	—	0.35	—	—	0.35	UI
Deterministic jitter	E.6.HV, E.12.HV Pattern = CJPAT	—	—	0.14	—	—	0.14	UI
	E.6.LV, E.12.LV, E.24.LV, E.30.LV Pattern = CJPAT	—	—	0.17	—	—	0.17	UI
CPRI Receiver Jitter Tolerance (14)								
Total jitter tolerance	E.6.HV, E.12.HV Pattern = CJPAT	> 0.66			> 0.66			UI
Deterministic jitter tolerance	E.6.HV, E.12.HV Pattern = CJPAT	> 0.4			> 0.4			UI
Total jitter tolerance	E.6.LV, E.12.LV, E.24.LV, E.30.LV Pattern = CJPAT	> 0.65			> 0.65			UI
Deterministic jitter tolerance	E.6.LV, E.12.LV, E.24.LV, E.30.LV Pattern = CJPAT	> 0.37			> 0.37			UI
Combined deterministic and random jitter tolerance	E.6.LV, E.12.LV, E.24.LV, E.30.LV Pattern = CJPAT	> 0.55			> 0.55			UI
OBSAI Transmit Jitter Generation (15)								
Total jitter at 768 Mbps, 1536 Mbps, and 3072 Mbps	REFCLK = 153.6 MHz Pattern CJPAT	—	—	0.35	—	—	0.35	UI
Deterministic jitter at 768 MBps, 1536 Mbps, and 3072 Mbps	REFCLK = 153.6 MHz Pattern CJPAT	—	—	0.17	—	—	0.17	UI

Table 1–44. PLL Specifications for Arria II GX Devices (Part 2 of 3)

Symbol	Description	Min	Typ	Max	Unit
f_{OUT}	Output frequency for internal global or regional clock (–4 Speed Grade)	—	—	500	MHz
	Output frequency for internal global or regional clock (–5 Speed Grade)	—	—	500	MHz
	Output frequency for internal global or regional clock (–6 Speed Grade)	—	—	400	MHz
f_{OUT_EXT}	Output frequency for external clock output (–4 Speed Grade)	—	—	670 (5)	MHz
	Output frequency for external clock output (–5 Speed Grade)	—	—	622 (5)	MHz
	Output frequency for external clock output (–6 Speed Grade)	—	—	500 (5)	MHz
$t_{OUTDUTY}$	Duty cycle for external clock output (when set to 50%)	45	50	55	%
t_{OUTPJ_DC}	Dedicated clock output period jitter ($f_{OUT} \geq 100$ MHz)	—	—	300	ps (p–p)
	Dedicated clock output period jitter ($f_{OUT} < 100$ MHz)	—	—	30	mUI (p–p)
t_{OUTCCJ_DC}	Dedicated clock output cycle-to-cycle jitter ($f_{OUT} \geq 100$ MHz)	—	—	300	ps (p–p)
	Dedicated clock output cycle-to-cycle jitter ($f_{OUT} < 100$ MHz)	—	—	30	mUI (p–p)
f_{OUTPJ_IO}	Regular I/O clock output period jitter ($f_{OUT} \geq 100$ MHz)	—	—	650	ps (p–p)
	Regular I/O clock output period jitter ($f_{OUT} < 100$ MHz)	—	—	65	mUI (p–p)
f_{OUTCCJ_IO}	Regular I/O clock output cycle-to-cycle jitter ($f_{OUT} \geq 100$ MHz)	—	—	650	ps (p–p)
	Regular I/O clock output cycle-to-cycle jitter ($f_{OUT} < 100$ MHz)	—	—	65	mUI (p–p)
$t_{CONFIGPLL}$	Time required to reconfigure PLL scan chains	—	3.5	—	SCANCLK cycles
$t_{CONFIGPHASE}$	Time required to reconfigure phase shift	—	1	—	SCANCLK cycles
$f_{SCANCLK}$	SCANCLK frequency	—	—	100	MHz
t_{LOCK}	Time required to lock from end of device configuration	—	—	1	ms
t_{DLOCK}	Time required to lock dynamically (after switchover or reconfiguring any non-post-scale counters/delays)	—	—	1	ms
$f_{CL\ BW}$	PLL closed-loop low bandwidth	—	0.3	—	MHz
	PLL closed-loop medium bandwidth	—	1.5	—	MHz
	PLL closed-loop high bandwidth	—	4	—	MHz
t_{PLL_PSERR}	Accuracy of PLL phase shift	—	—	±50	ps
t_{ARESET}	Minimum pulse width on areset signal	10	—	—	ns

Periphery Performance

This section describes periphery performance, including high-speed I/O, external memory interface, and IOE programmable delay.

I/O performance supports several system interfaces, for example the high-speed I/O interface, external memory interface, and the PCI/PCI-X bus interface. I/O using SSTL-18 Class I termination standard can achieve up to the stated DDR2 SDRAM interfacing speed with typical DDR2 SDRAM memory interface setup. I/O using general purpose I/O (GPIO) standards such as 3.0, 2.5, 1.8, or 1.5 LVTTTL/LVCMOS are capable of typical 200 MHz interfacing frequency with 10pF load.



Actual achievable frequency depends on design- and system-specific factors. You should perform HSPICE/IBIS simulations based on your specific design and system setup to determine the maximum achievable frequency in your system.

High-Speed I/O Specification

Table 1-53 lists the high-speed I/O timing for Arria II GX devices.

Table 1-53. High-Speed I/O Specifications for Arria II GX Devices (Part 1 of 4)

Symbol	Conditions	I3		C4		C5,I5		C6		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Clock										
f _{HCLK_IN} (input clock frequency)–Row I/O	Clock boost factor, W = 1 to 40 (1)	5	670	5	670	5	622	5	500	MHz
f _{HCLK_IN} (input clock frequency)–Column I/O	Clock boost factor, W = 1 to 40 (1)	5	500	5	500	5	472.5	5	472.5	MHz
f _{HCLK_OUT} (output clock frequency)–Row I/O	—	5	670	5	670	5	622	5	500	MHz
f _{HCLK_OUT} (output clock frequency)–Column I/O	—	5	500	5	500	5	472.5	5	472.5	MHz

Table 1-53. High-Speed I/O Specifications for Arria II GX Devices (Part 3 of 4)

Symbol	Conditions	I3		C4		C5,I5		C6		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{TX_JITTER} (4)	True LVDS with dedicated SERDES (data rate 600–1,250 Mbps)	—	175	—	175	—	225	—	300	ps
	True LVDS with dedicated SERDES (data rate < 600 Mbps)	—	0.105	—	0.105	—	0.135	—	0.18	UI
	True LVDS and emulated LVDS_E_3R with logic elements as SERDES (data rate 600 – 945 Mbps)	—	260	—	260	—	300	—	350	ps
	True LVDS and emulated LVDS_E_3R with logic elements as SERDES (data rate < 600 Mbps)	—	0.16	—	0.16	—	0.18	—	0.21	UI
t_{TX_DCD}	True LVDS and emulated LVDS_E_3R	45	55	45	55	45	55	45	55	%
t_{RISE} and t_{FALL}	True LVDS and emulated LVDS_E_3R	—	200	—	200	—	225	—	250	ps
TCCS	True LVDS (5)	—	150	—	150	—	175	—	200	ps
	Emulated LVDS_E_3R	—	200	—	200	—	250	—	300	ps
Receiver (6)										
True differential I/O standards - f_{HSDRPA} (data rate)	SERDES factor J = 3 to 10	150	1250	150	1250	150	1050	150	840	Mbps