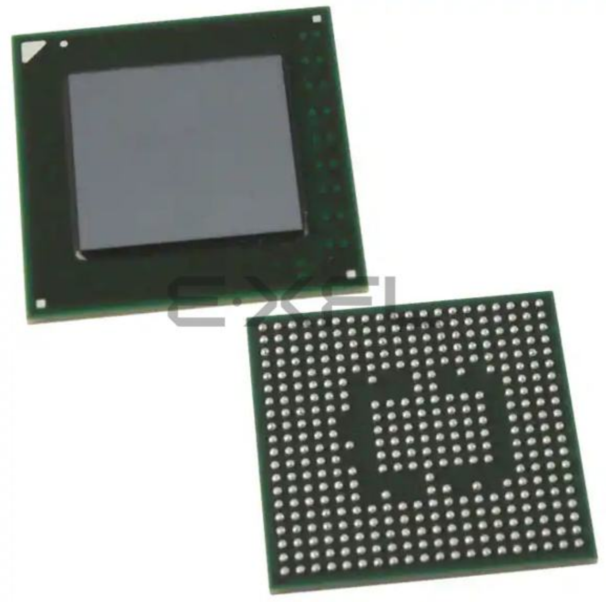

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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

| **Details** | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | 2530 |
| Number of Logic Elements/Cells | 60214 |
| Total RAM Bits | 5371904 |
| Number of I/O | 156 |
| Number of Gates | - |
| Voltage - Supply | 0.87V ~ 0.93V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 85°C (TJ) |
| Package / Case | 358-LFBGA, FCBGA |
| Supplier Device Package | 358-UBGA, FCBGA (17x17) |
| Purchase URL | https://www.e-xfl.com/product-detail/intel/ep2agx65cu17c5 |

**Table 1–3. Maximum Allowed Overshoot During Transitions for Arria II Devices**

| Symbol | Description | Condition (V) | Overshoot Duration as % of High Time | Unit |
|---|---|---|---|---|
| $V_I$ (AC) | AC Input Voltage | 4.0 | 100.000 | % |
| | | 4.05 | 79.330 | % |
| | | 4.1 | 46.270 | % |
| | | 4.15 | 27.030 | % |
| | | 4.2 | 15.800 | % |
| | | 4.25 | 9.240 | % |
| | | 4.3 | 5.410 | % |
| | | 4.35 | 3.160 | % |
| | | 4.4 | 1.850 | % |
| | | 4.45 | 1.080 | % |
| | | 4.5 | 0.630 | % |
| | | 4.55 | 0.370 | % |
| | | 4.6 | 0.220 | % |

## Maximum Allowed I/O Operating Frequency

Table 1–4 lists the maximum allowed I/O operating frequency for Arria II GX I/Os using the specified I/O standards to ensure device reliability.

**Table 1–4. Maximum Allowed I/O Operating Frequency for Arria II GX Devices**

| I/O Standard | I/O Frequency (MHz) |
|---|---|
| HSTL-18 and HSTL-15 | 333 |
| SSTL -15 | 400 |
| SSTL-18 | 333 |
| 2.5-V LVCMOS | 260 |
| 3.3-V and 3.0-V LVTTL | 250 |
| 3.3-V, 3.0-V, 1.8-V, and 1.5-V LVCMOS | |
| PCI and PCI-X | |
| SSTL-2 | |
| 1.2-V LVCMOS HSTL-12 | 200 |

The calibration accuracy for calibrated series and parallel OCTs are applicable at the moment of calibration. When process, voltage, and temperature (PVT) conditions change after calibration, the tolerance may change.

Table 1–13 lists the Arria II GZ OCT without calibration resistance tolerance to PVT changes.

**Table 1–13. OCT Without Calibration Resistance Tolerance Specifications for Arria II GZ Devices**

| Symbol | Description | Conditions (V) | Resistance Tolerance | | Unit |
|---|---|---|---|---|---|
| | | | C3,I3 | C4,I4 | |
| 25-Ω $R_S$ 3.0 and 2.5 | 25-Ω internal series OCT without calibration | $V_{CCIO}$ = 3.0, 2.5 | ± 40 | ± 40 | % |
| 25-Ω $R_S$ 1.8 and 1.5 | 25-Ω internal series OCT without calibration | $V_{CCIO}$ = 1.8, 1.5 | ± 40 | ± 40 | % |
| 25-Ω $R_S$ 1.2 | 25-Ω internal series OCT without calibration | $V_{CCIO}$ = 1.2 | ± 50 | ± 50 | % |
| 50-Ω $R_S$ 3.0 and 2.5 | 50-Ω internal series OCT without calibration | $V_{CCIO}$ = 3.0, 2.5 | ± 40 | ± 40 | % |
| 50-Ω $R_S$ 1.8 and 1.5 | 50-Ω internal series OCT without calibration | $V_{CCIO}$ = 1.8, 1.5 | ± 40 | ± 40 | % |
| 50-Ω $R_S$ 1.2 | 50-Ω internal series OCT without calibration | $V_{CCIO}$ = 1.2 | ± 50 | ± 50 | % |
| 100-Ω $R_D$ 2.5 | 100-Ω internal differential OCT | $V_{CCIO}$ = 2.5 | ± 25 | ± 25 | % |

OCT calibration is automatically performed at power up for OCT-enabled I/Os. When voltage and temperature conditions change after calibration, the resistance may change. Use Equation 1–1 and Table 1–14 to determine the OCT variation when voltage and temperature vary after power-up calibration for Arria II GX and GZ devices.

**Equation 1–1. OCT Variation *(Note 1)***

$$R_{OCT} = R_{SCAL}\left(1 + \langle\frac{dR}{dT} \times \Delta T\rangle \pm \langle\frac{dR}{dV} \times \Delta V\rangle\right)$$

**Notes to Equation 1–1:**

(1) $R_{OCT}$ value calculated from Equation 1–1shows the range of OCT resistance with the variation of temperature and $V_{CCIO}$.

Use the following with Equation 1–1:

- $R_{SCAL}$ is the OCT resistance value at power up.
- $\Delta T$ is the variation of temperature with respect to the temperature at power up.
- $\Delta V$ is the variation of voltage with respect to the $V_{CCIO}$ at power up.
- dR/dT is the percentage change of $R_{SCAL}$ with temperature.
- dR/dV is the percentage change of $R_{SCAL}$ with voltage.

Table 1–14 lists the OCT variation with temperature and voltage after power-up calibration for Arria II GX devices.

**Table 1–14. OCT Variation after Power-up Calibration for Arria II GX Devices**

| Nominal Voltage $V_{CCIO}$ (V) | dR/dT (%/°C) | dR/dV (%/mV) |
|---|---|---|
| 3.0 | 0.262 | 0.035 |
| 2.5 | 0.234 | 0.039 |
| 1.8 | 0.219 | 0.086 |
| 1.5 | 0.199 | 0.136 |
| 1.2 | 0.161 | 0.288 |

Table 1–15 lists the OCT variation with temperature and voltage after power-up calibration for Arria II GZ devices.

**Table 1–15. OCT Variation after Power-Up Calibration for Arria II GZ Devices *(Note 1)***

| Nominal Voltage, $V_{CCIO}$ (V) | dR/dT (%/°C) | dR/dV (%/mV) |
|---|---|---|
| 3.0 | 0.189 | 0.0297 |
| 2.5 | 0.208 | 0.0344 |
| 1.8 | 0.266 | 0.0499 |
| 1.5 | 0.273 | 0.0744 |
| 1.2 | 0.317 | 0.1241 |

**Note to Table 1–15:**

(1) Valid for $V_{CCIO}$ range of ±5% and temperature range of 0° to 85°C.

## Pin Capacitance

Table 1–16 lists the pin capacitance for Arria II GX devices.

**Table 1–16. Pin Capacitance for Arria II GX Devices**

| Symbol | Description | Typical | Unit |
|---|---|---|---|
| $C_{IO}$ | Input capacitance on I/O pins, dual-purpose pins (differential I/O, clock, $R_{up}$, $R_{dn}$), and dedicated clock input pins | 7 | pF |

Table 1–17 lists the pin capacitance for Arria II GZ devices.

**Table 1–17. Pin Capacitance for Arria II GZ Devices**

| Symbol | Description | Typical | Unit |
|---|---|---|---|
| $C_{IOTB}$ | Input capacitance on the top and bottom I/O pins | 4 | pF |
| $C_{IOLR}$ | Input capacitance on the left and right I/O pins | 4 | pF |
| $C_{CLKTB}$ | Input capacitance on the top and bottom non-dedicated clock input pins | 4 | pF |
| $C_{CLKLR}$ | Input capacitance on the left and right non-dedicated clock input pins | 4 | pF |
| $C_{OUTFB}$ | Input capacitance on the dual-purpose clock output and feedback pins | 5 | pF |
| $C_{CLK1}$, $C_{CLK3}$, $C_{CLK8}$, and $C_{CLK10}$ | Input capacitance for dedicated clock input pins | 2 | pF |

### Internal Weak Pull-Up and Weak Pull-Down Resistors

Table 1–18 lists the weak pull-up and pull-down resistor values for Arria II GX devices.

**Table 1–18. Internal Weak Pull-up and Weak Pull-Down Resistors for Arria II GX Devices** *(Note 1)*

| Symbol | Description | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $R_{PU}$ | Value of I/O pin pull-up resistor before and during configuration, as well as user mode if the programmable pull-up resistor option is enabled. | $V_{CCIO}$ = 3.3 V ±5% *(2)* | 7 | 25 | 41 | kΩ |
| | | $V_{CCIO}$ = 3.0 V ±5% *(2)* | 7 | 28 | 47 | kΩ |
| | | $V_{CCIO}$ = 2.5 V ±5% *(2)* | 8 | 35 | 61 | kΩ |
| | | $V_{CCIO}$ = 1.8 V ±5% *(2)* | 10 | 57 | 108 | kΩ |
| | | $V_{CCIO}$ = 1.5 V ±5% *(2)* | 13 | 82 | 163 | kΩ |
| | | $V_{CCIO}$ = 1.2 V ±5% *(2)* | 19 | 143 | 351 | kΩ |
| $R_{PD}$ | Value of TCK pin pull-down resistor | $V_{CCIO}$ = 3.3 V ±5% | 6 | 19 | 29 | kΩ |
| | | $V_{CCIO}$ = 3.0 V ±5% | 6 | 22 | 32 | kΩ |
| | | $V_{CCIO}$ = 2.5 V ±5% | 6 | 25 | 42 | kΩ |
| | | $V_{CCIO}$ = 1.8 V ±5% | 7 | 35 | 70 | kΩ |
| | | $V_{CCIO}$ = 1.5 V ±5% | 8 | 50 | 112 | kΩ |

**Notes to Table 1–18:**

(1) All I/O pins have an option to enable weak pull-up except configuration, test, and JTAG pins. The weak pull-down feature is only available for JTAG TCK.

(2) Pin pull-up resistance values may be lower if an external source drives the pin higher than $V_{CCIO}$.

**Table 1–23. Single-Ended I/O Standards for Arria II GZ Devices (Part 2 of 2)**

| I/O Standard | $V_{CCIO}$ (V) | | | $V_{IL}$ (V) | | $V_{IH}$ (V) | | $V_{OL}$ (V) | $V_{OH}$ (V) | $I_{OL}$ (mA) | $I_{OH}$ (mA) |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Max | Min | Max | Max | Min | | |
| 1.2 V | 1.14 | 1.2 | 1.26 | -0.3 | 0.35 × $V_{CCIO}$ | 0.65 × $V_{CCIO}$ | $V_{CCIO}$ + 0.3 | 0.25 × $V_{CCIO}$ | 0.75 × $V_{CCIO}$ | 2 | -2 |
| 3.0-V PCI | 2.85 | 3 | 3.15 | — | 0.3 × $V_{CCIO}$ | 0.5 × $V_{CCIO}$ | 3.6 | 0.1 × $V_{CCIO}$ | 0.9 × $V_{CCIO}$ | 1.5 | -0.5 |
| 3.0-V PCI-X | 2.85 | 3 | 3.15 | — | 0.35 × $V_{CCIO}$ | 0.5 × $V_{CCIO}$ | — | 0.1 × $V_{CCIO}$ | 0.9 × $V_{CCIO}$ | 1.5 | -0.5 |

Table 1–24 lists the single-ended SSTL and HSTL I/O reference voltage specifications for Arria II GX devices.

**Table 1–24. Single-Ended SSTL and HSTL I/O Reference Voltage Specifications for Arria II GX Devices**

| I/O Standard | $V_{CCIO}$ (V) | | | $V_{REF}$ (V) | | | $V_{TT}$ (V) | | |
|---|---|---|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max |
| SSTL-2 Class I, II | 2.375 | 2.5 | 2.625 | 0.49 × $V_{CCIO}$ | 0.5 × $V_{CCIO}$ | 0.51 × $V_{CCIO}$ | $V_{REF}$ - 0.04 | $V_{REF}$ | $V_{REF}$ + 0.04 |
| SSTL-18 Class I, II | 1.71 | 1.8 | 1.89 | 0.833 | 0.9 | 0.969 | $V_{REF}$ - 0.04 | $V_{REF}$ | $V_{REF}$ + 0.04 |
| SSTL-15 Class I, II | 1.425 | 1.5 | 1.575 | 0.47 × $V_{CCIO}$ | 0.5 × $V_{CCIO}$ | 0.53 × $V_{CCIO}$ | 0.47 × $V_{CCIO}$ | 0.5 × $V_{CCIO}$ | 0.53 × $V_{CCIO}$ |
| HSTL-18 Class I, II | 1.71 | 1.8 | 1.89 | 0.85 | 0.9 | 0.95 | 0.85 | 0.9 | 0.95 |
| HSTL-15 Class I, II | 1.425 | 1.5 | 1.575 | 0.71 | 0.75 | 0.79 | 0.71 | 0.75 | 0.79 |
| HSTL-12 Class I, II | 1.14 | 1.2 | 1.26 | 0.48 × $V_{CCIO}$ | 0.5 × $V_{CCIO}$ | 0.52 × $V_{CCIO}$ | — | $V_{CCIO}$/2 | — |

Table 1–25 lists the single-ended SSTL and HSTL I/O reference voltage specifications for Arria II GZ devices.

**Table 1–25. Single-Ended SSTL and HSTL I/O Reference Voltage Specifications for Arria II GZ Devices**

| I/O Standard | $V_{CCIO}$ (V) | | | $V_{REF}$ (V) | | | $V_{TT}$ (V) | | |
|---|---|---|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max |
| SSTL-2 Class I, II | 2.375 | 2.5 | 2.625 | 0.49 × $V_{CCIO}$ | 0.5 × $V_{CCIO}$ | 0.51 × $V_{CCIO}$ | $V_{REF}$ - 0.04 | $V_{REF}$ | $V_{REF}$ + 0.04 |
| SSTL-18 Class I, II | 1.71 | 1.8 | 1.89 | 0.833 | 0.9 | 0.969 | $V_{REF}$ - 0.04 | $V_{REF}$ | $V_{REF}$ + 0.04 |
| SSTL-15 Class I, II | 1.425 | 1.5 | 1.575 | 0.47 × $V_{CCIO}$ | 0.5 × $V_{CCIO}$ | 0.53 × $V_{CCIO}$ | 0.47 × $V_{CCIO}$ | $V_{REF}$ | 0.53 × $V_{CCIO}$ |
| HSTL-18 Class I, II | 1.71 | 1.8 | 1.89 | 0.85 | 0.9 | 0.95 | — | $V_{CCIO}$/2 | — |
| HSTL-15 Class I, II | 1.425 | 1.5 | 1.575 | 0.68 | 0.75 | 0.9 | — | $V_{CCIO}$/2 | — |
| HSTL-12 Class I, II | 1.14 | 1.2 | 1.26 | 0.47 × $V_{CCIO}$ | 0.5 × $V_{CCIO}$ | 0.53 × $V_{CCIO}$ | — | $V_{CCIO}$/2 | — |

Table 1–30 lists the HSTL I/O standards for Arria II GX devices.

**Table 1–30. Differential HSTL I/O Standards for Arria II GX Devices**

| I/O Standard | $V_{CCIO}$ (V) | | | $V_{DIF(DC)}$ (V) | | $V_{X(AC)}$ (V) | | | $V_{CM(DC)}$ (V) | | | $V_{DIF(AC)}$ (V) | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Max | Min | Typ | Max | Min | Typ | Max | Min | Max |
| HSTL-18 Class I | 1.71 | 1.8 | 1.89 | 0.2 | — | 0.85 | — | 0.95 | 0.88 | — | 0.95 | 0.4 | — |
| HSTL-15 Class I, II | 1.425 | 1.5 | 1.575 | 0.2 | — | 0.71 | — | 0.79 | 0.71 | — | 0.79 | 0.4 | — |
| HSTL-12 Class I, II | 1.14 | 1.2 | 1.26 | 0.16 | — | — | 0.5 × $V_{CCIO}$ | — | 0.48 × $V_{CCIO}$ | 0.5 × $V_{CCIO}$ | 0.52 × $V_{CCIO}$ | 0.3 | — |

Table 1–31 lists the HSTL I/O standards for Arria II GZ devices.

**Table 1–31. Differential HSTL I/O Standards for Arria II GZ Devices**

| I/O Standard | $V_{CCIO}$ (V) | | | $V_{DIF(DC)}$ (V) | | $V_{X(AC)}$ (V) | | | $V_{CM(DC)}$ (V) | | | $V_{DIF(AC)}$ (V) | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Max | Min | Typ | Max | Min | Typ | Max | Min | Max |
| HSTL-18 Class I | 1.71 | 1.8 | 1.89 | 0.2 | — | 0.78 | — | 1.12 | 0.78 | — | 1.12 | 0.4 | — |
| HSTL-15 Class I, II | 1.425 | 1.5 | 1.575 | 0.2 | — | 0.68 | — | 0.9 | 0.68 | — | 0.9 | 0.4 | — |
| HSTL-12 Class I, II | 1.14 | 1.2 | 1.26 | 0.16 | $V_{CCIO}$ + 0.3 | — | 0.5 × $V_{CCIO}$ | — | 0.4 × $V_{CCIO}$ | 0.5 × $V_{CCIO}$ | 0.6 × $V_{CCIO}$ | 0.3 | $V_{CCIO}$ + 0.48 |

Table 1–32 lists the differential I/O standard specifications for Arria II GX devices.

**Table 1–32. Differential I/O Standard Specifications for Arria II GX Devices *(Note 1)***

| I/O Standard | $V_{CCIO}$ (V) | | | $V_{ID}$ (mV) | | | $V_{ICM}$ (V) *(2)* | | $V_{OD}$ (V) *(3)* | | | $V_{OCM}$ (V) | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Cond. | Max | Min | Max | Min | Typ | Max | Min | Typ | Max |
| 2.5 V LVDS | 2.375 | 2.5 | 2.625 | 100 | $V_{CM}$ = 1.25 V | — | 0.05 | 1.80 | 0.247 | — | 0.6 | 1.125 | 1.25 | 1.375 |
| RSDS *(4)* | 2.375 | 2.5 | 2.625 | — | — | — | — | — | 0.1 | 0.2 | 0.6 | 0.5 | 1.2 | 1.4 |
| Mini-LVDS *(4)* | 2.375 | 2.5 | 2.625 | — | — | — | — | — | 0.25 | — | 0.6 | 1 | 1.2 | 1.4 |
| LVPECL *(5)* | 2.375 | 2.5 | 2.625 | 300 | — | — | 0.6 | 1.8 | — | — | — | — | — | — |
| BLVDS *(6)* | 2.375 | 2.5 | 2.625 | 100 | — | — | — | — | — | — | — | — | — | — |

**Notes to Table 1–32:**

(1) The 1.5 V PCML transceiver I/O standard specifications are described in "Transceiver Performance Specifications" on page 1–21.

(2) $V_{IN}$ range: 0 <= $V_{IN}$ <= 1.85 V.

(3) $R_L$ range: 90 <= RL <= 110 Ω.

(4) The RSDS and mini-LVDS I/O standards are only supported for differential outputs.

(5) The LVPECL input standard is supported at the dedicated clock input pins (GCLK) only.

(6) There are no fixed $V_{ICM}$, $V_{OD}$, and $V_{OCM}$ specifications for BLVDS. These specifications depend on the system topology.

**Table 1–34. Transceiver Specifications for Arria II GX Devices** *(Note 1)* **(Part 5 of 7)**

| Symbol/ Description | Condition | I3 | | | C4 | | | C5 and I5 | | | C6 | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| LTD lock time *(11)* | — | 0 | 100 | 4000 | 0 | 100 | 4000 | 0 | 100 | 4000 | 0 | 100 | 4000 | ns |
| Data lock time from `rx_freqlocked` *(12)* | — | — | — | 4000 | — | — | 4000 | — | — | 4000 | — | — | 4000 | ns |
| Programmable DC gain | DC Gain Setting = 0 | — | 0 | — | — | 0 | — | — | 0 | — | — | 0 | — | dB |
| | DC Gain Setting = 1 | — | 3 | — | — | 3 | — | — | 3 | — | — | 3 | — | dB |
| | DC Gain Setting = 2 | — | 6 | — | — | 6 | — | — | 6 | — | — | 6 | — | dB |
| **Transmitter** | | | | | | | | | | | | | | |
| Supported I/O Standards | 1.5-V PCML | | | | | | | | | | | | | |
| Data rate | — | 600 | — | 6375 | 600 | — | 3750 | 600 | — | 3750 | 600 | — | 3125 | Mbps |
| $V_{OCM}$ | 0.65 V setting | — | 650 | — | — | 650 | — | — | 650 | — | — | 650 | — | mV |
| Differential on-chip termination resistors | 100–Ω setting | — | 100 | — | — | 100 | — | — | 100 | — | — | 100 | — | Ω |
| Return loss differential mode | PCIe | 50 MHz to 1.25 GHz: –10dB | | | | | | | | | | | | |
| | XAUI | 312 MHz to 625 MHz: –10dB<br>625 MHz to 3.125 GHz: –10dB/decade slope | | | | | | | | | | | | |
| Return loss common mode | PCIe | 50 MHz to 1.25 GHz: –6dB | | | | | | | | | | | | |
| Rise time *(2)* | — | 50 | — | 200 | 50 | — | 200 | 50 | — | 200 | 50 | — | 200 | ps |
| Fall time | — | 50 | — | 200 | 50 | — | 200 | 50 | — | 200 | 50 | — | 200 | ps |

**Table 1–34. Transceiver Specifications for Arria II GX Devices** *(Note 1)* **(Part 6 of 7)**

| Symbol/ Description | Condition | I3 | | | C4 | | | C5 and I5 | | | C6 | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Intra-differential pair skew | — | — | — | 15 | — | — | 15 | — | — | 15 | — | — | 15 | ps |
| Intra-transceiver block skew | PCIe ×4 | — | — | 120 | — | — | 120 | — | — | 120 | — | — | 120 | ps |
| Inter-transceiver block skew | PCIe ×8 | — | — | 300 | — | — | 300 | — | — | 300 | — | — | 300 | ps |
| **CMU PLL0 and CMU PLL1** | | | | | | | | | | | | | | |
| CMU PLL lock time from `CMUPLL_reset` deassertion | — | — | — | 100 | — | — | 100 | — | — | 100 | — | — | 100 | µs |
| **PLD-Transceiver Interface** | | | | | | | | | | | | | | |
| Interface speed | — | 25 | — | 320 | 25 | — | 240 | 25 | — | 240 | 25 | — | 200 | MHz |

**Table 1–35. Transceiver Specifications for Arria II GZ Devices (Part 2 of 5)**

| Symbol/ Description | Conditions | –C3 and –I3 *(1)* | | | –C4 and –I4 | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| **Transceiver Clocks** | | | | | | | | |
| Calibration block clock frequency (`cal_blk_clk`) | — | 10 | — | 125 | 10 | — | 125 | MHz |
| `fixedclk` clock frequency | PCIe Receiver Detect | — | 125 | — | — | 125 | — | MHz |
| `reconfig_clk` clock frequency | Dynamic reconfiguration clock frequency | 2.5/ 37.5 *(4)* | — | 50 | 2.5/ 37.5 *(4)* | — | 50 | MHz |
| Delta time between `reconfig_clks` *(5)* | — | — | — | 2 | — | — | 2 | ms |
| Transceiver block minimum power-down (`gxb_powerdown`) pulse width | — | 1 | — | — | 1 | — | — | µs |
| **Receiver** | | | | | | | | |
| Supported I/O Standards | 1.4-V PCML, 1.5-V PCML, 2.5-V PCML, LVPECL, and LVDS | | | | | | | |
| Data rate *(16)* | — | 600 | — | 6375 | 600 | — | 3750 | Mbps |
| Absolute $V_{MAX}$ for a receiver pin *(6)* | — | — | — | 1.6 | — | — | 1.6 | V |
| Operational $V_{MAX}$ for a receiver pin | — | — | — | 1.5 | — | — | 1.5 | V |
| Absolute $V_{MIN}$ for a receiver pin | — | -0.4 | — | — | -0.4 | — | — | V |
| Maximum peak-to-peak differential input voltage $V_{ID}$ (diff p-p) before device configuration | — | — | — | 1.6 | — | — | 1.6 | V |
| Maximum peak-to-peak differential input voltage $V_{ID}$ (diff p-p) after device configuration | $V_{ICM}$ = 0.82 V setting | — | — | 2.7 | — | — | 2.7 | V |
| | $V_{ICM}$ =1.1 V setting *(7)* | — | — | 1.6 | — | — | 1.6 | V |
| Minimum differential eye opening at receiver serial input pins *(8)* | Data Rate = 600 Mbps to 5 Gbps<br>Equalization = 0<br>DC gain = 0 dB | 100 | — | — | 165 | — | — | mV |
| | Data Rate > 5 Gbps<br>Equalization = 0<br>DC gain = 0 dB | 165 | — | — | 165 | — | — | mV |
| $V_{ICM}$ | $V_{ICM}$ = 0.82 V setting | 820 ± 10% | | | 820 ± 10% | | | mV |
| | $V_{ICM}$ = 1.1 V setting *(7)* | 1100 ± 10% | | | 1100 ± 10% | | | mV |

Table 1–39 lists typical transmitter pre-emphasis levels for Arria II GZ devices (in dB) for the first post tap under the following conditions (low-frequency data pattern [five 1s and five 0s] at 6.25 Gbps). The levels listed in Table 1–39 are a representation of possible pre-emphasis levels under the specified conditions only and that the pre-emphasis levels may change with data pattern and data rate.

To predict the pre-emphasis level for your specific data rate and pattern, run simulations using the Arria II HSSI HSPICE models.

**Table 1–39. Transmitter Pre-Emphasis Levels for Arria II GZ Devices (Part 1 of 2)**

| Pre-Emphasis 1st Post-Tap Setting | $V_{OD}$ Setting | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | N/A | 0.7 | 0 | 0 | 0 | 0 | 0 | 0 |
| 2 | N/A | 1 | 0.3 | 0 | 0 | 0 | 0 | 0 |
| 3 | N/A | 1.5 | 0.6 | 0 | 0 | 0 | 0 | 0 |
| 4 | N/A | 2 | 0.7 | 0.3 | 0 | 0 | 0 | 0 |
| 5 | N/A | 2.7 | 1.2 | 0.5 | 0.3 | 0 | 0 | 0 |
| 6 | N/A | 3.1 | 1.3 | 0.8 | 0.5 | 0.2 | 0 | 0 |
| 7 | N/A | 3.7 | 1.8 | 1.1 | 0.7 | 0.4 | 0.2 | 0 |
| 8 | N/A | 4.2 | 2.1 | 1.3 | 0.9 | 0.6 | 0.3 | 0 |
| 9 | N/A | 4.9 | 2.4 | 1.6 | 1.2 | 0.8 | 0.5 | 0.2 |
| 10 | N/A | 5.4 | 2.8 | 1.9 | 1.4 | 1 | 0.7 | 0.3 |
| 11 | N/A | 6 | 3.2 | 2.2 | 1.7 | 1.2 | 0.9 | 0.4 |
| 12 | N/A | 6.8 | 3.5 | 2.6 | 1.9 | 1.4 | 1.1 | 0.6 |
| 13 | N/A | 7.5 | 3.8 | 2.8 | 2.1 | 1.6 | 1.2 | 0.6 |
| 14 | N/A | 8.1 | 4.2 | 3.1 | 2.3 | 1.7 | 1.3 | 0.7 |
| 15 | N/A | 8.8 | 4.5 | 3.4 | 2.6 | 1.9 | 1.5 | 0.8 |
| 16 | N/A | N/A | 4.9 | 3.7 | 2.9 | 2.2 | 1.7 | 0.9 |
| 17 | N/A | N/A | 5.3 | 4 | 3.1 | 2.4 | 1.8 | 1.1 |
| 18 | N/A | N/A | 5.7 | 4.4 | 3.4 | 2.6 | 2 | 1.2 |
| 19 | N/A | N/A | 6.1 | 4.7 | 3.6 | 2.8 | 2.2 | 1.4 |
| 20 | N/A | N/A | 6.6 | 5.1 | 4 | 3.1 | 2.4 | 1.5 |
| 21 | N/A | N/A | 7 | 5.4 | 4.3 | 3.3 | 2.7 | 1.7 |
| 22 | N/A | N/A | 8 | 6.1 | 4.8 | 3.8 | 3 | 2 |
| 23 | N/A | N/A | 9 | 6.8 | 5.4 | 4.3 | 3.4 | 2.3 |
| 24 | N/A | N/A | 10 | 7.6 | 6 | 4.8 | 3.9 | 2.6 |
| 25 | N/A | N/A | 11.4 | 8.4 | 6.8 | 5.4 | 4.4 | 3 |
| 26 | N/A | N/A | 12.6 | 9.4 | 7.4 | 5.9 | 4.9 | 3.3 |
| 27 | N/A | N/A | N/A | 10.3 | 8.1 | 6.4 | 5.3 | 3.6 |
| 28 | N/A | N/A | N/A | 11.3 | 8.8 | 7.1 | 5.8 | 4 |

**Table 1–40. Transceiver Block Jitter Specifications for Arria II GX Devices** *(Note 1)* **(Part 9 of 10)**

| Symbol/ Description | Conditions | I3 | | | C4 | | | C5, I5 | | | C6 | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| **OBSAI Receiver Jitter Tolerance** *(12)* | | | | | | | | | | | | | | |
| Deterministic jitter tolerance at 768 Mbps, 1536 Mbps, and 3072 Mbps | Pattern = CJPAT | > 0.37 | | | > 0.37 | | | > 0.37 | | | > 0.37 | | | UI |
| Combined deterministic and random jitter tolerance at 768 Mbps, 1536 Mbps, and 3072 Mbps | Pattern = CJPAT | > 0.55 | | | > 0.55 | | | > 0.55 | | | > 0.55 | | | UI |
| Sinusoidal jitter tolerance at 768 Mbps | Jitter frequency = 5.4 KHz<br>Pattern = CJPAT | > 8.5 | | | > 8.5 | | | > 8.5 | | | > 8.5 | | | UI |
| | Jitter frequency = 460.8 KHz to 20 MHz<br>Pattern = CJPAT | > 0.1 | | | > 0.1 | | | > 0.1 | | | > 0.1 | | | UI |
| Sinusoidal jitter tolerance at 1536 Mbps | Jitter frequency = 10.9 KHz<br>Pattern = CJPAT | > 8.5 | | | > 8.5 | | | > 8.5 | | | > 8.5 | | | UI |
| | Jitter frequency = 921.6 KHz to 20 MHz<br>Pattern = CJPAT | > 0.1 | | | > 0.1 | | | > 0.1 | | | > 0.1 | | | UI |

# Core Performance Specifications for the Arria II Device Family

This section describes the clock tree, phase-locked loop (PLL), digital signal processing (DSP), embedded memory, configuration, and JTAG specifications for Arria II GX and GZ devices.

## Clock Tree Specifications

Table 1–42 lists the clock tree specifications for Arria II GX devices.

**Table 1–42. Clock Tree Performance for Arria II GX Devices**

| Clock Network | Performance | | | Unit |
|---|---|---|---|---|
| | I3, C4 | C5,I5 | C6 | |
| GCLK and RCLK | 500 | 500 | 400 | MHz |
| PCLK | 420 | 350 | 280 | MHz |

Table 1–43 lists the clock tree specifications for Arria II GZ devices.

**Table 1–43. Clock Tree Performance for Arria II GZ Devices**

| Clock Network | Performance | | Unit |
|---|---|---|---|
| | –C3 and –I3 | –C4 and –I4 | |
| GCLK and RCLK | 700 | 500 | MHz |
| PCLK | 500 | 450 | MHz |

## PLL Specifications

Table 1–44 lists the PLL specifications for Arria II GX devices.

**Table 1–44. PLL Specifications for Arria II GX Devices (Part 1 of 3)**

| Symbol | Description | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $f_{IN}$ | Input clock frequency (from clock input pins residing in right/top/bottom banks) (–4 Speed Grade) | 5 | — | 670 *(1)* | MHz |
| | Input clock frequency (from clock input pins residing in right/top/bottom banks) (–5 Speed Grade) | 5 | — | 622 *(1)* | MHz |
| | Input clock frequency (from clock input pins residing in right/top/bottom banks) (–6 Speed Grade) | 5 | — | 500 *(1)* | MHz |
| $f_{INPFD}$ | Input frequency to the PFD | 5 | — | 325 | MHz |
| $f_{VCO}$ | PLL VCO operating Range *(2)* | 600 | — | 1,400 | MHz |
| $f_{INDUTY}$ | Input clock duty cycle | 40 | — | 60 | % |
| $f_{EINDUTY}$ | External feedback clock input duty cycle | 40 | — | 60 | % |
| $t_{INCCJ}$ *(3)*, *(4)* | Input clock cycle-to-cycle jitter (Frequency ≥ 100 MHz) | — | — | 0.15 | UI (p–p) |
| | Input clock cycle-to-cycle jitter (Frequency ≤ 100 MHz) | — | — | ±750 | ps (p–p) |

**Table 1–44. PLL Specifications for Arria II GX Devices (Part 2 of 3)**

| Symbol | Description | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $f_{OUT}$ | Output frequency for internal global or regional clock (–4 Speed Grade) | — | — | 500 | MHz |
| | Output frequency for internal global or regional clock (–5 Speed Grade) | — | — | 500 | MHz |
| | Output frequency for internal global or regional clock (–6 Speed Grade) | — | — | 400 | MHz |
| $f_{OUT\_EXT}$ | Output frequency for external clock output (–4 Speed Grade) | — | — | 670 *(5)* | MHz |
| | Output frequency for external clock output (–5 Speed Grade) | — | — | 622 *(5)* | MHz |
| | Output frequency for external clock output (–6 Speed Grade) | — | — | 500 *(5)* | MHz |
| $t_{OUTDUTY}$ | Duty cycle for external clock output (when set to 50%) | 45 | 50 | 55 | % |
| $t_{OUTPJ\_DC}$ | Dedicated clock output period jitter ($f_{OUT} \geq 100$ MHz) | — | — | 300 | ps (p–p) |
| | Dedicated clock output period jitter ($f_{OUT} < 100$ MHz) | — | — | 30 | mUI (p–p) |
| $t_{OUTCCJ\_DC}$ | Dedicated clock output cycle-to-cycle jitter ($f_{OUT} \geq 100$ MHz) | — | — | 300 | ps (p–p) |
| | Dedicated clock output cycle-to-cycle jitter ($f_{OUT} < 100$ MHz) | — | — | 30 | mUI (p–p) |
| $f_{OUTPJ\_IO}$ | Regular I/O clock output period jitter ($f_{OUT} \geq 100$ MHz) | — | — | 650 | ps (p–p) |
| | Regular I/O clock output period jitter ($f_{OUT} < 100$ MHz) | — | — | 65 | mUI (p–p) |
| $f_{OUTCCJ\_IO}$ | Regular I/O clock output cycle-to-cycle jitter ($f_{OUT} \geq 100$ MHz) | — | — | 650 | ps (p–p) |
| | Regular I/O clock output cycle-to-cycle jitter ($f_{OUT} < 100$ MHz) | — | — | 65 | mUI (p–p) |
| $t_{CONFIGPLL}$ | Time required to reconfigure PLL scan chains | — | 3.5 | — | SCANCLK cycles |
| $t_{CONFIGPHASE}$ | Time required to reconfigure phase shift | — | 1 | — | SCANCLK cycles |
| $f_{SCANCLK}$ | SCANCLK frequency | — | — | 100 | MHz |
| $t_{LOCK}$ | Time required to lock from end of device configuration | — | — | 1 | ms |
| $t_{DLOCK}$ | Time required to lock dynamically (after switchover or reconfiguring any non-post-scale counters/delays) | — | — | 1 | ms |
| $f_{CL\ B\ W}$ | PLL closed-loop low bandwidth | — | 0.3 | — | MHz |
| | PLL closed-loop medium bandwidth | — | 1.5 | — | MHz |
| | PLL closed-loop high bandwidth | — | 4 | — | MHz |
| $t_{PLL\_PSERR}$ | Accuracy of PLL phase shift | — | — | ±50 | ps |
| $t_{ARESET}$ | Minimum pulse width on `areset` signal | 10 | — | — | ns |

**Table 1–45. PLL Specifications for Arria II GZ Devices (Part 2 of 2)**

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $t_{DLOCK}$ | Time required to lock dynamically (after switchover or reconfiguring any non-post-scale counters/delays) | — | — | 1 | ms |
| $f_{CLBW}$ | PLL closed-loop low bandwidth | — | 0.3 | — | MHz |
| | PLL closed-loop medium bandwidth | — | 1.5 | — | MHz |
| | PLL closed-loop high bandwidth *(7)* | — | 4 | — | MHz |
| $t_{PLL\_PSERR}$ | Accuracy of PLL phase shift | — | — | ±50 | ps |
| $t_{ARESET}$ | Minimum pulse width on the `areset` signal | 10 | — | — | ns |
| $t_{INCCJ}$ *(3)*, *(4)* | Input clock cycle to cycle jitter ($F_{REF} \geq$ 100 MHz) | — | — | 0.15 | UI (p-p) |
| | Input clock cycle to cycle jitter ($F_{REF} <$ 100 MHz) | — | — | ±750 | ps (p-p) |
| $t_{OUTPJ\_DC}$ *(5)* | Period Jitter for dedicated clock output ($F_{OUT} \geq$ 100 MHz) | — | — | 175 | ps (p-p) |
| | Period Jitter for dedicated clock output ($F_{OUT} <$ 100 MHz) | — | — | 17.5 | mUI (p-p) |
| $t_{OUTCCJ\_DC}$ *(5)* | Cycle to Cycle Jitter for dedicated clock output ($F_{OUT} \geq$ 100 MHz) | — | — | 175 | ps (p-p) |
| | Cycle to Cycle Jitter for dedicated clock output ($F_{OUT} <$ 100 MHz) | — | — | 17.5 | mUI (p-p) |
| $t_{OUTPJ\_IO}$ *(5)*, *(8)* | Period Jitter for clock output on regular I/O ($F_{OUT} \geq$ 100 MHz) | — | — | 600 | ps (p-p) |
| | Period Jitter for clock output on regular I/O ($F_{OUT} <$ 100 MHz) | — | — | 60 | mUI (p-p) |
| $t_{OUTCCJ\_IO}$ *(5)*, *(8)* | Cycle to Cycle Jitter for clock output on regular I/O ($F_{OUT} \geq$ 100 MHz) | — | — | 600 | ps (p-p) |
| | Cycle to Cycle Jitter for clock output on regular I/O ($F_{OUT} <$ 100 MHz) | — | — | 60 | mUI (p-p) |
| $t_{CASC\_OUTPJ\_DC}$ *(5)*, *(6)* | Period Jitter for dedicated clock output in cascaded PLLs ($F_{OUT} \geq$100MHz) | — | — | 250 | ps (p-p) |
| | Period Jitter for dedicated clock output in cascaded PLLs ($F_{OUT} <$ 100MHz) | — | — | 25 | mUI (p-p) |
| $f_{DRIFT}$ | Frequency drift after PFDENA is disabled for duration of 100 us | — | — | ±10 | % |

**Notes to Table 1–45:**

(1) This specification is limited in the Quartus II software by the I/O maximum frequency. The maximum I/O frequency is different for each I/O standard.

(2) This specification is limited by the lower of the two: I/O $F_{MAX}$ or $F_{OUT}$ of the PLL.

(3) A high input jitter directly affects the PLL output jitter. To have low PLL output clock jitter, you must provide a clean clock source that is less than 120 ps.

(4) $F_{REF}$ is fIN/N when N = 1.

(5) Peak-to-peak jitter with a probability level of $10^{-12}$ (14 sigma, 99.99999999974404% confidence level). The output jitter specification applies to the intrinsic jitter of the PLL, when an input jitter of 30 ps is applied. The external memory interface clock output jitter specifications use a different measurement method and are available in Table 1–64 on page 1–71.

(6) The cascaded PLL specification is only applicable with the following condition:
a. Upstream PLL: 0.59 Mhz ≤ Upstream PLL BW < 1 MHz
b. Downstream PLL: Downstream PLL BW > 2 MHz

(7) High bandwidth PLL settings are not supported in external feedback mode.

(8) External memory interface clock output jitter specifications use a different measurement method, which is available in Table 1–63 on page 1–71.

## DSP Block Specifications

Table 1–46 lists the DSP block performance specifications for Arria II GX devices.

**Table 1–46. DSP Block Performance Specifications for Arria II GX Devices *(Note 1)***

| Mode | Resources Used | Performance | | | | Unit |
|---|---|---|---|---|---|---|
| | Number of Multipliers | C4 | I3 | C5,I5 | C6 | |
| 9 × 9-bit multiplier | 1 | 380 | 310 | 300 | 250 | MHz |
| 12 × 12-bit multiplier | 1 | 380 | 310 | 300 | 250 | MHz |
| 18 × 18-bit multiplier | 1 | 380 | 310 | 300 | 250 | MHz |
| 36 × 36-bit multiplier | 1 | 350 | 270 | 270 | 220 | MHz |
| 18 × 36-bit high-precision multiplier adder mode | 1 | 350 | 270 | 270 | 220 | MHz |
| 18 × 18-bit multiply accumulator | 4 | 380 | 310 | 300 | 250 | MHz |
| 18 × 18-bit multiply adder | 4 | 380 | 310 | 300 | 250 | MHz |
| 18 × 18-bit multiply adder-signed full precision | 2 | 380 | 310 | 300 | 250 | MHz |
| 18 × 18-bit multiply adder with loopback *(2)* | 2 | 275 | 220 | 220 | 180 | MHz |
| 36-bit shift (32-bit data) | 1 | 350 | 270 | 270 | 220 | MHz |
| Double mode | 1 | 350 | 270 | 270 | 220 | MHz |

**Notes to Table 1–46:**

(1) Maximum is for a fully-pipelined block with **Round** and **Saturation** disabled.

(2) Maximum is for loopback input registers disabled, **Round** and **Saturation** disabled, pipeline and output registers enabled.

Table 1–47 lists the DSP block performance specifications for Arria II GZ devices.

**Table 1–47. DSP Block Performance Specifications for Arria II GZ Devices *(Note 1)* (Part 1 of 2)**

| Mode | Resources Used | Performance | | Unit |
|---|---|---|---|---|
| | Number of Multipliers | –3 | –4 | |
| 9 × 9-bit multiplier | 1 | 460 | 400 | MHz |
| 12 × 12-bit multiplier | 1 | 500 | 440 | MHz |
| 18 × 18-bit multiplier | 1 | 550 | 480 | MHz |
| 36 × 36-bit multiplier | 1 | 440 | 380 | MHz |
| 18 × 18-bit multiply accumulator | 4 | 440 | 380 | MHz |
| 18 × 18-bit multiply adder | 4 | 470 | 410 | MHz |
| 18 × 18-bit multiply adder-signed full precision | 2 | 450 | 390 | MHz |
| 18 × 18-bit multiply adder with loopback *(2)* | 2 | 350 | 310 | MHz |
| 36-bit shift (32-bit data) | 1 | 440 | 380 | MHz |

**Table 1–53. High-Speed I/O Specifications for Arria II GX Devices (Part 4 of 4)**

| Symbol | Conditions | I3 | | C4 | | C5,I5 | | C6 | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| $f_{HSDR}$ (data rate) | SERDES factor J = 3 to 10 | *(3)* | 945 *(7)* | *(3)* | 945 *(7)* | *(3)* | 740 *(7)* | *(3)* | 640 *(7)* | Mbps |
| | SERDES factor J = 2 (using DDR registers) | *(3)* | *(7)* | *(3)* | *(7)* | *(3)* | *(7)* | *(3)* | *(7)* | Mbps |
| | SERDES factor J = 1 (using SDR registers) | *(3)* | *(7)* | *(3)* | *(7)* | *(3)* | *(7)* | *(3)* | *(7)* | Mbps |
| Soft-CDR PPM tolerance | Soft-CDR mode | — | 300 | — | 300 | — | 300 | — | 300 | ±PPM |
| DPA run length | DPA mode | — | 10,000 | — | 10,000 | — | 10,000 | — | 10,000 | UI |
| Sampling window (SW) | Non-DPA mode *(5)* | — | 300 | — | 300 | — | 350 | — | 400 | ps |

**Notes to Table 1–53:**

(1) $f_{HSCLK\_IN} = f_{HSDR}$ / W. Use W to determine the supported selection of input reference clock frequencies for the desired data rate.

(2) Applicable for interfacing with DPA receivers only. For interfacing with non-DPA receivers, you must calculate the leftover timing margin in the receiver by performing link timing closure analysis. For Arria II GX transmitter to Arria II GX non-DPA receiver, the maximum supported data rate is 945 Mbps. For data rates above 840 Mbps, perform PCB trace compensation by adjusting the PCB trace length for LVDS channels to improve channel-to-channel skews.

(3) The minimum and maximum specification depends on the clock source (for example, PLL and clock pin) and the clock routing resource you use (global, regional, or local). The I/O differential buffer and input register do not have a minimum toggle rate.

(4) The specification is only applicable under the influence of core noise.

(5) Applicable for true LVDS using dedicated SERDES only.

(6) Dedicated SERDES and DPA features are only available on the right banks.

(7) You must calculate the leftover timing margin in the receiver by performing link timing closure analysis. You must consider the board skew margin, transmitter channel-to-channel skew, and the receiver sampling margin to determine the leftover timing margin.

Table 1–54 lists the high-speed I/O timing for Arria II GZ devices.

**Table 1–54. High-Speed I/O Specifications for Arria II GZ Devices *(Note 1), (2), (10)* (Part 1 of 3)**

| Symbol | Conditions | C3, I3 | | | C4, I4 | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| **Clock** | | | | | | | | |
| $f_{HSCLK\_in}$ (input clock frequency) true differential I/O standards | Clock boost factor W = 1 to 40 *(3)* | 5 | — | 717 | 5 | — | 717 | MHz |
| $f_{HSCLK\_in}$ (input clock frequency) single ended I/O standards *(9)* | Clock boost factor W = 1 to 40 *(3)* | 5 | — | 717 | 5 | — | 717 | MHz |
| $f_{HSCLK\_in}$ (input clock frequency) single ended I/O standards *(10)* | Clock boost factor W = 1 to 40 *(3)* | 5 | — | 420 | 5 | — | 420 | MHz |

**Table 1–54. High-Speed I/O Specifications for Arria II GZ Devices** *(Note 1), (2), (10)* **(Part 2 of 3)**

| Symbol | Conditions | C3, I3 | | | C4, I4 | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| $f_{HSCLK\_OUT}$ (output clock frequency) | — | 5 | — | 717 *(7)* | 5 | — | 717 *(7)* | MHz |
| **Transmitter** | | | | | | | | |
| $f_{HSDR}$ (true LVDS output data rate) | SERDES factor, J = 3 to 10 (using dedicated SERDES) *(8)* | *(4)* | — | 1250 | *(4)* | — | 1250 | Mbps |
| | SERDES factor J = 2, (using DDR registers) | *(4)* | — | *(5)* | *(4)* | — | *(5)* | Mbps |
| | SERDES factor J = 1, (uses an SDR register) | *(4)* | — | *(5)* | *(4)* | — | *(5)* | Mbps |
| $f_{HSDR}$ (emulated LVDS_E_3R output data rate) *(5)* | SERDES factor J = 4 to 10 | *(4)* | — | 1152 | *(4)* | — | 800 | Mbps |
| $f_{HSDR}$ (emulated LVDS_E_1R output data rate) | | *(4)* | — | 200 | *(4)* | — | 200 | Mbps |
| $t_{x\ Jitter}$ | Total jitter for data rate, 600 Mbps to 1.6 Gbps | — | — | 160 | — | — | 160 | ps |
| | Total jitter for data rate, < 600 Mbps | — | — | 0.1 | — | — | 0.1 | UI |
| $t_{x\ Jitter}$ - emulated differential I/O standards with three external output resistor network | Total jitter for data rate, 600 Mbps to 1.25 Gbps | — | — | 300 | — | — | 325 | ps |
| | Total jitter for data rate < 600 Mbps | — | — | 0.2 | — | — | 0.25 | UI |
| $t_{x\ Jitter}$ - emulated differential I/O standards with one external output resistor network | — | — | — | 0.15 | — | — | 0.15 | UI |
| $t_{DUTY}$ | TX output clock duty cycle for both True and emulated differential I/O standards | 45 | 50 | 55 | 45 | 50 | 55 | % |

**Table 1–57. External Memory Interface Specifications for Arria II GX Devices (Part 2 of 2)**

| Frequency Mode | Frequency Range (MHz) | | | Resolution (°) | DQS Delay Buffer Mode *(1)* | Number of Delay Chains |
|---|---|---|---|---|---|---|
| | C4 | I3, C5, I5 | C6 | | | |
| 5 | 270-410 | 270-380 | 270-320 | 36 | High | 10 |
| 6 | 320-450 | 320-410 | 320-370 | 45 | High | 8 |

**Note to Table 1–57:**

(1) Low indicates a 6-bit DQS delay setting; high indicates a 5-bit DQS delay setting.

Table 1–58 lists the DLL frequency range specifications for Arria II GZ devices.

**Table 1–58. DLL Frequency Range Specifications for Arria II GZ Devices**

| Frequency Mode | Frequency Range (MHz) | | Available Phase Shift | DQS Delay Buffer Mode *(1)* | Number of Delay Chains |
|---|---|---|---|---|---|
| | –3 | –4 | | | |
| 0 | 90-130 | 90-120 | 22.5°, 45°, 67.5°, 90° | Low | 16 |
| 1 | 120-170 | 120-160 | 30°, 60°, 90°, 120° | Low | 12 |
| 2 | 150-210 | 150-200 | 36°, 72°, 108°, 144° | Low | 10 |
| 3 | 180-260 | 180-240 | 45°, 90°,135°, 180° | Low | 8 |
| 4 | 240-320 | 240-290 | 30°, 60°, 90°, 120° | High | 12 |
| 5 | 290-380 | 290-360 | 36°, 72°, 108°, 144° | High | 10 |
| 6 | 360-450 | 360-450 | 45°, 90°, 135°, 180° | High | 8 |
| 7 | 470-630 | 470-590 | 60°, 120°, 180°, 240° | High | 6 |

**Note to Table 1–58:**

(1) Low indicates a 6-bit DQS delay setting; high indicates a 5-bit DQS delay setting.

Table 1–59 lists the DQS phase offset delay per stage for Arria II GX devices.

**Table 1–59. DQS Phase Offset Delay Per Setting for Arria II GX Devices *(Note 1)*, *(2)*, *(3)***

| Speed Grade | Min | Max | Unit |
|---|---|---|---|
| C4 | 7.0 | 13.0 | ps |
| I3, C5, I5 | 7.0 | 15.0 | ps |
| C6 | 8.5 | 18.0 | ps |

**Notes to Table 1–59:**

(1) The valid settings for phase offset are -64 to +63 for frequency modes 0 to 3 and -32 to +31 for frequency modes 4 to 5.

(2) The typical value equals the average of the minimum and maximum values.

(3) The delay settings are linear.

**Table 1–68. Glossary (Part 3 of 4)**

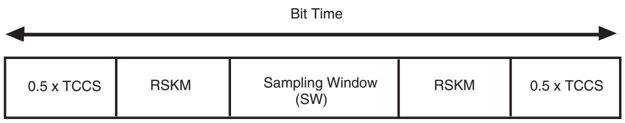
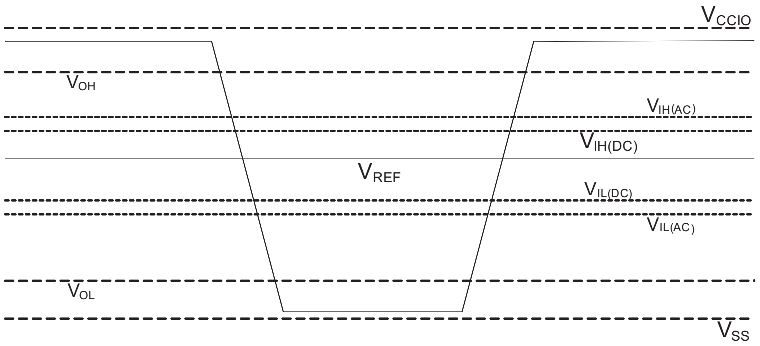
| Letter | Subject | Definitions |
|---|---|---|
| **S** | **SW (sampling window)** | The period of time during which the data must be valid in order to capture it correctly. The setup and hold times determine the ideal strobe position within the sampling window:<br>*Timing Diagram*<br> |
| | Single-ended Voltage Referenced I/O Standard | The JEDEC standard for SSTL and HSTL I/O standards define both the AC and DC input signal values. The AC values indicate the voltage levels at which the receiver must meet its timing specifications. The DC values indicate the voltage levels at which the final logic state of the receiver is unambiguously defined. After the receiver input has crossed the AC value, the receiver changes to the new logic state.<br>The new logic state is then maintained as long as the input stays beyond the AC threshold. This approach is intended to provide predictable receiver timing in the presence of input waveform ringing:<br>*Single-Ended Voltage Referenced I/O Standard*<br> |
| **T** | **$t_C$** | High-speed receiver and transmitter input and output clock period. |
| | **TCCS (channel-to-channel-skew)** | The timing difference between the fastest and slowest output edges, including $t_{CO}$ variation and clock skew, across channels driven by the same PLL. The clock is included in the TCCS measurement (refer to the *Timing Diagram* figure under **S** in this table). |
| | **$t_{DUTY}$** | High-speed I/O block: Duty cycle on the high-speed transmitter output clock.<br>**Timing Unit Interval (TUI)**<br>The timing budget allowed for skew, propagation delays, and data sampling window.<br>(TUI = 1/(Receiver Input Clock Frequency Multiplication Factor) = $t_C/w$) |
| | **$t_{FALL}$** | Signal high-to-low transition time (80-20%) |
| | **$t_{INCCJ}$** | Cycle-to-cycle jitter tolerance on the PLL clock input. |
| | **$t_{OUTPJ\_IO}$** | Period jitter on the general purpose I/O driven by a PLL. |
| | **$t_{OUTPJ\_DC}$** | Period jitter on the dedicated clock output driven by a PLL. |
| | **$t_{RISE}$** | Signal low-to-high transition time (20-80%). |

**Table 1–68. Glossary (Part 4 of 4)**

| Letter | Subject | Definitions |
|---|---|---|
| **U,**<br>**V** | **V**$_{CM(DC)}$ | DC common mode input voltage. |
| | **V**$_{ICM}$ | Input common mode voltage: The common mode of the differential signal at the receiver. |
| | **V**$_{ID}$ | Input differential voltage swing: The difference in voltage between the positive and complementary conductors of a differential transmission at the receiver. |
| | **V**$_{DIF(AC)}$ | AC differential input voltage: Minimum AC input differential voltage required for switching. |
| | **V**$_{DIF(DC)}$ | DC differential input voltage: Minimum DC input differential voltage required for switching. |
| | **V**$_{IH}$ | Voltage input high: The minimum positive voltage applied to the input which is accepted by the device as a logic high. |
| | **V**$_{IH(AC)}$ | High-level AC input voltage. |
| | **V**$_{IH(DC)}$ | High-level DC input voltage. |
| | **V**$_{IL}$ | Voltage input low: The maximum positive voltage applied to the input which is accepted by the device as a logic low. |
| | **V**$_{IL(AC)}$ | Low-level AC input voltage. |
| | **V**$_{IL(DC)}$ | Low-level DC input voltage. |
| | **V**$_{OCM}$ | Output common mode voltage: The common mode of the differential signal at the transmitter. |
| | **V**$_{OD}$ | Output differential voltage swing: The difference in voltage between the positive and complementary conductors of a differential transmission at the transmitter. |
| **W,**<br>X,<br>Y,<br>Z | W | High-speed I/O block: The clock boost factor. |

# Document Revision History

Table 1–69 lists the revision history for this chapter.

**Table 1–69. Document Revision History (Part 1 of 2)**

| Date | Version | Changes |
|---|---|---|
| December 2013 | 4.4 | Updated Table 1–34 and Table 1–35. |
| July 2012 | 4.3 | ■ Updated the V$_{CCH\_GXBL/R}$ operating conditions in Table 1–6.<br>■ Finalized Arria II GZ information in Table 1–20.<br>■ Added BLVDS specification in Table 1–32 and Table 1–33.<br>■ Updated input and output waveforms in Table 1–68. |
| December 2011 | 4.2 | ■ Updated Table 1–32, Table 1–33, Table 1–34, Table 1–35, Table 1–40, Table 1–41, Table 1–54, and Table 1–67.<br>■ Minor text edits. |
| June 2011 | 4.1 | ■ Added Table 1–60.<br>■ Updated Table 1–32, Table 1–33, Table 1–38, Table 1–41, and Table 1–61.<br>■ Updated the “Switching Characteristics” section introduction.<br>■ Minor text edits. |