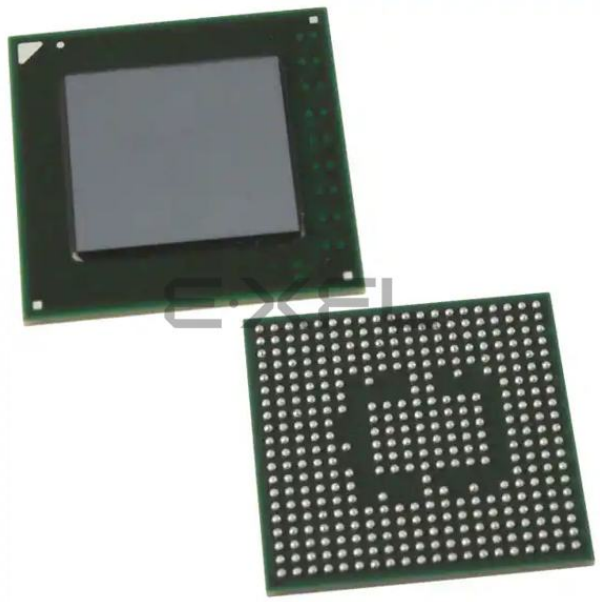
# Intel - EP2AGX65CU17C6NES Datasheet



**Welcome to E-XFL.COM**

## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | 2530 |
| Number of Logic Elements/Cells | 60214 |
| Total RAM Bits | 5371904 |
| Number of I/O | 156 |
| Number of Gates | - |
| Voltage - Supply | 0.87V ~ 0.93V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 85°C (TJ) |
| Package / Case | 358-LFBGA, FCBGA |
| Supplier Device Package | 358-UBGA, FCBGA (17x17) |
| Purchase URL | https://www.e-xfl.com/product-detail/intel/ep2agx65cu17c6nes |

**Table 1–2. Absolute Maximum Ratings for Arria II GZ Devices (Part 2 of 2)**

| Symbol | Description | Minimum | Maximum | Unit |
|---|---|---|---|---|
| $V_{CCA\_L}$ | Supplies transceiver high voltage power (left side) | -0.5 | 3.75 | V |
| $V_{CCA\_R}$ | Supplies transceiver high voltage power (right side) | -0.5 | 3.75 | V |
| $V_{CCHIP\_L}$ | Supplies transceiver HIP digital power (left side) | -0.5 | 1.35 | V |
| $V_{CCR\_L}$ | Supplies receiver power (left side) | -0.5 | 1.35 | V |
| $V_{CCR\_R}$ | Supplies receiver power (right side) | -0.5 | 1.35 | V |
| $V_{CCT\_L}$ | Supplies transmitter power (left side) | -0.5 | 1.35 | V |
| $V_{CCT\_R}$ | Supplies transmitter power (right side) | -0.5 | 1.35 | V |
| $V_{CCL\_GXBLn}$ *(1)* | Supplies power to the transceiver PMA TX, PMA RX, and clocking (left side) | -0.5 | 1.35 | V |
| $V_{CCL\_GXBRn}$ *(1)* | Supplies power to the transceiver PMA TX, PMA RX, and clocking (right side) | -0.5 | 1.35 | V |
| $V_{CCH\_GXBLn}$ *(1)* | Supplies power to the transceiver PMA output (TX) buffer (left side) | -0.5 | 1.8 | V |
| $V_{CCH\_GXBRn}$ *(1)* | Supplies power to the transceiver PMA output (TX) buffer (right side) | -0.5 | 1.8 | V |
| $T_J$ | Operating junction temperature | -55 | 125 | °C |
| $T_{STG}$ | Storage temperature (no bias) | -65 | 150 | °C |

**Note to Table 1–2:**

(1) n = 0, 1, or 2.

### Maximum Allowed Overshoot and Undershoot Voltage

During transitions, input signals may overshoot to the voltage shown in Table 1–3 and undershoot to –2.0 V for magnitude of currents less than 100 mA and periods shorter than 20 ns.

Table 1–3 lists the Arria II GX and GZ maximum allowed input overshoot voltage and the duration of the overshoot voltage as a percentage over the device lifetime. The maximum allowed overshoot duration is specified as a percentage of high-time over the lifetime of the device. A DC signal is equivalent to 100% duty cycle. For example, a signal that overshoots to 4.3 V can only be at 4.3 V for 5.41% over the lifetime of the device; for a device lifetime of 10 years, this amounts to 5.41/10ths of a year.

## Recommended Operating Conditions

This section lists the functional operation limits for AC and DC parameters for Arria II GX and GZ devices. All supplies are required to monotonically reach their full-rail values without plateaus within $t_{RAMP}$.

Table 1–5 lists the recommended operating conditions for Arria II GX devices.

**Table 1–5. Recommended Operating Conditions for Arria II GX Devices *(Note 1)* (Part 1 of 2)**

| Symbol | Description | Condition | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Supplies power to the core, periphery, I/O registers, PCIe HIP block, and transceiver PCS | — | 0.87 | 0.90 | 0.93 | V |
| $V_{CCCB}$ | Supplies power to the configuration RAM bits | — | 1.425 | 1.50 | 1.575 | V |
| $V_{CCBAT}$ *(2)* | Battery back-up power supply for design security volatile key registers | — | 1.2 | — | 3.3 | V |
| $V_{CCPD}$ *(3)* | Supplies power to the I/O pre-drivers, differential input buffers, and MSEL circuitry | — | 3.135 | 3.3 | 3.465 | V |
| | | — | 2.85 | 3.0 | 3.15 | V |
| | | — | 2.375 | 2.5 | 2.625 | V |
| $V_{CCIO}$ | Supplies power to the I/O banks *(4)* | — | 3.135 | 3.3 | 3.465 | V |
| | | — | 2.85 | 3.0 | 3.15 | V |
| | | — | 2.375 | 2.5 | 2.625 | V |
| | | — | 1.71 | 1.8 | 1.89 | V |
| | | — | 1.425 | 1.5 | 1.575 | V |
| | | — | 1.14 | 1.2 | 1.26 | V |
| $V_{CCD\_PLL}$ | Supplies power to the digital portions of the PLL | — | 0.87 | 0.90 | 0.93 | V |
| $V_{CCA\_PLL}$ | Supplies power to the analog portions of the PLL and device-wide power management circuitry | — | 2.375 | 2.5 | 2.625 | V |
| $V_I$ | DC Input voltage | — | –0.5 | — | 3.6 | V |
| $V_O$ | Output voltage | — | 0 | — | $V_{CCIO}$ | V |
| $V_{CCA}$ | Supplies power to the transceiver PMA regulator | — | 2.375 | 2.5 | 2.625 | V |
| $V_{CCL\_GXB}$ | Supplies power to the transceiver PMA TX, PMA RX, and clocking | — | 1.045 | 1.1 | 1.155 | V |
| $V_{CCH\_GXB}$ | Supplies power to the transceiver PMA output (TX) buffer | — | 1.425 | 1.5 | 1.575 | V |
| $T_J$ | Operating junction temperature | Commercial | 0 | — | 85 | °C |
| | | Industrial | –40 | — | 100 | °C |

**Table 1–6. Recommended Operating Conditions for Arria II GZ Devices *(Note 6)* (Part 2 of 2)**

| Symbol | Description | Condition | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|---|
| $V_{CCL\_GXBLn}$ *(3)* | Transceiver clock power (left side) | — | 1.05 | 1.1 | 1.15 | V |
| $V_{CCL\_GXBRn}$ *(3)* | Transceiver clock power (right side) | — | 1.05 | 1.1 | 1.15 | V |
| $V_{CCH\_GXBLn}$ *(3)* | Transmitter output buffer power (left side) | — | 1.33/1.425 | 1.4/1.5 *(5)* | 1.575 | V |
| $V_{CCH\_GXBRn}$ *(3)* | Transmitter output buffer power (right side) | — | | | | |
| $T_J$ | Operating junction temperature | Commercial | 0 | — | 85 | °C |
| | | Industrial | –40 | — | 100 | °C |
| $t_{RAMP}$ | Power supply ramp time | Normal POR (PORSEL=0) | 0.05 | — | 100 | ms |
| | | Fast POR (PORSEL=1) | 0.05 | — | 4 | ms |

**Notes to Table 1–6:**

(1) Altera recommends a 3.0-V nominal battery voltage when connecting $V_{CCBAT}$ to a battery for volatile key backup. If you do not use the volatile security key, you may connect the $V_{CCBAT}$ to either GND or a 3.0-V power supply.

(2) $V_{CCPD}$ must be 2.5 V when $V_{CCIO}$ is 2.5, 1.8, 1.5, or 1.2 V. $V_{CCPD}$ must be 3.0 V when $V_{CCIO}$ is 3.0 V.

(3) n = 0, 1, or 2.

(4) $V_{CCA\_L/R}$ must be connected to a 3.0-V supply if the clock multiplier unit (CMU) phase-locked loop (PLL), receiver clock data recovery (CDR), or both, are configured at a base data rate > 4.25 Gbps. For data rates up to 4.25 Gbps, you can connect $V_{CCA\_L/R}$ to either 3.0 V or 2.5 V.

(5) $V_{CCH\_GXBL/R}$ must be connected to a 1.4-V supply if the transmitter channel data rate is > 6.5 Gbps. For data rates up to 6.5 Gbps, you can connect $V_{CCH\_GXBL/R}$ to either 1.4 V or 1.5 V.

(6) Transceiver power supplies do not have power-on-reset (POR) circuitry. After initial power-up, violating the transceiver power supply operating conditions could lead to unpredictable link behavior.

## DC Characteristics

This section lists the supply current, I/O pin leakage current, on-chip termination (OCT) accuracy and variation, input pin capacitance, internal weak pull-up and pull-down resistance, hot socketing, and Schmitt trigger input specifications.

### Supply Current

Standby current is the current the device draws after the device is configured with no inputs or outputs toggling and no activity in the device. Because these currents vary largely with the resources used, use the Microsoft Excel-based Early Power Estimator (EPE) to get supply current estimates for your design.

For more information about power estimation tools, refer to the *PowerPlay Early Power Estimator User Guide* and the *PowerPlay Power Analysis* chapter.

**Table 1–11. OCT With and Without Calibration Specification for Arria II GX Device I/Os *(Note 1)* (Part 2 of 2)**

| Symbol | Description | Conditions (V) | Calibration Accuracy | | Unit |
|---|---|---|---|---|---|
| | | | Commercial | Industrial | |
| 50-Ω $R_S$ 3.0, 2.5, 1.8, 1.5, 1.2 | 50-Ω series OCT with calibration | $V_{CCIO}$ = 3.0, 2.5, 1.8, 1.5, 1.2 | ± 10 | ± 10 | % |
| 100-Ω $R_D$ 2.5 | 100-Ω differential OCT without calibration | $V_{CCIO}$ = 2.5 | ± 30 | ± 30 | % |

**Note to Table 1–11:**

(1) OCT with calibration accuracy is valid at the time of calibration only.

Table 1–12 lists the OCT termination calibration accuracy specifications for Arria II GZ devices.

**Table 1–12. OCT with Calibration Accuracy Specifications for Arria II GZ Devices *(Note 1)***

| Symbol | Description | Conditions (V) | Calibration Accuracy | | | Unit |
|---|---|---|---|---|---|---|
| | | | C2 | C3,I3 | C4,I4 | |
| 25-Ω $R_S$ 3.0, 2.5, 1.8, 1.5, 1.2 *(2)* | 25-Ω series OCT with calibration | $V_{CCIO}$ = 3.0, 2.5, 1.8, 1.5, 1.2 | ± 8 | ± 8 | ± 8 | % |
| 50-Ω $R_S$ 3.0, 2.5, 1.8, 1.5, 1.2 | 50-Ω internal series OCT with calibration | $V_{CCIO}$ = 3.0, 2.5, 1.8, 1.5, 1.2 | ± 8 | ± 8 | ± 8 | % |
| 50-Ω $R_T$ 2.5, 1.8, 1.5, 1.2 | 50-Ω internal parallel OCT with calibration | $V_{CCIO}$ = 2.5, 1.8, 1.5, 1.2 | ± 10 | ± 10 | ± 10 | % |
| 20-Ω , 40-Ω , and 60-Ω $R_S$ 3.0, 2.5, 1.8, 1.5, 1.2 *(3)* | 20-Ω , 40-Ω and 60-Ω $R_S$ expanded range for internal series OCT with calibration | $V_{CCIO}$ = 3.0, 2.5, 1.8, 1.5, 1.2 | ± 10 | ± 10 | ± 10 | % |
| 25-Ω $R_{S\_left\_shift}$ 3.0, 2.5, 1.8, 1.5, 1.2 | 25-Ω $R_{S\_left\_shift}$ internal left shift series OCT with calibration | $V_{CCIO}$ = 3.0, 2.5, 1.8, 1.5, 1.2 | ± 10 | ± 10 | ± 10 | % |

**Notes to Table 1–12:**

(1) OCT calibration accuracy is valid at the time of calibration only.

(2) 25-Ω $R_S$ is not supported for 1.5 V and 1.2 V in Row I/O.

(3) 20-Ω $R_S$ is not supported for 1.5 V and 1.2 V in Row I/O.

Table 1–26 lists the single-ended SSTL and HSTL I/O standard signal specifications for Arria II GX devices.

**Table 1–26. Single-Ended SSTL and HSTL I/O Standard Signal Specifications for Arria II GX Devices**

| I/O Standard | $V_{IL(DC)}$ (V) | | $V_{IH(DC)}$ (V) | | $V_{IL(AC)}$ (V) | $V_{IH(AC)}$ (V) | $V_{OL}$ (V) | $V_{OH}$ (V) | $I_{OL}$ (mA) | $I_{OH}$ (mA) |
|---|---|---|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Max | Min | Max | Min | | |
| SSTL-2 Class I | –0.3 | $V_{REF}$ - 0.18 | $V_{REF}$ + 0.18 | $V_{CCIO}$ + 0.3 | $V_{REF}$ - 0.35 | $V_{REF}$ + 0.35 | $V_{TT}$ - 0.57 | $V_{TT}$ + 0.57 | 8.1 | –8.1 |
| SSTL-2 Class II | –0.3 | $V_{REF}$ - 0.18 | $V_{REF}$ + 0.18 | $V_{CCIO}$ + 0.3 | $V_{REF}$ - 0.35 | $V_{REF}$ + 0.35 | $V_{TT}$ - 0.76 | $V_{TT}$ + 0.76 | 16.4 | –16.4 |
| SSTL-18 Class I | –0.3 | $V_{REF}$ - 0.125 | $V_{REF}$ + 0.125 | $V_{CCIO}$ + 0.3 | $V_{REF}$ - 0.25 | $V_{REF}$ + 0.25 | $V_{TT}$ - 0.475 | $V_{TT}$ + 0.475 | 6.7 | –6.7 |
| SSTL-18 Class II | –0.3 | $V_{REF}$ - 0.125 | $V_{REF}$ + 0.125 | $V_{CCIO}$ + 0.3 | $V_{REF}$ - 0.25 | $V_{REF}$ + 0.25 | 0.28 | $V_{CCIO}$ - 0.28 | 13.4 | –13.4 |
| SSTL-15 Class I | –0.3 | $V_{REF}$ - 0.1 | $V_{REF}$ + 0.1 | $V_{CCIO}$ + 0.3 | $V_{REF}$ - 0.175 | $V_{REF}$ + 0.175 | 0.2 × $V_{CCIO}$ | 0.8 × $V_{CCIO}$ | 8 | –8 |
| SSTL-15 Class II | –0.3 | $V_{REF}$ - 0.1 | $V_{REF}$ + 0.1 | $V_{CCIO}$ + 0.3 | $V_{REF}$ - 0.175 | $V_{REF}$ + 0.175 | 0.2 × $V_{CCIO}$ | 0.8 × $V_{CCIO}$ | 16 | –16 |
| HSTL-18 Class I | –0.3 | $V_{REF}$ - 0.1 | $V_{REF}$ + 0.1 | $V_{CCIO}$ + 0.3 | $V_{REF}$ - 0.2 | $V_{REF}$ + 0.2 | 0.4 | $V_{CCIO}$ - 0.4 | 8 | –8 |
| HSTL-18 Class II | –0.3 | $V_{REF}$ - 0.1 | $V_{REF}$ + 0.1 | $V_{CCIO}$ + 0.3 | $V_{REF}$ - 0.2 | $V_{REF}$ + 0.2 | 0.4 | $V_{CCIO}$ - 0.4 | 16 | –16 |
| HSTL-15 Class I | –0.3 | $V_{REF}$ - 0.1 | $V_{REF}$ + 0.1 | $V_{CCIO}$ + 0.3 | $V_{REF}$ - 0.2 | $V_{REF}$ + 0.2 | 0.4 | $V_{CCIO}$ - 0.4 | 8 | –8 |
| HSTL-15 Class II | –0.3 | $V_{REF}$ - 0.1 | $V_{REF}$ + 0.1 | $V_{CCIO}$ + 0.3 | $V_{REF}$ - 0.2 | $V_{REF}$ + 0.2 | 0.4 | $V_{CCIO}$ - 0.4 | 16 | –16 |
| HSTL-12 Class I | –0.15 | $V_{REF}$ - 0.08 | $V_{REF}$ + 0.08 | $V_{CCIO}$ + 0.15 | $V_{REF}$ - 0.15 | $V_{REF}$ + 0.15 | 0.25 × $V_{CCIO}$ | 0.75 × $V_{CCIO}$ | 8 | –8 |
| HSTL-12 Class II | –0.15 | $V_{REF}$ - 0.08 | $V_{REF}$ + 0.08 | $V_{CCIO}$ + 0.15 | $V_{REF}$ - 0.15 | $V_{REF}$ + 0.15 | 0.25 × $V_{CCIO}$ | 0.75 × $V_{CCIO}$ | 14 | –14 |

Table 1–27 lists the single-ended SSTL and HSTL I/O standard signal specifications for Arria II GZ devices.

**Table 1–27. Single-Ended SSTL and HSTL I/O Standards Signal Specifications for Arria II GZ Devices (Part 1 of 2)**

| I/O Standard | $V_{IL(DC)}$ (V) | | $V_{IH(DC)}$ (V) | | $V_{IL(AC)}$ (V) | $V_{IH(AC)}$ (V) | $V_{OL}$ (V) | $V_{OH}$ (V) | $I_{OL}$ (mA) | $I_{OH}$ (mA) |
|---|---|---|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Max | Min | Max | Min | | |
| SSTL-2 Class I | -0.3 | $V_{REF}$ - 0.15 | $V_{REF}$ + 0.15 | $V_{CCIO}$ + 0.3 | $V_{REF}$ - 0.31 | $V_{REF}$ + 0.31 | $V_{TT}$ - 0.57 | $V_{TT}$ + 0.57 | 8.1 | -8.1 |
| SSTL-2 Class II | -0.3 | $V_{REF}$ - 0.15 | $V_{REF}$ + 0.15 | $V_{CCIO}$ + 0.3 | $V_{REF}$ - 0.31 | $V_{REF}$ + 0.31 | $V_{TT}$ - 0.76 | $V_{TT}$ + 0.76 | 16.2 | -16.2 |
| SSTL-18 Class I | -0.3 | $V_{REF}$ - 0.125 | $V_{REF}$ + 0.125 | $V_{CCIO}$ + 0.3 | $V_{REF}$ - 0.25 | $V_{REF}$ + 0.25 | $V_{TT}$ - 0.475 | $V_{TT}$ + 0.475 | 6.7 | -6.7 |
| SSTL-18 Class II | -0.3 | $V_{REF}$ - 0.125 | $V_{REF}$ + 0.125 | $V_{CCIO}$ + 0.3 | $V_{REF}$ - 0.25 | $V_{REF}$ + 0.25 | 0.28 | $V_{CCIO}$ - 0.28 | 13.4 | -13.4 |
| SSTL-15 Class I | — | $V_{REF}$ - 0.1 | $V_{REF}$ + 0.1 | — | $V_{REF}$ - 0.175 | $V_{REF}$ + 0.175 | 0.2 × $V_{CCIO}$ | 0.8 × $V_{CCIO}$ | 8 | -8 |

**Table 1–35. Transceiver Specifications for Arria II GZ Devices (Part 3 of 5)**

| Symbol/ Description | Conditions | –C3 and –I3 *(1)* | | | –C4 and –I4 | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| Receiver DC Coupling Support | — | For more information about receiver DC coupling support, refer to the "DC-Coupled Links" section in the *Transceiver Architecture for Arria II Devices* chapter. | | | | | | |
| Differential on-chip termination resistors | 85–Ω setting | 85 ± 20% | | | 85 ± 20% | | | Ω |
| | 100–Ω setting | 100 ± 20% | | | 100 ± 20% | | | Ω |
| | 120–Ω setting | 120 ± 20% | | | 120 ± 20% | | | Ω |
| | 150-Ω setting | 150 ± 20% | | | 150 ± 20% | | | Ω |
| Differential and common mode return loss | PCIe (Gen 1 and Gen 2), XAUI, HiGig+, CEI SR/LR, SRIO SR/LR, CPRI LV/HV, OBSAI, SATA | Compliant | | | | | | — |
| Programmable PPM detector *(9)* | — | ± 62.5, 100, 125, 200, 250, 300, 500, 1,000 | | | | | | ppm |
| Run length | — | — | — | 200 | — | — | 200 | UI |
| Programmable equalization | — | — | — | 16 | — | — | 16 | dB |
| $t_{LTR}$ *(10)* | — | — | — | 75 | — | — | 75 | µs |
| $t_{LTR\_LTD\_Manual}$ *(11)* | — | 15 | — | — | 15 | — | — | µs |
| $t_{LTD\_Manual}$ *(12)* | — | — | — | 4000 | — | — | 4000 | ns |
| $t_{LTD\_Auto}$ *(13)* | — | — | — | 4000 | — | — | 4000 | ns |
| Receiver CDR 3 dB Bandwidth in lock-to-data (LTD) mode | PCIe Gen1 | 2.0 - 3.5 | | | | | | MHz |
| | PCIe Gen2 | 40 - 65 | | | | | | MHz |
| | (OIF) CEI PHY at 6.375 Gbps | 20 - 35 | | | | | | MHz |
| | XAUI | 10 - 18 | | | | | | MHz |
| | SRIO 1.25 Gbps | 10 - 18 | | | | | | MHz |
| | SRIO 2.5 Gbps | 10 - 18 | | | | | | MHz |
| | SRIO 3.125 Gbps | 6 - 10 | | | | | | MHz |
| | GIGE | 6 - 10 | | | | | | MHz |
| | SONET OC12 | 3 - 6 | | | | | | MHz |
| | SONET OC48 | 14 - 19 | | | | | | MHz |
| Receiver buffer and CDR offset cancellation time (per channel) | — | — | — | 17000 | — | — | 17000 | reconfig_clk cycles |
| Programmable DC gain | DC Gain Setting = 0 | — | 0 | — | — | 0 | — | dB |
| | DC Gain Setting = 1 | — | 3 | — | — | 3 | — | dB |
| | DC Gain Setting = 2 | — | 6 | — | — | 6 | — | dB |

Table 1–39 lists typical transmitter pre-emphasis levels for Arria II GZ devices (in dB) for the first post tap under the following conditions (low-frequency data pattern [five 1s and five 0s] at 6.25 Gbps). The levels listed in Table 1–39 are a representation of possible pre-emphasis levels under the specified conditions only and that the pre-emphasis levels may change with data pattern and data rate.

To predict the pre-emphasis level for your specific data rate and pattern, run simulations using the Arria II HSSI HSPICE models.

**Table 1–39. Transmitter Pre-Emphasis Levels for Arria II GZ Devices (Part 1 of 2)**

| Pre-Emphasis 1st Post-Tap Setting | $V_{OD}$ Setting | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | N/A | 0.7 | 0 | 0 | 0 | 0 | 0 | 0 |
| 2 | N/A | 1 | 0.3 | 0 | 0 | 0 | 0 | 0 |
| 3 | N/A | 1.5 | 0.6 | 0 | 0 | 0 | 0 | 0 |
| 4 | N/A | 2 | 0.7 | 0.3 | 0 | 0 | 0 | 0 |
| 5 | N/A | 2.7 | 1.2 | 0.5 | 0.3 | 0 | 0 | 0 |
| 6 | N/A | 3.1 | 1.3 | 0.8 | 0.5 | 0.2 | 0 | 0 |
| 7 | N/A | 3.7 | 1.8 | 1.1 | 0.7 | 0.4 | 0.2 | 0 |
| 8 | N/A | 4.2 | 2.1 | 1.3 | 0.9 | 0.6 | 0.3 | 0 |
| 9 | N/A | 4.9 | 2.4 | 1.6 | 1.2 | 0.8 | 0.5 | 0.2 |
| 10 | N/A | 5.4 | 2.8 | 1.9 | 1.4 | 1 | 0.7 | 0.3 |
| 11 | N/A | 6 | 3.2 | 2.2 | 1.7 | 1.2 | 0.9 | 0.4 |
| 12 | N/A | 6.8 | 3.5 | 2.6 | 1.9 | 1.4 | 1.1 | 0.6 |
| 13 | N/A | 7.5 | 3.8 | 2.8 | 2.1 | 1.6 | 1.2 | 0.6 |
| 14 | N/A | 8.1 | 4.2 | 3.1 | 2.3 | 1.7 | 1.3 | 0.7 |
| 15 | N/A | 8.8 | 4.5 | 3.4 | 2.6 | 1.9 | 1.5 | 0.8 |
| 16 | N/A | N/A | 4.9 | 3.7 | 2.9 | 2.2 | 1.7 | 0.9 |
| 17 | N/A | N/A | 5.3 | 4 | 3.1 | 2.4 | 1.8 | 1.1 |
| 18 | N/A | N/A | 5.7 | 4.4 | 3.4 | 2.6 | 2 | 1.2 |
| 19 | N/A | N/A | 6.1 | 4.7 | 3.6 | 2.8 | 2.2 | 1.4 |
| 20 | N/A | N/A | 6.6 | 5.1 | 4 | 3.1 | 2.4 | 1.5 |
| 21 | N/A | N/A | 7 | 5.4 | 4.3 | 3.3 | 2.7 | 1.7 |
| 22 | N/A | N/A | 8 | 6.1 | 4.8 | 3.8 | 3 | 2 |
| 23 | N/A | N/A | 9 | 6.8 | 5.4 | 4.3 | 3.4 | 2.3 |
| 24 | N/A | N/A | 10 | 7.6 | 6 | 4.8 | 3.9 | 2.6 |
| 25 | N/A | N/A | 11.4 | 8.4 | 6.8 | 5.4 | 4.4 | 3 |
| 26 | N/A | N/A | 12.6 | 9.4 | 7.4 | 5.9 | 4.9 | 3.3 |
| 27 | N/A | N/A | N/A | 10.3 | 8.1 | 6.4 | 5.3 | 3.6 |
| 28 | N/A | N/A | N/A | 11.3 | 8.8 | 7.1 | 5.8 | 4 |

**Table 1–40. Transceiver Block Jitter Specifications for Arria II GX Devices *(Note 1)* (Part 2 of 10)**

| Symbol/ Description | Conditions | I3 | | | C4 | | | C5, I5 | | | C6 | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Jitter tolerance at 2488.32 Mbps | Jitter frequency = 0.06 KHz Pattern = PRBS15 | | > 15 | | | > 15 | | | > 15 | | | > 15 | | UI |
| | Jitter frequency = 100 KHZ Pattern = PRBS15 | | > 1.5 | | | > 1.5 | | | > 1.5 | | | > 1.5 | | UI |
| | Jitter frequency = 1 MHz Pattern = PRBS15 | | > 0.15 | | | > 0.15 | | | > 0.15 | | | > 0.15 | | UI |
| | Jitter frequency = 10 MHz Pattern = PRBS15 | | > 0.15 | | | > 0.15 | | | > 0.15 | | | > 0.15 | | UI |
| **XAUI Transmit Jitter Generation *(3)*** | | | | | | | | | | | | | | |
| Total jitter at 3.125 Gbps | Pattern = CJPAT | — | — | 0.3 | — | — | 0.3 | — | — | 0.3 | — | — | 0.3 | UI |
| Deterministic jitter at 3.125 Gbps | Pattern = CJPAT | — | — | 0.17 | — | — | 0.17 | — | — | 0.17 | — | — | 0.17 | UI |
| **XAUI Receiver Jitter Tolerance *(3)*** | | | | | | | | | | | | | | |
| Total jitter | — | | > 0.65 | | | > 0.65 | | | > 0.65 | | | > 0.65 | | UI |
| Deterministic jitter | — | | > 0.37 | | | > 0.37 | | | > 0.37 | | | > 0.37 | | UI |
| Peak-to-peak jitter | Jitter frequency = 22.1 KHz | | > 8.5 | | | > 8.5 | | | > 8.5 | | | > 8.5 | | UI |
| Peak-to-peak jitter | Jitter frequency = 1.875 MHz | | > 0.1 | | | > 0.1 | | | > 0.1 | | | > 0.1 | | UI |
| Peak-to-peak jitter | Jitter frequency = 20 MHz | | > 0.1 | | | > 0.1 | | | > 0.1 | | | > 0.1 | | UI |
| **PCIe Transmit Jitter Generation *(4)*** | | | | | | | | | | | | | | |
| Total jitter at 2.5 Gbps (Gen1) | Compliance pattern | — | — | 0.25 | — | — | 0.25 | — | — | 0.25 | — | — | 0.25 | UI |

**Table 1–40. Transceiver Block Jitter Specifications for Arria II GX Devices *(Note 1)* (Part 5 of 10)**

| Symbol/ Description | Conditions | I3 | | | C4 | | | C5, I5 | | | C6 | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| **SDI Transmitter Jitter Generation *(8)*** | | | | | | | | | | | | | | |
| Alignment jitter (peak-to-peak) | Data rate = 1.485 Gbps (HD) pattern = Color Bar Low-frequency Roll-off = 100 KHz | 0.2 | — | — | 0.2 | — | — | 0.2 | — | — | 0.2 | — | — | UI |
| | Data rate = 2.97 Gbps (3G) pattern = Color bar Low-frequency Roll-off = 100 KHz | 0.3 | — | — | 0.3 | — | — | 0.3 | — | — | 0.3 | — | — | UI |
| **SDI Receiver Jitter Tolerance *(8)*** | | | | | | | | | | | | | | |
| Sinusoidal jitter tolerance (peak-to-peak) | Jitter frequency = 15 KHz<br>Data rate = 2.97 Gbps (3G) Pattern = single line scramble color bar | > 2 | | | > 2 | | | > 2 | | | > 2 | | | UI |
| | Jitter frequency = 100 KHz<br>Data rate = 2.97 Gbps (3G) Pattern = single line scramble color bar | > 0.3 | | | > 0.3 | | | > 0.3 | | | > 0.3 | | | UI |
| | Jitter frequency = 148.5 MHz<br>Data rate = 2.97 Gbps (3G) Pattern = single line scramble color bar | > 0.3 | | | > 0.3 | | | > 0.3 | | | > 0.3 | | | UI |

**Table 1–40. Transceiver Block Jitter Specifications for Arria II GX Devices *(Note 1)* (Part 8 of 10)**

| Symbol/ Description | Conditions | I3 | | | C4 | | | C5, I5 | | | C6 | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| **CPRI Transmit Jitter Generation** *(11)* | | | | | | | | | | | | | | |
| Total jitter | E.6.HV, E.12.HV Pattern = CJPAT | — | — | 0.279 | — | — | 0.279 | — | — | 0.279 | — | — | 0.279 | UI |
| | E.6.LV, E.12.LV, E.24.LV, E.30.LV Pattern = CJTPAT | — | — | 0.35 | — | — | 0.35 | — | — | 0.35 | — | — | 0.35 | UI |
| Deterministic jitter | E.6.HV, E.12.HV Pattern = CJPAT | — | — | 0.14 | — | — | 0.14 | — | — | 0.14 | — | — | 0.14 | UI |
| | E.6.LV, E.12.LV, E.24.LV, E.30.LV Pattern = CJTPAT | — | — | 0.17 | — | — | 0.17 | — | — | 0.17 | — | — | 0.17 | UI |
| **CPRI Receiver Jitter Tolerance** *(11)* | | | | | | | | | | | | | | |
| Total jitter tolerance | E.6.HV, E.12.HV Pattern = CJPAT | > 0.66 | | | > 0.66 | | | > 0.66 | | | > 0.66 | | | UI |
| Deterministic jitter tolerance | E.6.HV, E.12.HV Pattern = CJPAT | > 0.4 | | | > 0.4 | | | > 0.4 | | | > 0.4 | | | UI |
| Total jitter tolerance | E.6.LV, E.12.LV, E.24.LV, E.30.LV Pattern = CJTPAT | > 0.65 | | | > 0.65 | | | > 0.65 | | | > 0.65 | | | UI |
| | E.60.LV Pattern = PRBS31 | > 0.6 | | | — | | | — | | | — | | | UI |
| Deterministic jitter tolerance | E.6.LV, E.12.LV, E.24.LV, E.30.LV Pattern = CJTPAT | > 0.37 | | | > 0.37 | | | > 0.37 | | | > 0.37 | | | UI |
| | E.60.LV Pattern = PRBS31 | > 0.45 | | | — | | | — | | | — | | | UI |
| Combined deterministic and random jitter tolerance | E.6.LV, E.12.LV, E.24.LV, E.30.LV Pattern = CJTPAT | > 0.55 | | | > 0.55 | | | > 0.55 | | | > 0.55 | | | UI |
| **OBSAI Transmit Jitter Generation** *(12)* | | | | | | | | | | | | | | |
| Total jitter at 768 Mbps, 1536 Mbps, and 3072 Mbps | REFCLK = 153.6 MHz Pattern = CJPAT | — | — | 0.35 | — | — | 0.35 | — | — | 0.35 | — | — | 0.35 | UI |
| Deterministic jitter at 768 Mbps, 1536 Mbps, and 3072 Mbps | REFCLK = 153.6 MHz Pattern = CJPAT | — | — | 0.17 | — | — | 0.17 | — | — | 0.17 | — | — | 0.17 | UI |

**Table 1–40. Transceiver Block Jitter Specifications for Arria II GX Devices *(Note 1)* (Part 10 of 10)**

| Symbol/ Description | Conditions | I3 | | | C4 | | | C5, I5 | | | C6 | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Sinusoidal jitter tolerance at 3072 Mbps | Jitter frequency = 21.8 KHz<br>Pattern = CJPAT | | > 8.5 | | | > 8.5 | | | > 8.5 | | | > 8.5 | | UI |
| | Jitter frequency = 1843.2 KHz to 20 MHz<br>Pattern = CJPAT | | > 0.1 | | | > 0.1 | | | > 0.1 | | | > 0.1 | | UI |

**Notes to Table 1–40:**

(1) Dedicated `refclk` pins are used to drive the input reference clocks. The jitter numbers are valid for the stated conditions only.
(2) The jitter numbers for SONET/SDH are compliant to the GR-253-CORE Issue 3 Specification.
(3) The jitter numbers for XAUI are compliant to the IEEE802.3ae-2002 Specification.
(4) The jitter numbers for PCIe are compliant to the PCIe Base Specification 2.0.
(5) The jitter numbers for SRIO are compliant to the RapidIO Specification 1.3.
(6) The jitter numbers for GIGE are compliant to the IEEE802.3-2002 Specification.
(7) The jitter numbers for HiGig are compliant to the IEEE802.3ae-2002 Specification.
(8) The HD-SDI and 3G-SDI jitter numbers are compliant to the SMPTE292M and SMPTE424M Specifications.
(9) Arria II PCIe receivers are compliant to this specification provided the VTX_CM-DC-ACTIVEIDLE-DELTA of the upstream transmitter is less than 50 mV.
(10) The jitter numbers for Serial Advanced Technology Attachment (SATA) are compliant to the Serial ATA Revision 3.0 Specification.
(11) The jitter numbers for Common Public Radio Interface (CPRI) are compliant to the CPRI Specification V3.0.
(12) The jitter numbers for Open Base Station Architecture Initiative (OBSAI) are compliant to the OBSAI RP3 Specification V4.1.

Table 1–41 lists the transceiver jitter specifications for all supported protocols for Arria II GZ devices.

**Table 1–41. Transceiver Block Jitter Specifications for Arria II GZ Devices *(Note 1)*, *(2)* (Part 1 of 7)**

| Symbol/ Description | Conditions | –C3 and –I3 | | | –C4 and –I4 | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| **SONET/SDH Transmit Jitter Generation *(3)*** | | | | | | | | |
| Peak-to-peak jitter at 622.08 Mbps | Pattern = PRBS15 | — | — | 0.1 | — | — | 0.1 | UI |
| RMS jitter at 622.08 Mbps | Pattern = PRBS15 | — | — | 0.01 | — | — | 0.01 | UI |
| Peak-to-peak jitter at 2488.32 Mbps | Pattern = PRBS15 | — | — | 0.1 | — | — | 0.1 | UI |
| RMS jitter at 2488.32 Mbps | Pattern = PRBS15 | — | — | 0.01 | — | — | 0.01 | UI |
| **SONET/SDH Receiver Jitter Tolerance *(3)*** | | | | | | | | |
| Jitter tolerance at 622.08 Mbps | Jitter frequency = 0.03 KHz<br>Pattern = PRBS15 | | > 15 | | | > 15 | | UI |
| | Jitter frequency = 25 KHZ<br>Pattern = PRBS15 | | > 1.5 | | | > 1.5 | | UI |
| | Jitter frequency = 250 KHz<br>Pattern = PRBS15 | | > 0.15 | | | > 0.15 | | UI |

**Table 1–41. Transceiver Block Jitter Specifications for Arria II GZ Devices *(Note 1)*, *(2)* (Part 4 of 7)**

| Symbol/ Description | Conditions | –C3 and –I3 | | | –C4 and –I4 | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| **GIGE Receiver Jitter Tolerance *(11)*** | | | | | | | | |
| Deterministic jitter tolerance (peak-to-peak) | Pattern = CJPAT | | > 0.4 | | | > 0.4 | | UI |
| Combined deterministic and random jitter tolerance (peak-to-peak) | Pattern = CJPAT | | > 0.66 | | | > 0.66 | | UI |
| **HiGig Transmit Jitter Generation** | | | | | | | | |
| Deterministic jitter (peak-to-peak) | Data rate = 3.75 Gbps<br>Pattern = CJPAT | — | — | 0.17 | — | — | — | UI |
| Total jitter (peak-to-peak) | Data rate = 3.75 Gbps<br>Pattern = CJPAT | — | — | 0.35 | — | — | — | UI |
| **HiGig Receiver Jitter Tolerance** | | | | | | | | |
| Deterministic jitter tolerance (peak-to-peak) | Data rate = 3.75 Gbps<br>Pattern = CJPAT | | > 0.37 | | — | — | — | UI |
| Combined deterministic and random jitter tolerance (peak-to-peak) | Data rate = 3.75 Gbps<br>Pattern = CJPAT | | > 0.65 | | — | — | — | UI |
| Sinusoidal jitter tolerance (peak-to-peak) | Jitter frequency = 22.1 KHz<br>Data rate = 3.75 Gbps<br>Pattern = CJPAT | | > 8.5 | | — | — | — | UI |
| | Jitter frequency = 22.1 KHz<br>Data rate = 3.75 Gbps<br>Pattern = CJPAT | | > 0.1 | | — | — | — | UI |
| | Jitter frequency = 22.1 KHz<br>Data rate = 3.75 Gbps<br>Pattern = CJPAT | | > 0.1 | | — | — | — | UI |
| **(OIF) CEI Transmitter Jitter Generation** | | | | | | | | |
| Total jitter (peak-to-peak) | Data rate = 6.375 Gbps<br>Pattern = PRBS15 BER = $10^{-12}$ | — | — | 0.3 | — | — | 0.3 | UI |
| **(OIF) CEI Receiver Jitter Tolerance** | | | | | | | | |
| Deterministic jitter tolerance (peak-to-peak) | Data rate = 6.375 Gbps<br>Pattern = PRBS31 BER = $10^{-12}$ | | > 0.675 | | — | — | — | UI |
| Combined deterministic and random jitter tolerance (peak-to-peak) | Data rate = 6.375 Gbps<br>Pattern = PRBS31 BER = $10^{-12}$ | | > 0.988 | | — | — | — | UI |

**Table 1–41. Transceiver Block Jitter Specifications for Arria II GZ Devices *(Note 1)*, *(2)* (Part 5 of 7)**

| Symbol/ Description | Conditions | –C3 and –I3 | | | –C4 and –I4 | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| Sinusoidal jitter tolerance (peak-to-peak) | Jitter Frequency = 38.2 KHz<br>Data rate = 6.375 Gbps<br>Pattern = PRBS31 BER = $10^{-12}$ | > 0.5 | | | — | — | — | UI |
| | Jitter Frequency = 3.82 MHz<br>Data rate = 6.375 Gbps<br>Pattern = PRBS31 BER = $10^{-12}$ | > 0.05 | | | — | — | — | UI |
| | Jitter Frequency = 20 MHz<br>Data rate = 6.375 Gbps<br>Pattern = PRBS31 BER = $10^{-12}$ | > 0.05 | | | — | — | — | UI |
| **SDI Transmitter Jitter Generation *(12)*** | | | | | | | | |
| Alignment jitter (peak-to-peak) | Data rate = 1.485 Gbps (HD) Pattern = color bar Low-frequency roll-off = 100 KHz | 0.2 | — | — | 0.2 | — | — | UI |
| | Data rate = 2.97 Gbps (3G) Pattern = color bar Low-frequency roll-off = 100 KHz | 0.3 | — | — | 0.3 | — | — | UI |
| **SDI Receiver Jitter Tolerance *(12)*** | | | | | | | | |
| Sinusoidal jitter tolerance (peak-to-peak) | Jitter frequency = 15 KHz<br>Data rate = 2.97 Gbps (3G) Pattern = single line scramble color bar | > 2 | | | > 2 | | | UI |
| | Jitter frequency = 100 KHz<br>Data rate = 2.97 Gbps (3G) Pattern = single line scramble color bar | > 0.3 | | | > 0.3 | | | UI |
| | Jitter frequency = 148.5 MHz<br>Data rate = 2.97 Gbps (3G) Pattern = single line scramble color bar | > 0.3 | | | > 0.3 | | | UI |
| Sinusoidal jitter tolerance (peak-to-peak) | Jitter frequency = 20 KHz<br>Data rate = 1.485 Gbps (HD) pattern = 75% color bar | > 1 | | | > 1 | | | UI |
| | Jitter frequency = 100 KHz<br>Data rate = 1.485 Gbps (HD) Pattern = 75% color bar | > 0.2 | | | > 0.2 | | | UI |
| | Jitter frequency = 148.5 MHz<br>Data rate = 1.485 Gbps (HD) Pattern = 75% color bar | > 0.2 | | | > 0.2 | | | UI |
| **SAS Transmit Jitter Generation *(13)*** | | | | | | | | |
| Total jitter at 1.5 Gbps (G1) | Pattern = CJPAT | — | — | 0.55 | — | — | 0.55 | UI |
| Deterministic jitter at 1.5 Gbps (G1) | Pattern = CJPAT | — | — | 0.35 | — | — | 0.35 | UI |
| Total jitter at 3.0 Gbps (G2) | Pattern = CJPAT | — | — | 0.55 | — | — | 0.55 | UI |

**Table 1–44. PLL Specifications for Arria II GX Devices (Part 3 of 3)**

| Symbol | Description | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $t_{CASC\_OUTJITTER\_PERIOD\_DEDCLK}$ *(6), (7)* | Period Jitter for dedicated clock output in cascaded PLLs (FOUT ≥ 100 MHz) | — | — | 425 | ps (p-p) |
| | Period Jitter for dedicated clock output in cascaded PLLs (FOUT ≤ 100 MHz) | — | — | 42.5 | mUI (p-p) |

**Notes to Table 1–44:**

(1) $f_{IN}$ is limited by the I/O $f_{MAX}$.

(2) The VCO frequency reported by the Quartus II software in the PLL summary section of the compilation report takes into consideration the VCO post-scale counter K value. Therefore, if the counter K has a value of 2, the frequency reported can be lower than the $f_{VCO}$ specification.

(3) A high-input jitter directly affects the PLL output jitter. To have low PLL output clock jitter, you must provide a clean-clock source, which is less than 200 ps.

(4) $F_{REF}$ is fIN/N when N = 1.

(5) This specification is limited by the lower of the two: I/O $f_{MAX}$ or $f_{OUT}$ of the PLL.

(6) Peak-to-peak jitter with a probability level of $10^{-12}$ (14 sigma, 99.99999999974404% confidence level). The output jitter specification applies to the intrinsic jitter of the PLL, when an input jitter of 30 ps is applied. The external memory interface clock output jitter specifications use a different measurement method and are available in Table 1–62 on page 1–70.

(7) The cascaded PLL specification is only applicable with the following condition:
a. Upstream PLL: 0.59 Mhz ≤ Upstream PLL BW < 1 MHz
b. Downstream PLL: Downstream PLL BW > 2 MHz

Table 1–45 lists the PLL specifications for Arria II GZ devices when operating in both the commercial junction temperature range (0° to 85°C) and the industrial junction temperature range (-40° to 100°C).

**Table 1–45. PLL Specifications for Arria II GZ Devices (Part 1 of 2)**

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $f_{IN}$ | Input clock frequency (–3 speed grade) | 5 | — | 717 *(1)* | MHz |
| | Input clock frequency (–4 speed grade) | 5 | — | 717 *(1)* | MHz |
| $f_{INPFD}$ | Input frequency to the PFD | 5 | — | 325 | MHz |
| $f_{VCO}$ | PLL VCO operating range (–3 speed grade) | 600 | — | 1,300 | MHz |
| | PLL VCO operating range (–4 speed grade) | 600 | — | 1,300 | MHz |
| $t_{EINDUTY}$ | Input clock or external feedback clock input duty cycle | 40 | — | 60 | % |
| $f_{OUT}$ | Output frequency for internal global or regional clock (–3 speed grade) | — | — | 700 *(2)* | MHz |
| | Output frequency for internal global or regional clock (–4 speed grade) | — | — | 500 *(2)* | MHz |
| $f_{OUT\_EXT}$ | Output frequency for external clock output (–3 speed grade) | — | — | 717 *(2)* | MHz |
| | Output frequency for external clock output (–4 speed grade) | — | — | 717 *(2)* | MHz |
| $t_{OUTDUTY}$ | Duty cycle for external clock output (when set to 50%) | 45 | 50 | 55 | % |
| $t_{FCOMP}$ | External feedback clock compensation time | — | — | 10 | ns |
| $t_{CONFIGPLL}$ | Time required to reconfigure scan chain | — | 3.5 | — | scanclk cycles |
| $t_{CONFIGPHASE}$ | Time required to reconfigure phase shift | — | 1 | — | scanclk cycles |
| $f_{SCANCLK}$ | scanclk frequency | — | — | 100 | MHz |
| $t_{LOCK}$ | Time required to lock from end-of-device configuration or de-assertion of areset | — | — | 1 | ms |

## DSP Block Specifications

Table 1–46 lists the DSP block performance specifications for Arria II GX devices.

**Table 1–46. DSP Block Performance Specifications for Arria II GX Devices *(Note 1)***

| Mode | Resources Used | Performance | | | | Unit |
|---|---|---|---|---|---|---|
| | Number of Multipliers | C4 | I3 | C5,I5 | C6 | |
| 9 × 9-bit multiplier | 1 | 380 | 310 | 300 | 250 | MHz |
| 12 × 12-bit multiplier | 1 | 380 | 310 | 300 | 250 | MHz |
| 18 × 18-bit multiplier | 1 | 380 | 310 | 300 | 250 | MHz |
| 36 × 36-bit multiplier | 1 | 350 | 270 | 270 | 220 | MHz |
| 18 × 36-bit high-precision multiplier adder mode | 1 | 350 | 270 | 270 | 220 | MHz |
| 18 × 18-bit multiply accumulator | 4 | 380 | 310 | 300 | 250 | MHz |
| 18 × 18-bit multiply adder | 4 | 380 | 310 | 300 | 250 | MHz |
| 18 × 18-bit multiply adder-signed full precision | 2 | 380 | 310 | 300 | 250 | MHz |
| 18 × 18-bit multiply adder with loopback *(2)* | 2 | 275 | 220 | 220 | 180 | MHz |
| 36-bit shift (32-bit data) | 1 | 350 | 270 | 270 | 220 | MHz |
| Double mode | 1 | 350 | 270 | 270 | 220 | MHz |

**Notes to Table 1–46:**

(1) Maximum is for a fully-pipelined block with **Round** and **Saturation** disabled.

(2) Maximum is for loopback input registers disabled, **Round** and **Saturation** disabled, pipeline and output registers enabled.

Table 1–47 lists the DSP block performance specifications for Arria II GZ devices.

**Table 1–47. DSP Block Performance Specifications for Arria II GZ Devices *(Note 1)* (Part 1 of 2)**

| Mode | Resources Used | Performance | | Unit |
|---|---|---|---|---|
| | Number of Multipliers | –3 | –4 | |
| 9 × 9-bit multiplier | 1 | 460 | 400 | MHz |
| 12 × 12-bit multiplier | 1 | 500 | 440 | MHz |
| 18 × 18-bit multiplier | 1 | 550 | 480 | MHz |
| 36 × 36-bit multiplier | 1 | 440 | 380 | MHz |
| 18 × 18-bit multiply accumulator | 4 | 440 | 380 | MHz |
| 18 × 18-bit multiply adder | 4 | 470 | 410 | MHz |
| 18 × 18-bit multiply adder-signed full precision | 2 | 450 | 390 | MHz |
| 18 × 18-bit multiply adder with loopback *(2)* | 2 | 350 | 310 | MHz |
| 36-bit shift (32-bit data) | 1 | 440 | 380 | MHz |

Table 1–49 lists the embedded memory block specifications for Arria II GZ devices.

**Table 1–49. Embedded Memory Block Performance Specifications for Arria II GZ Devices *(Note 1)***

| Memory | Mode | Resources Used | | Performance | | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | ALUTs | TriMatrix Memory | C3 | I3 | C4 | I4 | |
| MLAB *(2)* | Single port 64 × 10 | 0 | 1 | 500 | 500 | 450 | 450 | MHz |
| | Simple dual-port 32 × 20 | 0 | 1 | 500 | 500 | 450 | 450 | MHz |
| | Simple dual-port 64 × 10 | 0 | 1 | 500 | 500 | 450 | 450 | MHz |
| | ROM 64 × 10 | 0 | 1 | 500 | 500 | 450 | 450 | MHz |
| | ROM 32 × 20 | 0 | 1 | 500 | 500 | 450 | 450 | MHz |
| M9K Block *(2)* | Single-port 256 × 36 | 0 | 1 | 540 | 540 | 475 | 475 | MHz |
| | Simple dual-port 256 × 36 | 0 | 1 | 490 | 490 | 420 | 420 | MHz |
| | Simple dual-port 256 × 36, with the read-during-write option set to **Old Data** | 0 | 1 | 340 | 340 | 300 | 300 | MHz |
| | True dual port 512 × 18 | 0 | 1 | 430 | 430 | 370 | 370 | MHz |
| | True dual-port 512 × 18, with the read-during-write option set to **Old Data** | 0 | 1 | 335 | 335 | 290 | 290 | MHz |
| | ROM 1 Port | 0 | 1 | 540 | 540 | 475 | 475 | MHz |
| | ROM 2 Port | 0 | 1 | 540 | 540 | 475 | 475 | MHz |
| | Min Pulse Width (clock high time) | — | — | 800 | 800 | 850 | 850 | ps |
| | Min Pulse Width (clock low time) | — | — | 625 | 625 | 690 | 690 | ps |
| M144K Block *(2)* | Single-port 2K × 72 | 0 | 1 | 440 | 400 | 380 | 350 | MHz |
| | Simple dual-port 2K × 72 | 0 | 1 | 435 | 375 | 385 | 325 | MHz |
| | Simple dual-port 2K × 72, with the read-during-write option set to **Old Data** | 0 | 1 | 240 | 225 | 205 | 200 | MHz |
| | Simple dual-port 2K × 64 (with ECC) | 0 | 1 | 300 | 295 | 255 | 250 | MHz |
| | True dual-port 4K × 36 | 0 | 1 | 375 | 350 | 330 | 310 | MHz |
| | True dual-port 4K × 36, with the read-during-write option set to **Old Data** | 0 | 1 | 230 | 225 | 205 | 200 | MHz |
| | ROM 1 Port | 0 | 1 | 500 | 450 | 435 | 420 | MHz |
| | ROM 2 Port | 0 | 1 | 465 | 425 | 400 | 400 | MHz |
| | Min Pulse Width (clock high time) | — | — | 755 | 860 | 860 | 950 | ps |
| | Min Pulse Width (clock low time) | — | — | 625 | 690 | 690 | 690 | ps |

**Notes to Table 1–48:**

(1) To achieve the maximum memory block performance, use a memory block clock that comes through global clock routing from an on-chip PLL set to 50% output duty cycle. Use the Quartus II software to report timing for this and other memory block clocking schemes.

(2) When you use the error detection CRC feature, there is no degradation in $F_{MAX}$.

**Table 1–54. High-Speed I/O Specifications for Arria II GZ Devices *(Note 1), (2), (10)* (Part 3 of 3)**

| Symbol | Conditions | C3, I3 | | | C4, I4 | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| $t_{RISE}$ & $t_{FALL}$ | True differential I/O standards | — | — | 200 | — | — | 200 | ps |
| | Emulated differential I/O standards with three external output resistor networks | — | — | 250 | — | — | 300 | ps |
| | Emulated differential I/O standards with one external output resistor | — | — | 500 | — | — | 500 | ps |
| TCCS | True LVDS | — | — | 100 | — | — | 100 | ps |
| | Emulated LVDS_E_3R | — | — | 250 | — | — | 250 | ps |
| **Receiver** | | | | | | | | |
| True differential I/O standards - $f_{HSDRDPA}$ (data rate) | SERDES factor J = 3 to 10 | 150 | — | 1250 | 150 | — | 1250 | Mbps |
| $f_{HSDR}$ (data rate) | SERDES factor J = 3 to 10 | *(4)* | — | *(6)* | *(4)* | — | *(6)* | Mbps |
| | SERDES factor J = 2, uses DDR registers | *(4)* | — | *(5)* | *(4)* | — | *(5)* | Mbps |
| | SERDES factor J = 1, uses an SDR register | *(4)* | — | *(5)* | *(4)* | — | *(5)* | Mbps |
| DPA run length | DPA mode | — | — | 10000 | — | — | 10000 | UI |
| Soft-CDR PPM tolerance | Soft-CDR mode | — | — | 300 | — | — | 300 | ± PPM |
| Sampling Window (SW) | Non-DPA mode | — | — | 300 | — | — | 300 | ps |

**Notes to Table 1–54:**

(1) When J = 3 to 10, use the SERDES block.

(2) When J = 1 or 2, bypass the SERDES block.

(3) Clock Boost Factor (W) is the ratio between input data rate to the input clock rate.

(4) The minimum specification depends on the clock source (for example, the PLL and clock pin) and the clock routing resource (global, regional, or local) that you use. The I/O differential buffer and input register do not have a minimum toggle rate.

(5) You must calculate the leftover timing margin in the receiver by performing link timing closure analysis. You must consider the board skew margin, transmitter channel-to-channel skew, and receiver sampling margin to determine leftover timing margin.

(6) You can estimate the achievable maximum data rate for non-DPA mode by performing link timing closure analysis. You must consider the board skew margin, transmitter delay margin, and the receiver sampling margin to determine the maximum data rate supported.

(7) This is achieved by using the LVDS and DPA clock network.

(8) If the receiver with DPA enabled and transmitter are using shared PLLs, the minimum data rate is 150 Mbps.

(9) This only applies to DPA and soft-CDR modes.

(10) This only applies to LVDS source synchronous mode.

Table 1–55 lists DPA lock time specifications for Arria II GX and GZ devices.

# Glossary

Table 1–68 lists the glossary for this chapter.

**Table 1–68. Glossary (Part 1 of 4)**

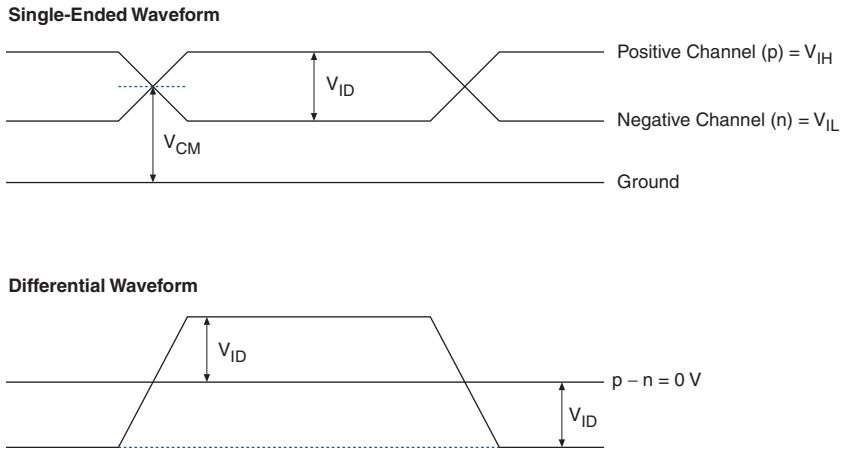
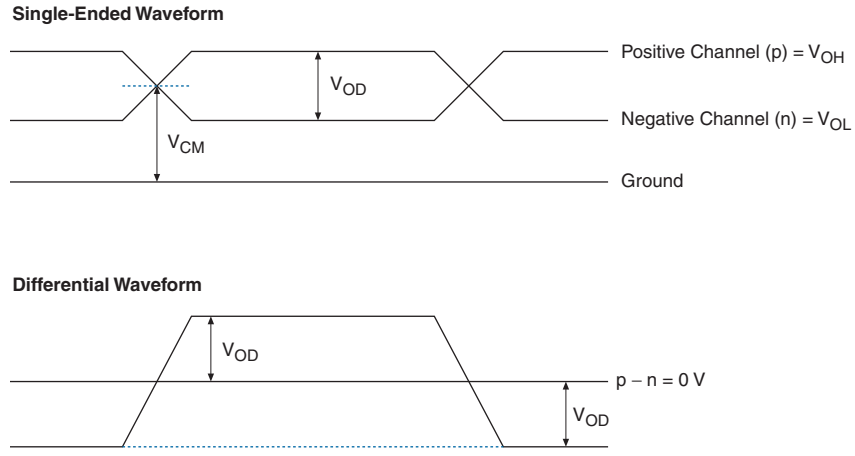
| Letter | Subject | Definitions |
|---|---|---|
| A, B, C, D | Differential I/O Standards | *Receiver Input Waveforms*<br>  <br>*Transmitter Output Waveforms*<br>  |
| E, F | $f_{HSCLK}$ | Left/Right PLL input clock frequency. |
| | $f_{HSDR}$ | High-speed I/O block: Maximum/minimum LVDS data transfer rate ($f_{HSDR}$ = 1/TUI), non-DPA. |
| | $f_{HSDRDPA}$ | High-speed I/O block: Maximum/minimum LVDS data transfer rate ($f_{HSDRDPA}$ = 1/TUI), DPA. |

**Table 1–68. Glossary (Part 2 of 4)**

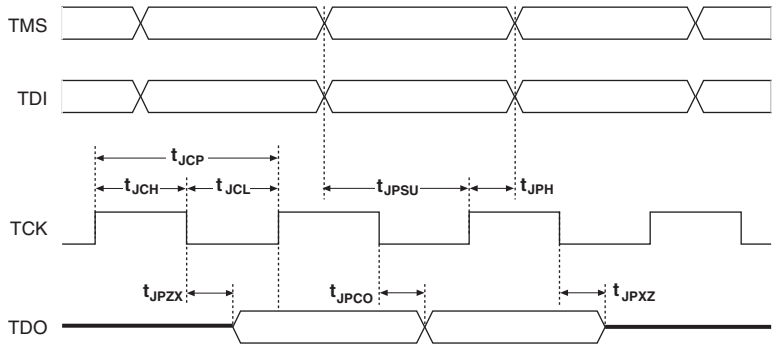
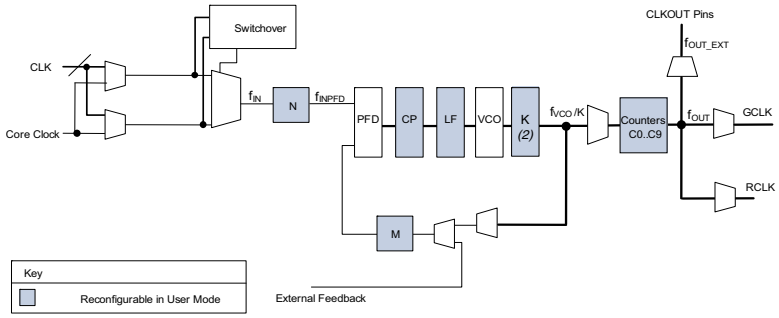
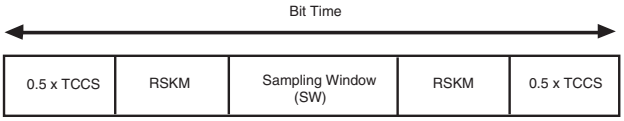
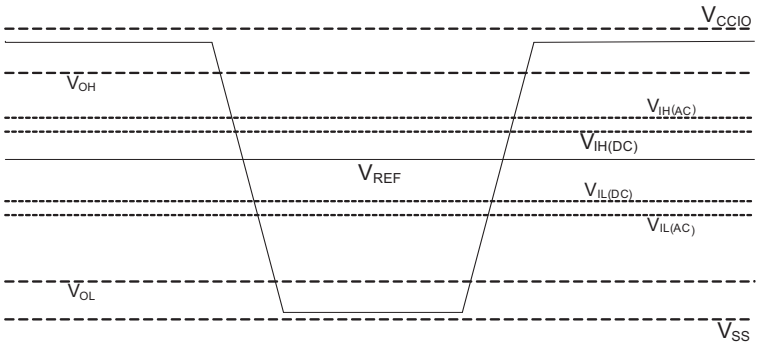
| Letter | Subject | Definitions |
|---|---|---|
| **G, H, I, J** | J | High-speed I/O block: Deserialization factor (width of parallel data bus). |
| | JTAG Timing Specifications | JTAG Timing Specifications:<br>  |
| **K, L, M, N, O, P** | PLL Specifications | PLL Specification parameters:<br>**Diagram of PLL Specifications** ***(1)***<br>  <br>**Notes:**<br>(1) CoreClock can only be fed by dedicated clock input pins or PLL outputs.<br>(2) This is the VCO post-scale counter K. |
| **Q, R** | $R_L$ | Receiver differential input discrete resistor (external to the Arria II device). |

**Table 1–68. Glossary (Part 3 of 4)**

| Letter | Subject | Definitions |
|---|---|---|
| S | **SW (sampling window)** | The period of time during which the data must be valid in order to capture it correctly. The setup and hold times determine the ideal strobe position within the sampling window:<br>*Timing Diagram*<br>  |
| | Single-ended Voltage Referenced I/O Standard | The JEDEC standard for SSTL and HSTL I/O standards define both the AC and DC input signal values. The AC values indicate the voltage levels at which the receiver must meet its timing specifications. The DC values indicate the voltage levels at which the final logic state of the receiver is unambiguously defined. After the receiver input has crossed the AC value, the receiver changes to the new logic state.<br>The new logic state is then maintained as long as the input stays beyond the AC threshold. This approach is intended to provide predictable receiver timing in the presence of input waveform ringing:<br>*Single-Ended Voltage Referenced I/O Standard*<br>  |
| T | $t_C$ | High-speed receiver and transmitter input and output clock period. |
| | **TCCS (channel-to-channel-skew)** | The timing difference between the fastest and slowest output edges, including $t_{CO}$ variation and clock skew, across channels driven by the same PLL. The clock is included in the TCCS measurement (refer to the *Timing Diagram* figure under **S** in this table). |
| | $t_{DUTY}$ | High-speed I/O block: Duty cycle on the high-speed transmitter output clock. |
| | | **Timing Unit Interval (TUI)**<br>The timing budget allowed for skew, propagation delays, and data sampling window. (TUI = 1/(Receiver Input Clock Frequency Multiplication Factor) = $t_C/w$) |
| | $t_{FALL}$ | Signal high-to-low transition time (80-20%) |
| | $t_{INCCJ}$ | Cycle-to-cycle jitter tolerance on the PLL clock input. |
| | $t_{OUTPJ\_IO}$ | Period jitter on the general purpose I/O driven by a PLL. |
| | $t_{OUTPJ\_DC}$ | Period jitter on the dedicated clock output driven by a PLL. |
| | $t_{RISE}$ | Signal low-to-high transition time (20-80%). |