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### Understanding **Embedded - FPGAs (Field Programmable Gate Array)**

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

Product Status	Obsolete
Number of LABs/CLBs	2530
Number of Logic Elements/Cells	60214
Total RAM Bits	5371904
Number of I/O	252
Number of Gates	-
Voltage - Supply	0.87V ~ 0.93V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	572-BGA, FCBGA
Supplier Device Package	572-FBGA, FC (25x25)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/intel/ep2agx65df25c6n">https://www.e-xfl.com/product-detail/intel/ep2agx65df25c6n</a>

**Table 1-3. Maximum Allowed Overshoot During Transitions for Arria II Devices**

Symbol	Description	Condition (V)	Overshoot Duration as % of High Time	Unit
V <sub>I</sub> (AC)	AC Input Voltage	4.0	100.000	%
		4.05	79.330	%
		4.1	46.270	%
		4.15	27.030	%
		4.2	15.800	%
		4.25	9.240	%
		4.3	5.410	%
		4.35	3.160	%
		4.4	1.850	%
		4.45	1.080	%
		4.5	0.630	%
		4.55	0.370	%
		4.6	0.220	%

### Maximum Allowed I/O Operating Frequency

Table 1-4 lists the maximum allowed I/O operating frequency for Arria II GX I/Os using the specified I/O standards to ensure device reliability.

**Table 1-4. Maximum Allowed I/O Operating Frequency for Arria II GX Devices**

I/O Standard	I/O Frequency (MHz)
HSTL-18 and HSTL-15	333
SSTL -15	400
SSTL-18	333
2.5-V LVCMOS	260
3.3-V and 3.0-V LVTTTL	250
3.3-V, 3.0-V, 1.8-V, and 1.5-V LVCMOS	
PCI and PCI-X	
SSTL-2	
1.2-V LVCMOS HSTL-12	200

**I/O Pin Leakage Current**

Table 1-7 lists the Arria II GX I/O pin leakage current specifications.

**Table 1-7. I/O Pin Leakage Current for Arria II GX Devices**

Symbol	Description	Conditions	Min	Typ	Max	Unit
$I_I$	Input pin	$V_I = 0\text{ V to }V_{CCIO\text{MAX}}$	-10	—	10	$\mu\text{A}$
$I_{OZ}$	Tri-stated I/O pin	$V_O = 0\text{ V to }V_{CCIO\text{MAX}}$	-10	—	10	$\mu\text{A}$

Table 1-8 lists the Arria II GZ I/O pin leakage current specifications.

**Table 1-8. I/O Pin Leakage Current for Arria II GZ Devices**

Symbol	Description	Conditions	Min	Typ	Max	Unit
$I_I$	Input pin	$V_I = 0\text{ V to }V_{CCIO\text{MAX}}$	-20	—	20	$\mu\text{A}$
$I_{OZ}$	Tri-stated I/O pin	$V_O = 0\text{ V to }V_{CCIO\text{MAX}}$	-20	—	20	$\mu\text{A}$

**Bus Hold**

Bus hold retains the last valid logic state after the source driving it either enters the high impedance state or is removed. Each I/O pin has an option to enable bus hold in user mode. Bus hold is always disabled in configuration mode.

Table 1-9 lists bus hold specifications for Arria II GX devices.

**Table 1-9. Bus Hold Parameters for Arria II GX Devices (Note 1)**

Parameter	Symbol	Cond.	$V_{CCIO}\text{ (V)}$												Unit
			1.2		1.5		1.8		2.5		3.0		3.3		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Bus-hold low, sustaining current	$I_{SUSL}$	$V_{IN} > V_{IL}$ (max.)	8	—	12	—	30	—	50	—	70	—	70	—	$\mu\text{A}$
Bus-hold high, sustaining current	$I_{SUSH}$	$V_{IN} < V_{IL}$ (min.)	-8	—	-12	—	-30	—	-50	—	-70	—	-70	—	$\mu\text{A}$
Bus-hold low, overdrive current	$I_{ODL}$	$0\text{ V} < V_{IN} < V_{CCIO}$	—	125	—	175	—	200	—	300	—	500	—	500	$\mu\text{A}$
Bus-hold high, overdrive current	$I_{ODH}$	$0\text{ V} < V_{IN} < V_{CCIO}$	—	-125	—	-175	—	-200	—	-300	—	-500	—	-500	$\mu\text{A}$
Bus-hold trip point	$V_{TRIP}$	—	0.3	0.9	0.375	1.125	0.68	1.07	0.7	1.7	0.8	2	0.8	2	V

**Note to Table 1-9:**

(1) The bus-hold trip points are based on calculated input voltages from the JEDEC standard.

Table 1-17 lists the pin capacitance for Arria II GZ devices.

**Table 1-17. Pin Capacitance for Arria II GZ Devices**

Symbol	Description	Typical	Unit
$C_{IOTB}$	Input capacitance on the top and bottom I/O pins	4	pF
$C_{IOLR}$	Input capacitance on the left and right I/O pins	4	pF
$C_{CLKTB}$	Input capacitance on the top and bottom non-dedicated clock input pins	4	pF
$C_{CLKLR}$	Input capacitance on the left and right non-dedicated clock input pins	4	pF
$C_{OUTFB}$	Input capacitance on the dual-purpose clock output and feedback pins	5	pF
$C_{CLK1}$ , $C_{CLK3}$ , $C_{CLK8}$ , and $C_{CLK10}$	Input capacitance for dedicated clock input pins	2	pF

### Internal Weak Pull-Up and Weak Pull-Down Resistors

Table 1-18 lists the weak pull-up and pull-down resistor values for Arria II GX devices.

**Table 1-18. Internal Weak Pull-up and Weak Pull-Down Resistors for Arria II GX Devices (Note 1)**

Symbol	Description	Conditions	Min	Typ	Max	Unit
$R_{PU}$	Value of I/O pin pull-up resistor before and during configuration, as well as user mode if the programmable pull-up resistor option is enabled.	$V_{CCIO} = 3.3\text{ V} \pm 5\%$ (2)	7	25	41	k $\Omega$
		$V_{CCIO} = 3.0\text{ V} \pm 5\%$ (2)	7	28	47	k $\Omega$
		$V_{CCIO} = 2.5\text{ V} \pm 5\%$ (2)	8	35	61	k $\Omega$
		$V_{CCIO} = 1.8\text{ V} \pm 5\%$ (2)	10	57	108	k $\Omega$
		$V_{CCIO} = 1.5\text{ V} \pm 5\%$ (2)	13	82	163	k $\Omega$
$R_{PD}$	Value of TCK pin pull-down resistor	$V_{CCIO} = 3.3\text{ V} \pm 5\%$	6	19	29	k $\Omega$
		$V_{CCIO} = 3.0\text{ V} \pm 5\%$	6	22	32	k $\Omega$
		$V_{CCIO} = 2.5\text{ V} \pm 5\%$	6	25	42	k $\Omega$
		$V_{CCIO} = 1.8\text{ V} \pm 5\%$	7	35	70	k $\Omega$
		$V_{CCIO} = 1.5\text{ V} \pm 5\%$	8	50	112	k $\Omega$

**Notes to Table 1-18:**

- (1) All I/O pins have an option to enable weak pull-up except configuration, test, and JTAG pins. The weak pull-down feature is only available for JTAG TCK.
- (2) Pin pull-up resistance values may be lower if an external source drives the pin higher than  $V_{CCIO}$ .

Table 1-26 lists the single-ended SSTL and HSTL I/O standard signal specifications for Arria II GX devices.

**Table 1-26. Single-Ended SSTL and HSTL I/O Standard Signal Specifications for Arria II GX Devices**

I/O Standard	$V_{IL(DC)} (V)$		$V_{IH(DC)} (V)$		$V_{IL(AC)} (V)$	$V_{IH(AC)} (V)$	$V_{OL} (V)$	$V_{OH} (V)$	$I_{OL} (mA)$	$I_{OH} (mA)$
	Min	Max	Min	Max	Max	Min	Max	Min		
SSTL-2 Class I	-0.3	$V_{REF} - 0.18$	$V_{REF} + 0.18$	$V_{CCIO} + 0.3$	$V_{REF} - 0.35$	$V_{REF} + 0.35$	$V_{TT} - 0.57$	$V_{TT} + 0.57$	8.1	-8.1
SSTL-2 Class II	-0.3	$V_{REF} - 0.18$	$V_{REF} + 0.18$	$V_{CCIO} + 0.3$	$V_{REF} - 0.35$	$V_{REF} + 0.35$	$V_{TT} - 0.76$	$V_{TT} + 0.76$	16.4	-16.4
SSTL-18 Class I	-0.3	$V_{REF} - 0.125$	$V_{REF} + 0.125$	$V_{CCIO} + 0.3$	$V_{REF} - 0.25$	$V_{REF} + 0.25$	$V_{TT} - 0.475$	$V_{TT} + 0.475$	6.7	-6.7
SSTL-18 Class II	-0.3	$V_{REF} - 0.125$	$V_{REF} + 0.125$	$V_{CCIO} + 0.3$	$V_{REF} - 0.25$	$V_{REF} + 0.25$	0.28	$V_{CCIO} - 0.28$	13.4	-13.4
SSTL-15 Class I	-0.3	$V_{REF} - 0.1$	$V_{REF} + 0.1$	$V_{CCIO} + 0.3$	$V_{REF} - 0.175$	$V_{REF} + 0.175$	$0.2 \times V_{CCIO}$	$0.8 \times V_{CCIO}$	8	-8
SSTL-15 Class II	-0.3	$V_{REF} - 0.1$	$V_{REF} + 0.1$	$V_{CCIO} + 0.3$	$V_{REF} - 0.175$	$V_{REF} + 0.175$	$0.2 \times V_{CCIO}$	$0.8 \times V_{CCIO}$	16	-16
HSTL-18 Class I	-0.3	$V_{REF} - 0.1$	$V_{REF} + 0.1$	$V_{CCIO} + 0.3$	$V_{REF} - 0.2$	$V_{REF} + 0.2$	0.4	$V_{CCIO} - 0.4$	8	-8
HSTL-18 Class II	-0.3	$V_{REF} - 0.1$	$V_{REF} + 0.1$	$V_{CCIO} + 0.3$	$V_{REF} - 0.2$	$V_{REF} + 0.2$	0.4	$V_{CCIO} - 0.4$	16	-16
HSTL-15 Class I	-0.3	$V_{REF} - 0.1$	$V_{REF} + 0.1$	$V_{CCIO} + 0.3$	$V_{REF} - 0.2$	$V_{REF} + 0.2$	0.4	$V_{CCIO} - 0.4$	8	-8
HSTL-15 Class II	-0.3	$V_{REF} - 0.1$	$V_{REF} + 0.1$	$V_{CCIO} + 0.3$	$V_{REF} - 0.2$	$V_{REF} + 0.2$	0.4	$V_{CCIO} - 0.4$	16	-16
HSTL-12 Class I	-0.15	$V_{REF} - 0.08$	$V_{REF} + 0.08$	$V_{CCIO} + 0.15$	$V_{REF} - 0.15$	$V_{REF} + 0.15$	$0.25 \times V_{CCIO}$	$0.75 \times V_{CCIO}$	8	-8
HSTL-12 Class II	-0.15	$V_{REF} - 0.08$	$V_{REF} + 0.08$	$V_{CCIO} + 0.15$	$V_{REF} - 0.15$	$V_{REF} + 0.15$	$0.25 \times V_{CCIO}$	$0.75 \times V_{CCIO}$	14	-14

Table 1-27 lists the single-ended SSTL and HSTL I/O standard signal specifications for Arria II GZ devices.

**Table 1-27. Single-Ended SSTL and HSTL I/O Standards Signal Specifications for Arria II GZ Devices (Part 1 of 2)**

I/O Standard	$V_{IL(DC)} (V)$		$V_{IH(DC)} (V)$		$V_{IL(AC)} (V)$	$V_{IH(AC)} (V)$	$V_{OL} (V)$	$V_{OH} (V)$	$I_{OL} (mA)$	$I_{OH} (mA)$
	Min	Max	Min	Max	Max	Min	Max	Min		
SSTL-2 Class I	-0.3	$V_{REF} - 0.15$	$V_{REF} + 0.15$	$V_{CCIO} + 0.3$	$V_{REF} - 0.31$	$V_{REF} + 0.31$	$V_{TT} - 0.57$	$V_{TT} + 0.57$	8.1	-8.1
SSTL-2 Class II	-0.3	$V_{REF} - 0.15$	$V_{REF} + 0.15$	$V_{CCIO} + 0.3$	$V_{REF} - 0.31$	$V_{REF} + 0.31$	$V_{TT} - 0.76$	$V_{TT} + 0.76$	16.2	-16.2
SSTL-18 Class I	-0.3	$V_{REF} - 0.125$	$V_{REF} + 0.125$	$V_{CCIO} + 0.3$	$V_{REF} - 0.25$	$V_{REF} + 0.25$	$V_{TT} - 0.475$	$V_{TT} + 0.475$	6.7	-6.7
SSTL-18 Class II	-0.3	$V_{REF} - 0.125$	$V_{REF} + 0.125$	$V_{CCIO} + 0.3$	$V_{REF} - 0.25$	$V_{REF} + 0.25$	0.28	$V_{CCIO} - 0.28$	13.4	-13.4
SSTL-15 Class I	—	$V_{REF} - 0.1$	$V_{REF} + 0.1$	—	$V_{REF} - 0.175$	$V_{REF} + 0.175$	$0.2 \times V_{CCIO}$	$0.8 \times V_{CCIO}$	8	-8

Table 1-30 lists the HSTL I/O standards for Arria II GX devices.

**Table 1-30. Differential HSTL I/O Standards for Arria II GX Devices**

I/O Standard	V <sub>CCIO</sub> (V)			V <sub>DIF(DC)</sub> (V)		V <sub>X(AC)</sub> (V)			V <sub>CM(DC)</sub> (V)			V <sub>DIF(AC)</sub> (V)	
	Min	Typ	Max	Min	Max	Min	Typ	Max	Min	Typ	Max	Min	Max
HSTL-18 Class I	1.71	1.8	1.89	0.2	—	0.85	—	0.95	0.88	—	0.95	0.4	—
HSTL-15 Class I, II	1.425	1.5	1.575	0.2	—	0.71	—	0.79	0.71	—	0.79	0.4	—
HSTL-12 Class I, II	1.14	1.2	1.26	0.16	—	—	0.5 × V <sub>CCIO</sub>	—	0.48 × V <sub>CCIO</sub>	0.5 × V <sub>CCIO</sub>	0.52 × V <sub>CCIO</sub>	0.3	—

Table 1-31 lists the HSTL I/O standards for Arria II GZ devices.

**Table 1-31. Differential HSTL I/O Standards for Arria II GZ Devices**

I/O Standard	V <sub>CCIO</sub> (V)			V <sub>DIF(DC)</sub> (V)		V <sub>X(AC)</sub> (V)			V <sub>CM(DC)</sub> (V)			V <sub>DIF(AC)</sub> (V)	
	Min	Typ	Max	Min	Max	Min	Typ	Max	Min	Typ	Max	Min	Max
HSTL-18 Class I	1.71	1.8	1.89	0.2	—	0.78	—	1.12	0.78	—	1.12	0.4	—
HSTL-15 Class I, II	1.425	1.5	1.575	0.2	—	0.68	—	0.9	0.68	—	0.9	0.4	—
HSTL-12 Class I, II	1.14	1.2	1.26	0.16	V <sub>CCIO</sub> + 0.3	—	0.5 × V <sub>CCIO</sub>	—	0.4 × V <sub>CCIO</sub>	0.5 × V <sub>CCIO</sub>	0.6 × V <sub>CCIO</sub>	0.3	V <sub>CCIO</sub> + 0.48

Table 1-32 lists the differential I/O standard specifications for Arria II GX devices.

**Table 1-32. Differential I/O Standard Specifications for Arria II GX Devices (Note 1)**

I/O Standard	V <sub>CCIO</sub> (V)			V <sub>ID</sub> (mV)			V <sub>ICM</sub> (V) (2)		V <sub>OD</sub> (V) (3)			V <sub>OCM</sub> (V)		
	Min	Typ	Max	Min	Cond.	Max	Min	Max	Min	Typ	Max	Min	Typ	Max
2.5 V LVDS	2.375	2.5	2.625	100	V <sub>CM</sub> = 1.25 V	—	0.05	1.80	0.247	—	0.6	1.125	1.25	1.375
RSDS (4)	2.375	2.5	2.625	—	—	—	—	—	0.1	0.2	0.6	0.5	1.2	1.4
Mini-LVDS (4)	2.375	2.5	2.625	—	—	—	—	—	0.25	—	0.6	1	1.2	1.4
LVPECL (5)	2.375	2.5	2.625	300	—	—	0.6	1.8	—	—	—	—	—	—
BLVDS (6)	2.375	2.5	2.625	100	—	—	—	—	—	—	—	—	—	—

**Notes to Table 1-32:**

- (1) The 1.5 V PCML transceiver I/O standard specifications are described in “Transceiver Performance Specifications” on page 1-21.
- (2) V<sub>IN</sub> range: 0 ≤ V<sub>IN</sub> ≤ 1.85 V.
- (3) R<sub>L</sub> range: 90 ≤ R<sub>L</sub> ≤ 110 Ω.
- (4) The RSDS and mini-LVDS I/O standards are only supported for differential outputs.
- (5) The LVPECL input standard is supported at the dedicated clock input pins (GCLK) only.
- (6) There are no fixed V<sub>ICM</sub>, V<sub>OD</sub>, and V<sub>OCM</sub> specifications for BLVDS. These specifications depend on the system topology.

Table 1-33 lists the differential I/O standard specifications for Arria II GZ devices.

**Table 1-33. Differential I/O Standard Specifications for Arria II GZ Devices (Note 1)**

I/O Standard (2)	V <sub>CCIO</sub> (V)			V <sub>ID</sub> (mV)			V <sub>ICM(DC)</sub> (V)		V <sub>OD</sub> (V) (3)			V <sub>OCM</sub> (V) (3)		
	Min	Typ	Max	Min	Cond.	Max	Min	Max	Min	Typ	Max	Min	Typ	Max
2.5 V LVDS (HIO)	2.375	2.5	2.625	100	V <sub>CM</sub> = 1.25 V	—	0.05	1.8	0.247	—	0.6	1.125	1.25	1.375
2.5 V LVDS (VIO)	2.375	2.5	2.625	100	V <sub>CM</sub> = 1.25 V	—	0.05	1.8	0.247	—	0.6	1	1.25	1.5
RSDS (HIO)	2.375	2.5	2.625	100	V <sub>CM</sub> = 1.25 V	—	0.3	1.4	0.1	0.2	0.6	0.5	1.2	1.4
RSDS (VIO)	2.375	2.5	2.625	100	V <sub>CM</sub> = 1.25 V	—	0.3	1.4	0.1	0.2	0.6	0.5	1.2	1.5
Mini-LVDS (HIO)	2.375	2.5	2.625	200	—	600	0.4	1.325	0.25	—	0.6	1	1.2	1.4
Mini-LVDS (VIO)	2.375	2.5	2.625	200	—	600	0.4	1.325	0.25	—	0.6	1	1.2	1.5
LVPECL	2.375	2.5	2.625	300	—	—	0.6	1.8	—	—	—	—	—	—
BLVDS (4)	2.375	2.5	2.625	100	—	—	—	—	—	—	—	—	—	—

**Notes to Table 1-33:**

- (1) 1.4-V/1.5-V PCML transceiver I/O standard specifications are described in “Transceiver Performance Specifications” on page 1-21.
- (2) Vertical I/O (VIO) is top and bottom I/Os; horizontal I/O (HIO) is left and right I/Os.
- (3) R<sub>L</sub> range: 90 ≤ R<sub>L</sub> ≤ 110 Ω.
- (4) There are no fixed V<sub>ICM</sub>, V<sub>OD</sub>, and V<sub>OCM</sub> specifications for BLVDS. These specifications depend on the system topology.

## Power Consumption for the Arria II Device Family

Altera offers two ways to estimate power for a design:

- Using the Microsoft Excel-based Early Power Estimator
- Using the Quartus® II PowerPlay Power Analyzer feature

The interactive Microsoft Excel-based Early Power Estimator is typically used prior to designing the FPGA in order to get a magnitude estimate of the device power. The Quartus II PowerPlay Power Analyzer provides better quality estimates based on the specifics of the design after place-and-route is complete. The PowerPlay Power Analyzer can apply a combination of user-entered, simulation-derived, and estimated signal activities which, when combined with detailed circuit models, can yield very accurate power estimates.



For more information about power estimation tools, refer to the *PowerPlay Early Power Estimator User Guide* and the *PowerPlay Power Analysis* chapter in volume 3 of the *Quartus II Handbook*.

**Table 1–34. Transceiver Specifications for Arria II GX Devices (Note 1) (Part 2 of 7)**

Symbol/ Description	Condition	I3			C4			C5 and I5			C6			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Spread-spectrum downspread	PCIe	—	0 to –0.5%	—	—	0 to –0.5%	—	—	0 to –0.5%	—	—	0 to –0.5%	—	—
On-chip termination resistors	—	—	100	—	—	100	—	—	100	—	—	100	—	Ω
V <sub>ICM</sub> (AC coupled)	—	1100 ± 5%			1100 ± 5%			1100 ± 5%			1100 ± 5%			mV
V <sub>ICM</sub> (DC coupled)	HCSL I/O standard for PCIe reference clock	250	—	550	250	—	550	250	—	550	250	—	550	mV
Transmitter REFCLK Phase Noise	10 Hz	—	—	-50	—	—	-50	—	—	-50	—	—	-50	dBc/Hz
	100 Hz	—	—	-80	—	—	-80	—	—	-80	—	—	-80	dBc/Hz
	1 KHz	—	—	-110	—	—	-110	—	—	-110	—	—	-110	dBc/Hz
	10 KHz	—	—	-120	—	—	-120	—	—	-120	—	—	-120	dBc/Hz
	100 KHz	—	—	-120	—	—	-120	—	—	-120	—	—	-120	dBc/Hz
	≥ 1 MHz	—	—	-130	—	—	-130	—	—	-130	—	—	-130	dBc/Hz
Transmitter REFCLK Phase Jitter (rms) for 100 MHz REFCLK (3)	10 KHz to 20 MHz	—	—	3	—	—	3	—	—	3	—	—	3	ps
R <sub>ref</sub>	—	—	2000 ± 1%	—	—	2000 ± 1%	—	—	2000 ± 1%	—	—	2000 ± 1%	—	Ω
<b>Transceiver Clocks</b>														
Calibration block clock frequency (cal_blk_clk)	—	10	—	125	10	—	125	10	—	125	10	—	125	MHz



**Table 1–34. Transceiver Specifications for Arria II GX Devices (Note 1) (Part 6 of 7)**

Symbol/ Description	Condition	I3			C4			C5 and I5			C6			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Intra-differential pair skew	—	—	—	15	—	—	15	—	—	15	—	—	15	ps
Intra-transceiver block skew	PCIe x4	—	—	120	—	—	120	—	—	120	—	—	120	ps
Inter-transceiver block skew	PCIe x8	—	—	300	—	—	300	—	—	300	—	—	300	ps
<b>CMU PLL0 and CMU PLL1</b>														
CMU PLL lock time from CMUPLL_reset deassertion	—	—	—	100	—	—	100	—	—	100	—	—	100	μs
<b>PLD-Transceiver Interface</b>														
Interface speed	—	25	—	320	25	—	240	25	—	240	25	—	200	MHz

**Table 1-35. Transceiver Specifications for Arria II GZ Devices (Part 5 of 5)**

Symbol/ Description	Conditions	-C3 and -I3 (1)			-C4 and -I4			Unit
		Min	Typ	Max	Min	Typ	Max	
-3 dB Bandwidth	PCIe Gen1	2.5 - 3.5						MHz
	PCIe Gen2	6 - 8						MHz
	(OIF) CEI PHY at 4.976 Gbps	7 - 11						MHz
	(OIF) CEI PHY at 6.375 Gbps	5 - 10						MHz
	XAUI	2 - 4						MHz
	SRIO 1.25 Gbps	3 - 5.5						MHz
	SRIO 2.5 Gbps	3 - 5.5						MHz
	SRIO 3.125 Gbps	2 - 4						MHz
	GIGE	2.5 - 4.5						MHz
	SONET OC12	1.5 - 2.5						MHz
SONET OC48	3.5 - 6						MHz	
<b>Transceiver-FPGA Fabric Interface</b>								
Interface speed	—	25	—	325	25	—	250	MHz
Digital reset pulse width	—	Minimum is two parallel clock cycles						—

**Notes to Table 1-35:**

- (1) The 3x speed grade is the fastest speed grade offered in the following Arria II GZ devices: EP2AGZ225, EP2AGZ300, and EP2AGZ350.
- (2) The rise and fall time transition is specified from 20% to 80%.
- (3) To calculate the REFCLK rms phase jitter requirement at reference clock frequencies other than 100 MHz, use the following formula:  
REFCLK rms phase jitter at f (MHz) = REFCLK rms phase jitter at 100 MHz \* 100/f.
- (4) The minimum `reconfig_clk` frequency is 2.5 MHz if the transceiver channel is configured in **Transmitter only** mode. The minimum `reconfig_clk` frequency is 37.5 MHz if the transceiver channel is configured in **Receiver only** or **Receiver and Transmitter** mode.
- (5) If your design uses more than one dynamic reconfiguration controller (`altgx_reconfig`) instances to control the transceiver (`altgx`) channels physically located on the same side of the device AND if you use different `reconfig_clk` sources for these `altgx_reconfig` instances, the delta time between any two of these `reconfig_clk` sources becoming stable must not exceed the maximum specification listed.
- (6) The device cannot tolerate prolonged operation at this absolute maximum.
- (7) You must use the 1.1-V RX  $V_{ICM}$  setting if the input serial data standard is LVDS.
- (8) The differential eye opening specification at the receiver input pins assumes that Receiver Equalization is disabled. If you enable Receiver Equalization, the receiver circuitry can tolerate a lower minimum eye opening, depending on the equalization level. Use H-Spice simulation to derive the minimum eye opening requirement with Receiver Equalization enabled.
- (9) The rate matcher supports only up to  $\pm 300$  ppm.
- (10) Time taken to `rx_pll_locked` goes high from `rx_analogreset` de-assertion. Refer to [Figure 1-1 on page 1-33](#).
- (11) Time for which the CDR must be kept in lock-to-reference mode after `rx_pll_locked` goes high and before `rx_locktodata` is asserted in manual mode. Refer to [Figure 1-1 on page 1-33](#).
- (12) Time taken to recover valid data after the `rx_locktodata` signal is asserted in manual mode. Refer to [Figure 1-1 on page 1-33](#).
- (13) Time taken to recover valid data after the `rx_freqlocked` signal goes high in automatic mode. Refer to [Figure 1-2 on page 1-33](#).
- (14) A GPLL may be required to meet the PMA-FPGA fabric interface timing above certain data rates. For more information, refer to the [Transceiver Clocking for Arria II Devices](#) chapter.
- (15) The Quartus II software automatically selects the appropriate slew rate depending on the configured data rate or functional mode.
- (16) To support data rates lower than the minimum specification through oversampling, use the CDR in LTR mode only.

Table 1-39 lists typical transmitter pre-emphasis levels for Arria II GZ devices (in dB) for the first post tap under the following conditions (low-frequency data pattern [five 1s and five 0s] at 6.25 Gbps). The levels listed in Table 1-39 are a representation of possible pre-emphasis levels under the specified conditions only and that the pre-emphasis levels may change with data pattern and data rate.

 To predict the pre-emphasis level for your specific data rate and pattern, run simulations using the [Arria II HSSI HSPICE](#) models.

**Table 1-39. Transmitter Pre-Emphasis Levels for Arria II GZ Devices (Part 1 of 2)**

Pre-Emphasis 1st Post-Tap Setting	V <sub>DD</sub> Setting							
	0	1	2	3	4	5	6	7
0	0	0	0	0	0	0	0	0
1	N/A	0.7	0	0	0	0	0	0
2	N/A	1	0.3	0	0	0	0	0
3	N/A	1.5	0.6	0	0	0	0	0
4	N/A	2	0.7	0.3	0	0	0	0
5	N/A	2.7	1.2	0.5	0.3	0	0	0
6	N/A	3.1	1.3	0.8	0.5	0.2	0	0
7	N/A	3.7	1.8	1.1	0.7	0.4	0.2	0
8	N/A	4.2	2.1	1.3	0.9	0.6	0.3	0
9	N/A	4.9	2.4	1.6	1.2	0.8	0.5	0.2
10	N/A	5.4	2.8	1.9	1.4	1	0.7	0.3
11	N/A	6	3.2	2.2	1.7	1.2	0.9	0.4
12	N/A	6.8	3.5	2.6	1.9	1.4	1.1	0.6
13	N/A	7.5	3.8	2.8	2.1	1.6	1.2	0.6
14	N/A	8.1	4.2	3.1	2.3	1.7	1.3	0.7
15	N/A	8.8	4.5	3.4	2.6	1.9	1.5	0.8
16	N/A	N/A	4.9	3.7	2.9	2.2	1.7	0.9
17	N/A	N/A	5.3	4	3.1	2.4	1.8	1.1
18	N/A	N/A	5.7	4.4	3.4	2.6	2	1.2
19	N/A	N/A	6.1	4.7	3.6	2.8	2.2	1.4
20	N/A	N/A	6.6	5.1	4	3.1	2.4	1.5
21	N/A	N/A	7	5.4	4.3	3.3	2.7	1.7
22	N/A	N/A	8	6.1	4.8	3.8	3	2
23	N/A	N/A	9	6.8	5.4	4.3	3.4	2.3
24	N/A	N/A	10	7.6	6	4.8	3.9	2.6
25	N/A	N/A	11.4	8.4	6.8	5.4	4.4	3
26	N/A	N/A	12.6	9.4	7.4	5.9	4.9	3.3
27	N/A	N/A	N/A	10.3	8.1	6.4	5.3	3.6
28	N/A	N/A	N/A	11.3	8.8	7.1	5.8	4

**Table 1–39. Transmitter Pre-Emphasis Levels for Arria II GZ Devices (Part 2 of 2)**

Pre-Emphasis 1st Post-Tap Setting	V <sub>00</sub> Setting							
	0	1	2	3	4	5	6	7
29	N/A	N/A	N/A	12.5	9.6	7.7	6.3	4.3
30	N/A	N/A	N/A	N/A	11.4	9	7.4	N/A
31	N/A	N/A	N/A	N/A	12.9	10	8.2	N/A

Table 1–40 lists the transceiver jitter specifications for all supported protocols for Arria II GX devices.

**Table 1–40. Transceiver Block Jitter Specifications for Arria II GX Devices (Note 1) (Part 1 of 10)**

Symbol/ Description	Conditions	I3			C4			C5, I5			C6			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
<b>SONET/SDH Transmit Jitter Generation (2)</b>														
Peak-to-peak jitter at 622.08 Mbps	Pattern = PRBS15	—	—	0.1	—	—	0.1	—	—	0.1	—	—	0.1	UI
RMS jitter at 622.08 Mbps	Pattern = PRBS15	—	—	0.01	—	—	0.01	—	—	0.01	—	—	0.01	UI
Peak-to-peak jitter at 2488.32 Mbps	Pattern = PRBS15	—	—	0.1	—	—	0.1	—	—	0.1	—	—	0.1	UI
RMS jitter at 2488.32 Mbps	Pattern = PRBS15	—	—	0.01	—	—	0.01	—	—	0.01	—	—	0.01	UI
<b>SONET/SDH Receiver Jitter Tolerance (2)</b>														
Jitter tolerance at 622.08 Mbps	Jitter frequency = 0.03 KHz Pattern = PRBS15	> 15			> 15			> 15			> 15			UI
	Jitter frequency = 25 KHZ Pattern = PRBS15	> 1.5			> 1.5			> 1.5			> 1.5			UI
	Jitter frequency = 250 KHz Pattern = PRBS15	> 0.15			> 0.15			> 0.15			> 0.15			UI

**Table 1-40. Transceiver Block Jitter Specifications for Arria II GX Devices (Note 1) (Part 4 of 10)**

Symbol/ Description	Conditions	I3			C4			C5, I5			C6			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Total jitter (peak-to-peak)	Pattern = CRPAT	—	—	0.27 9	—	—	0.279	—	—	0.279	—	—	0.279	UI
<b>GIGE Receiver Jitter Tolerance (6)</b>														
Deterministic jitter tolerance (peak-to-peak)	Pattern = CJPAT	> 0.4			> 0.4			> 0.4			> 0.4			UI
Combined deterministic and random jitter tolerance (peak-to-peak)	Pattern = CJPAT	> 0.66			> 0.66			> 0.66			> 0.66			UI
<b>HiGig Transmit Jitter Generation (7)</b>														
Deterministic jitter (peak-to-peak)	Data rate = 3.75 Gbps Pattern = CJPAT	—	—	0.17	—	—	0.17	—	—	—	—	—	—	UI
Total jitter (peak-to-peak)	Data rate = 3.75 Gbps Pattern = CJPAT	—	—	0.35	—	—	0.35	—	—	—	—	—	—	UI
<b>HiGig Receiver Jitter Tolerance (7)</b>														
Deterministic jitter tolerance (peak-to-peak)	Data rate = 3.75 Gbps Pattern = CJPAT	> 0.37			> 0.37			—	—	—	—	—	—	UI
Combined deterministic and random jitter tolerance (peak-to-peak)	Data rate = 3.75 Gbps Pattern = CJPAT	> 0.65			> 0.65			—	—	—	—	—	—	UI
Sinusoidal jitter tolerance (peak-to-peak)	Jitter frequency = 22.1 KHz Data rate = 3.75 Gbps Pattern = CJPAT	> 8.5			> 8.5			—	—	—	—	—	—	UI
	Jitter frequency = 1.875MHz Data rate = 3.75 Gbps Pattern = CJPAT	> 0.1			> 0.1			—	—	—	—	—	—	UI
	Jitter frequency = 20 MHz Data rate = 3.75 Gbps Pattern = CJPAT	> 0.1			> 0.1			—	—	—	—	—	—	UI

**Table 1-41. Transceiver Block Jitter Specifications for Arria II GZ Devices (Note 1), (2) (Part 4 of 7)**

Symbol/ Description	Conditions	-C3 and -I3			-C4 and -I4			Unit
		Min	Typ	Max	Min	Typ	Max	
<b>GIGE Receiver Jitter Tolerance (11)</b>								
Deterministic jitter tolerance (peak-to-peak)	Pattern = CJPAT	> 0.4			> 0.4			UI
Combined deterministic and random jitter tolerance (peak-to-peak)	Pattern = CJPAT	> 0.66			> 0.66			UI
<b>HiGig Transmit Jitter Generation</b>								
Deterministic jitter (peak-to-peak)	Data rate = 3.75 Gbps Pattern = CJPAT	—	—	0.17	—	—	—	UI
Total jitter (peak-to-peak)	Data rate = 3.75 Gbps Pattern = CJPAT	—	—	0.35	—	—	—	UI
<b>HiGig Receiver Jitter Tolerance</b>								
Deterministic jitter tolerance (peak-to-peak)	Data rate = 3.75 Gbps Pattern = CJPAT	> 0.37			—	—	—	UI
Combined deterministic and random jitter tolerance (peak-to-peak)	Data rate = 3.75 Gbps Pattern = CJPAT	> 0.65			—	—	—	UI
Sinusoidal jitter tolerance (peak-to-peak)	Jitter frequency = 22.1 KHz Data rate = 3.75 Gbps Pattern = CJPAT	> 8.5			—	—	—	UI
	Jitter frequency = 22.1 KHz Data rate = 3.75 Gbps Pattern = CJPAT	> 0.1			—	—	—	UI
	Jitter frequency = 22.1 KHz Data rate = 3.75 Gbps Pattern = CJPAT	> 0.1			—	—	—	UI
<b>(OIF) CEI Transmitter Jitter Generation</b>								
Total jitter (peak-to-peak)	Data rate = 6.375 Gbps Pattern = PRBS15 BER = $10^{-12}$	—	—	0.3	—	—	0.3	UI
<b>(OIF) CEI Receiver Jitter Tolerance</b>								
Deterministic jitter tolerance (peak-to-peak)	Data rate = 6.375 Gbps Pattern = PRBS31 BER = $10^{-12}$	> 0.675			—	—	—	UI
Combined deterministic and random jitter tolerance (peak-to-peak)	Data rate = 6.375 Gbps Pattern = PRBS31 BER = $10^{-12}$	> 0.988			—	—	—	UI

## DSP Block Specifications

Table 1-46 lists the DSP block performance specifications for Arria II GX devices.

**Table 1-46. DSP Block Performance Specifications for Arria II GX Devices (Note 1)**

Mode	Resources Used	Performance				Unit
	Number of Multipliers	C4	I3	C5,I5	C6	
9 × 9-bit multiplier	1	380	310	300	250	MHz
12 × 12-bit multiplier	1	380	310	300	250	MHz
18 × 18-bit multiplier	1	380	310	300	250	MHz
36 × 36-bit multiplier	1	350	270	270	220	MHz
18 × 36-bit high-precision multiplier adder mode	1	350	270	270	220	MHz
18 × 18-bit multiply accumulator	4	380	310	300	250	MHz
18 × 18-bit multiply adder	4	380	310	300	250	MHz
18 × 18-bit multiply adder-signed full precision	2	380	310	300	250	MHz
18 × 18-bit multiply adder with loopback (2)	2	275	220	220	180	MHz
36-bit shift (32-bit data)	1	350	270	270	220	MHz
Double mode	1	350	270	270	220	MHz

**Notes to Table 1-46:**

- (1) Maximum is for a fully-pipelined block with **Round** and **Saturation** disabled.
- (2) Maximum is for loopback input registers disabled, **Round** and **Saturation** disabled, pipeline and output registers enabled.

Table 1-47 lists the DSP block performance specifications for Arria II GZ devices.

**Table 1-47. DSP Block Performance Specifications for Arria II GZ Devices (Note 1) (Part 1 of 2)**

Mode	Resources Used	Performance		Unit
	Number of Multipliers	-3	-4	
9 × 9-bit multiplier	1	460	400	MHz
12 × 12-bit multiplier	1	500	440	MHz
18 × 18-bit multiplier	1	550	480	MHz
36 × 36-bit multiplier	1	440	380	MHz
18 × 18-bit multiply accumulator	4	440	380	MHz
18 × 18-bit multiply adder	4	470	410	MHz
18 × 18-bit multiply adder-signed full precision	2	450	390	MHz
18 × 18-bit multiply adder with loopback (2)	2	350	310	MHz
36-bit shift (32-bit data)	1	440	380	MHz

**Table 1–47. DSP Block Performance Specifications for Arria II GZ Devices (Note 1) (Part 2 of 2)**

Mode	Resources Used	Performance		Unit
	Number of Multipliers	–3	–4	
Double mode	1	440	380	MHz

**Notes to Table 1–47:**

- (1) Maximum is for fully pipelined block with **Round** and **Saturation** disabled.  
(2) Maximum for loopback input registers disabled, **Round** and **Saturation** disabled, and pipeline and output registers enabled.

**Embedded Memory Block Specifications**

Table 1–48 lists the embedded memory block specifications for Arria II GX devices.

**Table 1–48. Embedded Memory Block Performance Specifications for Arria II GX Devices**

Memory	Mode	Resources Used		Performance				Unit
		ALUTs	Embedded Memory	I3	C4	C5,I5	C6	
Memory Logic Array Block (MLAB)	Single port 64 × 10	0	1	450	500	450	378	MHz
	Simple dual-port 32 × 20 single clock	0	1	270	500	450	378	MHz
	Simple dual-port 64 × 10 single clock	0	1	428	500	450	378	MHz
M9K Block	Single-port 256 × 36	0	1	360	400	360	310	MHz
	Single-port 256 × 36, with the <b>read-during-write</b> option set to <b>Old Data</b>	0	1	250	280	250	210	MHz
	Simple dual-port 256 × 36 single CLK	0	1	360	400	360	310	MHz
	Single-port 256 × 36 single CLK, with the <b>read-during-write</b> option set to <b>Old Data</b>	0	1	250	280	250	210	MHz
	True dual port 512 × 18 single CLK	0	1	360	400	360	310	MHz
	True dual-port 512 × 18 single CLK, with the <b>read-during-write</b> option set to <b>Old Data</b>	0	1	250	280	250	210	MHz
	Min Pulse Width (clock high time)	—	—	900	850	950	1130	ps
	Min Pulse Width (clock low time)	—	—	730	690	770	920	ps



Table 1-53. High-Speed I/O Specifications for Arria II GX Devices (Part 2 of 4)

Symbol	Conditions	I3		C4		C5,I5		C6		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
<b>Transmitter</b>										
$f_{\text{HSDR\_TX}}$ (true LVDS output data rate)	SERDES factor, J = 3 to 10 (using dedicated SERDES)	150	1250 (2)	150	1250 (2)	150	1050 (2)	150	840	Mbps
	SERDES factor, J = 4 to 10 (using logic elements as SERDES)	(3)	945	(3)	945	(3)	840	(3)	740	Mbps
	SERDES factor, J = 2 (using DDR registers) and J = 1 (using SDR register)	(3)	(3)	(3)	(3)	(3)	(3)	(3)	(3)	Mbps
$f_{\text{HSDR\_TX\_E3R}}$ (emulated LVDS_E_3R output data rate) (7)	SERDES factor, J = 4 to 10	(3)	945	(3)	945	(3)	840	(3)	740	Mbps

Table 1-63 lists the memory output clock jitter specifications for Arria II GZ devices.

**Table 1-63. Memory Output Clock Jitter Specification for Arria II GZ Devices (Note 1), (2), (3)**

Parameter	Clock Network	Symbol	-3		-4		Unit
			Min	Max	Min	Max	
Clock period jitter	Regional	$t_{JIT(per)}$	-55	55	-55	55	ps
Cycle-to-cycle period jitter	Regional	$t_{JIT(cc)}$	-110	110	-110	110	ps
Duty cycle jitter	Regional	$t_{JIT(duty)}$	-82.5	82.5	-82.5	82.5	ps
Clock period jitter	Global	$t_{JIT(per)}$	-82.5	82.5	-82.5	82.5	ps
Cycle-to-cycle period jitter	Global	$t_{JIT(cc)}$	-165	165	-165	165	ps
Duty cycle jitter	Global	$t_{JIT(duty)}$	-90	90	-90	90	ps

**Notes to Table 1-63:**

- (1) The memory output clock jitter measurements are for 200 consecutive clock cycles, as specified in the JEDEC DDR2/DDR3 SDRAM standard.
- (2) The clock jitter specification applies to memory output clock pins generated using differential signal-splitter and DDIO circuits clocked by a PLL output routed on a regional or global clock network as specified. Altera recommends using regional clock networks whenever possible.
- (3) The memory output clock jitter stated in Table 1-63 is applicable when an input jitter of 30 ps is applied.

### Duty Cycle Distortion (DCD) Specifications

Table 1-64 lists the worst-case DCD specifications for Arria II GX devices.

**Table 1-64. Duty Cycle Distortion on I/O Pins for Arria II GX Devices (Note 1)**

Symbol	C4		I3, C5, I5		C6		Unit
	Min	Max	Min	Max	Min	Max	
Output Duty Cycle	45	55	45	55	45	55	%

**Note to Table 1-64:**

- (1) The DCD specification applies to clock outputs from the PLL, global clock tree, IOE driving dedicated, and general purpose I/O pins.

Table 1-65 lists the worst-case DCD specifications for Arria II GZ devices.

**Table 1-65. Duty Cycle Distortion on I/O Pins for Arria II GZ Devices (Note 1)**

Symbol	C3, I3		C4, I4		Unit
	Min	Max	Min	Max	
Output Duty Cycle	45	55	45	55	%

**Note to Table 1-65:**

- (1) The DCD specification applies to clock outputs from the PLL, global clock tree, IOE driving dedicated, and general purpose I/O pins.

## IOE Programmable Delay

Table 1-66 lists the delay associated with each supported IOE programmable delay chain for Arria II GX devices.

**Table 1-66. IOE Programmable Delay for Arria II GX Devices**

Parameter	Available Settings (1)	Minimum Offset (2)	Maximum Offset								Unit
			Fast Model			Slow Model					
			I3	C4	I5	I3	C4	C5	I5	C6	
Output enable pin delay	7	0	0.413	0.442	0.413	0.814	0.713	0.796	0.801	0.873	ns
Delay from output register to output pin	7	0	0.339	0.362	0.339	0.671	0.585	0.654	0.661	0.722	ns
Input delay from pin to internal cell	52	0	1.494	1.607	1.494	2.895	2.520	2.733	2.775	2.944	ns
Input delay from pin to input register	52	0	1.493	1.607	1.493	2.896	2.503	2.732	2.774	2.944	ns
DQS bus to input register delay	4	0	0.074	0.076	0.074	0.140	0.124	0.147	0.147	0.167	ns

**Notes to Table 1-66:**

- (1) The available setting for every delay chain starts with zero and ends with the specified maximum number of settings.
- (2) The minimum offset represented in the table does not include intrinsic delay.

Table 1-67 lists the IOE programmable delay settings for Arria II GZ devices.

**Table 1-67. IOE Programmable Delay for Arria II GZ Devices**

Parameter	Available Settings (1)	Minimum Offset (2)	Maximum Offset						Unit
			Fast Model		Slow Model				
			Industrial	Commercial	C3	I3	C4	I4	
D1	15	0	0.462	0.505	0.795	0.801	0.857	0.864	ns
D2	7	0	0.234	0.232	0.372	0.371	0.407	0.405	ns
D3	7	0	1.700	1.769	2.927	2.948	3.157	3.178	ns
D4	15	0	0.508	0.554	0.882	0.889	0.952	0.959	ns
D5	15	0	0.472	0.500	0.799	0.817	0.875	0.882	ns
D6	6	0	0.186	0.195	0.319	0.321	0.345	0.347	ns

**Notes to Table 1-67:**

- (1) You can set this value in the Quartus II software by selecting **D1**, **D2**, **D3**, **D4**, **D5**, and **D6** in the **Assignment Name** column.
- (2) Minimum offset does not include the intrinsic delay.

Table 1-68. Glossary (Part 2 of 4)

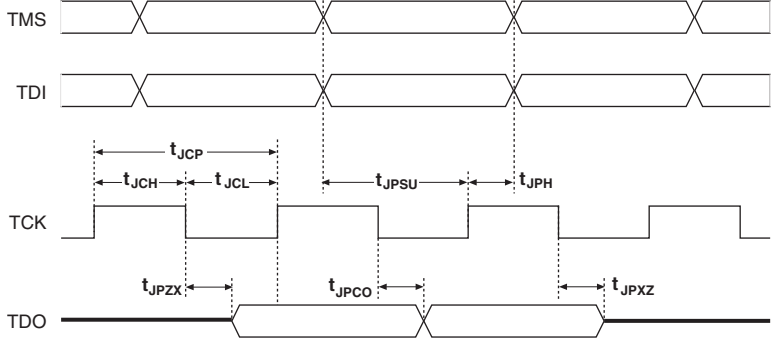
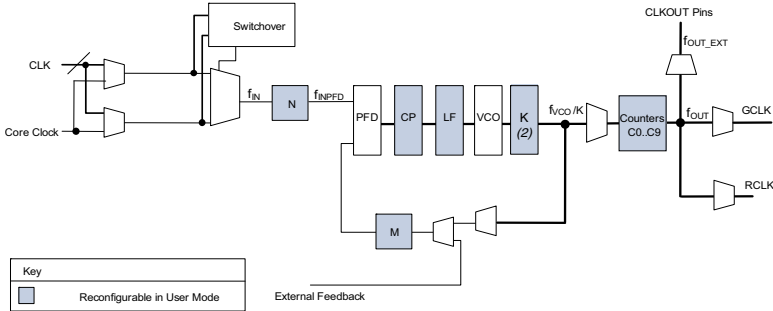
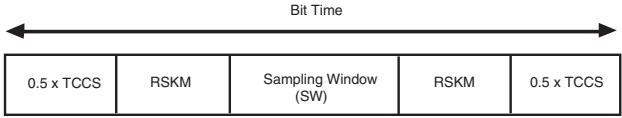
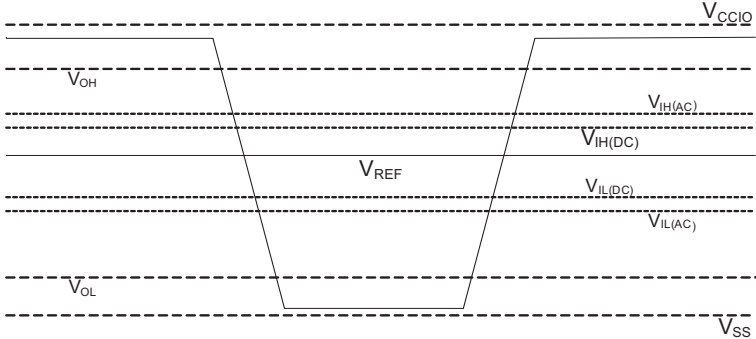
Letter	Subject	Definitions
G, H, I, J	J	<p>High-speed I/O block: Deserialization factor (width of parallel data bus).</p> <p>JTAG Timing Specifications:</p> 
	JTAG Timing Specifications	<p>PLL Specification parameters: <b>Diagram of PLL Specifications (1)</b></p>  <p><b>Notes:</b></p> <p>(1) CoreClock can only be fed by dedicated clock input pins or PLL outputs.</p> <p>(2) This is the VCO post-scale counter K.</p>
Q, R	$R_L$	Receiver differential input discrete resistor (external to the Arria II device).

Table 1-68. Glossary (Part 3 of 4)

Letter	Subject	Definitions
S	SW (sampling window)	<p>The period of time during which the data must be valid in order to capture it correctly. The setup and hold times determine the ideal strobe position within the sampling window:</p> <p><i>Timing Diagram</i></p> 
	Single-ended Voltage Referenced I/O Standard	<p>The JEDEC standard for SSTL and HSTL I/O standards define both the AC and DC input signal values. The AC values indicate the voltage levels at which the receiver must meet its timing specifications. The DC values indicate the voltage levels at which the final logic state of the receiver is unambiguously defined. After the receiver input has crossed the AC value, the receiver changes to the new logic state.</p> <p>The new logic state is then maintained as long as the input stays beyond the AC threshold. This approach is intended to provide predictable receiver timing in the presence of input waveform ringing:</p> <p><i>Single-Ended Voltage Referenced I/O Standard</i></p> 
T	$t_c$	High-speed receiver and transmitter input and output clock period.
	<b>TCCS (channel-to-channel-skew)</b>	The timing difference between the fastest and slowest output edges, including $t_{CO}$ variation and clock skew, across channels driven by the same PLL. The clock is included in the TCCS measurement (refer to the <i>Timing Diagram</i> figure under <b>S</b> in this table).
	$t_{DUTY}$	High-speed I/O block: Duty cycle on the high-speed transmitter output clock. <b>Timing Unit Interval (TUI)</b> The timing budget allowed for skew, propagation delays, and data sampling window. (TUI = $1/(\text{Receiver Input Clock Frequency Multiplication Factor}) = t_c/w$ )
	$t_{FALL}$	Signal high-to-low transition time (80-20%)
	$t_{INCCJ}$	Cycle-to-cycle jitter tolerance on the PLL clock input.
	$t_{OUTPJ\_IO}$	Period jitter on the general purpose I/O driven by a PLL.
	$t_{OUTPJ\_DC}$	Period jitter on the dedicated clock output driven by a PLL.
	$t_{RISE}$	Signal low-to-high transition time (20-80%).