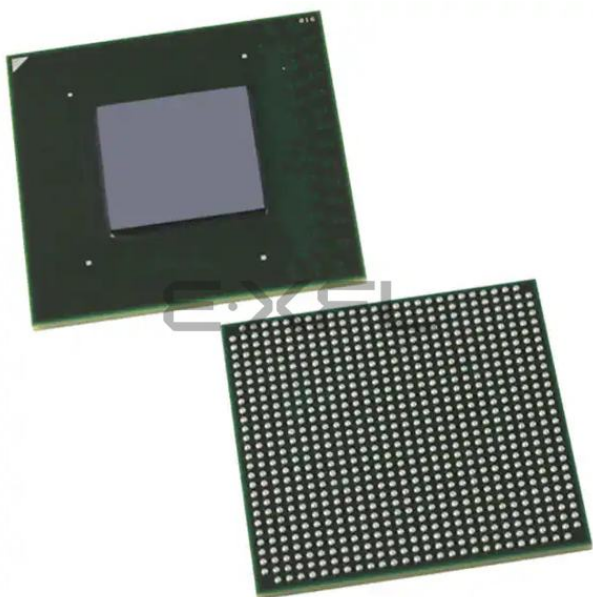




Welcome to [E-XFL.COM](https://www.e-xfl.com)

### Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

|                                |                                                                                                                                   |
|--------------------------------|-----------------------------------------------------------------------------------------------------------------------------------|
| Product Status                 | Obsolete                                                                                                                          |
| Number of LABs/CLBs            | 2530                                                                                                                              |
| Number of Logic Elements/Cells | 60214                                                                                                                             |
| Total RAM Bits                 | 5371904                                                                                                                           |
| Number of I/O                  | 364                                                                                                                               |
| Number of Gates                | -                                                                                                                                 |
| Voltage - Supply               | 0.87V ~ 0.93V                                                                                                                     |
| Mounting Type                  | Surface Mount                                                                                                                     |
| Operating Temperature          | 0°C ~ 85°C (TJ)                                                                                                                   |
| Package / Case                 | 780-BBGA, FCBGA                                                                                                                   |
| Supplier Device Package        | 780-FBGA (29x29)                                                                                                                  |
| Purchase URL                   | <a href="https://www.e-xfl.com/product-detail/intel/ep2agx65df29c4">https://www.e-xfl.com/product-detail/intel/ep2agx65df29c4</a> |

Table 1-10 lists the bus hold specifications for Arria II GZ devices.

**Table 1-10. Bus Hold Parameters for Arria II GZ Devices**

| Parameter                        | Symbol            | Cond.                                       | V <sub>CCIO</sub> (V) |      |       |      |       |      |       |      |       |      | Unit |
|----------------------------------|-------------------|---------------------------------------------|-----------------------|------|-------|------|-------|------|-------|------|-------|------|------|
|                                  |                   |                                             | 1.2                   |      | 1.5   |      | 1.8   |      | 2.5   |      | 3.0   |      |      |
|                                  |                   |                                             | Min                   | Max  | Min   | Max  | Min   | Max  | Min   | Max  | Min   | Max  |      |
| Bus-hold Low sustaining current  | I <sub>SUSL</sub> | V <sub>IN</sub> > V <sub>IL</sub><br>(max.) | 22.5                  | —    | 25.0  | —    | 30.0  | —    | 50.0  | —    | 70.0  | —    | μA   |
| Bus-hold High sustaining current | I <sub>SUSH</sub> | V <sub>IN</sub> < V <sub>IH</sub><br>(min.) | -22.5                 | —    | -25.0 | —    | -30.0 | —    | -50.0 | —    | -70.0 | —    | μA   |
| Bus-hold Low overdrive current   | I <sub>ODL</sub>  | 0V < V <sub>IN</sub> < V <sub>CCIO</sub>    | —                     | 120  | —     | 160  | —     | 200  | —     | 300  | —     | 500  | μA   |
| Bus-hold High overdrive current  | I <sub>ODH</sub>  | 0V < V <sub>IN</sub> < V <sub>CCIO</sub>    | —                     | -120 | —     | -160 | —     | -200 | —     | -300 | —     | -500 | μA   |
| Bus-hold trip point              | V <sub>TRIP</sub> | —                                           | 0.45                  | 0.95 | 0.50  | 1.00 | 0.68  | 1.07 | 0.70  | 1.70 | 0.80  | 2.00 | V    |

### OCT Specifications

Table 1-11 lists the Arria II GX device and differential OCT with and without calibration accuracy.

**Table 1-11. OCT With and Without Calibration Specification for Arria II GX Device I/Os (Note 1) (Part 1 of 2)**

| Symbol                                        | Description                                 | Conditions (V)                       | Calibration Accuracy |            | Unit |
|-----------------------------------------------|---------------------------------------------|--------------------------------------|----------------------|------------|------|
|                                               |                                             |                                      | Commercial           | Industrial |      |
| 25- $\Omega$ $R_S$<br>3.0, 2.5                | 25- $\Omega$ series OCT without calibration | $V_{CCIO} = 3.0, 2.5$                | $\pm 30$             | $\pm 40$   | %    |
| 50- $\Omega$ $R_S$<br>3.0, 2.5                | 50- $\Omega$ series OCT without calibration | $V_{CCIO} = 3.0, 2.5$                | $\pm 30$             | $\pm 40$   | %    |
| 25- $\Omega$ $R_S$<br>1.8                     | 25- $\Omega$ series OCT without calibration | $V_{CCIO} = 1.8$                     | $\pm 40$             | $\pm 50$   | %    |
| 50- $\Omega$ $R_S$<br>1.8                     | 50- $\Omega$ series OCT without calibration | $V_{CCIO} = 1.8$                     | $\pm 40$             | $\pm 50$   | %    |
| 25- $\Omega$ $R_S$<br>1.5, 1.2                | 25- $\Omega$ series OCT without calibration | $V_{CCIO} = 1.5, 1.2$                | $\pm 50$             | $\pm 50$   | %    |
| 50- $\Omega$ $R_S$<br>1.5, 1.2                | 50- $\Omega$ series OCT without calibration | $V_{CCIO} = 1.5, 1.2$                | $\pm 50$             | $\pm 50$   | %    |
| 25- $\Omega$ $R_S$<br>3.0, 2.5, 1.8, 1.5, 1.2 | 25- $\Omega$ series OCT with calibration    | $V_{CCIO} = 3.0, 2.5, 1.8, 1.5, 1.2$ | $\pm 10$             | $\pm 10$   | %    |

**Table 1-11. OCT With and Without Calibration Specification for Arria II GX Device I/Os (Note 1) (Part 2 of 2)**

| Symbol                                           | Description                                              | Conditions (V)                          | Calibration Accuracy |            | Unit |
|--------------------------------------------------|----------------------------------------------------------|-----------------------------------------|----------------------|------------|------|
|                                                  |                                                          |                                         | Commercial           | Industrial |      |
| 50- $\Omega$ $R_S$<br>3.0, 2.5, 1.8, 1.5,<br>1.2 | 50- $\Omega$ series OCT<br>with calibration              | $V_{CCIO} = 3.0, 2.5,$<br>1.8, 1.5, 1.2 | $\pm 10$             | $\pm 10$   | %    |
| 100- $\Omega$ $R_D$<br>2.5                       | 100- $\Omega$ differential<br>OCT without<br>calibration | $V_{CCIO} = 2.5$                        | $\pm 30$             | $\pm 30$   | %    |

**Note to Table 1-11:**

(1) OCT with calibration accuracy is valid at the time of calibration only.

Table 1-12 lists the OCT termination calibration accuracy specifications for Arria II GZ devices.

**Table 1-12. OCT with Calibration Accuracy Specifications for Arria II GZ Devices (Note 1)**

| Symbol                                                                                    | Description                                                                                                            | Conditions (V)                          | Calibration Accuracy |          |          | Unit |
|-------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------|-----------------------------------------|----------------------|----------|----------|------|
|                                                                                           |                                                                                                                        |                                         | C2                   | C3,I3    | C4,I4    |      |
| 25- $\Omega$ $R_S$<br>3.0, 2.5, 1.8, 1.5,<br>1.2 (2)                                      | 25- $\Omega$ series OCT<br>with calibration                                                                            | $V_{CCIO} = 3.0, 2.5,$<br>1.8, 1.5, 1.2 | $\pm 8$              | $\pm 8$  | $\pm 8$  | %    |
| 50- $\Omega$ $R_S$<br>3.0, 2.5, 1.8, 1.5,<br>1.2                                          | 50- $\Omega$ internal series<br>OCT with calibration                                                                   | $V_{CCIO} = 3.0, 2.5,$<br>1.8, 1.5, 1.2 | $\pm 8$              | $\pm 8$  | $\pm 8$  | %    |
| 50- $\Omega$ $R_T$<br>2.5, 1.8, 1.5, 1.2                                                  | 50- $\Omega$ internal parallel<br>OCT with calibration                                                                 | $V_{CCIO} = 2.5, 1.8,$<br>1.5, 1.2      | $\pm 10$             | $\pm 10$ | $\pm 10$ | %    |
| 20- $\Omega$ , 40- $\Omega$ , and<br>60- $\Omega$ $R_S$<br>3.0, 2.5, 1.8, 1.5,<br>1.2 (3) | 20- $\Omega$ , 40- $\Omega$ and<br>60- $\Omega$ $R_S$ expanded<br>range for internal<br>series OCT with<br>calibration | $V_{CCIO} = 3.0, 2.5,$<br>1.8, 1.5, 1.2 | $\pm 10$             | $\pm 10$ | $\pm 10$ | %    |
| 25- $\Omega$ $R_{S\_left\_shift}$<br>3.0, 2.5, 1.8, 1.5,<br>1.2                           | 25- $\Omega$ $R_{S\_left\_shift}$<br>internal left shift<br>series OCT with<br>calibration                             | $V_{CCIO} = 3.0, 2.5,$<br>1.8, 1.5, 1.2 | $\pm 10$             | $\pm 10$ | $\pm 10$ | %    |

**Notes to Table 1-12:**

- (1) OCT calibration accuracy is valid at the time of calibration only.  
 (2) 25- $\Omega$   $R_S$  is not supported for 1.5 V and 1.2 V in Row I/O.  
 (3) 20- $\Omega$   $R_S$  is not supported for 1.5 V and 1.2 V in Row I/O.

Table 1-30 lists the HSTL I/O standards for Arria II GX devices.

**Table 1-30. Differential HSTL I/O Standards for Arria II GX Devices**

| I/O Standard        | V <sub>CCIO</sub> (V) |     |       | V <sub>DIF(DC)</sub> (V) |     | V <sub>X(AC)</sub> (V) |                         |      | V <sub>CM(DC)</sub> (V)  |                         |                          | V <sub>DIF(AC)</sub> (V) |     |
|---------------------|-----------------------|-----|-------|--------------------------|-----|------------------------|-------------------------|------|--------------------------|-------------------------|--------------------------|--------------------------|-----|
|                     | Min                   | Typ | Max   | Min                      | Max | Min                    | Typ                     | Max  | Min                      | Typ                     | Max                      | Min                      | Max |
| HSTL-18 Class I     | 1.71                  | 1.8 | 1.89  | 0.2                      | —   | 0.85                   | —                       | 0.95 | 0.88                     | —                       | 0.95                     | 0.4                      | —   |
| HSTL-15 Class I, II | 1.425                 | 1.5 | 1.575 | 0.2                      | —   | 0.71                   | —                       | 0.79 | 0.71                     | —                       | 0.79                     | 0.4                      | —   |
| HSTL-12 Class I, II | 1.14                  | 1.2 | 1.26  | 0.16                     | —   | —                      | 0.5 × V <sub>CCIO</sub> | —    | 0.48 × V <sub>CCIO</sub> | 0.5 × V <sub>CCIO</sub> | 0.52 × V <sub>CCIO</sub> | 0.3                      | —   |

Table 1-31 lists the HSTL I/O standards for Arria II GZ devices.

**Table 1-31. Differential HSTL I/O Standards for Arria II GZ Devices**

| I/O Standard        | V <sub>CCIO</sub> (V) |     |       | V <sub>DIF(DC)</sub> (V) |                         | V <sub>X(AC)</sub> (V) |                         |      | V <sub>CM(DC)</sub> (V) |                         |                         | V <sub>DIF(AC)</sub> (V) |                          |
|---------------------|-----------------------|-----|-------|--------------------------|-------------------------|------------------------|-------------------------|------|-------------------------|-------------------------|-------------------------|--------------------------|--------------------------|
|                     | Min                   | Typ | Max   | Min                      | Max                     | Min                    | Typ                     | Max  | Min                     | Typ                     | Max                     | Min                      | Max                      |
| HSTL-18 Class I     | 1.71                  | 1.8 | 1.89  | 0.2                      | —                       | 0.78                   | —                       | 1.12 | 0.78                    | —                       | 1.12                    | 0.4                      | —                        |
| HSTL-15 Class I, II | 1.425                 | 1.5 | 1.575 | 0.2                      | —                       | 0.68                   | —                       | 0.9  | 0.68                    | —                       | 0.9                     | 0.4                      | —                        |
| HSTL-12 Class I, II | 1.14                  | 1.2 | 1.26  | 0.16                     | V <sub>CCIO</sub> + 0.3 | —                      | 0.5 × V <sub>CCIO</sub> | —    | 0.4 × V <sub>CCIO</sub> | 0.5 × V <sub>CCIO</sub> | 0.6 × V <sub>CCIO</sub> | 0.3                      | V <sub>CCIO</sub> + 0.48 |

Table 1-32 lists the differential I/O standard specifications for Arria II GX devices.

**Table 1-32. Differential I/O Standard Specifications for Arria II GX Devices (Note 1)**

| I/O Standard  | V <sub>CCIO</sub> (V) |     |       | V <sub>ID</sub> (mV) |                          |     | V <sub>ICM</sub> (V) (2) |      | V <sub>OD</sub> (V) (3) |     |     | V <sub>OCM</sub> (V) |      |       |
|---------------|-----------------------|-----|-------|----------------------|--------------------------|-----|--------------------------|------|-------------------------|-----|-----|----------------------|------|-------|
|               | Min                   | Typ | Max   | Min                  | Cond.                    | Max | Min                      | Max  | Min                     | Typ | Max | Min                  | Typ  | Max   |
| 2.5 V LVDS    | 2.375                 | 2.5 | 2.625 | 100                  | V <sub>CM</sub> = 1.25 V | —   | 0.05                     | 1.80 | 0.247                   | —   | 0.6 | 1.125                | 1.25 | 1.375 |
| RSDS (4)      | 2.375                 | 2.5 | 2.625 | —                    | —                        | —   | —                        | —    | 0.1                     | 0.2 | 0.6 | 0.5                  | 1.2  | 1.4   |
| Mini-LVDS (4) | 2.375                 | 2.5 | 2.625 | —                    | —                        | —   | —                        | —    | 0.25                    | —   | 0.6 | 1                    | 1.2  | 1.4   |
| LVPECL (5)    | 2.375                 | 2.5 | 2.625 | 300                  | —                        | —   | 0.6                      | 1.8  | —                       | —   | —   | —                    | —    | —     |
| BLVDS (6)     | 2.375                 | 2.5 | 2.625 | 100                  | —                        | —   | —                        | —    | —                       | —   | —   | —                    | —    | —     |

**Notes to Table 1-32:**

- (1) The 1.5 V PCML transceiver I/O standard specifications are described in “Transceiver Performance Specifications” on page 1-21.
- (2) V<sub>IN</sub> range: 0 ≤ V<sub>IN</sub> ≤ 1.85 V.
- (3) R<sub>L</sub> range: 90 ≤ R<sub>L</sub> ≤ 110 Ω.
- (4) The RSDS and mini-LVDS I/O standards are only supported for differential outputs.
- (5) The LVPECL input standard is supported at the dedicated clock input pins (GCLK) only.
- (6) There are no fixed V<sub>ICM</sub>, V<sub>OD</sub>, and V<sub>OCM</sub> specifications for BLVDS. These specifications depend on the system topology.

## Switching Characteristics

This section provides performance characteristics of the Arria II GX and GZ core and periphery blocks for commercial grade devices. The following tables are considered final and are based on actual silicon characterization and testing. These numbers reflect the actual performance of the device under worst-case silicon process, voltage, and junction temperature conditions.

### Transceiver Performance Specifications

Table 1–34 lists the Arria II GX transceiver specifications.

**Table 1–34. Transceiver Specifications for Arria II GX Devices (Note 1) (Part 1 of 7)**

| Symbol/<br>Description                     | Condition                                                               | I3   |     |        | C4   |     |        | C5 and I5 |     |        | C6   |     |        | Unit |
|--------------------------------------------|-------------------------------------------------------------------------|------|-----|--------|------|-----|--------|-----------|-----|--------|------|-----|--------|------|
|                                            |                                                                         | Min  | Typ | Max    | Min  | Typ | Max    | Min       | Typ | Max    | Min  | Typ | Max    |      |
| Reference Clock                            |                                                                         |      |     |        |      |     |        |           |     |        |      |     |        |      |
| Supported I/O Standards                    | 1.2-V PCML, 1.5-V PCML, 2.5-V PCML, Differential LVPECL, LVDS, and HCSL |      |     |        |      |     |        |           |     |        |      |     |        |      |
| Input frequency from REFCLK input pins     | —                                                                       | 50   | —   | 622.08 | 50   | —   | 622.08 | 50        | —   | 622.08 | 50   | —   | 622.08 | MHz  |
| Input frequency from PLD input             | —                                                                       | 50   | —   | 200    | 50   | —   | 200    | 50        | —   | 200    | 50   | —   | 200    | MHz  |
| Absolute V <sub>MAX</sub> for a REFCLK pin | —                                                                       | —    | —   | 2.2    | —    | —   | 2.2    | —         | —   | 2.2    | —    | —   | 2.2    | V    |
| Absolute V <sub>MIN</sub> for a REFCLK pin | —                                                                       | −0.3 | —   | —      | −0.3 | —   | —      | −0.3      | —   | —      | −0.3 | —   | —      | V    |
| Rise/fall time (2)                         | —                                                                       | —    | —   | 0.2    | —    | —   | 0.2    | —         | —   | 0.2    | —    | —   | 0.2    | UI   |
| Duty cycle                                 | —                                                                       | 45   | —   | 55     | 45   | —   | 55     | 45        | —   | 55     | 45   | —   | 55     | %    |
| Peak-to-peak differential input voltage    | —                                                                       | 200  | —   | 2000   | 200  | —   | 2000   | 200       | —   | 2000   | 200  | —   | 2000   | mV   |
| Spread-spectrum modulating clock frequency | PCIe                                                                    | 30   | —   | 33     | 30   | —   | 33     | 30        | —   | 33     | 30   | —   | 33     | kHz  |

**Table 1–34. Transceiver Specifications for Arria II GX Devices (Note 1) (Part 3 of 7)**

| Symbol/<br>Description                                                     | Condition                                                        | I3                  |     |      | C4                  |     |      | C5 and I5           |     |      | C6                  |     |      | Unit |
|----------------------------------------------------------------------------|------------------------------------------------------------------|---------------------|-----|------|---------------------|-----|------|---------------------|-----|------|---------------------|-----|------|------|
|                                                                            |                                                                  | Min                 | Typ | Max  | Min                 | Typ | Max  | Min                 | Typ | Max  | Min                 | Typ | Max  |      |
| fixedclk clock frequency                                                   | PCIe Receiver Detect                                             | —                   | 125 | —    | —                   | 125 | —    | —                   | 125 | —    | —                   | 125 | —    | MHz  |
| reconfig_clk clock frequency                                               | Dynamic reconfig. clock frequency                                | 2.5/<br>37.5<br>(4) | —   | 50   | 2.5/<br>37.5<br>(4) | —   | 50   | 2.5/<br>37.5<br>(4) | —   | 50   | 2.5/<br>37.5<br>(4) | —   | 50   | MHz  |
| Delta time between reconfig_clks (5)                                       | —                                                                | —                   | —   | 2    | —                   | —   | 2    | —                   | —   | 2    | —                   | —   | 2    | ms   |
| Transceiver block minimum power-down pulse width                           | —                                                                | —                   | 1   | —    | —                   | 1   | —    | —                   | 1   | —    | —                   | 1   | —    | μs   |
| <b>Receiver</b>                                                            |                                                                  |                     |     |      |                     |     |      |                     |     |      |                     |     |      |      |
| Supported I/O Standards                                                    | 1.4-V PCML, 1.5-V PCML, 2.5-V PCML, 2.5-V PCML, LVPECL, and LVDS |                     |     |      |                     |     |      |                     |     |      |                     |     |      |      |
| Data rate (13)                                                             | —                                                                | 600                 | —   | 6375 | 600                 | —   | 3750 | 600                 | —   | 3750 | 600                 | —   | 3125 | Mbps |
| Absolute V <sub>MAX</sub> for a receiver pin (6)                           | —                                                                | —                   | —   | 1.5  | —                   | —   | 1.5  | —                   | —   | 1.5  | —                   | —   | 1.5  | V    |
| Absolute V <sub>MIN</sub> for a receiver pin                               | —                                                                | -0.4                | —   | —    | -0.4                | —   | —    | -0.4                | —   | —    | -0.4                | —   | —    | V    |
| Maximum peak-to-peak differential input voltage V <sub>ID</sub> (diff p-p) | V <sub>ICM</sub> = 0.82 V setting                                | —                   | —   | 2.7  | —                   | —   | 2.7  | —                   | —   | 2.7  | —                   | —   | 2.7  | V    |
|                                                                            | V <sub>ICM</sub> = 1.1 V setting (7)                             | —                   | —   | 1.6  | —                   | —   | 1.6  | —                   | —   | 1.6  | —                   | —   | 1.6  | V    |

Table 1–35 lists the transceiver specifications for Arria II GZ devices.

**Table 1–35. Transceiver Specifications for Arria II GZ Devices (Part 1 of 5)**

| Symbol/<br>Description                                       | Conditions                                                              | –C3 and –I3 (1) |            |      | –C4 and –I4 |            |       | Unit   |
|--------------------------------------------------------------|-------------------------------------------------------------------------|-----------------|------------|------|-------------|------------|-------|--------|
|                                                              |                                                                         | Min             | Typ        | Max  | Min         | Typ        | Max   |        |
| Reference Clock                                              |                                                                         |                 |            |      |             |            |       |        |
| Supported I/O Standards                                      | 1.2-V PCML, 1.5-V PCML, 2.5-V PCML, Differential LVPECL, LVDS, and HCSL |                 |            |      |             |            |       |        |
| Input frequency from REFCLK input pins                       | —                                                                       | 50              | —          | 697  | 50          | —          | 637.5 | MHz    |
| Phase frequency detector (CMU PLL and receiver CDR)          | —                                                                       | 50              | —          | 325  | 50          | —          | 325   | MHz    |
| Absolute V <sub>MAX</sub> for a REFCLK pin                   | —                                                                       | —               | —          | 1.6  | —           | —          | 1.6   | V      |
| Operational V <sub>MAX</sub> for a REFCLK pin                | —                                                                       | —               | —          | 1.5  | —           | —          | 1.5   | V      |
| Absolute V <sub>MIN</sub> for a REFCLK pin                   | —                                                                       | -0.4            | —          | —    | -0.4        | —          | —     | V      |
| Rise/fall time (2)                                           | —                                                                       | —               | —          | 0.2  | —           | —          | 0.2   | UI     |
| Duty cycle                                                   | —                                                                       | 45              | —          | 55   | 45          | —          | 55    | %      |
| Peak-to-peak differential input voltage                      | —                                                                       | 200             | —          | 1600 | 200         | —          | 1600  | mV     |
| Spread-spectrum modulating clock frequency                   | PCIe                                                                    | 30              | —          | 33   | 30          | —          | 33    | kHz    |
| Spread-spectrum downspread                                   | PCIe                                                                    | —               | 0 to -0.5% | —    | —           | 0 to -0.5% | —     | —      |
| On-chip termination resistors                                | —                                                                       | —               | 100        | —    | —           | 100        | —     | Ω      |
| V <sub>ICM</sub> (AC coupled)                                | —                                                                       | 1100 ± 10%      |            |      | 1100 ± 10%  |            |       | mV     |
| V <sub>ICM</sub> (DC coupled)                                | HCSL I/O standard for PCIe reference clock                              | 250             | —          | 550  | 250         | —          | 550   | mV     |
| Transmitter REFCLK Phase Noise                               | 10 Hz                                                                   | —               | —          | -50  | —           | —          | -50   | dBc/Hz |
|                                                              | 100 Hz                                                                  | —               | —          | -80  | —           | —          | -80   | dBc/Hz |
|                                                              | 1 KHz                                                                   | —               | —          | -110 | —           | —          | -110  | dBc/Hz |
|                                                              | 10 KHz                                                                  | —               | —          | -120 | —           | —          | -120  | dBc/Hz |
|                                                              | 100 KHz                                                                 | —               | —          | -120 | —           | —          | -120  | dBc/Hz |
|                                                              | ≥ 1 MHz                                                                 | —               | —          | -130 | —           | —          | -130  | dBc/Hz |
| Transmitter REFCLK Phase Jitter (rms) for 100 MHz REFCLK (3) | 10 KHz to 20 MHz                                                        | —               | —          | 3    | —           | —          | 3     | ps     |
| R <sub>REF</sub>                                             | —                                                                       | —               | 2000 ± 1%  | —    | —           | 2000 ± 1%  | —     | Ω      |

Table 1–35. Transceiver Specifications for Arria II GZ Devices (Part 3 of 5)

| Symbol/<br>Description                                         | Conditions                                                                           | –C3 and –I3 (1)                                                                                                                                                       |     |       | –C4 and –I4 |     |       | Unit                  |
|----------------------------------------------------------------|--------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|-------|-------------|-----|-------|-----------------------|
|                                                                |                                                                                      | Min                                                                                                                                                                   | Typ | Max   | Min         | Typ | Max   |                       |
| Receiver DC Coupling Support                                   | —                                                                                    | For more information about receiver DC coupling support, refer to the “DC-Coupled Links” section in the <i>Transceiver Architecture for Arria II Devices</i> chapter. |     |       |             |     |       |                       |
| Differential on-chip termination resistors                     | 85–Ω setting                                                                         | 85 ± 20%                                                                                                                                                              |     |       | 85 ± 20%    |     |       | Ω                     |
|                                                                | 100–Ω setting                                                                        | 100 ± 20%                                                                                                                                                             |     |       | 100 ± 20%   |     |       | Ω                     |
|                                                                | 120–Ω setting                                                                        | 120 ± 20%                                                                                                                                                             |     |       | 120 ± 20%   |     |       | Ω                     |
|                                                                | 150–Ω setting                                                                        | 150 ± 20%                                                                                                                                                             |     |       | 150 ± 20%   |     |       | Ω                     |
| Differential and common mode return loss                       | PCIe (Gen 1 and Gen 2), XAUI, HiGig+, CEI SR/LR, SRIO SR/LR, CPRI LV/HV, OBSAI, SATA | Compliant                                                                                                                                                             |     |       |             |     |       | —                     |
| Programmable PPM detector (9)                                  | —                                                                                    | ± 62.5, 100, 125, 200, 250, 300, 500, 1,000                                                                                                                           |     |       |             |     |       | ppm                   |
| Run length                                                     | —                                                                                    | —                                                                                                                                                                     | —   | 200   | —           | —   | 200   | UI                    |
| Programmable equalization                                      | —                                                                                    | —                                                                                                                                                                     | —   | 16    | —           | —   | 16    | dB                    |
| t <sub>LTR</sub> (10)                                          | —                                                                                    | —                                                                                                                                                                     | —   | 75    | —           | —   | 75    | μs                    |
| t <sub>LTR_LTD_Manual</sub> (11)                               | —                                                                                    | 15                                                                                                                                                                    | —   | —     | 15          | —   | —     | μs                    |
| t <sub>LTD_Manual</sub> (12)                                   | —                                                                                    | —                                                                                                                                                                     | —   | 4000  | —           | —   | 4000  | ns                    |
| t <sub>LTD_Auto</sub> (13)                                     | —                                                                                    | —                                                                                                                                                                     | —   | 4000  | —           | —   | 4000  | ns                    |
| Receiver CDR<br>3 dB Bandwidth in lock-to-data (LTD) mode      | PCIe Gen1                                                                            | 2.0 - 3.5                                                                                                                                                             |     |       |             |     |       | MHz                   |
|                                                                | PCIe Gen2                                                                            | 40 - 65                                                                                                                                                               |     |       |             |     |       | MHz                   |
|                                                                | (OIF) CEI PHY at 6.375 Gbps                                                          | 20 - 35                                                                                                                                                               |     |       |             |     |       | MHz                   |
|                                                                | XAUI                                                                                 | 10 - 18                                                                                                                                                               |     |       |             |     |       | MHz                   |
|                                                                | SRIO 1.25 Gbps                                                                       | 10 - 18                                                                                                                                                               |     |       |             |     |       | MHz                   |
|                                                                | SRIO 2.5 Gbps                                                                        | 10 - 18                                                                                                                                                               |     |       |             |     |       | MHz                   |
|                                                                | SRIO 3.125 Gbps                                                                      | 6 - 10                                                                                                                                                                |     |       |             |     |       | MHz                   |
|                                                                | GIGE                                                                                 | 6 - 10                                                                                                                                                                |     |       |             |     |       | MHz                   |
|                                                                | SONET OC12                                                                           | 3 - 6                                                                                                                                                                 |     |       |             |     |       | MHz                   |
|                                                                | SONET OC48                                                                           | 14 - 19                                                                                                                                                               |     |       |             |     |       | MHz                   |
| Receiver buffer and CDR offset cancellation time (per channel) | —                                                                                    | —                                                                                                                                                                     | —   | 17000 | —           | —   | 17000 | recon fig_ clk cycles |
| Programmable DC gain                                           | DC Gain Setting = 0                                                                  | —                                                                                                                                                                     | 0   | —     | —           | 0   | —     | dB                    |
|                                                                | DC Gain Setting = 1                                                                  | —                                                                                                                                                                     | 3   | —     | —           | 3   | —     | dB                    |
|                                                                | DC Gain Setting = 2                                                                  | —                                                                                                                                                                     | 6   | —     | —           | 6   | —     | dB                    |



Figure 1-3 shows the differential receiver input waveform.

**Figure 1-3. Receiver Input Waveform**

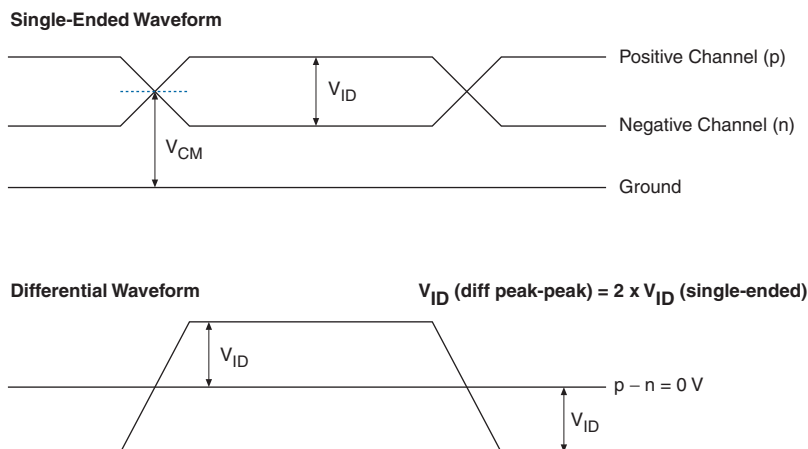


Figure 1-4 shows the transmitter output waveform.

**Figure 1-4. Transmitter Output Waveform**

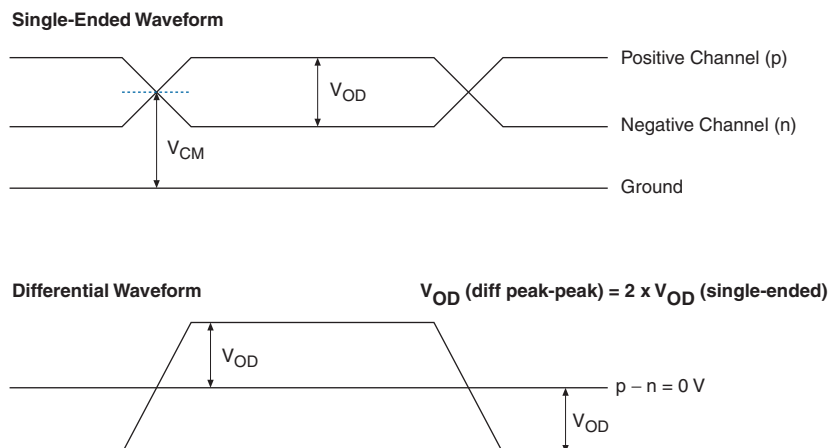


Table 1-36 lists the typical  $V_{OD}$  for TX term that equals  $85\ \Omega$  for Arria II GZ devices.

**Table 1-36. Typical  $V_{OD}$  Setting, TX Term =  $85\ \Omega$  for Arria II GZ Devices**

| Symbol                                          | $V_{OD}$ Setting (mV) |                |                |                |                |                |                |                 |
|-------------------------------------------------|-----------------------|----------------|----------------|----------------|----------------|----------------|----------------|-----------------|
|                                                 | 0                     | 1              | 2              | 3              | 4              | 5              | 6              | 7               |
| $V_{OD}$ differential peak-to-peak Typical (mV) | $170 \pm 20\%$        | $340 \pm 20\%$ | $510 \pm 20\%$ | $595 \pm 20\%$ | $680 \pm 20\%$ | $765 \pm 20\%$ | $850 \pm 20\%$ | $1020 \pm 20\%$ |

Table 1–39 lists typical transmitter pre-emphasis levels for Arria II GZ devices (in dB) for the first post tap under the following conditions (low-frequency data pattern [five 1s and five 0s] at 6.25 Gbps). The levels listed in Table 1–39 are a representation of possible pre-emphasis levels under the specified conditions only and that the pre-emphasis levels may change with data pattern and data rate.



To predict the pre-emphasis level for your specific data rate and pattern, run simulations using the **Arria II HSSI HSPICE** models.

**Table 1–39. Transmitter Pre-Emphasis Levels for Arria II GZ Devices (Part 1 of 2)**

| Pre-Emphasis<br>1st<br>Post-Tap<br>Setting | V <sub>DD</sub> Setting |     |      |      |     |     |     |     |
|--------------------------------------------|-------------------------|-----|------|------|-----|-----|-----|-----|
|                                            | 0                       | 1   | 2    | 3    | 4   | 5   | 6   | 7   |
| 0                                          | 0                       | 0   | 0    | 0    | 0   | 0   | 0   | 0   |
| 1                                          | N/A                     | 0.7 | 0    | 0    | 0   | 0   | 0   | 0   |
| 2                                          | N/A                     | 1   | 0.3  | 0    | 0   | 0   | 0   | 0   |
| 3                                          | N/A                     | 1.5 | 0.6  | 0    | 0   | 0   | 0   | 0   |
| 4                                          | N/A                     | 2   | 0.7  | 0.3  | 0   | 0   | 0   | 0   |
| 5                                          | N/A                     | 2.7 | 1.2  | 0.5  | 0.3 | 0   | 0   | 0   |
| 6                                          | N/A                     | 3.1 | 1.3  | 0.8  | 0.5 | 0.2 | 0   | 0   |
| 7                                          | N/A                     | 3.7 | 1.8  | 1.1  | 0.7 | 0.4 | 0.2 | 0   |
| 8                                          | N/A                     | 4.2 | 2.1  | 1.3  | 0.9 | 0.6 | 0.3 | 0   |
| 9                                          | N/A                     | 4.9 | 2.4  | 1.6  | 1.2 | 0.8 | 0.5 | 0.2 |
| 10                                         | N/A                     | 5.4 | 2.8  | 1.9  | 1.4 | 1   | 0.7 | 0.3 |
| 11                                         | N/A                     | 6   | 3.2  | 2.2  | 1.7 | 1.2 | 0.9 | 0.4 |
| 12                                         | N/A                     | 6.8 | 3.5  | 2.6  | 1.9 | 1.4 | 1.1 | 0.6 |
| 13                                         | N/A                     | 7.5 | 3.8  | 2.8  | 2.1 | 1.6 | 1.2 | 0.6 |
| 14                                         | N/A                     | 8.1 | 4.2  | 3.1  | 2.3 | 1.7 | 1.3 | 0.7 |
| 15                                         | N/A                     | 8.8 | 4.5  | 3.4  | 2.6 | 1.9 | 1.5 | 0.8 |
| 16                                         | N/A                     | N/A | 4.9  | 3.7  | 2.9 | 2.2 | 1.7 | 0.9 |
| 17                                         | N/A                     | N/A | 5.3  | 4    | 3.1 | 2.4 | 1.8 | 1.1 |
| 18                                         | N/A                     | N/A | 5.7  | 4.4  | 3.4 | 2.6 | 2   | 1.2 |
| 19                                         | N/A                     | N/A | 6.1  | 4.7  | 3.6 | 2.8 | 2.2 | 1.4 |
| 20                                         | N/A                     | N/A | 6.6  | 5.1  | 4   | 3.1 | 2.4 | 1.5 |
| 21                                         | N/A                     | N/A | 7    | 5.4  | 4.3 | 3.3 | 2.7 | 1.7 |
| 22                                         | N/A                     | N/A | 8    | 6.1  | 4.8 | 3.8 | 3   | 2   |
| 23                                         | N/A                     | N/A | 9    | 6.8  | 5.4 | 4.3 | 3.4 | 2.3 |
| 24                                         | N/A                     | N/A | 10   | 7.6  | 6   | 4.8 | 3.9 | 2.6 |
| 25                                         | N/A                     | N/A | 11.4 | 8.4  | 6.8 | 5.4 | 4.4 | 3   |
| 26                                         | N/A                     | N/A | 12.6 | 9.4  | 7.4 | 5.9 | 4.9 | 3.3 |
| 27                                         | N/A                     | N/A | N/A  | 10.3 | 8.1 | 6.4 | 5.3 | 3.6 |
| 28                                         | N/A                     | N/A | N/A  | 11.3 | 8.8 | 7.1 | 5.8 | 4   |

**Table 1–40. Transceiver Block Jitter Specifications for Arria II GX Devices (Note 1) (Part 2 of 10)**

| Symbol/<br>Description                   | Conditions                                         | I3     |     |      | C4     |     |      | C5, I5 |     |      | C6     |     |      | Unit |
|------------------------------------------|----------------------------------------------------|--------|-----|------|--------|-----|------|--------|-----|------|--------|-----|------|------|
|                                          |                                                    | Min    | Typ | Max  | Min    | Typ | Max  | Min    | Typ | Max  | Min    | Typ | Max  |      |
| Jitter tolerance at<br>2488.32 Mbps      | Jitter frequency =<br>0.06 KHz<br>Pattern = PRBS15 | > 15   |     |      | > 15   |     |      | > 15   |     |      | > 15   |     |      | UI   |
|                                          | Jitter frequency =<br>100 KHz<br>Pattern = PRBS15  | > 1.5  |     |      | > 1.5  |     |      | > 1.5  |     |      | > 1.5  |     |      | UI   |
|                                          | Jitter frequency =<br>1 MHz<br>Pattern = PRBS15    | > 0.15 |     |      | > 0.15 |     |      | > 0.15 |     |      | > 0.15 |     |      | UI   |
|                                          | Jitter frequency =<br>10 MHz<br>Pattern = PRBS15   | > 0.15 |     |      | > 0.15 |     |      | > 0.15 |     |      | > 0.15 |     |      | UI   |
| XAUI Transmit Jitter Generation (3)      |                                                    |        |     |      |        |     |      |        |     |      |        |     |      |      |
| Total jitter at<br>3.125 Gbps            | Pattern = CJPAT                                    | —      | —   | 0.3  | —      | —   | 0.3  | —      | —   | 0.3  | —      | —   | 0.3  | UI   |
| Deterministic<br>jitter at<br>3.125 Gbps | Pattern = CJPAT                                    | —      | —   | 0.17 | —      | —   | 0.17 | —      | —   | 0.17 | —      | —   | 0.17 | UI   |
| XAUI Receiver Jitter Tolerance (3)       |                                                    |        |     |      |        |     |      |        |     |      |        |     |      |      |
| Total jitter                             | —                                                  | > 0.65 |     |      | > 0.65 |     |      | > 0.65 |     |      | > 0.65 |     |      | UI   |
| Deterministic<br>jitter                  | —                                                  | > 0.37 |     |      | > 0.37 |     |      | > 0.37 |     |      | > 0.37 |     |      | UI   |
| Peak-to-peak<br>jitter                   | Jitter frequency =<br>22.1 KHz                     | > 8.5  |     |      | > 8.5  |     |      | > 8.5  |     |      | > 8.5  |     |      | UI   |
| Peak-to-peak<br>jitter                   | Jitter frequency =<br>1.875 MHz                    | > 0.1  |     |      | > 0.1  |     |      | > 0.1  |     |      | > 0.1  |     |      | UI   |
| Peak-to-peak<br>jitter                   | Jitter frequency =<br>20 MHz                       | > 0.1  |     |      | > 0.1  |     |      | > 0.1  |     |      | > 0.1  |     |      | UI   |
| PCIe Transmit Jitter Generation (4)      |                                                    |        |     |      |        |     |      |        |     |      |        |     |      |      |
| Total jitter at<br>2.5 Gbps (Gen1)       | Compliance<br>pattern                              | —      | —   | 0.25 | —      | —   | 0.25 | —      | —   | 0.25 | —      | —   | 0.25 | UI   |

**Table 1–41. Transceiver Block Jitter Specifications for Arria II GZ Devices (Note 1), (2) (Part 3 of 7)**

| Symbol/<br>Description                                                   | Conditions                                                                           | –C3 and –I3   |     |       | –C4 and –I4   |     |       | Unit |
|--------------------------------------------------------------------------|--------------------------------------------------------------------------------------|---------------|-----|-------|---------------|-----|-------|------|
|                                                                          |                                                                                      | Min           | Typ | Max   | Min           | Typ | Max   |      |
| Peak-to-peak jitter                                                      | Jitter frequency = 22.1 KHz                                                          | > 8.5         |     |       | > 8.5         |     |       | UI   |
| Peak-to-peak jitter                                                      | Jitter frequency = 1.875 MHz                                                         | > 0.1         |     |       | > 0.1         |     |       | UI   |
| Peak-to-peak jitter                                                      | Jitter frequency = 20 MHz                                                            | > 0.1         |     |       | > 0.1         |     |       | UI   |
| PCIe Transmit Jitter Generation (8)                                      |                                                                                      |               |     |       |               |     |       |      |
| Total jitter at 2.5 Gbps (Gen1)—<br>x1, x4, and x8                       | Compliance pattern                                                                   | —             | —   | 0.25  | —             | —   | 0.25  | UI   |
| Total jitter at 5 Gbps (Gen2)—<br>x1, x4, and x8                         | Compliance pattern                                                                   | —             | —   | 0.25  | —             | —   | —     | UI   |
| PCIe Receiver Jitter Tolerance (8)                                       |                                                                                      |               |     |       |               |     |       |      |
| Total jitter at 2.5 Gbps (Gen1)                                          | Compliance pattern                                                                   | > 0.6         |     |       | > 0.6         |     |       | UI   |
| Total jitter at 5 Gbps (Gen2)                                            | Compliance pattern                                                                   | Not supported |     |       | Not supported |     |       | UI   |
| PCIe (Gen 1) Electrical Idle Detect Threshold                            |                                                                                      |               |     |       |               |     |       |      |
| V <sub>RX-IDLE-DETDIFFp-p</sub> (9)                                      | Compliance pattern                                                                   | 65            | —   | 175   | 65            | —   | 175   | UI   |
| SRIO Transmit Jitter Generation (10)                                     |                                                                                      |               |     |       |               |     |       |      |
| Deterministic jitter<br>(peak-to-peak)                                   | Data rate = 1.25, 2.5, 3.125 Gbps<br>Pattern = CJPAT                                 | —             | —   | 0.17  | —             | —   | 0.17  | UI   |
| Total jitter (peak-to-peak)                                              | Data rate = 1.25, 2.5, 3.125 Gbps<br>Pattern = CJPAT                                 | —             | —   | 0.35  | —             | —   | 0.35  | UI   |
| SRIO Receiver Jitter Tolerance (10)                                      |                                                                                      |               |     |       |               |     |       |      |
| Deterministic jitter tolerance<br>(peak-to-peak)                         | Data rate = 1.25, 2.5, 3.125 Gbps<br>Pattern = CJPAT                                 | > 0.37        |     |       | > 0.37        |     |       | UI   |
| Combined deterministic and<br>random jitter tolerance (peak-to-<br>peak) | Data rate = 1.25, 2.5, 3.125 Gbps<br>Pattern = CJPAT                                 | > 0.55        |     |       | > 0.55        |     |       | UI   |
| Sinusoidal jitter tolerance (peak-<br>to-peak)                           | Jitter frequency = 22.1 KHz<br>Data rate = 1.25, 2.5, 3.125 Gbps<br>Pattern = CJPAT  | > 8.5         |     |       | > 8.5         |     |       | UI   |
|                                                                          | Jitter frequency = 1.875 MHz<br>Data rate = 1.25, 2.5, 3.125 Gbps<br>Pattern = CJPAT | > 0.1         |     |       | > 0.1         |     |       | UI   |
|                                                                          | Jitter frequency = 20 MHz<br>Data rate = 1.25, 2.5, 3.125 Gbps<br>Pattern = CJPAT    | > 0.1         |     |       | > 0.1         |     |       | UI   |
| GIGE Transmit Jitter Generation (11)                                     |                                                                                      |               |     |       |               |     |       |      |
| Deterministic jitter<br>(peak-to-peak)                                   | Pattern = CRPAT                                                                      | —             | —   | 0.14  | —             | —   | 0.14  | UI   |
| Total jitter (peak-to-peak)                                              | Pattern = CRPAT                                                                      | —             | —   | 0.279 | —             | —   | 0.279 | UI   |

**Table 1-41. Transceiver Block Jitter Specifications for Arria II GZ Devices (Note 1), (2) (Part 4 of 7)**

| Symbol/<br>Description                                            | Conditions                                                              | –C3 and –I3 |     |      | –C4 and –I4 |     |     | Unit |
|-------------------------------------------------------------------|-------------------------------------------------------------------------|-------------|-----|------|-------------|-----|-----|------|
|                                                                   |                                                                         | Min         | Typ | Max  | Min         | Typ | Max |      |
| GIGE Receiver Jitter Tolerance (11)                               |                                                                         |             |     |      |             |     |     |      |
| Deterministic jitter tolerance (peak-to-peak)                     | Pattern = CJPAT                                                         | > 0.4       |     |      | > 0.4       |     |     | UI   |
| Combined deterministic and random jitter tolerance (peak-to-peak) | Pattern = CJPAT                                                         | > 0.66      |     |      | > 0.66      |     |     | UI   |
| HiGig Transmit Jitter Generation                                  |                                                                         |             |     |      |             |     |     |      |
| Deterministic jitter (peak-to-peak)                               | Data rate = 3.75 Gbps<br>Pattern = CJPAT                                | —           | —   | 0.17 | —           | —   | —   | UI   |
| Total jitter (peak-to-peak)                                       | Data rate = 3.75 Gbps<br>Pattern = CJPAT                                | —           | —   | 0.35 | —           | —   | —   | UI   |
| HiGig Receiver Jitter Tolerance                                   |                                                                         |             |     |      |             |     |     |      |
| Deterministic jitter tolerance (peak-to-peak)                     | Data rate = 3.75 Gbps<br>Pattern = CJPAT                                | > 0.37      |     |      | —           | —   | —   | UI   |
| Combined deterministic and random jitter tolerance (peak-to-peak) | Data rate = 3.75 Gbps<br>Pattern = CJPAT                                | > 0.65      |     |      | —           | —   | —   | UI   |
| Sinusoidal jitter tolerance (peak-to-peak)                        | Jitter frequency = 22.1 KHz<br>Data rate = 3.75 Gbps<br>Pattern = CJPAT | > 8.5       |     |      | —           | —   | —   | UI   |
|                                                                   | Jitter frequency = 22.1 KHz<br>Data rate = 3.75 Gbps<br>Pattern = CJPAT | > 0.1       |     |      | —           | —   | —   | UI   |
|                                                                   | Jitter frequency = 22.1 KHz<br>Data rate = 3.75 Gbps<br>Pattern = CJPAT | > 0.1       |     |      | —           | —   | —   | UI   |
| (OIF) CEI Transmitter Jitter Generation                           |                                                                         |             |     |      |             |     |     |      |
| Total jitter (peak-to-peak)                                       | Data rate = 6.375 Gbps<br>Pattern = PRBS15 BER = 10 <sup>-12</sup>      | —           | —   | 0.3  | —           | —   | 0.3 | UI   |
| (OIF) CEI Receiver Jitter Tolerance                               |                                                                         |             |     |      |             |     |     |      |
| Deterministic jitter tolerance (peak-to-peak)                     | Data rate = 6.375 Gbps<br>Pattern = PRBS31 BER = 10 <sup>-12</sup>      | > 0.675     |     |      | —           | —   | —   | UI   |
| Combined deterministic and random jitter tolerance (peak-to-peak) | Data rate = 6.375 Gbps<br>Pattern = PRBS31 BER = 10 <sup>-12</sup>      | > 0.988     |     |      | —           | —   | —   | UI   |

**Table 1–41. Transceiver Block Jitter Specifications for Arria II GZ Devices (Note 1), (2) (Part 6 of 7)**

| Symbol/<br>Description                                     | Conditions                                                          | –C3 and –I3 |     |       | –C4 and –I4 |     |       | Unit |
|------------------------------------------------------------|---------------------------------------------------------------------|-------------|-----|-------|-------------|-----|-------|------|
|                                                            |                                                                     | Min         | Typ | Max   | Min         | Typ | Max   |      |
| Deterministic jitter at 3.0 Gbps (G2)                      | Pattern = CJPAT                                                     | —           | —   | 0.35  | —           | —   | 0.35  | UI   |
| Total jitter at 6.0 Gbps (G3)                              | Pattern = CJPAT                                                     | —           | —   | 0.25  | —           | —   | 0.25  | UI   |
| Random jitter at 6.0 Gbps (G3)                             | Pattern = CJPAT                                                     | —           | —   | 0.15  | —           | —   | 0.15  | UI   |
| SAS Receiver Jitter Tolerance (13)                         |                                                                     |             |     |       |             |     |       |      |
| Total jitter tolerance at 1.5 Gbps (G1)                    | Pattern = CJPAT                                                     | —           | —   | 0.65  | —           | —   | 0.65  | UI   |
| Deterministic jitter tolerance at 1.5 Gbps (G1)            | Pattern = CJPAT                                                     | —           | —   | 0.35  | —           | —   | 0.35  | UI   |
| Sinusoidal jitter tolerance at 1.5 Gbps (G1)               | Jitter frequency = 900 KHz to 5 MHz<br>Pattern = CJTPAT BER = 1E-12 | > 0.1       |     |       | > 0.1       |     |       | UI   |
| CPRI Transmit Jitter Generation (14)                       |                                                                     |             |     |       |             |     |       |      |
| Total jitter                                               | E.6.HV, E.12.HV<br>Pattern = CJPAT                                  | —           | —   | 0.279 | —           | —   | 0.279 | UI   |
|                                                            | E.6.LV, E.12.LV, E.24.LV, E.30.LV<br>Pattern = CJPAT                | —           | —   | 0.35  | —           | —   | 0.35  | UI   |
| Deterministic jitter                                       | E.6.HV, E.12.HV<br>Pattern = CJPAT                                  | —           | —   | 0.14  | —           | —   | 0.14  | UI   |
|                                                            | E.6.LV, E.12.LV, E.24.LV, E.30.LV<br>Pattern = CJPAT                | —           | —   | 0.17  | —           | —   | 0.17  | UI   |
| CPRI Receiver Jitter Tolerance (14)                        |                                                                     |             |     |       |             |     |       |      |
| Total jitter tolerance                                     | E.6.HV, E.12.HV<br>Pattern = CJPAT                                  | > 0.66      |     |       | > 0.66      |     |       | UI   |
| Deterministic jitter tolerance                             | E.6.HV, E.12.HV<br>Pattern = CJPAT                                  | > 0.4       |     |       | > 0.4       |     |       | UI   |
| Total jitter tolerance                                     | E.6.LV, E.12.LV, E.24.LV, E.30.LV<br>Pattern = CJPAT                | > 0.65      |     |       | > 0.65      |     |       | UI   |
| Deterministic jitter tolerance                             | E.6.LV, E.12.LV, E.24.LV, E.30.LV<br>Pattern = CJPAT                | > 0.37      |     |       | > 0.37      |     |       | UI   |
| Combined deterministic and random jitter tolerance         | E.6.LV, E.12.LV, E.24.LV, E.30.LV<br>Pattern = CJPAT                | > 0.55      |     |       | > 0.55      |     |       | UI   |
| OBSAI Transmit Jitter Generation (15)                      |                                                                     |             |     |       |             |     |       |      |
| Total jitter at 768 Mbps, 1536 Mbps, and 3072 Mbps         | REFCLK = 153.6 MHz<br>Pattern CJPAT                                 | —           | —   | 0.35  | —           | —   | 0.35  | UI   |
| Deterministic jitter at 768 MBps, 1536 Mbps, and 3072 Mbps | REFCLK = 153.6 MHz<br>Pattern CJPAT                                 | —           | —   | 0.17  | —           | —   | 0.17  | UI   |

**Table 1-45. PLL Specifications for Arria II GZ Devices (Part 2 of 2)**

| Symbol                         | Parameter                                                                                                | Min | Typ | Max  | Unit      |
|--------------------------------|----------------------------------------------------------------------------------------------------------|-----|-----|------|-----------|
| $t_{DLOCK}$                    | Time required to lock dynamically (after switchover or reconfiguring any non-post-scale counters/delays) | —   | —   | 1    | ms        |
| $f_{CLBW}$                     | PLL closed-loop low bandwidth                                                                            | —   | 0.3 | —    | MHz       |
|                                | PLL closed-loop medium bandwidth                                                                         | —   | 1.5 | —    | MHz       |
|                                | PLL closed-loop high bandwidth (7)                                                                       | —   | 4   | —    | MHz       |
| $t_{PLL\_PSERR}$               | Accuracy of PLL phase shift                                                                              | —   | —   | ±50  | ps        |
| $t_{ARESET}$                   | Minimum pulse width on the $areset$ signal                                                               | 10  | —   | —    | ns        |
| $t_{INCCJ}$ (3), (4)           | Input clock cycle to cycle jitter ( $F_{REF} \geq 100$ MHz)                                              | —   | —   | 0.15 | UI (p-p)  |
|                                | Input clock cycle to cycle jitter ( $F_{REF} < 100$ MHz)                                                 | —   | —   | ±750 | ps (p-p)  |
| $t_{OUTPJ\_DC}$ (5)            | Period Jitter for dedicated clock output ( $F_{OUT} \geq 100$ MHz)                                       | —   | —   | 175  | ps (p-p)  |
|                                | Period Jitter for dedicated clock output ( $F_{OUT} < 100$ MHz)                                          | —   | —   | 17.5 | mUI (p-p) |
| $t_{OUTCCJ\_DC}$ (5)           | Cycle to Cycle Jitter for dedicated clock output ( $F_{OUT} \geq 100$ MHz)                               | —   | —   | 175  | ps (p-p)  |
|                                | Cycle to Cycle Jitter for dedicated clock output ( $F_{OUT} < 100$ MHz)                                  | —   | —   | 17.5 | mUI (p-p) |
| $t_{OUTPJ\_IO}$ (5), (8)       | Period Jitter for clock output on regular I/O ( $F_{OUT} \geq 100$ MHz)                                  | —   | —   | 600  | ps (p-p)  |
|                                | Period Jitter for clock output on regular I/O ( $F_{OUT} < 100$ MHz)                                     | —   | —   | 60   | mUI (p-p) |
| $t_{OUTCCJ\_IO}$ (5), (8)      | Cycle to Cycle Jitter for clock output on regular I/O ( $F_{OUT} \geq 100$ MHz)                          | —   | —   | 600  | ps (p-p)  |
|                                | Cycle to Cycle Jitter for clock output on regular I/O ( $F_{OUT} < 100$ MHz)                             | —   | —   | 60   | mUI (p-p) |
| $t_{CASC\_OUTPJ\_DC}$ (5), (6) | Period Jitter for dedicated clock output in cascaded PLLs ( $F_{OUT} \geq 100$ MHz)                      | —   | —   | 250  | ps (p-p)  |
|                                | Period Jitter for dedicated clock output in cascaded PLLs ( $F_{OUT} < 100$ MHz)                         | —   | —   | 25   | mUI (p-p) |
| $f_{DRIFT}$                    | Frequency drift after PFDENA is disabled for duration of 100 $\mu$ s                                     | —   | —   | ±10  | %         |

**Notes to Table 1-45:**

- (1) This specification is limited in the Quartus II software by the I/O maximum frequency. The maximum I/O frequency is different for each I/O standard.
- (2) This specification is limited by the lower of the two: I/O  $F_{MAX}$  or  $F_{OUT}$  of the PLL.
- (3) A high input jitter directly affects the PLL output jitter. To have low PLL output clock jitter, you must provide a clean clock source that is less than 120 ps.
- (4)  $F_{REF}$  is  $f_{IN}/N$  when  $N = 1$ .
- (5) Peak-to-peak jitter with a probability level of  $10^{-12}$  (14 sigma, 99.9999999974404% confidence level). The output jitter specification applies to the intrinsic jitter of the PLL, when an input jitter of 30 ps is applied. The external memory interface clock output jitter specifications use a different measurement method and are available in [Table 1-64 on page 1-71](#).
- (6) The cascaded PLL specification is only applicable with the following condition:
  - a. Upstream PLL:  $0.59 \text{ MHz} \leq \text{Upstream PLL BW} < 1 \text{ MHz}$
  - b. Downstream PLL:  $\text{Downstream PLL BW} > 2 \text{ MHz}$
- (7) High bandwidth PLL settings are not supported in external feedback mode.
- (8) External memory interface clock output jitter specifications use a different measurement method, which is available in [Table 1-63 on page 1-71](#).

## DSP Block Specifications

Table 1-46 lists the DSP block performance specifications for Arria II GX devices.

**Table 1-46. DSP Block Performance Specifications for Arria II GX Devices (Note 1)**

| Mode                                             | Resources Used        | Performance |     |       |     | Unit |
|--------------------------------------------------|-----------------------|-------------|-----|-------|-----|------|
|                                                  | Number of Multipliers | C4          | I3  | C5,I5 | C6  |      |
| 9 × 9-bit multiplier                             | 1                     | 380         | 310 | 300   | 250 | MHz  |
| 12 × 12-bit multiplier                           | 1                     | 380         | 310 | 300   | 250 | MHz  |
| 18 × 18-bit multiplier                           | 1                     | 380         | 310 | 300   | 250 | MHz  |
| 36 × 36-bit multiplier                           | 1                     | 350         | 270 | 270   | 220 | MHz  |
| 18 × 36-bit high-precision multiplier adder mode | 1                     | 350         | 270 | 270   | 220 | MHz  |
| 18 × 18-bit multiply accumulator                 | 4                     | 380         | 310 | 300   | 250 | MHz  |
| 18 × 18-bit multiply adder                       | 4                     | 380         | 310 | 300   | 250 | MHz  |
| 18 × 18-bit multiply adder-signed full precision | 2                     | 380         | 310 | 300   | 250 | MHz  |
| 18 × 18-bit multiply adder with loopback (2)     | 2                     | 275         | 220 | 220   | 180 | MHz  |
| 36-bit shift (32-bit data)                       | 1                     | 350         | 270 | 270   | 220 | MHz  |
| Double mode                                      | 1                     | 350         | 270 | 270   | 220 | MHz  |

**Notes to Table 1-46:**

- (1) Maximum is for a fully-pipelined block with **Round** and **Saturation** disabled.
- (2) Maximum is for loopback input registers disabled, **Round** and **Saturation** disabled, pipeline and output registers enabled.

Table 1-47 lists the DSP block performance specifications for Arria II GZ devices.

**Table 1-47. DSP Block Performance Specifications for Arria II GZ Devices (Note 1) (Part 1 of 2)**

| Mode                                             | Resources Used        | Performance |     | Unit |
|--------------------------------------------------|-----------------------|-------------|-----|------|
|                                                  | Number of Multipliers | -3          | -4  |      |
| 9 × 9-bit multiplier                             | 1                     | 460         | 400 | MHz  |
| 12 × 12-bit multiplier                           | 1                     | 500         | 440 | MHz  |
| 18 × 18-bit multiplier                           | 1                     | 550         | 480 | MHz  |
| 36 × 36-bit multiplier                           | 1                     | 440         | 380 | MHz  |
| 18 × 18-bit multiply accumulator                 | 4                     | 440         | 380 | MHz  |
| 18 × 18-bit multiply adder                       | 4                     | 470         | 410 | MHz  |
| 18 × 18-bit multiply adder-signed full precision | 2                     | 450         | 390 | MHz  |
| 18 × 18-bit multiply adder with loopback (2)     | 2                     | 350         | 310 | MHz  |
| 36-bit shift (32-bit data)                       | 1                     | 440         | 380 | MHz  |



Table 1-49 lists the embedded memory block specifications for Arria II GZ devices.

**Table 1-49. Embedded Memory Block Performance Specifications for Arria II GZ Devices (Note 1)**

| Memory             | Mode                                                                                | Resources Used |                  | Performance |     |     |     | Unit |
|--------------------|-------------------------------------------------------------------------------------|----------------|------------------|-------------|-----|-----|-----|------|
|                    |                                                                                     | ALUTs          | TriMatrix Memory | C3          | I3  | C4  | I4  |      |
| MLAB<br>(2)        | Single port 64 × 10                                                                 | 0              | 1                | 500         | 500 | 450 | 450 | MHz  |
|                    | Simple dual-port 32 × 20                                                            | 0              | 1                | 500         | 500 | 450 | 450 | MHz  |
|                    | Simple dual-port 64 × 10                                                            | 0              | 1                | 500         | 500 | 450 | 450 | MHz  |
|                    | ROM 64 × 10                                                                         | 0              | 1                | 500         | 500 | 450 | 450 | MHz  |
|                    | ROM 32 × 20                                                                         | 0              | 1                | 500         | 500 | 450 | 450 | MHz  |
| M9K<br>Block (2)   | Single-port 256 × 36                                                                | 0              | 1                | 540         | 540 | 475 | 475 | MHz  |
|                    | Simple dual-port 256 × 36                                                           | 0              | 1                | 490         | 490 | 420 | 420 | MHz  |
|                    | Simple dual-port 256 × 36, with the read-during-write option set to <b>Old Data</b> | 0              | 1                | 340         | 340 | 300 | 300 | MHz  |
|                    | True dual port 512 × 18                                                             | 0              | 1                | 430         | 430 | 370 | 370 | MHz  |
|                    | True dual-port 512 × 18, with the read-during-write option set to <b>Old Data</b>   | 0              | 1                | 335         | 335 | 290 | 290 | MHz  |
|                    | ROM 1 Port                                                                          | 0              | 1                | 540         | 540 | 475 | 475 | MHz  |
|                    | ROM 2 Port                                                                          | 0              | 1                | 540         | 540 | 475 | 475 | MHz  |
|                    | Min Pulse Width (clock high time)                                                   | —              | —                | 800         | 800 | 850 | 850 | ps   |
|                    | Min Pulse Width (clock low time)                                                    | —              | —                | 625         | 625 | 690 | 690 | ps   |
| M144K<br>Block (2) | Single-port 2K × 72                                                                 | 0              | 1                | 440         | 400 | 380 | 350 | MHz  |
|                    | Simple dual-port 2K × 72                                                            | 0              | 1                | 435         | 375 | 385 | 325 | MHz  |
|                    | Simple dual-port 2K × 72, with the read-during-write option set to <b>Old Data</b>  | 0              | 1                | 240         | 225 | 205 | 200 | MHz  |
|                    | Simple dual-port 2K × 64 (with ECC)                                                 | 0              | 1                | 300         | 295 | 255 | 250 | MHz  |
|                    | True dual-port 4K × 36                                                              | 0              | 1                | 375         | 350 | 330 | 310 | MHz  |
|                    | True dual-port 4K × 36, with the read-during-write option set to <b>Old Data</b>    | 0              | 1                | 230         | 225 | 205 | 200 | MHz  |
|                    | ROM 1 Port                                                                          | 0              | 1                | 500         | 450 | 435 | 420 | MHz  |
|                    | ROM 2 Port                                                                          | 0              | 1                | 465         | 425 | 400 | 400 | MHz  |
|                    | Min Pulse Width (clock high time)                                                   | —              | —                | 755         | 860 | 860 | 950 | ps   |
|                    | Min Pulse Width (clock low time)                                                    | —              | —                | 625         | 690 | 690 | 690 | ps   |

**Notes to Table 1-48:**

- (1) To achieve the maximum memory block performance, use a memory block clock that comes through global clock routing from an on-chip PLL set to 50% output duty cycle. Use the Quartus II software to report timing for this and other memory block clocking schemes.
- (2) When you use the error detection CRC feature, there is no degradation in  $F_{MAX}$ .

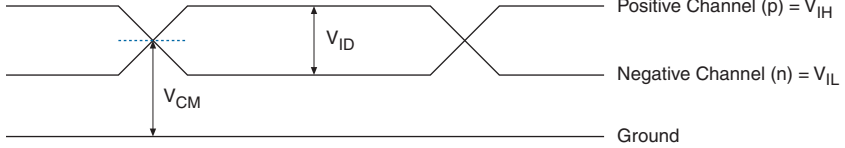
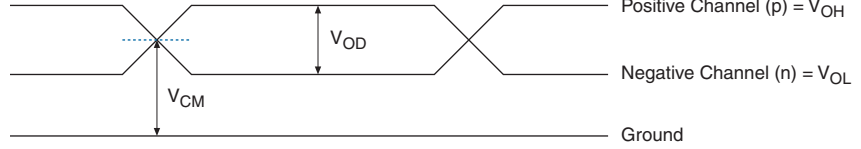
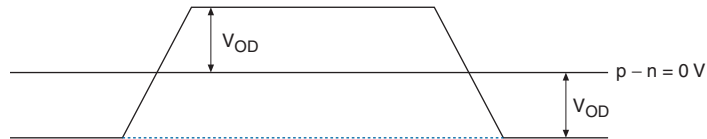
**Table 1-54. High-Speed I/O Specifications for Arria II GZ Devices (Note 1), (2), (10) (Part 2 of 3)**

| Symbol                                                                                                  | Conditions                                                                       | C3, I3 |     |         | C4, I4 |     |         | Unit |
|---------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------|--------|-----|---------|--------|-----|---------|------|
|                                                                                                         |                                                                                  | Min    | Typ | Max     | Min    | Typ | Max     |      |
| $f_{\text{HCLK\_OUT}}$ (output clock frequency)                                                         | —                                                                                | 5      | —   | 717 (7) | 5      | —   | 717 (7) | MHz  |
| <b>Transmitter</b>                                                                                      |                                                                                  |        |     |         |        |     |         |      |
| $f_{\text{HSDR}}$ (true LVDS output data rate)                                                          | SERDES factor, J = 3 to 10 (using dedicated SERDES) (8)                          | (4)    | —   | 1250    | (4)    | —   | 1250    | Mbps |
|                                                                                                         | SERDES factor J = 2, (using DDR registers)                                       | (4)    | —   | (5)     | (4)    | —   | (5)     | Mbps |
|                                                                                                         | SERDES factor J = 1, (uses an SDR register)                                      | (4)    | —   | (5)     | (4)    | —   | (5)     | Mbps |
| $f_{\text{HSDR}}$ (emulated LVDS_E_3R output data rate) (5)                                             | SERDES factor J = 4 to 10                                                        | (4)    | —   | 1152    | (4)    | —   | 800     | Mbps |
| $f_{\text{HSDR}}$ (emulated LVDS_E_1R output data rate)                                                 |                                                                                  | (4)    | —   | 200     | (4)    | —   | 200     | Mbps |
| $t_{\text{x Jitter}}$                                                                                   | Total jitter for data rate, 600 Mbps to 1.6 Gbps                                 | —      | —   | 160     | —      | —   | 160     | ps   |
|                                                                                                         | Total jitter for data rate, < 600 Mbps                                           | —      | —   | 0.1     | —      | —   | 0.1     | UI   |
| $t_{\text{x Jitter}}$ - emulated differential I/O standards with three external output resistor network | Total jitter for data rate, 600 Mbps to 1.25 Gbps                                | —      | —   | 300     | —      | —   | 325     | ps   |
|                                                                                                         | Total jitter for data rate < 600 Mbps                                            | —      | —   | 0.2     | —      | —   | 0.25    | UI   |
| $t_{\text{x Jitter}}$ - emulated differential I/O standards with one external output resistor network   | —                                                                                | —      | —   | 0.15    | —      | —   | 0.15    | UI   |
| $t_{\text{DUTY}}$                                                                                       | TX output clock duty cycle for both True and emulated differential I/O standards | 45     | 50  | 55      | 45     | 50  | 55      | %    |

# Glossary

Table 1-68 lists the glossary for this chapter.

**Table 1-68. Glossary (Part 1 of 4)**

| Letter              | Subject                    | Definitions                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
|---------------------|----------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| A,<br>B,<br>C,<br>D | Differential I/O Standards | <p><i>Receiver Input Waveforms</i></p> <p><b>Single-Ended Waveform</b></p>  <p>Positive Channel (p) = <math>V_{IH}</math></p> <p>Negative Channel (n) = <math>V_{IL}</math></p> <p>Ground</p> <p><b>Differential Waveform</b></p>  <p><i>Transmitter Output Waveforms</i></p> <p><b>Single-Ended Waveform</b></p>  <p>Positive Channel (p) = <math>V_{OH}</math></p> <p>Negative Channel (n) = <math>V_{OL}</math></p> <p>Ground</p> <p><b>Differential Waveform</b></p>  |
|                     |                            |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
|                     |                            |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
|                     |                            |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| E,<br>F             | $f_{HSCLK}$                | Left/Right PLL input clock frequency.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|                     | $f_{HSDR}$                 | High-speed I/O block: Maximum/minimum LVDS data transfer rate ( $f_{HSDR} = 1/TUI$ ), non-DPA.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
|                     | $f_{HSRDPA}$               | High-speed I/O block: Maximum/minimum LVDS data transfer rate ( $f_{HSRDPA} = 1/TUI$ ), DPA.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |

**Table 1–68. Glossary (Part 4 of 4)**

| Letter              | Subject       | Definitions                                                                                                                                                       |
|---------------------|---------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| U,<br>V             | $V_{CM(DC)}$  | DC common mode input voltage.                                                                                                                                     |
|                     | $V_{ICM}$     | Input common mode voltage: The common mode of the differential signal at the receiver.                                                                            |
|                     | $V_{ID}$      | Input differential voltage swing: The difference in voltage between the positive and complementary conductors of a differential transmission at the receiver.     |
|                     | $V_{DIF(AC)}$ | AC differential input voltage: Minimum AC input differential voltage required for switching.                                                                      |
|                     | $V_{DIF(DC)}$ | DC differential input voltage: Minimum DC input differential voltage required for switching.                                                                      |
|                     | $V_{IH}$      | Voltage input high: The minimum positive voltage applied to the input which is accepted by the device as a logic high.                                            |
|                     | $V_{IH(AC)}$  | High-level AC input voltage.                                                                                                                                      |
|                     | $V_{IH(DC)}$  | High-level DC input voltage.                                                                                                                                      |
|                     | $V_{IL}$      | Voltage input low: The maximum positive voltage applied to the input which is accepted by the device as a logic low.                                              |
|                     | $V_{IL(AC)}$  | Low-level AC input voltage.                                                                                                                                       |
|                     | $V_{IL(DC)}$  | Low-level DC input voltage.                                                                                                                                       |
|                     | $V_{OCM}$     | Output common mode voltage: The common mode of the differential signal at the transmitter.                                                                        |
|                     | $V_{OD}$      | Output differential voltage swing: The difference in voltage between the positive and complementary conductors of a differential transmission at the transmitter. |
| W,<br>X,<br>Y,<br>Z | W             | High-speed I/O block: The clock boost factor.                                                                                                                     |

## Document Revision History

Table 1–69 lists the revision history for this chapter.

**Table 1–69. Document Revision History (Part 1 of 2)**

| Date          | Version | Changes                                                                                                                                                                                                                                                                                                             |
|---------------|---------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| December 2013 | 4.4     | Updated Table 1–34 and Table 1–35.                                                                                                                                                                                                                                                                                  |
| July 2012     | 4.3     | <ul style="list-style-type: none"> <li>Updated the <math>V_{CCH\_GXBL/R}</math> operating conditions in Table 1–6.</li> <li>Finalized Arria II GZ information in Table 1–20.</li> <li>Added BLVDS specification in Table 1–32 and Table 1–33.</li> <li>Updated input and output waveforms in Table 1–68.</li> </ul> |
| December 2011 | 4.2     | <ul style="list-style-type: none"> <li>Updated Table 1–32, Table 1–33, Table 1–34, Table 1–35, Table 1–40, Table 1–41, Table 1–54, and Table 1–67.</li> <li>Minor text edits.</li> </ul>                                                                                                                            |
| June 2011     | 4.1     | <ul style="list-style-type: none"> <li>Added Table 1–60.</li> <li>Updated Table 1–32, Table 1–33, Table 1–38, Table 1–41, and Table 1–61.</li> <li>Updated the “Switching Characteristics” section introduction.</li> <li>Minor text edits.</li> </ul>                                                              |

**Table 1-69. Document Revision History (Part 2 of 2)**

| Date          | Version | Changes                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
|---------------|---------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| December 2010 | 4.0     | <ul style="list-style-type: none"> <li>■ Added Arria II GZ information.</li> <li>■ Added Table 1-61 with Arria II GX information.</li> <li>■ Updated Table 1-1, Table 1-2, Table 1-5, Table 1-6, Table 1-7, Table 1-11, Table 1-35, Table 1-37, Table 1-40, Table 1-42, Table 1-44, Table 1-45, Table 1-57, Table 1-61, and Table 1-63.</li> <li>■ Updated Figure 1-5.</li> <li>■ Updated for the Quartus II version 10.0 release.</li> <li>■ Updated the first paragraph for searchability.</li> <li>■ Minor text edits.</li> </ul>                                                                                                                                                                  |
| July 2010     | 3.0     | <ul style="list-style-type: none"> <li>■ Updated Table 1-1, Table 1-4, Table 1-16, Table 1-19, Table 1-21, Table 1-23, Table 1-25, Table 1-26, Table 1-30, and Table 1-35</li> <li>■ Added Table 1-27 and Table 1-29.</li> <li>■ Added I3 speed grade information to Table 1-19, Table 1-21, Table 1-22, Table 1-24, Table 1-25, Table 1-30, Table 1-32, Table 1-33, Table 1-34, and Table 1-35.</li> <li>■ Updated the “Operating Conditions” section.</li> <li>■ Removed “Preliminary” from Table 1-19, Table 1-21, Table 1-22, Table 1-23, Table 1-24, Table 1-25, Table 1-26, Table 1-28, Table 1-30, Table 1-32, Table 1-33, Table 1-34, and Figure 1-4.</li> <li>■ Minor text edits.</li> </ul> |
| March 2010    | 2.3     | <p>Updated for the Quartus II version 9.1 SP2 release:</p> <ul style="list-style-type: none"> <li>■ Updated Table 1-3, Table 1-7, Table 1-19, Table 1-21, Table 1-22, Table 1-24, Table 1-25 and Table 1-33.</li> <li>■ Updated “Recommended Operating Conditions” section.</li> <li>■ Minor text edits.</li> </ul>                                                                                                                                                                                                                                                                                                                                                                                   |
| February 2010 | 2.2     | Updated Table 1-19.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| February 2010 | 2.1     | <p>Updated for Arria II GX v9.1 SP1 release:</p> <ul style="list-style-type: none"> <li>■ Updated Table 1-19, Table 1-23, Table 1-28, Table 1-30, and Table 1-33.</li> <li>■ Added Figure 1-5.</li> <li>■ Minor text edits.</li> </ul>                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| November 2009 | 2.0     | <p>Updated for Arria II GX v9.1 release:</p> <ul style="list-style-type: none"> <li>■ Updated Table 1-1, Table 1-4, Table 1-13, Table 1-14, Table 1-19, Table 1-15, Table 1-22, Table 1-24, and Table 1-28.</li> <li>■ Added Table 1-6 and Table 1-33.</li> <li>■ Added “Bus Hold” on page 1-5.</li> <li>■ Added “IOE Programmable Delay” section.</li> <li>■ Minor text edit.</li> </ul>                                                                                                                                                                                                                                                                                                             |
| June 2009     | 1.2     | <ul style="list-style-type: none"> <li>■ Updated Table 1-1, Table 1-3, Table 1-7, Table 1-8, Table 1-18, Table 1-23, Table 1-25, Table 1-26, Table 1-29, Table 1-30, Table 1-31, Table 1-32, and Table 1-33.</li> <li>■ Added Table 1-32.</li> <li>■ Updated Equation 1-1.</li> </ul>                                                                                                                                                                                                                                                                                                                                                                                                                 |
| March 2009    | 1.1     | Added “I/O Timing” section.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| February 2009 | 1.0     | Initial release.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |