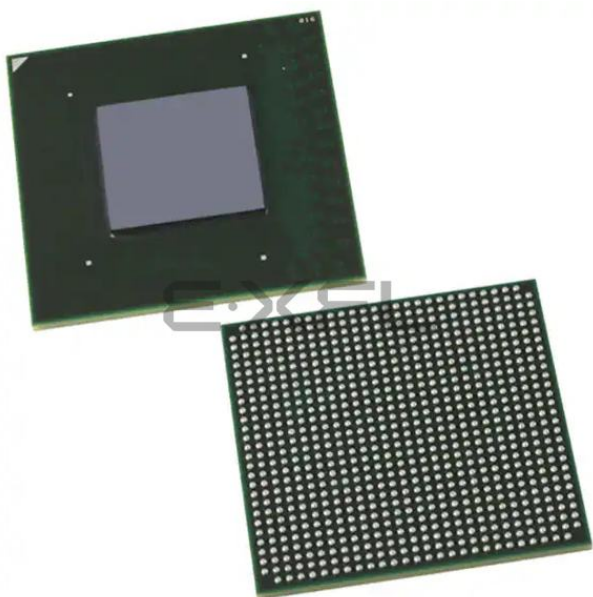




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Details

Product Status	Obsolete
Number of LABs/CLBs	2530
Number of Logic Elements/Cells	60214
Total RAM Bits	5371904
Number of I/O	364
Number of Gates	-
Voltage - Supply	0.87V ~ 0.93V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	780-BBGA, FCBGA
Supplier Device Package	780-FBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep2agx65df29c5n

Table 1-19 lists the weak pull-up resistor values for Arria II GZ devices.

Table 1-19. Internal Weak Pull-Up Resistor for Arria II GZ Devices (Note 1), (2)

Symbol	Description	Conditions	Min	Typ	Max	Unit
R_{PU}	Value of the I/O pin pull-up resistor before and during configuration, as well as user mode if the programmable pull-up resistor option is enabled.	$V_{CCIO} = 3.0\text{ V} \pm 5\%$ (3)	—	25	—	$k\Omega$
		$V_{CCIO} = 2.5\text{ V} \pm 5\%$ (3)	—	25	—	$k\Omega$
		$V_{CCIO} = 1.8\text{ V} \pm 5\%$ (3)	—	25	—	$k\Omega$
		$V_{CCIO} = 1.5\text{ V} \pm 5\%$ (3)	—	25	—	$k\Omega$
		$V_{CCIO} = 1.2\text{ V} \pm 5\%$ (3)	—	25	—	$k\Omega$

Notes to Table 1-19:

- (1) All I/O pins have an option to enable weak pull-up except configuration, test, and JTAG pins.
- (2) The internal weak pull-down feature is only available for the JTAG TCK pin. The typical value for this internal weak pull-down resistor is approximately $25\text{ k}\Omega$.
- (3) Pin pull-up resistance values may be lower if an external source drives the pin higher than V_{CCIO} .

Hot Socketing

Table 1-20 lists the hot-socketing specification for Arria II GX and GZ devices.

Table 1-20. Hot Socketing Specifications for Arria II Devices

Symbol	Description	Maximum
$I_{IOPIN(DC)}$	DC current per I/O pin	$300\text{ }\mu\text{A}$
$I_{IOPIN(AC)}$	AC current per I/O pin	8 mA (1)
$I_{XCVR TX(DC)}$	DC current per transceiver TX pin	100 mA
$I_{XCVR RX(DC)}$	DC current per transceiver RX pin	50 mA

Note to Table 1-20:

- (1) The I/O ramp rate is 10 ns or more. For ramp rates faster than 10 ns , $|I_{IOPIN}| = C\text{ dv/dt}$, in which “C” is I/O pin capacitance and “dv/dt” is slew rate.

Schmitt Trigger Input

The Arria II GX device supports Schmitt trigger input on the TDI, TMS, TCK, nSTATUS, nCONFIG, nCE, CONF_DONE, and DCLK pins. A Schmitt trigger feature introduces hysteresis to the input signal for improved noise immunity, especially for signals with slow edge rates.

Table 1-21 lists the hysteresis specifications across the supported V_{CCIO} range for Schmitt trigger inputs in Arria II GX devices.

Table 1-21. Schmitt Trigger Input Hysteresis Specifications for Arria II GX Devices

Symbol	Description	Condition (V)	Minimum	Unit
$V_{Schmitt}$	Hysteresis for Schmitt trigger input	$V_{CCIO} = 3.3$	220	mV
		$V_{CCIO} = 2.5$	180	mV
		$V_{CCIO} = 1.8$	110	mV
		$V_{CCIO} = 1.5$	70	mV

I/O Standard Specifications

Table 1–22 through Table 1–35 list input voltage (V_{IH} and V_{IL}), output voltage (V_{OH} and V_{OL}), and current drive characteristics (I_{OH} and I_{OL}) for various I/O standards supported by the Arria II device family. They also show the Arria II device family I/O standard specifications. V_{OL} and V_{OH} values are valid at the corresponding I_{OH} and I_{OL} , respectively.



For an explanation of terms used in Table 1–22 through Table 1–35, refer to “Glossary” on page 1–74.

Table 1–22 lists the single-ended I/O standards for Arria II GX devices.

Table 1–22. Single-Ended I/O Standards for Arria II GX Devices

I/O Standard	V_{CCIO} (V)			V_{IL} (V)		V_{IH} (V)		V_{OL} (V)	V_{OH} (V)	I_{OL} (mA)	I_{OH} (mA)
	Min	Typ	Max	Min	Max	Min	Max	Max	Min		
3.3 V LVTTTL	3.135	3.3	3.465	–0.3	0.8	1.7	3.6	0.45	2.4	4	–4
3.3 V LVCMOS	3.135	3.3	3.465	–0.3	0.8	1.7	3.6	0.2	$V_{CCIO} - 0.2$	2	–2
3.0 V LVTTTL	2.85	3	3.15	–0.3	0.8	1.7	$V_{CCIO} + 0.3$	0.45	2.4	4	–4
3.0 V LVCMOS	2.85	3	3.15	–0.3	0.8	1.7	$V_{CCIO} + 0.3$	0.2	$V_{CCIO} - 0.2$	0.1	–0.1
2.5 V LVCMOS	2.375	2.5	2.625	–0.3	0.7	1.7	$V_{CCIO} + 0.3$	0.4	2	1	–1
1.8 V LVCMOS	1.71	1.8	1.89	–0.3	$0.35 \times V_{CCIO}$	$0.65 \times V_{CCIO}$	$V_{CCIO} + 0.3$	0.45	$V_{CCIO} - 0.45$	2	–2
1.5 V LVCMOS	1.425	1.5	1.575	–0.3	$0.35 \times V_{CCIO}$	$0.65 \times V_{CCIO}$	$V_{CCIO} + 0.3$	$0.25 \times V_{CCIO}$	$0.75 \times V_{CCIO}$	2	–2
1.2 V LVCMOS	1.14	1.2	1.26	–0.3	$0.35 \times V_{CCIO}$	$0.65 \times V_{CCIO}$	$V_{CCIO} + 0.3$	$0.25 \times V_{CCIO}$	$0.75 \times V_{CCIO}$	2	–2
3.0-V PCI	2.85	3	3.15	—	$0.3 \times V_{CCIO}$	$0.5 \times V_{CCIO}$	$V_{CCIO} + 0.3$	$0.1 \times V_{CCIO}$	$0.9 \times V_{CCIO}$	1.5	–0.5
3.0-V PCI-X	2.85	3	3.15	—	$0.35 \times V_{CCIO}$	$0.5 \times V_{CCIO}$	$V_{CCIO} + 0.3$	$0.1 \times V_{CCIO}$	$0.9 \times V_{CCIO}$	1.5	–0.5

Table 1–23 lists the single-ended I/O standards for Arria II GZ devices.

Table 1–23. Single-Ended I/O Standards for Arria II GZ Devices (Part 1 of 2)

I/O Standard	V_{CCIO} (V)			V_{IL} (V)		V_{IH} (V)		V_{OL} (V)	V_{OH} (V)	I_{OL} (mA)	I_{OH} (mA)
	Min	Typ	Max	Min	Max	Min	Max	Max	Min		
LVTTTL	2.85	3	3.15	–0.3	0.8	1.7	3.6	0.4	2.4	2	–2
LVCMOS	2.85	3	3.15	–0.3	0.8	1.7	3.6	0.2	$V_{CCIO} - 0.2$	0.1	–0.1
2.5 V	2.375	2.5	2.625	–0.3	0.7	1.7	3.6	0.4	2	1	–1
1.8 V	1.71	1.8	1.89	–0.3	$0.35 \times V_{CCIO}$	$0.65 \times V_{CCIO}$	$V_{CCIO} + 0.3$	0.45	$V_{CCIO} - 0.45$	2	–2
1.5 V	1.425	1.5	1.575	–0.3	$0.35 \times V_{CCIO}$	$0.65 \times V_{CCIO}$	$V_{CCIO} + 0.3$	$0.25 \times V_{CCIO}$	$0.75 \times V_{CCIO}$	2	–2

Table 1-27. Single-Ended SSTL and HSTL I/O Standards Signal Specifications for Arria II GZ Devices (Part 2 of 2)

I/O Standard	$V_{IL(DC)} (V)$		$V_{IH(DC)} (V)$		$V_{IL(AC)} (V)$	$V_{IH(AC)} (V)$	$V_{OL} (V)$	$V_{OH} (V)$	$I_{OL} (mA)$	$I_{OH} (mA)$
	Min	Max	Min	Max	Max	Min	Max	Min		
SSTL-15 Class II	—	$V_{REF} - 0.1$	$V_{REF} + 0.1$	—	$V_{REF} - 0.175$	$V_{REF} + 0.175$	$0.2 \times V_{CCIO}$	$0.8 \times V_{CCIO}$	16	-16
HSTL-18 Class I	—	$V_{REF} - 0.1$	$V_{REF} + 0.1$	—	$V_{REF} - 0.2$	$V_{REF} + 0.2$	0.4	$V_{CCIO} - 0.4$	8	-8
HSTL-18 Class II	—	$V_{REF} - 0.1$	$V_{REF} + 0.1$	—	$V_{REF} - 0.2$	$V_{REF} + 0.2$	0.4	$V_{CCIO} - 0.4$	16	-16
HSTL-15 Class I	—	$V_{REF} - 0.1$	$V_{REF} + 0.1$	—	$V_{REF} - 0.2$	$V_{REF} + 0.2$	0.4	$V_{CCIO} - 0.4$	8	-8
HSTL-15 Class II	—	$V_{REF} - 0.1$	$V_{REF} + 0.1$	—	$V_{REF} - 0.2$	$V_{REF} + 0.2$	0.4	$V_{CCIO} - 0.4$	16	-16
HSTL-12 Class I	-0.15	$V_{REF} - 0.08$	$V_{REF} + 0.08$	$V_{CCIO} + 0.15$	$V_{REF} - 0.15$	$V_{REF} + 0.15$	$0.25 \times V_{CCIO}$	$0.75 \times V_{CCIO}$	8	-8
HSTL-12 Class II	-0.15	$V_{REF} - 0.08$	$V_{REF} + 0.08$	$V_{CCIO} + 0.15$	$V_{REF} - 0.15$	$V_{REF} + 0.15$	$0.25 \times V_{CCIO}$	$0.75 \times V_{CCIO}$	16	-16

Table 1-28 lists the differential SSTL I/O standards for Arria II GX devices.

Table 1-28. Differential SSTL I/O Standards for Arria II GX Devices

I/O Standard	$V_{CCIO} (V)$			$V_{SWING(DC)} (V)$		$V_{X(AC)} (V)$			$V_{SWING(AC)} (V)$		$V_{OX(AC)} (V)$		
	Min	Typ	Max	Min	Max	Min	Typ	Max	Min	Max	Min	Typ	Max
SSTL-2 Class I, II	2.375	2.5	2.625	0.36	V_{CCIO}	$V_{CCIO}/2 - 0.2$	—	$V_{CCIO}/2 + 0.2$	0.7	V_{CCIO}	$V_{CCIO}/2 - 0.15$	—	$V_{CCIO}/2 + 0.15$
SSTL-18 Class I, II	1.71	1.8	1.89	0.25	V_{CCIO}	$V_{CCIO}/2 - 0.175$	—	$V_{CCIO}/2 + 0.175$	0.5	V_{CCIO}	$V_{CCIO}/2 - 0.125$	—	$V_{CCIO}/2 + 0.125$
SSTL-15 Class I, II	1.425	1.5	1.575	0.2	—	—	$V_{CCIO}/2$	—	0.35	—	—	$V_{CCIO}/2$	—

Table 1-29 lists the differential SSTL I/O standards for Arria II GZ devices

Table 1-29. Differential SSTL I/O Standards for Arria II GZ Devices

I/O Standard	$V_{CCIO} (V)$			$V_{SWING(DC)} (V)$		$V_{X(AC)} (V)$			$V_{SWING(AC)} (V)$		$V_{OX(AC)} (V)$		
	Min	Typ	Max	Min	Max	Min	Typ	Max	Min	Max	Min	Typ	Max
SSTL-2 Class I, II	2.375	2.5	2.625	0.3	$V_{CCIO} + 0.6$	$V_{CCIO}/2 - 0.2$	—	$V_{CCIO}/2 + 0.2$	0.62	$V_{CCIO} + 0.6$	$V_{CCIO}/2 - 0.15$	—	$V_{CCIO}/2 + 0.15$
SSTL-18 Class I, II	1.71	1.8	1.89	0.25	$V_{CCIO} + 0.6$	$V_{CCIO}/2 - 0.175$	—	$V_{CCIO}/2 + 0.175$	0.5	$V_{CCIO} + 0.6$	$V_{CCIO}/2 - 0.125$	—	$V_{CCIO}/2 + 0.125$
SSTL-15 Class I, II	1.425	1.5	1.575	0.2	—	—	$V_{CCIO}/2$	—	0.35	—	—	$V_{CCIO}/2$	—

Table 1–34. Transceiver Specifications for Arria II GX Devices (Note 1) (Part 3 of 7)

Symbol/ Description	Condition	I3			C4			C5 and I5			C6			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
fixedclk clock frequency	PCIe Receiver Detect	—	125	—	—	125	—	—	125	—	—	125	—	MHz
reconfig_clk clock frequency	Dynamic reconfig. clock frequency	2.5/ 37.5 (4)	—	50	2.5/ 37.5 (4)	—	50	2.5/ 37.5 (4)	—	50	2.5/ 37.5 (4)	—	50	MHz
Delta time between reconfig_clks (5)	—	—	—	2	—	—	2	—	—	2	—	—	2	ms
Transceiver block minimum power-down pulse width	—	—	1	—	—	1	—	—	1	—	—	1	—	μs
Receiver														
Supported I/O Standards	1.4-V PCML, 1.5-V PCML, 2.5-V PCML, 2.5-V PCML, LVPECL, and LVDS													
Data rate (13)	—	600	—	6375	600	—	3750	600	—	3750	600	—	3125	Mbps
Absolute V _{MAX} for a receiver pin (6)	—	—	—	1.5	—	—	1.5	—	—	1.5	—	—	1.5	V
Absolute V _{MIN} for a receiver pin	—	-0.4	—	—	-0.4	—	—	-0.4	—	—	-0.4	—	—	V
Maximum peak-to-peak differential input voltage V _{ID} (diff p-p)	V _{ICM} = 0.82 V setting	—	—	2.7	—	—	2.7	—	—	2.7	—	—	2.7	V
	V _{ICM} = 1.1 V setting (7)	—	—	1.6	—	—	1.6	—	—	1.6	—	—	1.6	V

Table 1–34. Transceiver Specifications for Arria II GX Devices (Note 1) (Part 4 of 7)

Symbol/ Description	Condition	I3			C4			C5 and I5			C6			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Minimum peak-to-peak differential input voltage V_{ID} (diff p-p)	—	100	—	—	100	—	—	100	—	—	100	—	—	mV
V_{ICM}	$V_{ICM} = 0.82$ V setting	—	820	—	—	820	—	—	820	—	—	820	—	mV
	$V_{ICM} = 1.1$ V setting (7)	—	1100	—	—	1100	—	—	1100	—	—	1100	—	mV
Differential on-chip termination resistors	100- Ω setting	—	100	—	—	100	—	—	100	—	—	100	—	Ω
Return loss differential mode	PCIe				50 MHz to 1.25 GHz: –10dB									
	XAUI				100 MHz to 2.5 GHz: –10dB									
Return loss common mode	PCIe				50 MHz to 1.25 GHz: –6dB									
	XAUI				100 MHz to 2.5 GHz: –6dB									
Programmable PPM detector (8)	—	$\pm 62.5, 100, 125, 200, 250, 300, 500, 1000$												ppm
Run length	—	—	80	—	—	80	—	—	80	—	—	80	—	UI
Programmable equalization	—	—	—	7	—	—	7	—	—	7	—	—	7	dB
Signal detect/loss threshold	PCIe Mode	65	—	175	65	—	175	65	—	175	65	—	175	mV
CDR LTR time (9)	—	—	—	75	—	—	75	—	—	75	—	—	75	μ s
CDR minimum T1b (10)	—	15	—	—	15	—	—	15	—	—	15	—	—	μ s

Figure 1-1 shows the lock time parameters in manual mode.

 LTD = lock-to-data. LTR = lock-to-reference.

Figure 1-1. Lock Time Parameters for Manual Mode

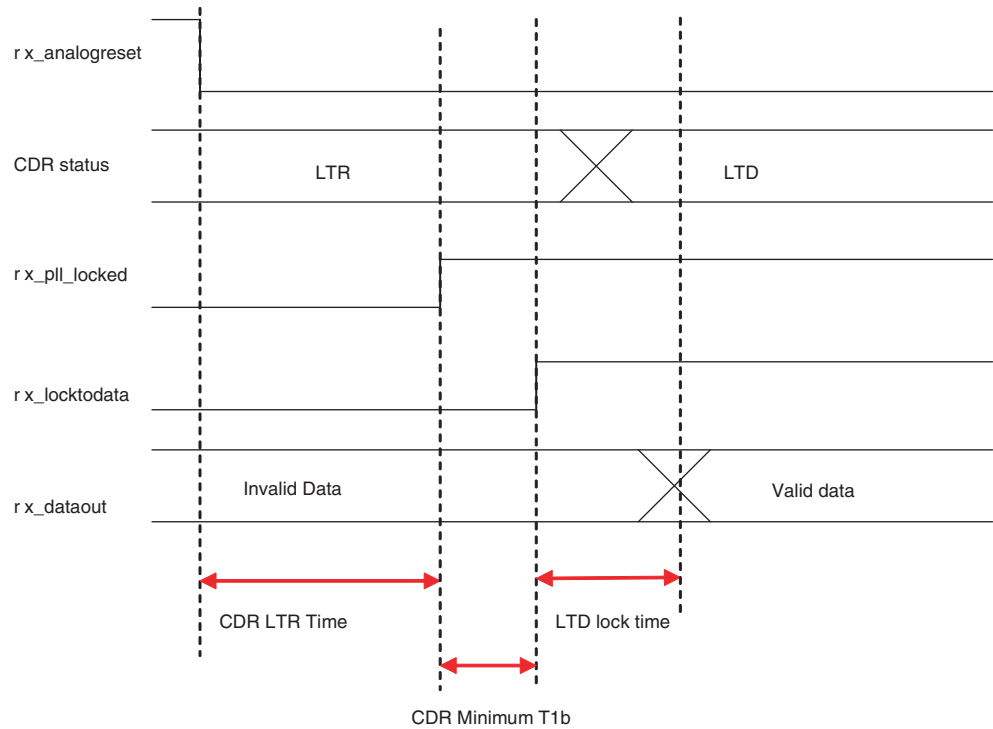


Figure 1-2 shows the lock time parameters in automatic mode.

Figure 1-2. Lock Time Parameters for Automatic Mode

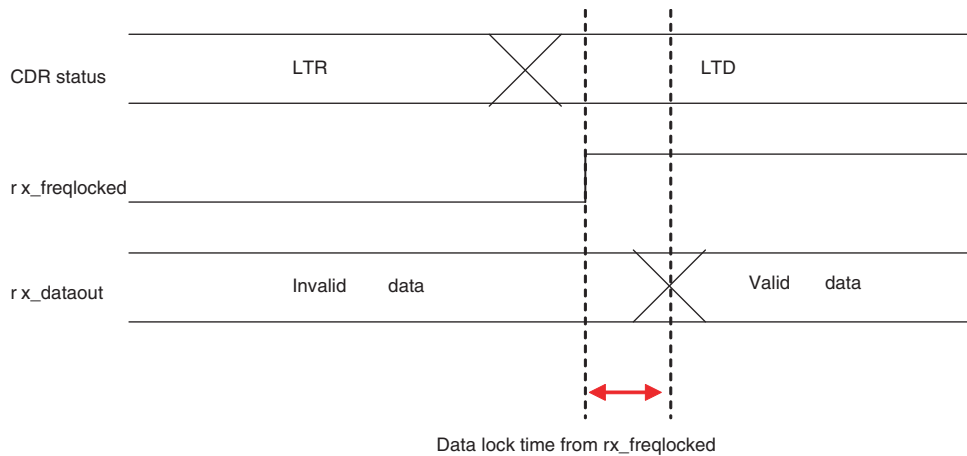


Table 1–40. Transceiver Block Jitter Specifications for Arria II GX Devices (Note 1) (Part 4 of 10)

Symbol/ Description	Conditions	I3			C4			C5, I5			C6			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Total jitter (peak-to-peak)	Pattern = CRPAT	—	—	0.27 9	—	—	0.279	—	—	0.279	—	—	0.279	UI
GIGE Receiver Jitter Tolerance (6)														
Deterministic jitter tolerance (peak-to-peak)	Pattern = CJPAT	> 0.4			> 0.4			> 0.4			> 0.4			UI
Combined deterministic and random jitter tolerance (peak-to-peak)	Pattern = CJPAT	> 0.66			> 0.66			> 0.66			> 0.66			UI
HiGig Transmit Jitter Generation (7)														
Deterministic jitter (peak-to-peak)	Data rate = 3.75 Gbps Pattern = CJPAT	—	—	0.17	—	—	0.17	—	—	—	—	—	—	UI
Total jitter (peak-to-peak)	Data rate = 3.75 Gbps Pattern = CJPAT	—	—	0.35	—	—	0.35	—	—	—	—	—	—	UI
HiGig Receiver Jitter Tolerance (7)														
Deterministic jitter tolerance (peak-to-peak)	Data rate = 3.75 Gbps Pattern = CJPAT	> 0.37			> 0.37			—	—	—	—	—	—	UI
Combined deterministic and random jitter tolerance (peak-to-peak)	Data rate = 3.75 Gbps Pattern = CJPAT	> 0.65			> 0.65			—	—	—	—	—	—	UI
Sinusoidal jitter tolerance (peak-to-peak)	Jitter frequency = 22.1 KHz Data rate = 3.75 Gbps Pattern = CJPAT	> 8.5			> 8.5			—	—	—	—	—	—	UI
	Jitter frequency = 1.875MHz Data rate = 3.75 Gbps Pattern = CJPAT	> 0.1			> 0.1			—	—	—	—	—	—	UI
	Jitter frequency = 20 MHz Data rate = 3.75 Gbps Pattern = CJPAT	> 0.1			> 0.1			—	—	—	—	—	—	UI

Table 1–40. Transceiver Block Jitter Specifications for Arria II GX Devices (Note 1) (Part 6 of 10)

Symbol/ Description	Conditions	I3			C4			C5, I5			C6			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Sinusoidal jitter tolerance (peak-to-peak)	Jitter frequency = 20 KHz Data rate = 1.485 Gbps (HD) Pattern = 75% color bar		> 1			> 1			> 1			> 1		UI
	Jitter frequency = 100 KHz Data rate = 1.485 Gbps (HD) Pattern = 75% color bar		> 0.2			> 0.2			> 0.2			> 0.2		UI
	Jitter frequency = 148.5 MHz Data rate = 1.485 Gbps (HD) Pattern = 75% color bar		> 0.2			> 0.2			> 0.2			> 0.2		UI
SATA Transmit Jitter Generation (10)														
Total jitter at 1.5 Gbps (G1)	Compliance pattern	—	—	0.55	—	—	0.55	—	—	0.55	—	—	0.55	UI
Deterministic jitter at 1.5 Gbps (G1)	Compliance pattern	—	—	0.35	—	—	0.35	—	—	0.35	—	—	0.35	UI
Total jitter at 3.0 Gbps (G2)	Compliance pattern	—	—	0.55	—	—	0.55	—	—	0.55	—	—	0.55	UI
Deterministic jitter at 3.0 Gbps (G2)	Compliance pattern	—	—	0.35	—	—	0.35	—	—	0.35	—	—	0.35	UI
Total jitter at 6.0 Gbps (G3)	Compliance pattern	—	—	0.52	—	—	—	—	—	—	—	—	—	UI
Random jitter at 6.0 Gbps (G3)	Compliance pattern	—	—	0.18	—	—	—	—	—	—	—	—	—	UI
SATA Receiver Jitter Tolerance (10)														
Total jitter tolerance at 1.5 Gbps (G1)	Compliance pattern		> 0.65			> 0.65			> 0.65			> 0.65		UI
Deterministic jitter tolerance at 1.5 Gbps (G1)	Compliance pattern		> 0.35			> 0.35			> 0.35			> 0.35		UI
SSC modulation frequency at 1.5 Gbps (G1)	Compliance pattern		33			33			33			33		kHz

Table 1-40. Transceiver Block Jitter Specifications for Arria II GX Devices (Note 1) (Part 9 of 10)

Symbol/ Description	Conditions	I3			C4			C5, I5			C6			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
OBSAI Receiver Jitter Tolerance (12)														
Deterministic jitter tolerance at 768 Mbps, 1536 Mbps, and 3072 Mbps	Pattern = CJPAT	> 0.37			> 0.37			> 0.37			> 0.37			UI
Combined deterministic and random jitter tolerance at 768 Mbps, 1536 Mbps, and 3072 Mbps	Pattern = CJPAT	> 0.55			> 0.55			> 0.55			> 0.55			UI
Sinusoidal jitter tolerance at 768 Mbps	Jitter frequency = 5.4 KHz Pattern = CJPAT	> 8.5			> 8.5			> 8.5			> 8.5			UI
	Jitter frequency = 460.8 KHz to 20 MHz Pattern = CJPAT	> 0.1			> 0.1			> 0.1			> 0.1			UI
Sinusoidal jitter tolerance at 1536 Mbps	Jitter frequency = 10.9 KHz Pattern = CJPAT	> 8.5			> 8.5			> 8.5			> 8.5			UI
	Jitter frequency = 921.6 KHz to 20 MHz Pattern = CJPAT	> 0.1			> 0.1			> 0.1			> 0.1			UI

Table 1–41. Transceiver Block Jitter Specifications for Arria II GZ Devices (Note 1), (2) (Part 2 of 7)

Symbol/ Description	Conditions	–C3 and –I3			–C4 and –I4			Unit
		Min	Typ	Max	Min	Typ	Max	
Jitter tolerance at 2488.32 Mbps	Jitter frequency = 0.06 KHz Pattern = PRBS15	> 15			> 15			UI
	Jitter frequency = 100 KHZ Pattern = PRBS15	> 1.5			> 1.5			UI
	Jitter frequency = 1 MHz Pattern = PRBS15	> 0.15			> 0.15			UI
	Jitter frequency = 10 MHz Pattern = PRBS15	> 0.15			> 0.15			UI
Fibre Channel Transmit Jitter Generation (4), (5)								
Total jitter FC-1	Pattern = CRPAT	—	—	0.23	—	—	0.23	UI
Deterministic jitter FC-1	Pattern = CRPAT	—	—	0.11	—	—	0.11	UI
Total jitter FC-2	Pattern = CRPAT	—	—	0.33	—	—	0.33	UI
Deterministic jitter FC-2	Pattern = CRPAT	—	—	0.2	—	—	0.2	UI
Total jitter FC-4	Pattern = CRPAT	—	—	0.52	—	—	0.52	UI
Deterministic jitter FC-4	Pattern = CRPAT	—	—	0.33	—	—	0.33	UI
Fibre Channel Receiver Jitter Tolerance (4), (6)								
Deterministic jitter FC-1	Pattern = CJTPAT	> 0.37			> 0.37			UI
Random jitter FC-1	Pattern = CJTPAT	> 0.31			> 0.31			UI
Sinusoidal jitter FC-1	Fc/25000	> 1.5			> 1.5			UI
	Fc/1667	> 0.1			> 0.1			UI
Deterministic jitter FC-2	Pattern = CJTPAT	> 0.33			> 0.33			UI
Random jitter FC-2	Pattern = CJTPAT	> 0.29			> 0.29			UI
Sinusoidal jitter FC-2	Fc/25000	> 1.5			> 1.5			UI
	Fc/1667	> 0.1			> 0.1			UI
Deterministic jitter FC-4	Pattern = CJTPAT	> 0.33			> 0.33			UI
Random jitter FC-4	Pattern = CJTPAT	> 0.29			> 0.29			UI
Sinusoidal jitter FC-4	Fc/25000	> 1.5			> 1.5			UI
	Fc/1667	> 0.1			> 0.1			UI
XAUI Transmit Jitter Generation (7)								
Total jitter at 3.125 Gbps	Pattern = CJPAT	—	—	0.3	—	—	0.3	UI
Deterministic jitter at 3.125 Gbps	Pattern = CJPAT	—	—	0.17	—	—	0.17	UI
XAUI Receiver Jitter Tolerance (7)								
Total jitter	—	> 0.65			> 0.65			UI
Deterministic jitter	—	> 0.37			> 0.37			UI

Table 1-41. Transceiver Block Jitter Specifications for Arria II GZ Devices (Note 1), (2) (Part 4 of 7)

Symbol/ Description	Conditions	–C3 and –I3			–C4 and –I4			Unit
		Min	Typ	Max	Min	Typ	Max	
GIGE Receiver Jitter Tolerance (11)								
Deterministic jitter tolerance (peak-to-peak)	Pattern = CJPAT	> 0.4			> 0.4			UI
Combined deterministic and random jitter tolerance (peak-to-peak)	Pattern = CJPAT	> 0.66			> 0.66			UI
HiGig Transmit Jitter Generation								
Deterministic jitter (peak-to-peak)	Data rate = 3.75 Gbps Pattern = CJPAT	—	—	0.17	—	—	—	UI
Total jitter (peak-to-peak)	Data rate = 3.75 Gbps Pattern = CJPAT	—	—	0.35	—	—	—	UI
HiGig Receiver Jitter Tolerance								
Deterministic jitter tolerance (peak-to-peak)	Data rate = 3.75 Gbps Pattern = CJPAT	> 0.37			—	—	—	UI
Combined deterministic and random jitter tolerance (peak-to-peak)	Data rate = 3.75 Gbps Pattern = CJPAT	> 0.65			—	—	—	UI
Sinusoidal jitter tolerance (peak-to-peak)	Jitter frequency = 22.1 KHz Data rate = 3.75 Gbps Pattern = CJPAT	> 8.5			—	—	—	UI
	Jitter frequency = 22.1 KHz Data rate = 3.75 Gbps Pattern = CJPAT	> 0.1			—	—	—	UI
	Jitter frequency = 22.1 KHz Data rate = 3.75 Gbps Pattern = CJPAT	> 0.1			—	—	—	UI
(OIF) CEI Transmitter Jitter Generation								
Total jitter (peak-to-peak)	Data rate = 6.375 Gbps Pattern = PRBS15 BER = 10 ⁻¹²	—	—	0.3	—	—	0.3	UI
(OIF) CEI Receiver Jitter Tolerance								
Deterministic jitter tolerance (peak-to-peak)	Data rate = 6.375 Gbps Pattern = PRBS31 BER = 10 ⁻¹²	> 0.675			—	—	—	UI
Combined deterministic and random jitter tolerance (peak-to-peak)	Data rate = 6.375 Gbps Pattern = PRBS31 BER = 10 ⁻¹²	> 0.988			—	—	—	UI

Table 1–41. Transceiver Block Jitter Specifications for Arria II GZ Devices (Note 1), (2) (Part 7 of 7)

Symbol/ Description	Conditions	–C3 and –I3			–C4 and –I4			Unit
		Min	Typ	Max	Min	Typ	Max	
OBSAI Receiver Jitter Tolerance (15)								
Deterministic jitter tolerance at 768 Mbps, 1536 Mbps, and 3072 Mbps	Pattern = CJPAT	> 0.37			> 0.37			UI
Combined deterministic and random jitter tolerance at 768 Mbps, 1536 Mbps, and 3072 Mbps	Pattern = CJPAT	> 0.55			> 0.55			UI
Sinusoidal jitter tolerance at 768 Mbps	Jitter frequency = 5.4 KHz Pattern = CJPAT	> 8.5			> 8.5			UI
	Jitter frequency = 460 MHz to 20 MHz Pattern = CJPAT	> 0.1			> 0.1			UI
Sinusoidal jitter tolerance at 1536 Mbps	Jitter frequency = 10.9 KHz Pattern = CJPAT	> 8.5			> 8.5			UI
	Jitter frequency = 921.6 MHz to 20 MHz Pattern = CJPAT	> 0.1			> 0.1			UI
Sinusoidal jitter tolerance at 3072 Mbps	Jitter frequency = 21.8 KHz Pattern = CJPAT	> 8.5			> 8.5			UI
	Jitter frequency = 1843.2 MHz to 20 MHz Pattern = CJPAT	> 0.1			> 0.1			UI

Notes to Table 1–41:

- (1) Dedicated `refclk` pins were used to drive the input reference clocks.
- (2) The jitter numbers are valid for the stated conditions only.
- (3) The jitter numbers for SONET/SDH are compliant to the GR-253-CORE Issue 3 Specification.
- (4) The jitter numbers for Fibre Channel are compliant to the FC-P1-4 Specification revision 6.10.
- (5) The Fibre Channel transmitter jitter generation numbers are compliant to the specification at the δ_T inter operability point.
- (6) The Fibre Channel receiver jitter tolerance numbers are compliant to the specification at the δ_R interpretability point.
- (7) The jitter numbers for XAUI are compliant to the IEEE802.3ae-2002 Specification.
- (8) The jitter numbers for PCIe are compliant to the PCIe Base Specification 2.0.
- (9) Arria II GZ PCIe receivers are compliant to this specification provided the $V_{TX-CM-DC-ACTIVEIDLE-DELTA}$ of the upstream transmitter is less than 50 mV.
- (10) The jitter numbers for SRIO are compliant to the RapidIO Specification 1.3.
- (11) The jitter numbers for GIGE are compliant to the IEEE802.3-2002 Specification.
- (12) The HD-SDI and 3G-SDI jitter numbers are compliant to the SMPTE292M and SMPTE424M Specifications.
- (13) The jitter numbers for Serial Attached SCSI (SAS) are compliant to the SAS-2.1 Specification.
- (14) The jitter numbers for CPRI are compliant to the CPRI Specification V3.0.
- (15) The jitter numbers for OBSAI are compliant to the OBSAI RP3 Specification V4.1.

Table 1–44. PLL Specifications for Arria II GX Devices (Part 2 of 3)

Symbol	Description	Min	Typ	Max	Unit
f_{OUT}	Output frequency for internal global or regional clock (–4 Speed Grade)	—	—	500	MHz
	Output frequency for internal global or regional clock (–5 Speed Grade)	—	—	500	MHz
	Output frequency for internal global or regional clock (–6 Speed Grade)	—	—	400	MHz
f_{OUT_EXT}	Output frequency for external clock output (–4 Speed Grade)	—	—	670 (5)	MHz
	Output frequency for external clock output (–5 Speed Grade)	—	—	622 (5)	MHz
	Output frequency for external clock output (–6 Speed Grade)	—	—	500 (5)	MHz
$t_{OUTDUTY}$	Duty cycle for external clock output (when set to 50%)	45	50	55	%
t_{OUTPJ_DC}	Dedicated clock output period jitter ($f_{OUT} \geq 100$ MHz)	—	—	300	ps (p–p)
	Dedicated clock output period jitter ($f_{OUT} < 100$ MHz)	—	—	30	mUI (p–p)
t_{OUTCCJ_DC}	Dedicated clock output cycle-to-cycle jitter ($f_{OUT} \geq 100$ MHz)	—	—	300	ps (p–p)
	Dedicated clock output cycle-to-cycle jitter ($f_{OUT} < 100$ MHz)	—	—	30	mUI (p–p)
f_{OUTPJ_IO}	Regular I/O clock output period jitter ($f_{OUT} \geq 100$ MHz)	—	—	650	ps (p–p)
	Regular I/O clock output period jitter ($f_{OUT} < 100$ MHz)	—	—	65	mUI (p–p)
f_{OUTCCJ_IO}	Regular I/O clock output cycle-to-cycle jitter ($f_{OUT} \geq 100$ MHz)	—	—	650	ps (p–p)
	Regular I/O clock output cycle-to-cycle jitter ($f_{OUT} < 100$ MHz)	—	—	65	mUI (p–p)
$t_{CONFIGPLL}$	Time required to reconfigure PLL scan chains	—	3.5	—	SCANCLK cycles
$t_{CONFIGPHASE}$	Time required to reconfigure phase shift	—	1	—	SCANCLK cycles
$f_{SCANCLK}$	SCANCLK frequency	—	—	100	MHz
t_{LOCK}	Time required to lock from end of device configuration	—	—	1	ms
t_{DLOCK}	Time required to lock dynamically (after switchover or reconfiguring any non-post-scale counters/delays)	—	—	1	ms
$f_{CL\ BW}$	PLL closed-loop low bandwidth	—	0.3	—	MHz
	PLL closed-loop medium bandwidth	—	1.5	—	MHz
	PLL closed-loop high bandwidth	—	4	—	MHz
t_{PLL_PSERR}	Accuracy of PLL phase shift	—	—	±50	ps
t_{ARESET}	Minimum pulse width on areset signal	10	—	—	ns

Table 1-44. PLL Specifications for Arria II GX Devices (Part 3 of 3)

Symbol	Description	Min	Typ	Max	Unit
$t_{CASC_OUTJITTER_PERIOD_DEDCLK}$ (6), (7)	Period jitter for dedicated clock output in cascaded PLLs ($F_{OUT} \geq 100$ MHz)	—	—	425	ps (p-p)
	Period jitter for dedicated clock output in cascaded PLLs ($F_{OUT} \leq 100$ MHz)	—	—	42.5	mUI (p-p)

Notes to Table 1-44:

- (1) f_{IN} is limited by the I/O f_{MAX} .
- (2) The VCO frequency reported by the Quartus II software in the PLL summary section of the compilation report takes into consideration the VCO post-scale counter K value. Therefore, if the counter K has a value of 2, the frequency reported can be lower than the f_{VCO} specification.
- (3) A high-input jitter directly affects the PLL output jitter. To have low PLL output clock jitter, you must provide a clean-clock source, which is less than 200 ps.
- (4) F_{REF} is f_{IN}/N when $N = 1$.
- (5) This specification is limited by the lower of the two: I/O f_{MAX} or f_{OUT} of the PLL.
- (6) Peak-to-peak jitter with a probability level of 10^{-12} (14 sigma, 99.999999974404% confidence level). The output jitter specification applies to the intrinsic jitter of the PLL, when an input jitter of 30 ps is applied. The external memory interface clock output jitter specifications use a different measurement method and are available in Table 1-62 on page 1-70.
- (7) The cascaded PLL specification is only applicable with the following condition:
 - a. Upstream PLL: $0.59 \text{ MHz} \leq \text{Upstream PLL BW} < 1 \text{ MHz}$
 - b. Downstream PLL: $\text{Downstream PLL BW} > 2 \text{ MHz}$

Table 1-45 lists the PLL specifications for Arria II GZ devices when operating in both the commercial junction temperature range (0° to 85°C) and the industrial junction temperature range (-40° to 100°C).

Table 1-45. PLL Specifications for Arria II GZ Devices (Part 1 of 2)

Symbol	Parameter	Min	Typ	Max	Unit
f_{IN}	Input clock frequency (-3 speed grade)	5	—	717 (1)	MHz
	Input clock frequency (-4 speed grade)	5	—	717 (1)	MHz
f_{INPFD}	Input frequency to the PFD	5	—	325	MHz
f_{VCO}	PLL VCO operating range (-3 speed grade)	600	—	1,300	MHz
	PLL VCO operating range (-4 speed grade)	600	—	1,300	MHz
$t_{EINDUTY}$	Input clock or external feedback clock input duty cycle	40	—	60	%
f_{OUT}	Output frequency for internal global or regional clock (-3 speed grade)	—	—	700 (2)	MHz
	Output frequency for internal global or regional clock (-4 speed grade)	—	—	500 (2)	MHz
f_{OUT_EXT}	Output frequency for external clock output (-3 speed grade)	—	—	717 (2)	MHz
	Output frequency for external clock output (-4 speed grade)	—	—	717 (2)	MHz
$t_{OUTDUTY}$	Duty cycle for external clock output (when set to 50%)	45	50	55	%
t_{FCOMP}	External feedback clock compensation time	—	—	10	ns
$t_{CONFIGPLL}$	Time required to reconfigure scan chain	—	3.5	—	scanclk cycles
$t_{CONFIGPHASE}$	Time required to reconfigure phase shift	—	1	—	scanclk cycles
$f_{SCANCLK}$	scanclk frequency	—	—	100	MHz
t_{LOCK}	Time required to lock from end-of-device configuration or de-assertion of areset	—	—	1	ms

Table 1-53. High-Speed I/O Specifications for Arria II GX Devices (Part 3 of 4)

Symbol	Conditions	I3		C4		C5,I5		C6		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{TX_JITTER} (4)	True LVDS with dedicated SERDES (data rate 600–1,250 Mbps)	—	175	—	175	—	225	—	300	ps
	True LVDS with dedicated SERDES (data rate < 600 Mbps)	—	0.105	—	0.105	—	0.135	—	0.18	UI
	True LVDS and emulated LVDS_E_3R with logic elements as SERDES (data rate 600 – 945 Mbps)	—	260	—	260	—	300	—	350	ps
	True LVDS and emulated LVDS_E_3R with logic elements as SERDES (data rate < 600 Mbps)	—	0.16	—	0.16	—	0.18	—	0.21	UI
t_{TX_DCD}	True LVDS and emulated LVDS_E_3R	45	55	45	55	45	55	45	55	%
t_{RISE} and t_{FALL}	True LVDS and emulated LVDS_E_3R	—	200	—	200	—	225	—	250	ps
TCCS	True LVDS (5)	—	150	—	150	—	175	—	200	ps
	Emulated LVDS_E_3R	—	200	—	200	—	250	—	300	ps
Receiver (6)										
True differential I/O standards - f_{HSDRPA} (data rate)	SERDES factor J = 3 to 10	150	1250	150	1250	150	1050	150	840	Mbps

Table 1-54. High-Speed I/O Specifications for Arria II GZ Devices (Note 1), (2), (10) (Part 2 of 3)

Symbol	Conditions	C3, I3			C4, I4			Unit
		Min	Typ	Max	Min	Typ	Max	
$f_{\text{HCLK_OUT}}$ (output clock frequency)	—	5	—	717 (7)	5	—	717 (7)	MHz
Transmitter								
f_{HSDR} (true LVDS output data rate)	SERDES factor, J = 3 to 10 (using dedicated SERDES) (8)	(4)	—	1250	(4)	—	1250	Mbps
	SERDES factor J = 2, (using DDR registers)	(4)	—	(5)	(4)	—	(5)	Mbps
	SERDES factor J = 1, (uses an SDR register)	(4)	—	(5)	(4)	—	(5)	Mbps
f_{HSDR} (emulated LVDS_E_3R output data rate) (5)	SERDES factor J = 4 to 10	(4)	—	1152	(4)	—	800	Mbps
f_{HSDR} (emulated LVDS_E_1R output data rate)		(4)	—	200	(4)	—	200	Mbps
$t_{\text{x Jitter}}$	Total jitter for data rate, 600 Mbps to 1.6 Gbps	—	—	160	—	—	160	ps
	Total jitter for data rate, < 600 Mbps	—	—	0.1	—	—	0.1	UI
$t_{\text{x Jitter}}$ - emulated differential I/O standards with three external output resistor network	Total jitter for data rate, 600 Mbps to 1.25 Gbps	—	—	300	—	—	325	ps
	Total jitter for data rate < 600 Mbps	—	—	0.2	—	—	0.25	UI
$t_{\text{x Jitter}}$ - emulated differential I/O standards with one external output resistor network	—	—	—	0.15	—	—	0.15	UI
t_{DUTY}	TX output clock duty cycle for both True and emulated differential I/O standards	45	50	55	45	50	55	%

Figure 1-6 shows the LVDS soft-CDR/DPA sinusoidal jitter tolerance specification for Arria II GZ devices at 1.25 Gbps data rate.

Figure 1-6. LVDS Soft-CDR/DPA Sinusoidal Jitter Tolerance Specification for Arria II GZ Devices at a 1.25 Gbps Data Rate

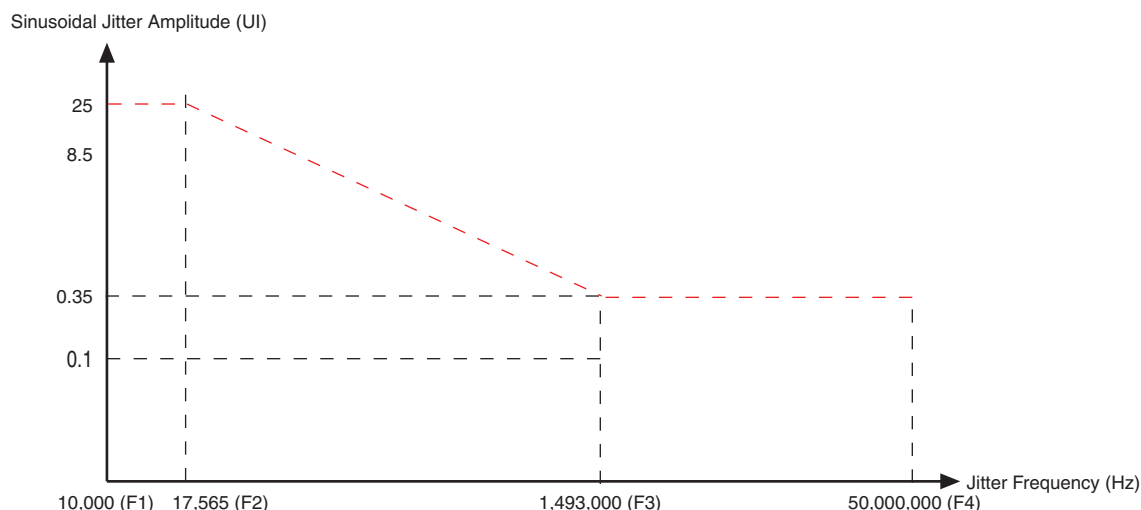


Table 1-56 lists the LVDS soft-CDR/DPA sinusoidal jitter tolerance specification for Arria II GZ devices at 1.25 Gbps data rate.

Table 1-56. LVDS Soft-CDR/DPA Sinusoidal Jitter Mask Values for Arria II GZ Devices at 1.25 Gbps Data Rate

Jitter Frequency (Hz)		Sinusoidal Jitter (UI)
F1	10,000	25.000
F2	17,565	25.000
F3	1,493,000	0.350
F4	50,000,000	0.350

External Memory Interface Specifications

 For the maximum clock rate supported for Arria II GX and GZ device family, refer to the [External Memory Interface Spec Estimator](#) page on the Altera website.

Table 1-57 lists the external memory interface specifications for Arria II GX devices.

Table 1-57. External Memory Interface Specifications for Arria II GX Devices (Part 1 of 2)

Frequency Mode	Frequency Range (MHz)			Resolution (°)	DQS Delay Buffer Mode ⁽¹⁾	Number of Delay Chains
	C4	I3, C5, I5	C6			
0	90-140	90-130	90-110	22.5	Low	16
1	110-180	110-170	110-150	30	Low	12
2	140-220	140-210	140-180	36	Low	10
3	170-270	170-260	170-220	45	Low	8
4	220-340	220-310	220-270	30	High	12

Table 1-57. External Memory Interface Specifications for Arria II GX Devices (Part 2 of 2)

Frequency Mode	Frequency Range (MHz)			Resolution (°)	DQS Delay Buffer Mode (1)	Number of Delay Chains
	C4	I3, C5, I5	C6			
5	270-410	270-380	270-320	36	High	10
6	320-450	320-410	320-370	45	High	8

Note to Table 1-57:

(1) Low indicates a 6-bit DQS delay setting; high indicates a 5-bit DQS delay setting.

Table 1-58 lists the DLL frequency range specifications for Arria II GZ devices.

Table 1-58. DLL Frequency Range Specifications for Arria II GZ Devices

Frequency Mode	Frequency Range (MHz)		Available Phase Shift	DQS Delay Buffer Mode (1)	Number of Delay Chains
	-3	-4			
0	90-130	90-120	22.5°, 45°, 67.5°, 90°	Low	16
1	120-170	120-160	30°, 60°, 90°, 120°	Low	12
2	150-210	150-200	36°, 72°, 108°, 144°	Low	10
3	180-260	180-240	45°, 90°, 135°, 180°	Low	8
4	240-320	240-290	30°, 60°, 90°, 120°	High	12
5	290-380	290-360	36°, 72°, 108°, 144°	High	10
6	360-450	360-450	45°, 90°, 135°, 180°	High	8
7	470-630	470-590	60°, 120°, 180°, 240°	High	6

Note to Table 1-58:

(1) Low indicates a 6-bit DQS delay setting; high indicates a 5-bit DQS delay setting.

Table 1-59 lists the DQS phase offset delay per stage for Arria II GX devices.

Table 1-59. DQS Phase Offset Delay Per Setting for Arria II GX Devices (Note 1), (2), (3)

Speed Grade	Min	Max	Unit
C4	7.0	13.0	ps
I3, C5, I5	7.0	15.0	ps
C6	8.5	18.0	ps

Notes to Table 1-59:

- (1) The valid settings for phase offset are -64 to +63 for frequency modes 0 to 3 and -32 to +31 for frequency modes 4 to 5.
- (2) The typical value equals the average of the minimum and maximum values.
- (3) The delay settings are linear.

Table 1-63 lists the memory output clock jitter specifications for Arria II GZ devices.

Table 1-63. Memory Output Clock Jitter Specification for Arria II GZ Devices (Note 1), (2), (3)

Parameter	Clock Network	Symbol	-3		-4		Unit
			Min	Max	Min	Max	
Clock period jitter	Regional	$t_{JIT(per)}$	-55	55	-55	55	ps
Cycle-to-cycle period jitter	Regional	$t_{JIT(cc)}$	-110	110	-110	110	ps
Duty cycle jitter	Regional	$t_{JIT(duty)}$	-82.5	82.5	-82.5	82.5	ps
Clock period jitter	Global	$t_{JIT(per)}$	-82.5	82.5	-82.5	82.5	ps
Cycle-to-cycle period jitter	Global	$t_{JIT(cc)}$	-165	165	-165	165	ps
Duty cycle jitter	Global	$t_{JIT(duty)}$	-90	90	-90	90	ps

Notes to Table 1-63:

- (1) The memory output clock jitter measurements are for 200 consecutive clock cycles, as specified in the JEDEC DDR2/DDR3 SDRAM standard.
- (2) The clock jitter specification applies to memory output clock pins generated using differential signal-splitter and DDIO circuits clocked by a PLL output routed on a regional or global clock network as specified. Altera recommends using regional clock networks whenever possible.
- (3) The memory output clock jitter stated in Table 1-63 is applicable when an input jitter of 30 ps is applied.

Duty Cycle Distortion (DCD) Specifications

Table 1-64 lists the worst-case DCD specifications for Arria II GX devices.

Table 1-64. Duty Cycle Distortion on I/O Pins for Arria II GX Devices (Note 1)

Symbol	C4		I3, C5, I5		C6		Unit
	Min	Max	Min	Max	Min	Max	
Output Duty Cycle	45	55	45	55	45	55	%

Note to Table 1-64:

- (1) The DCD specification applies to clock outputs from the PLL, global clock tree, IOE driving dedicated, and general purpose I/O pins.

Table 1-65 lists the worst-case DCD specifications for Arria II GZ devices.

Table 1-65. Duty Cycle Distortion on I/O Pins for Arria II GZ Devices (Note 1)

Symbol	C3, I3		C4, I4		Unit
	Min	Max	Min	Max	
Output Duty Cycle	45	55	45	55	%

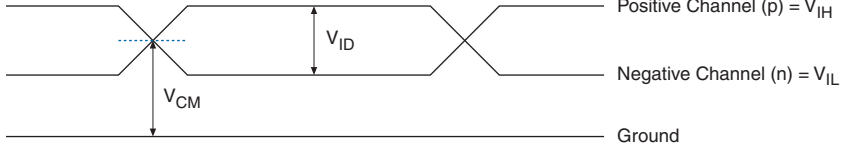
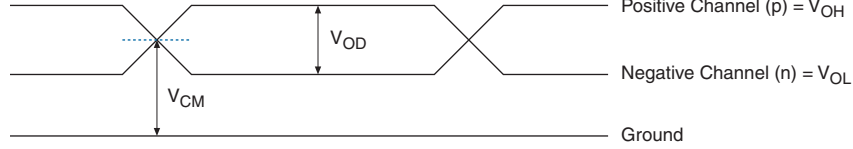
Note to Table 1-65:

- (1) The DCD specification applies to clock outputs from the PLL, global clock tree, IOE driving dedicated, and general purpose I/O pins.

Glossary

Table 1-68 lists the glossary for this chapter.

Table 1-68. Glossary (Part 1 of 4)

Letter	Subject	Definitions
A, B, C, D	Differential I/O Standards	<i>Receiver Input Waveforms</i> Single-Ended Waveform  Positive Channel (p) = V_{IH} Negative Channel (n) = V_{IL} Ground Differential Waveform  <i>Transmitter Output Waveforms</i> Single-Ended Waveform  Positive Channel (p) = V_{OH} Negative Channel (n) = V_{OL} Ground Differential Waveform 
E, F	f_{HSCLK}	Left/Right PLL input clock frequency.
	f_{HSDR}	High-speed I/O block: Maximum/minimum LVDS data transfer rate ($f_{HSDR} = 1/TUI$), non-DPA.
	f_{HSRDPA}	High-speed I/O block: Maximum/minimum LVDS data transfer rate ($f_{HSRDPA} = 1/TUI$), DPA.