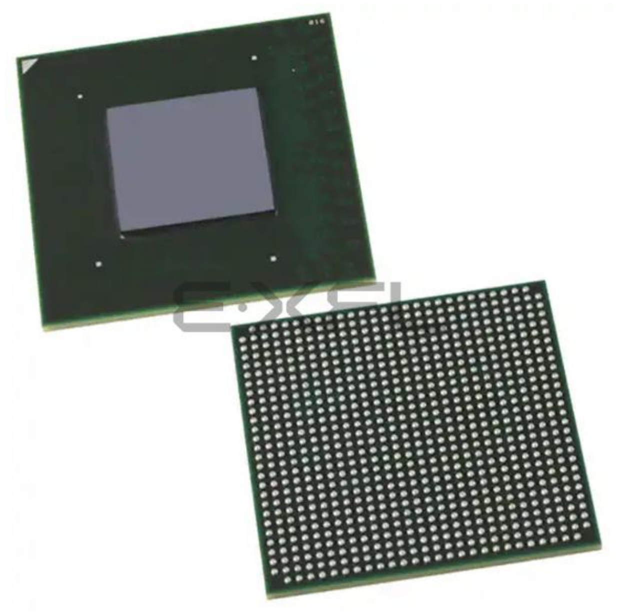
# Intel - EP2AGX65DF29C6 Datasheet



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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | 2530 |
| Number of Logic Elements/Cells | 60214 |
| Total RAM Bits | 5371904 |
| Number of I/O | 364 |
| Number of Gates | - |
| Voltage - Supply | 0.87V ~ 0.93V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 85°C (TJ) |
| Package / Case | 780-BBGA, FCBGA |
| Supplier Device Package | 780-FBGA (29x29) |
| Purchase URL | https://www.e-xfl.com/product-detail/intel/ep2agx65df29c6 |

**Table 1–3. Maximum Allowed Overshoot During Transitions for Arria II Devices**

| Symbol | Description | Condition (V) | Overshoot Duration as % of High Time | Unit |
|---|---|---|---|---|
| $V_I$ (AC) | AC Input Voltage | 4.0 | 100.000 | % |
| | | 4.05 | 79.330 | % |
| | | 4.1 | 46.270 | % |
| | | 4.15 | 27.030 | % |
| | | 4.2 | 15.800 | % |
| | | 4.25 | 9.240 | % |
| | | 4.3 | 5.410 | % |
| | | 4.35 | 3.160 | % |
| | | 4.4 | 1.850 | % |
| | | 4.45 | 1.080 | % |
| | | 4.5 | 0.630 | % |
| | | 4.55 | 0.370 | % |
| | | 4.6 | 0.220 | % |

## Maximum Allowed I/O Operating Frequency

Table 1–4 lists the maximum allowed I/O operating frequency for Arria II GX I/Os using the specified I/O standards to ensure device reliability.

**Table 1–4. Maximum Allowed I/O Operating Frequency for Arria II GX Devices**

| I/O Standard | I/O Frequency (MHz) |
|---|---|
| HSTL-18 and HSTL-15 | 333 |
| SSTL -15 | 400 |
| SSTL-18 | 333 |
| 2.5-V LVCMOS | 260 |
| 3.3-V and 3.0-V LVTTL | 250 |
| 3.3-V, 3.0-V, 1.8-V, and 1.5-V LVCMOS | |
| PCI and PCI-X | |
| SSTL-2 | |
| 1.2-V LVCMOS HSTL-12 | 200 |

**Table 1–5. Recommended Operating Conditions for Arria II GX Devices *(Note 1)* (Part 2 of 2)**

| Symbol | Description | Condition | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|---|
| $t_{RAMP}$ | Power Supply Ramp time | Normal POR | 0.05 | — | 100 | ms |
| | | Fast POR | 0.05 | — | 4 | ms |

**Notes to Table 1–5:**

(1) For more information about supply pin connections, refer to the *Arria II Device Family Pin Connection Guidelines*.

(2) Altera recommends a 3.0-V nominal battery voltage when connecting $V_{CCBAT}$ to a battery for volatile key backup. If you do not use the volatile security key, you may connect the $V_{CCBAT}$ to either GND or a 3.0-V power supply.

(3) $V_{CCPD}$ must be 2.5-V for I/O banks with 2.5-V and lower $V_{CCIO}$, 3.0-V for 3.0-V $V_{CCIO}$, and 3.3-V for 3.3-V $V_{CCIO}$.

(4) $V_{CCIO}$ for 3C and 8C I/O banks where the configuration pins reside only supports 3.3-, 3.0-, 2.5-, or 1.8-V voltage levels.

Table 1–6 lists the recommended operating conditions for Arria II GZ devices.

**Table 1–6. Recommended Operating Conditions for Arria II GZ Devices *(Note 6)* (Part 1 of 2)**

| Symbol | Description | Condition | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Core voltage and periphery circuitry power supply | — | 0.87 | 0.90 | 0.93 | V |
| $V_{CCCB}$ | Supplies power for the configuration RAM bits | — | 1.45 | 1.50 | 1.55 | V |
| $V_{CCAUX}$ | Auxiliary supply | — | 2.375 | 2.5 | 2.625 | V |
| $V_{CCPD}$ *(2)* | I/O pre-driver (3.0 V) power supply | — | 2.85 | 3.0 | 3.15 | V |
| | I/O pre-driver (2.5 V) power supply | — | 2.375 | 2.5 | 2.625 | V |
| $V_{CCIO}$ | I/O buffers (3.0 V) power supply | — | 2.85 | 3.0 | 3.15 | V |
| | I/O buffers (2.5 V) power supply | — | 2.375 | 2.5 | 2.625 | V |
| | I/O buffers (1.8 V) power supply | — | 1.71 | 1.8 | 1.89 | V |
| | I/O buffers (1.5 V) power supply | — | 1.425 | 1.5 | 1.575 | V |
| | I/O buffers (1.2 V) power supply | — | 1.14 | 1.2 | 1.26 | V |
| $V_{CCPGM}$ | Configuration pins (3.0 V) power supply | — | 2.85 | 3.0 | 3.15 | V |
| | Configuration pins (2.5 V) power supply | — | 2.375 | 2.5 | 2.625 | V |
| | Configuration pins (1.8 V) power supply | — | 1.71 | 1.8 | 1.89 | V |
| $V_{CCA\_PLL}$ | PLL analog voltage regulator power supply | — | 2.375 | 2.5 | 2.625 | V |
| $V_{CCD\_PLL}$ | PLL digital voltage regulator power supply | — | 0.87 | 0.90 | 0.93 | V |
| $V_{CC\_CLKIN}$ | Differential clock input power supply | — | 2.375 | 2.5 | 2.625 | V |
| $V_{CCBAT}$ *(1)* | Battery back-up power supply (For design security volatile key register) | — | 1.2 | — | 3.3 | V |
| $V_I$ | DC input voltage | — | –0.5 | — | 3.6 | V |
| $V_O$ | Output voltage | — | 0 | — | $V_{CCIO}$ | V |
| $V_{CCA\_L}$ | Transceiver high voltage power (left side) | — | 2.85/2.375 | 3.0/2.5 *(4)* | 3.15/2.625 | V |
| $V_{CCA\_R}$ | Transceiver high voltage power (right side) | — | | | | |
| $V_{CCHIP\_L}$ | Transceiver HIP digital power (left side) | — | 0.87 | 0.9 | 0.93 | V |
| $V_{CCR\_L}$ | Receiver power (left side) | — | 1.05 | 1.1 | 1.15 | V |
| $V_{CCR\_R}$ | Receiver power (right side) | — | 1.05 | 1.1 | 1.15 | V |
| $V_{CCT\_L}$ | Transmitter power (left side) | — | 1.05 | 1.1 | 1.15 | V |
| $V_{CCT\_R}$ | Transmitter power (right side) | — | 1.05 | 1.1 | 1.15 | V |

**Table 1–6. Recommended Operating Conditions for Arria II GZ Devices *(Note 6)* (Part 2 of 2)**

| Symbol | Description | Condition | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|---|
| $V_{CCL\_GXBLn}$ *(3)* | Transceiver clock power (left side) | — | 1.05 | 1.1 | 1.15 | V |
| $V_{CCL\_GXBRn}$ *(3)* | Transceiver clock power (right side) | — | 1.05 | 1.1 | 1.15 | V |
| $V_{CCH\_GXBLn}$ *(3)* | Transmitter output buffer power (left side) | — | 1.33/1.425 | 1.4/1.5 *(5)* | 1.575 | V |
| $V_{CCH\_GXBRn}$ *(3)* | Transmitter output buffer power (right side) | — | | | | |
| $T_J$ | Operating junction temperature | Commercial | 0 | — | 85 | °C |
| | | Industrial | –40 | — | 100 | °C |
| $t_{RAMP}$ | Power supply ramp time | Normal POR (PORSEL=0) | 0.05 | — | 100 | ms |
| | | Fast POR (PORSEL=1) | 0.05 | — | 4 | ms |

**Notes to Table 1–6:**

(1) Altera recommends a 3.0-V nominal battery voltage when connecting $V_{CCBAT}$ to a battery for volatile key backup. If you do not use the volatile security key, you may connect the $V_{CCBAT}$ to either GND or a 3.0-V power supply.

(2) $V_{CCPD}$ must be 2.5 V when $V_{CCIO}$ is 2.5, 1.8, 1.5, or 1.2 V. $V_{CCPD}$ must be 3.0 V when $V_{CCIO}$ is 3.0 V.

(3) n = 0, 1, or 2.

(4) $V_{CCA\_L/R}$ must be connected to a 3.0-V supply if the clock multiplier unit (CMU) phase-locked loop (PLL), receiver clock data recovery (CDR), or both, are configured at a base data rate > 4.25 Gbps. For data rates up to 4.25 Gbps, you can connect $V_{CCA\_L/R}$ to either 3.0 V or 2.5 V.

(5) $V_{CCH\_GXBL/R}$ must be connected to a 1.4-V supply if the transmitter channel data rate is > 6.5 Gbps. For data rates up to 6.5 Gbps, you can connect $V_{CCH\_GXBL/R}$ to either 1.4 V or 1.5 V.

(6) Transceiver power supplies do not have power-on-reset (POR) circuitry. After initial power-up, violating the transceiver power supply operating conditions could lead to unpredictable link behavior.

## DC Characteristics

This section lists the supply current, I/O pin leakage current, on-chip termination (OCT) accuracy and variation, input pin capacitance, internal weak pull-up and pull-down resistance, hot socketing, and Schmitt trigger input specifications.

### Supply Current

Standby current is the current the device draws after the device is configured with no inputs or outputs toggling and no activity in the device. Because these currents vary largely with the resources used, use the Microsoft Excel-based Early Power Estimator (EPE) to get supply current estimates for your design.

For more information about power estimation tools, refer to the *PowerPlay Early Power Estimator User Guide* and the *PowerPlay Power Analysis* chapter.

The calibration accuracy for calibrated series and parallel OCTs are applicable at the moment of calibration. When process, voltage, and temperature (PVT) conditions change after calibration, the tolerance may change.

Table 1–13 lists the Arria II GZ OCT without calibration resistance tolerance to PVT changes.

**Table 1–13. OCT Without Calibration Resistance Tolerance Specifications for Arria II GZ Devices**

| Symbol | Description | Conditions (V) | Resistance Tolerance | | Unit |
|---|---|---|---|---|---|
| | | | C3,I3 | C4,I4 | |
| 25-Ω $R_S$ 3.0 and 2.5 | 25-Ω internal series OCT without calibration | $V_{CCIO}$ = 3.0, 2.5 | ± 40 | ± 40 | % |
| 25-Ω $R_S$ 1.8 and 1.5 | 25-Ω internal series OCT without calibration | $V_{CCIO}$ = 1.8, 1.5 | ± 40 | ± 40 | % |
| 25-Ω $R_S$ 1.2 | 25-Ω internal series OCT without calibration | $V_{CCIO}$ = 1.2 | ± 50 | ± 50 | % |
| 50-Ω $R_S$ 3.0 and 2.5 | 50-Ω internal series OCT without calibration | $V_{CCIO}$ = 3.0, 2.5 | ± 40 | ± 40 | % |
| 50-Ω $R_S$ 1.8 and 1.5 | 50-Ω internal series OCT without calibration | $V_{CCIO}$ = 1.8, 1.5 | ± 40 | ± 40 | % |
| 50-Ω $R_S$ 1.2 | 50-Ω internal series OCT without calibration | $V_{CCIO}$ = 1.2 | ± 50 | ± 50 | % |
| 100-Ω $R_D$ 2.5 | 100-Ω internal differential OCT | $V_{CCIO}$ = 2.5 | ± 25 | ± 25 | % |

OCT calibration is automatically performed at power up for OCT-enabled I/Os. When voltage and temperature conditions change after calibration, the resistance may change. Use Equation 1–1 and Table 1–14 to determine the OCT variation when voltage and temperature vary after power-up calibration for Arria II GX and GZ devices.

**Equation 1–1. OCT Variation** ***(Note 1)***

$$R_{OCT} = R_{SCAL}\left(1 + \langle\frac{dR}{dT} \times \Delta T\rangle \pm \langle\frac{dR}{dV} \times \Delta V\rangle\right)$$

**Notes to Equation 1–1:**

(1) $R_{OCT}$ value calculated from Equation 1–1shows the range of OCT resistance with the variation of temperature and $V_{CCIO}$.

Table 1–17 lists the pin capacitance for Arria II GZ devices.

**Table 1–17. Pin Capacitance for Arria II GZ Devices**

| Symbol | Description | Typical | Unit |
|---|---|---|---|
| $C_{IOTB}$ | Input capacitance on the top and bottom I/O pins | 4 | pF |
| $C_{IOLR}$ | Input capacitance on the left and right I/O pins | 4 | pF |
| $C_{CLKTB}$ | Input capacitance on the top and bottom non-dedicated clock input pins | 4 | pF |
| $C_{CLKLR}$ | Input capacitance on the left and right non-dedicated clock input pins | 4 | pF |
| $C_{OUTFB}$ | Input capacitance on the dual-purpose clock output and feedback pins | 5 | pF |
| $C_{CLK1}$, $C_{CLK3}$, $C_{CLK8}$, and $C_{CLK10}$ | Input capacitance for dedicated clock input pins | 2 | pF |

### Internal Weak Pull-Up and Weak Pull-Down Resistors

Table 1–18 lists the weak pull-up and pull-down resistor values for Arria II GX devices.

**Table 1–18. Internal Weak Pull-up and Weak Pull-Down Resistors for Arria II GX Devices** *(Note 1)*

| Symbol | Description | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $R_{PU}$ | Value of I/O pin pull-up resistor before and during configuration, as well as user mode if the programmable pull-up resistor option is enabled. | $V_{CCIO}$ = 3.3 V ±5% *(2)* | 7 | 25 | 41 | kΩ |
| | | $V_{CCIO}$ = 3.0 V ±5% *(2)* | 7 | 28 | 47 | kΩ |
| | | $V_{CCIO}$ = 2.5 V ±5% *(2)* | 8 | 35 | 61 | kΩ |
| | | $V_{CCIO}$ = 1.8 V ±5% *(2)* | 10 | 57 | 108 | kΩ |
| | | $V_{CCIO}$ = 1.5 V ±5% *(2)* | 13 | 82 | 163 | kΩ |
| | | $V_{CCIO}$ = 1.2 V ±5% *(2)* | 19 | 143 | 351 | kΩ |
| $R_{PD}$ | Value of TCK pin pull-down resistor | $V_{CCIO}$ = 3.3 V ±5% | 6 | 19 | 29 | kΩ |
| | | $V_{CCIO}$ = 3.0 V ±5% | 6 | 22 | 32 | kΩ |
| | | $V_{CCIO}$ = 2.5 V ±5% | 6 | 25 | 42 | kΩ |
| | | $V_{CCIO}$ = 1.8 V ±5% | 7 | 35 | 70 | kΩ |
| | | $V_{CCIO}$ = 1.5 V ±5% | 8 | 50 | 112 | kΩ |

**Notes to Table 1–18:**

(1) All I/O pins have an option to enable weak pull-up except configuration, test, and JTAG pins. The weak pull-down feature is only available for JTAG TCK.

(2) Pin pull-up resistance values may be lower if an external source drives the pin higher than $V_{CCIO}$.

# Switching Characteristics

This section provides performance characteristics of the Arria II GX and GZ core and periphery blocks for commercial grade devices. The following tables are considered final and are based on actual silicon characterization and testing. These numbers reflect the actual performance of the device under worst-case silicon process, voltage, and junction temperature conditions.

## Transceiver Performance Specifications

Table 1–34 lists the Arria II GX transceiver specifications.

**Table 1–34. Transceiver Specifications for Arria II GX Devices *(Note 1)* (Part 1 of 7)**

| Symbol/ Description | Condition | I3 | | | C4 | | | C5 and I5 | | | C6 | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| **Reference Clock** | | | | | | | | | | | | | | |
| Supported I/O Standards | 1.2-V PCML, 1.5-V PCML, 2.5-V PCML, Differential LVPECL, LVDS, and HCSL | | | | | | | | | | | | | |
| Input frequency from REFCLK input pins | — | 50 | — | 622.08 | 50 | — | 622.08 | 50 | — | 622.08 | 50 | — | 622.08 | MHz |
| Input frequency from PLD input | — | 50 | — | 200 | 50 | — | 200 | 50 | — | 200 | 50 | — | 200 | MHz |
| Absolute $V_{MAX}$ for a REFCLK pin | — | — | — | 2.2 | — | — | 2.2 | — | — | 2.2 | — | — | 2.2 | V |
| Absolute $V_{MIN}$ for a REFCLK pin | — | –0.3 | — | — | –0.3 | — | — | –0.3 | — | — | –0.3 | — | — | V |
| Rise/fall time *(2)* | — | — | — | 0.2 | — | — | 0.2 | — | — | 0.2 | — | — | 0.2 | UI |
| Duty cycle | — | 45 | — | 55 | 45 | — | 55 | 45 | — | 55 | 45 | — | 55 | % |
| Peak-to-peak differential input voltage | — | 200 | — | 2000 | 200 | — | 2000 | 200 | — | 2000 | 200 | — | 2000 | mV |
| Spread-spectrum modulating clock frequency | PCIe | 30 | — | 33 | 30 | — | 33 | 30 | — | 33 | 30 | — | 33 | kHz |

**Table 1–34. Transceiver Specifications for Arria II GX Devices** *(Note 1)* **(Part 3 of 7)**

| Symbol/ Description | Condition | I3 | | | C4 | | | C5 and I5 | | | C6 | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| `fixedclk` clock frequency | PCIe Receiver Detect | — | 125 | — | — | 125 | — | — | 125 | — | — | 125 | — | MHz |
| `reconfig_clk` clock frequency | Dynamic reconfig. clock frequency | 2.5/ 37.5 *(4)* | — | 50 | 2.5/ 37.5 *(4)* | — | 50 | 2.5/ 37.5 *(4)* | — | 50 | 2.5/ 37.5 *(4)* | — | 50 | MHz |
| Delta time between `reconfig_clks` *(5)* | — | — | — | 2 | — | — | 2 | — | — | 2 | — | — | 2 | ms |
| Transceiver block minimum power-down pulse width | — | — | 1 | — | — | 1 | — | — | 1 | — | — | 1 | — | µs |
| **Receiver** | | | | | | | | | | | | | | |
| Supported I/O Standards | 1.4-V PCML, 1.5-V PCML, 2.5-V PCML, 2.5-V PCML, LVPECL, and LVDS | | | | | | | | | | | | | |
| Data rate *(13)* | — | 600 | — | 6375 | 600 | — | 3750 | 600 | — | 3750 | 600 | — | 3125 | Mbps |
| Absolute $V_{MAX}$ for a receiver pin *(6)* | — | — | — | 1.5 | — | — | 1.5 | — | — | 1.5 | — | — | 1.5 | V |
| Absolute $V_{MIN}$ for a receiver pin | — | -0.4 | — | — | -0.4 | — | — | -0.4 | — | — | -0.4 | — | — | V |
| Maximum peak-to-peak differential input voltage $V_{ID}$ (diff p-p) | $V_{ICM}$ = 0.82 V setting | — | — | 2.7 | — | — | 2.7 | — | — | 2.7 | — | — | 2.7 | V |
| | $V_{ICM}$ =1.1 V setting *(7)* | — | — | 1.6 | — | — | 1.6 | — | — | 1.6 | — | — | 1.6 | V |

**Table 1–34. Transceiver Specifications for Arria II GX Devices** *(Note 1)* **(Part 4 of 7)**

| Symbol/ Description | Condition | I3 | | | C4 | | | C5 and I5 | | | C6 | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Minimum peak-to-peak differential input voltage $V_{ID}$ (diff p-p) | — | 100 | — | — | 100 | — | — | 100 | — | — | 100 | — | — | mV |
| $V_{ICM}$ | $V_{ICM}$ = 0.82 V setting | — | 820 | — | — | 820 | — | — | 820 | — | — | 820 | — | mV |
| | $V_{ICM}$ =1.1 V setting *(7)* | — | 1100 | — | — | 1100 | — | — | 1100 | — | — | 1100 | — | mV |
| Differential on-chip termination resistors | 100–Ω setting | — | 100 | — | — | 100 | — | — | 100 | — | — | 100 | — | Ω |
| Return loss differential mode | PCIe | | | | 50 MHz to 1.25 GHz: –10dB | | | | | | | | | |
| | XAUI | | | | 100 MHz to 2.5 GHz: –10dB | | | | | | | | | |
| Return loss common mode | PCIe | | | | 50 MHz to 1.25 GHz: –6dB | | | | | | | | | |
| | XAUI | | | | 100 MHz to 2.5 GHz: –6dB | | | | | | | | | |
| Programmable PPM detector *(8)* | — | ± 62.5, 100, 125, 200, 250, 300, 500, 1000 | | | | | | | | | | | | ppm |
| Run length | — | — | 80 | — | — | 80 | — | — | 80 | — | — | 80 | — | UI |
| Programmable equalization | — | — | — | 7 | — | — | 7 | — | — | 7 | — | — | 7 | dB |
| Signal detect/loss threshold | PCIe Mode | 65 | — | 175 | 65 | — | 175 | 65 | — | 175 | 65 | — | 175 | mV |
| CDR LTR time *(9)* | — | — | — | 75 | — | — | 75 | — | — | 75 | — | — | 75 | µs |
| CDR minimum T1b *(10)* | — | 15 | — | — | 15 | — | | 15 | — | — | 15 | — | — | µs |

**Table 1–34. Transceiver Specifications for Arria II GX Devices *(Note 1)* (Part 7 of 7)**

| Symbol/ Description | Condition | I3 | | | C4 | | | C5 and I5 | | | C6 | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Digital reset pulse width | — | Minimum is 2 parallel clock cycles | | | | | | | | | | | | |

**Notes to Table 1–34:**

(1) For AC-coupled links, the on-chip biasing circuit is switched off before and during configuration. Ensure that input specifications are not violated during this period.

(2) The rise/fall time is specified from 20% to 80%.

(3) To calculate the REFCLK rms phase jitter requirement at reference clock frequencies other than 100 MHz, use the following formula:
REFCLK rms phase jitter at f (MHz) = REFCLK rms phase jitter at 100 MHz * 100/f.

(4) The minimum `reconfig_clk` frequency is 2.5 MHz if the transceiver channel is configured in **Transmitter only** mode. The minimum `reconfig_clk` frequency is 37.5 MHz if the transceiver channel is configured in **Receiver only** or **Receiver and Transmitter** mode. For more information, refer to *AN 558: Implementing Dynamic Reconfiguration in Arria II Devices*.

(5) If your design uses more than one dynamic reconfiguration controller instances (`altgx_reconfig`) to control the transceiver channels (`altgx`) physically located on the same side of the device, and if you use different `reconfig_clk` sources for these `altgx_reconfig` instances, the delta time between any two of these `reconfig_clk` sources becoming stable must not exceed the maximum specification listed.

(6) The device cannot tolerate prolonged operation at this absolute maximum.

(7) You must use the 1.1-V RX $V_{ICM}$ setting if the input serial data standard is LVDS and the link is DC-coupled.

(8) The rate matcher supports only up to ±300 parts per million (ppm).

(9) Time taken to `rx_pll_locked` goes high from `rx_analogreset` de-assertion. Refer to Figure 1–1.

(10) The time in which the CDR must be kept in lock-to-reference mode after `rx_pll_locked` goes high and before `rx_locktodata` is asserted in manual mode. Refer to Figure 1–1.

(11) The time taken to recover valid data after the `rx_locktodata` signal is asserted in manual mode. Refer to Figure 1–1.

(12) The time taken to recover valid data after the `rx_freqlocked` signal goes high in automatic mode. Refer to Figure 1–2.

(13) To support data rates lower than the minimum specification through oversampling, use the CDR in LTR mode only.

Table 1–37 lists the typical $V_{OD}$ for TX term that equals 100 Ω for Arria II GX and GZ devices.

**Table 1–37. Typical $V_{OD}$ Setting, TX Termination = 100 Ω for Arria II Devices**

| Quartus II Setting | $V_{OD}$ Setting (mV) |
|---|---|
| 1 | 400 |
| 2 | 600 |
| 3 (Arria II GZ) | 700 |
| 4 | 800 |
| 5 | 900 |
| 6 | 1000 |
| 7 | 1200 |

Table 1–38 lists the typical transmitter pre-emphasis levels in dB for the first post tap under the following conditions: low-frequency data pattern (five 1s and five 0s) at 6.375 Gbps. The levels listed in Table 1–38 are a representation of possible pre-emphasis levels under these specified conditions only, the pre-emphasis levels may change with data pattern and data rate.

To predict the pre-emphasis level for your specific data rate and pattern, run simulations using the Arria II GX HSSI HSPICE models.

**Table 1–38. Transmitter Pre-Emphasis Levels for Arria II GX Devices**

| Arria II GX (Quartus II Software) First Post Tap Setting | Arria II GX (Quartus II Software) VOD Setting | | | | | | |
|---|---|---|---|---|---|---|---|
| | 1 | 2 | 4 | 5 | 6 | 7 | Unit |
| 0 (off) | 0 | 0 | 0 | 0 | 0 | 0 | — |
| 1 | 0.7 | 0 | 0 | 0 | 0 | 0 | dB |
| 2 | 2.7 | 1.2 | 0.3 | 0 | 0 | 0 | dB |
| 3 | 4.9 | 2.4 | 1.2 | 0.8 | 0.5 | 0.2 | dB |
| 4 | 7.5 | 3.8 | 2.1 | 1.6 | 1.2 | 0.6 | dB |
| 5 | — | 5.3 | 3.1 | 2.4 | 1.8 | 1.1 | dB |
| 6 | — | 7 | 4.3 | 3.3 | 2.7 | 1.7 | dB |

**Table 1–39. Transmitter Pre-Emphasis Levels for Arria II GZ Devices (Part 2 of 2)**

| Pre-Emphasis 1st Post-Tap Setting | $V_{OD}$ Setting | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| 29 | N/A | N/A | N/A | 12.5 | 9.6 | 7.7 | 6.3 | 4.3 |
| 30 | N/A | N/A | N/A | N/A | 11.4 | 9 | 7.4 | N/A |
| 31 | N/A | N/A | N/A | N/A | 12.9 | 10 | 8.2 | N/A |

Table 1–40 lists the transceiver jitter specifications for all supported protocols for Arria II GX devices.

**Table 1–40. Transceiver Block Jitter Specifications for Arria II GX Devices *(Note 1)* (Part 1 of 10)**

| Symbol/ Description | Conditions | I3 | | | C4 | | | C5, I5 | | | C6 | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| **SONET/SDH Transmit Jitter Generation *(2)*** | | | | | | | | | | | | | | |
| Peak-to-peak jitter at 622.08 Mbps | Pattern = PRBS15 | — | — | 0.1 | — | — | 0.1 | — | — | 0.1 | — | — | 0.1 | UI |
| RMS jitter at 622.08 Mbps | Pattern = PRBS15 | — | — | 0.01 | — | — | 0.01 | — | — | 0.01 | — | — | 0.01 | UI |
| Peak-to-peak jitter at 2488.32 Mbps | Pattern = PRBS15 | — | — | 0.1 | — | — | 0.1 | — | — | 0.1 | — | — | 0.1 | UI |
| RMS jitter at 2488.32 Mbps | Pattern = PRBS15 | — | — | 0.01 | — | — | 0.01 | — | — | 0.01 | — | — | 0.01 | UI |
| **SONET/SDH Receiver Jitter Tolerance *(2)*** | | | | | | | | | | | | | | |
| Jitter tolerance at 622.08 Mbps | Jitter frequency = 0.03 KHz Pattern = PRBS15 | > 15 | | | > 15 | | | > 15 | | | > 15 | | | UI |
| | Jitter frequency = 25 KHZ Pattern = PRBS15 | > 1.5 | | | > 1.5 | | | > 1.5 | | | > 1.5 | | | UI |
| | Jitter frequency = 250 KHz Pattern = PRBS15 | > 0.15 | | | > 0.15 | | | > 0.15 | | | > 0.15 | | | UI |

**Table 1–40. Transceiver Block Jitter Specifications for Arria II GX Devices *(Note 1)* (Part 4 of 10)**

| Symbol/ Description | Conditions | I3 | | | C4 | | | C5, I5 | | | C6 | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Total jitter (peak-to-peak) | Pattern = CRPAT | — | — | 0.279 | — | — | 0.279 | — | — | 0.279 | — | — | 0.279 | UI |
| **GIGE Receiver Jitter Tolerance *(6)*** | | | | | | | | | | | | | | |
| Deterministic jitter tolerance (peak-to-peak) | Pattern = CJPAT | > 0.4 | | | > 0.4 | | | > 0.4 | | | > 0.4 | | | UI |
| Combined deterministic and random jitter tolerance (peak-to-peak) | Pattern = CJPAT | > 0.66 | | | > 0.66 | | | > 0.66 | | | > 0.66 | | | UI |
| **HiGig Transmit Jitter Generation *(7)*** | | | | | | | | | | | | | | |
| Deterministic jitter (peak-to-peak) | Data rate = 3.75 Gbps<br>Pattern = CJPAT | — | — | 0.17 | — | — | 0.17 | — | — | — | — | — | — | UI |
| Total jitter (peak-to-peak) | Data rate = 3.75 Gbps<br>Pattern = CJPAT | — | — | 0.35 | — | — | 0.35 | — | — | — | — | — | — | UI |
| **HiGig Receiver Jitter Tolerance *(7)*** | | | | | | | | | | | | | | |
| Deterministic jitter tolerance (peak-to-peak) | Data rate = 3.75 Gbps<br>Pattern = CJPAT | > 0.37 | | | > 0.37 | | | — | — | — | — | — | — | UI |
| Combined deterministic and random jitter tolerance (peak-to-peak) | Data rate = 3.75 Gbps<br>Pattern = CJPAT | > 0.65 | | | > 0.65 | | | — | — | — | — | — | — | UI |
| Sinusoidal jitter tolerance (peak-to-peak) | Jitter frequency = 22.1 KHz<br>Data rate = 3.75 Gbps<br>Pattern = CJPAT | > 8.5 | | | > 8.5 | | | — | — | — | — | — | — | UI |
| | Jitter frequency = 1.875MHz<br>Data rate = 3.75 Gbps<br>Pattern = CJPAT | > 0.1 | | | > 0.1 | | | — | — | — | — | — | — | UI |
| | Jitter frequency = 20 MHz<br>Data rate = 3.75 Gbps<br>Pattern = CJPAT | > 0.1 | | | > 0.1 | | | — | — | — | — | — | — | UI |

**Table 1–40. Transceiver Block Jitter Specifications for Arria II GX Devices** *(Note 1)* **(Part 8 of 10)**

| Symbol/ Description | Conditions | I3 | | | C4 | | | C5, I5 | | | C6 | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| **CPRI Transmit Jitter Generation** *(11)* | | | | | | | | | | | | | | |
| Total jitter | E.6.HV, E.12.HV<br>Pattern = CJPAT | — | — | 0.27<br>9 | — | — | 0.279 | — | — | 0.279 | — | — | 0.279 | UI |
| | E.6.LV, E.12.LV, E.24.LV, E.30.LV<br>Pattern = CJTPAT | — | — | 0.35 | — | — | 0.35 | — | — | 0.35 | — | — | 0.35 | UI |
| Deterministic jitter | E.6.HV, E.12.HV<br>Pattern = CJPAT | — | — | 0.14 | — | — | 0.14 | — | — | 0.14 | — | — | 0.14 | UI |
| | E.6.LV, E.12.LV, E.24.LV, E.30.LV<br>Pattern = CJTPAT | — | — | 0.17 | — | — | 0.17 | — | — | 0.17 | — | — | 0.17 | UI |
| **CPRI Receiver Jitter Tolerance** *(11)* | | | | | | | | | | | | | | |
| Total jitter tolerance | E.6.HV, E.12.HV<br>Pattern = CJPAT | > 0.66 | | | > 0.66 | | | > 0.66 | | | > 0.66 | | | UI |
| Deterministic jitter tolerance | E.6.HV, E.12.HV<br>Pattern = CJPAT | > 0.4 | | | > 0.4 | | | > 0.4 | | | > 0.4 | | | UI |
| Total jitter tolerance | E.6.LV, E.12.LV, E.24.LV, E.30.LV<br>Pattern = CJTPAT | > 0.65 | | | > 0.65 | | | > 0.65 | | | > 0.65 | | | UI |
| | E.60.LV<br>Pattern = PRBS31 | > 0.6 | | | — | | | — | | | — | | | UI |
| Deterministic jitter tolerance | E.6.LV, E.12.LV, E.24.LV, E.30.LV<br>Pattern = CJTPAT | > 0.37 | | | > 0.37 | | | > 0.37 | | | > 0.37 | | | UI |
| | E.60.LV<br>Pattern = PRBS31 | > 0.45 | | | — | | | — | | | — | | | UI |
| Combined deterministic and random jitter tolerance | E.6.LV, E.12.LV, E.24.LV, E.30.LV<br>Pattern = CJTPAT | > 0.55 | | | > 0.55 | | | > 0.55 | | | > 0.55 | | | UI |
| **OBSAI Transmit Jitter Generation** *(12)* | | | | | | | | | | | | | | |
| Total jitter at 768 Mbps, 1536 Mbps, and 3072 Mbps | REFCLK = 153.6 MHz<br>Pattern = CJPAT | — | — | 0.35 | — | — | 0.35 | — | — | 0.35 | — | — | 0.35 | UI |
| Deterministic jitter at 768 Mbps, 1536 Mbps, and 3072 Mbps | REFCLK = 153.6 MHz<br>Pattern = CJPAT | — | — | 0.17 | — | — | 0.17 | — | — | 0.17 | — | — | 0.17 | UI |

**Table 1–40. Transceiver Block Jitter Specifications for Arria II GX Devices *(Note 1)* (Part 9 of 10)**

| Symbol/ Description | Conditions | I3 | | | C4 | | | C5, I5 | | | C6 | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| **OBSAI Receiver Jitter Tolerance** *(12)* | | | | | | | | | | | | | | |
| Deterministic jitter tolerance at 768 Mbps, 1536 Mbps, and 3072 Mbps | Pattern = CJPAT | > 0.37 | | | > 0.37 | | | > 0.37 | | | > 0.37 | | | UI |
| Combined deterministic and random jitter tolerance at 768 Mbps, 1536 Mbps, and 3072 Mbps | Pattern = CJPAT | > 0.55 | | | > 0.55 | | | > 0.55 | | | > 0.55 | | | UI |
| Sinusoidal jitter tolerance at 768 Mbps | Jitter frequency = 5.4 KHz<br>Pattern = CJPAT | > 8.5 | | | > 8.5 | | | > 8.5 | | | > 8.5 | | | UI |
| | Jitter frequency = 460.8 KHz to 20 MHz<br>Pattern = CJPAT | > 0.1 | | | > 0.1 | | | > 0.1 | | | > 0.1 | | | UI |
| Sinusoidal jitter tolerance at 1536 Mbps | Jitter frequency = 10.9 KHz<br>Pattern = CJPAT | > 8.5 | | | > 8.5 | | | > 8.5 | | | > 8.5 | | | UI |
| | Jitter frequency = 921.6 KHz to 20 MHz<br>Pattern = CJPAT | > 0.1 | | | > 0.1 | | | > 0.1 | | | > 0.1 | | | UI |

**Table 1–40. Transceiver Block Jitter Specifications for Arria II GX Devices *(Note 1)* (Part 10 of 10)**

| Symbol/ Description | Conditions | I3 | | | C4 | | | C5, I5 | | | C6 | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Sinusoidal jitter tolerance at 3072 Mbps | Jitter frequency = 21.8 KHz<br>Pattern = CJPAT | > 8.5 | | | > 8.5 | | | > 8.5 | | | > 8.5 | | | UI |
| | Jitter frequency = 1843.2 KHz to 20 MHz<br>Pattern = CJPAT | > 0.1 | | | > 0.1 | | | > 0.1 | | | > 0.1 | | | UI |

**Notes to Table 1–40:**

(1) Dedicated `refclk` pins are used to drive the input reference clocks. The jitter numbers are valid for the stated conditions only.
(2) The jitter numbers for SONET/SDH are compliant to the GR-253-CORE Issue 3 Specification.
(3) The jitter numbers for XAUI are compliant to the IEEE802.3ae-2002 Specification.
(4) The jitter numbers for PCIe are compliant to the PCIe Base Specification 2.0.
(5) The jitter numbers for SRIO are compliant to the RapidIO Specification 1.3.
(6) The jitter numbers for GIGE are compliant to the IEEE802.3-2002 Specification.
(7) The jitter numbers for HiGig are compliant to the IEEE802.3ae-2002 Specification.
(8) The HD-SDI and 3G-SDI jitter numbers are compliant to the SMPTE292M and SMPTE424M Specifications.
(9) Arria II PCIe receivers are compliant to this specification provided the VTX_CM-DC-ACTIVEIDLE-DELTA of the upstream transmitter is less than 50 mV.
(10) The jitter numbers for Serial Advanced Technology Attachment (SATA) are compliant to the Serial ATA Revision 3.0 Specification.
(11) The jitter numbers for Common Public Radio Interface (CPRI) are compliant to the CPRI Specification V3.0.
(12) The jitter numbers for Open Base Station Architecture Initiative (OBSAI) are compliant to the OBSAI RP3 Specification V4.1.

Table 1–41 lists the transceiver jitter specifications for all supported protocols for Arria II GZ devices.

**Table 1–41. Transceiver Block Jitter Specifications for Arria II GZ Devices *(Note 1)*, *(2)* (Part 1 of 7)**

| Symbol/ Description | Conditions | –C3 and –I3 | | | –C4 and –I4 | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| **SONET/SDH Transmit Jitter Generation *(3)*** | | | | | | | | |
| Peak-to-peak jitter at 622.08 Mbps | Pattern = PRBS15 | — | — | 0.1 | — | — | 0.1 | UI |
| RMS jitter at 622.08 Mbps | Pattern = PRBS15 | — | — | 0.01 | — | — | 0.01 | UI |
| Peak-to-peak jitter at 2488.32 Mbps | Pattern = PRBS15 | — | — | 0.1 | — | — | 0.1 | UI |
| RMS jitter at 2488.32 Mbps | Pattern = PRBS15 | — | — | 0.01 | — | — | 0.01 | UI |
| **SONET/SDH Receiver Jitter Tolerance *(3)*** | | | | | | | | |
| Jitter tolerance at 622.08 Mbps | Jitter frequency = 0.03 KHz<br>Pattern = PRBS15 | > 15 | | | > 15 | | | UI |
| | Jitter frequency = 25 KHZ<br>Pattern = PRBS15 | > 1.5 | | | > 1.5 | | | UI |
| | Jitter frequency = 250 KHz<br>Pattern = PRBS15 | > 0.15 | | | > 0.15 | | | UI |

**Table 1–45. PLL Specifications for Arria II GZ Devices (Part 2 of 2)**

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $t_{DLOCK}$ | Time required to lock dynamically (after switchover or reconfiguring any non-post-scale counters/delays) | — | — | 1 | ms |
| $f_{CLBW}$ | PLL closed-loop low bandwidth | — | 0.3 | — | MHz |
| | PLL closed-loop medium bandwidth | — | 1.5 | — | MHz |
| | PLL closed-loop high bandwidth *(7)* | — | 4 | — | MHz |
| $t_{PLL\_PSERR}$ | Accuracy of PLL phase shift | — | — | ±50 | ps |
| $t_{ARESET}$ | Minimum pulse width on the `areset` signal | 10 | — | — | ns |
| $t_{INCCJ}$ *(3)*, *(4)* | Input clock cycle to cycle jitter ($F_{REF} \geq 100$ MHz) | — | — | 0.15 | UI (p-p) |
| | Input clock cycle to cycle jitter ($F_{REF} < 100$ MHz) | — | — | ±750 | ps (p-p) |
| $t_{OUTPJ\_DC}$ *(5)* | Period Jitter for dedicated clock output ($F_{OUT} \geq 100$ MHz) | — | — | 175 | ps (p-p) |
| | Period Jitter for dedicated clock output ($F_{OUT} < 100$ MHz) | — | — | 17.5 | mUI (p-p) |
| $t_{OUTCCJ\_DC}$ *(5)* | Cycle to Cycle Jitter for dedicated clock output ($F_{OUT} \geq 100$ MHz) | — | — | 175 | ps (p-p) |
| | Cycle to Cycle Jitter for dedicated clock output ($F_{OUT} < 100$ MHz) | — | — | 17.5 | mUI (p-p) |
| $t_{OUTPJ\_IO}$ *(5)*, *(8)* | Period Jitter for clock output on regular I/O ($F_{OUT} \geq 100$ MHz) | — | — | 600 | ps (p-p) |
| | Period Jitter for clock output on regular I/O ($F_{OUT} < 100$ MHz) | — | — | 60 | mUI (p-p) |
| $t_{OUTCCJ\_IO}$ *(5)*, *(8)* | Cycle to Cycle Jitter for clock output on regular I/O ($F_{OUT} \geq 100$ MHz) | — | — | 600 | ps (p-p) |
| | Cycle to Cycle Jitter for clock output on regular I/O ($F_{OUT} < 100$ MHz) | — | — | 60 | mUI (p-p) |
| $t_{CASC\_OUTPJ\_DC}$ *(5)*, *(6)* | Period Jitter for dedicated clock output in cascaded PLLs ($F_{OUT} \geq$100MHz) | — | — | 250 | ps (p-p) |
| | Period Jitter for dedicated clock output in cascaded PLLs ($F_{OUT} <$ 100MHz) | — | — | 25 | mUI (p-p) |
| $f_{DRIFT}$ | Frequency drift after PFDENA is disabled for duration of 100 us | — | — | ±10 | % |

**Notes to Table 1–45:**

(1) This specification is limited in the Quartus II software by the I/O maximum frequency. The maximum I/O frequency is different for each I/O standard.

(2) This specification is limited by the lower of the two: I/O $F_{MAX}$ or $F_{OUT}$ of the PLL.

(3) A high input jitter directly affects the PLL output jitter. To have low PLL output clock jitter, you must provide a clean clock source that is less than 120 ps.

(4) $F_{REF}$ is fIN/N when N = 1.

(5) Peak-to-peak jitter with a probability level of $10^{-12}$ (14 sigma, 99.99999999974404% confidence level). The output jitter specification applies to the intrinsic jitter of the PLL, when an input jitter of 30 ps is applied. The external memory interface clock output jitter specifications use a different measurement method and are available in Table 1–64 on page 1–71.

(6) The cascaded PLL specification is only applicable with the following condition:
a. Upstream PLL: 0.59 Mhz ≤ Upstream PLL BW < 1 MHz
b. Downstream PLL: Downstream PLL BW > 2 MHz

(7) High bandwidth PLL settings are not supported in external feedback mode.

(8) External memory interface clock output jitter specifications use a different measurement method, which is available in Table 1–63 on page 1–71.

## IOE Programmable Delay

Table 1–66 lists the delay associated with each supported IOE programmable delay chain for Arria II GX devices.

**Table 1–66. IOE Programmable Delay for Arria II GX Devices**

| Parameter | Available Settings *(1)* | Minimum Offset *(2)* | Maximum Offset | | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Fast Model | | | Slow Model | | | | | |
| | | | I3 | C4 | I5 | I3 | C4 | C5 | I5 | C6 | |
| Output enable pin delay | 7 | 0 | 0.413 | 0.442 | 0.413 | 0.814 | 0.713 | 0.796 | 0.801 | 0.873 | ns |
| Delay from output register to output pin | 7 | 0 | 0.339 | 0.362 | 0.339 | 0.671 | 0.585 | 0.654 | 0.661 | 0.722 | ns |
| Input delay from pin to internal cell | 52 | 0 | 1.494 | 1.607 | 1.494 | 2.895 | 2.520 | 2.733 | 2.775 | 2.944 | ns |
| Input delay from pin to input register | 52 | 0 | 1.493 | 1.607 | 1.493 | 2.896 | 2.503 | 2.732 | 2.774 | 2.944 | ns |
| DQS bus to input register delay | 4 | 0 | 0.074 | 0.076 | 0.074 | 0.140 | 0.124 | 0.147 | 0.147 | 0.167 | ns |

**Notes to Table 1–66:**

(1) The available setting for every delay chain starts with zero and ends with the specified maximum number of settings.

(2) The minimum offset represented in the table does not include intrinsic delay.

Table 1–67 lists the IOE programmable delay settings for Arria II GZ devices.

**Table 1–67. IOE Programmable Delay for Arria II GZ Devices**

| Parameter | Available Settings *(1)* | Minimum Offset *(2)* | Maximum Offset | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | Fast Model | | Slow Model | | | | |
| | | | Industrial | Commercial | C3 | I3 | C4 | I4 | |
| D1 | 15 | 0 | 0.462 | 0.505 | 0.795 | 0.801 | 0.857 | 0.864 | ns |
| D2 | 7 | 0 | 0.234 | 0.232 | 0.372 | 0.371 | 0.407 | 0.405 | ns |
| D3 | 7 | 0 | 1.700 | 1.769 | 2.927 | 2.948 | 3.157 | 3.178 | ns |
| D4 | 15 | 0 | 0.508 | 0.554 | 0.882 | 0.889 | 0.952 | 0.959 | ns |
| D5 | 15 | 0 | 0.472 | 0.500 | 0.799 | 0.817 | 0.875 | 0.882 | ns |
| D6 | 6 | 0 | 0.186 | 0.195 | 0.319 | 0.321 | 0.345 | 0.347 | ns |

**Notes to Table 1–67:**

(1) You can set this value in the Quartus II software by selecting **D1**, **D2**, **D3**, **D4**, **D5**, and **D6** in the **Assignment Name** column.

(2) Minimum offset does not include the intrinsic delay.

# I/O Timing

Altera offers two ways to determine I/O timing:

- Using the Microsoft Excel-based I/O Timing.
- Using the Quartus II Timing Analyzer.

The Microsoft Excel-based I/O Timing provides pin timing performance for each device density and speed grade. The data is typically used prior to designing the FPGA to get an estimate of the timing budget as part of the link timing analysis. The Quartus II timing analyzer provides a more accurate and precise I/O timing data based on the specifics of the design after place-and-route is complete.

The Microsoft Excel-based I/O Timing spreadsheet is downloadable from the Literature: Arria II Devices web page.

**Table 1–68. Glossary (Part 2 of 4)**

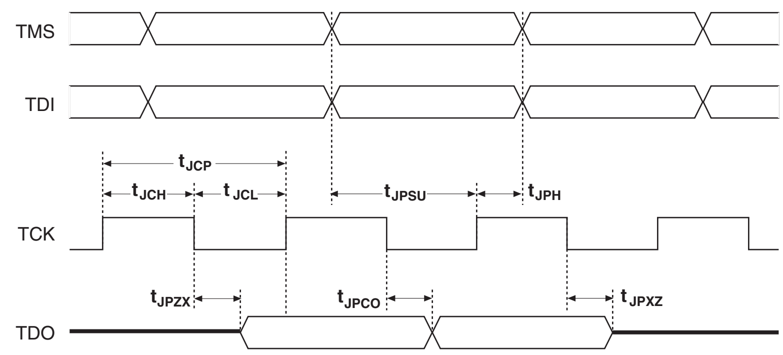
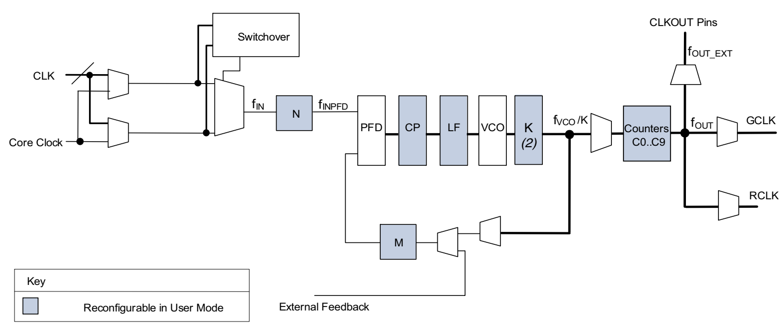
<table>
<tr><th>Letter</th><th>Subject</th><th>Definitions</th></tr>
<tr><td rowspan="2">G,<br>H,<br>I,<br>J</td><td>J</td><td>High-speed I/O block: Deserialization factor (width of parallel data bus).</td></tr>
<tr><td>JTAG Timing Specifications</td><td>JTAG Timing Specifications:<br>
</td></tr>
<tr><td>K,<br>L,<br>M,<br>N,<br>O,<br>P</td><td>PLL Specifications</td><td>PLL Specification parameters:<br>**Diagram of PLL Specifications** *(1)*<br>
<br>**Notes:**<br>(1) CoreClock can only be fed by dedicated clock input pins or PLL outputs.<br>(2) This is the VCO post-scale counter K.</td></tr>
<tr><td>Q,<br>R</td><td>$R_L$</td><td>Receiver differential input discrete resistor (external to the Arria II device).</td></tr>
</table>

**Table 1–68. Glossary (Part 4 of 4)**

| Letter | Subject | Definitions |
|---|---|---|
| U, V | $V_{CM(DC)}$ | DC common mode input voltage. |
| | $V_{ICM}$ | Input common mode voltage: The common mode of the differential signal at the receiver. |
| | $V_{ID}$ | Input differential voltage swing: The difference in voltage between the positive and complementary conductors of a differential transmission at the receiver. |
| | $V_{DIF(AC)}$ | AC differential input voltage: Minimum AC input differential voltage required for switching. |
| | $V_{DIF(DC)}$ | DC differential input voltage: Minimum DC input differential voltage required for switching. |
| | $V_{IH}$ | Voltage input high: The minimum positive voltage applied to the input which is accepted by the device as a logic high. |
| | $V_{IH(AC)}$ | High-level AC input voltage. |
| | $V_{IH(DC)}$ | High-level DC input voltage. |
| | $V_{IL}$ | Voltage input low: The maximum positive voltage applied to the input which is accepted by the device as a logic low. |
| | $V_{IL(AC)}$ | Low-level AC input voltage. |
| | $V_{IL(DC)}$ | Low-level DC input voltage. |
| | $V_{OCM}$ | Output common mode voltage: The common mode of the differential signal at the transmitter. |
| | $V_{OD}$ | Output differential voltage swing: The difference in voltage between the positive and complementary conductors of a differential transmission at the transmitter. |
| W, X, Y, Z | W | High-speed I/O block: The clock boost factor. |

# Document Revision History

Table 1–69 lists the revision history for this chapter.

**Table 1–69. Document Revision History (Part 1 of 2)**

| Date | Version | Changes |
|---|---|---|
| December 2013 | 4.4 | Updated Table 1–34 and Table 1–35. |
| July 2012 | 4.3 | ■ Updated the $V_{CCH\_GXBL/R}$ operating conditions in Table 1–6.<br>■ Finalized Arria II GZ information in Table 1–20.<br>■ Added BLVDS specification in Table 1–32 and Table 1–33.<br>■ Updated input and output waveforms in Table 1–68. |
| December 2011 | 4.2 | ■ Updated Table 1–32, Table 1–33, Table 1–34, Table 1–35, Table 1–40, Table 1–41, Table 1–54, and Table 1–67.<br>■ Minor text edits. |
| June 2011 | 4.1 | ■ Added Table 1–60.<br>■ Updated Table 1–32, Table 1–33, Table 1–38, Table 1–41, and Table 1–61.<br>■ Updated the “Switching Characteristics” section introduction.<br>■ Minor text edits. |