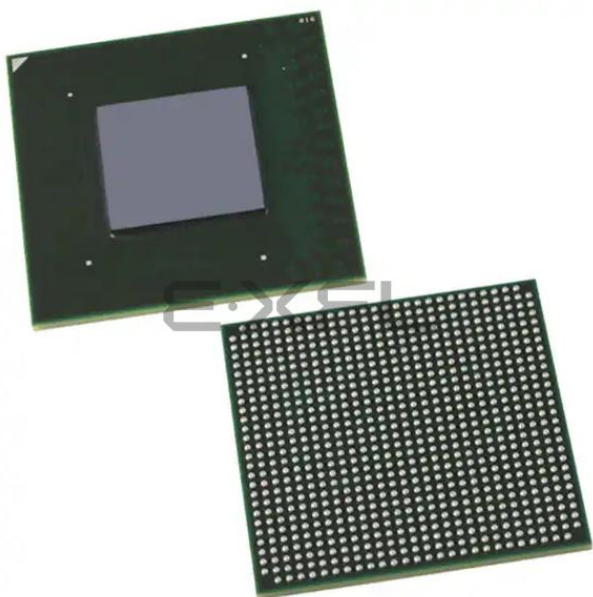




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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	2530
Number of Logic Elements/Cells	60214
Total RAM Bits	5371904
Number of I/O	364
Number of Gates	-
Voltage - Supply	0.87V ~ 0.93V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	780-BBGA, FCBGA
Supplier Device Package	780-FBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep2agx65df29i3n



Conditions beyond those listed in [Table 1-1](#) and [Table 1-2](#) may cause permanent damage to the device. Additionally, device operation at the absolute maximum ratings for extended periods of time may have adverse effects on the device.

[Table 1-1](#) lists the absolute maximum ratings for Arria II GX devices.

Table 1-1. Absolute Maximum Ratings for Arria II GX Devices

Symbol	Description	Minimum	Maximum	Unit
V_{CC}	Supplies power to the core, periphery, I/O registers, PCI Express® (PIPE) (PCIe) HIP block, and transceiver PCS	-0.5	1.35	V
V_{CCCB}	Supplies power for the configuration RAM bits	-0.5	1.8	V
V_{CCBAT}	Battery back-up power supply for design security volatile key register	-0.5	3.75	V
V_{CCPD}	Supplies power to the I/O pre-drivers, differential input buffers, and MSEL circuitry	-0.5	3.75	V
V_{CCIO}	Supplies power to the I/O banks	-0.5	3.9	V
V_{CCD_PLL}	Supplies power to the digital portions of the PLL	-0.5	1.35	V
V_{CCA_PLL}	Supplies power to the analog portions of the PLL and device-wide power management circuitry	-0.5	3.75	V
V_I	DC input voltage	-0.5	4.0	V
I_{OUT}	DC output current, per pin	-25	40	mA
V_{CCA}	Supplies power to the transceiver PMA regulator	—	3.75	V
V_{CCL_GXB}	Supplies power to the transceiver PMA TX, PMA RX, and clocking	—	1.21	V
V_{CCH_GXB}	Supplies power to the transceiver PMA output (TX) buffer	—	1.8	V
T_J	Operating junction temperature	-55	125	°C
T_{STG}	Storage temperature (no bias)	-65	150	°C

[Table 1-2](#) lists the absolute maximum ratings for Arria II GZ devices.

Table 1-2. Absolute Maximum Ratings for Arria II GZ Devices (Part 1 of 2)

Symbol	Description	Minimum	Maximum	Unit
V_{CC}	Supplies power to the core, periphery, I/O registers, PCIe HIP block, and transceiver PCS	-0.5	1.35	V
V_{CCCB}	Power supply to the configuration RAM bits	-0.5	1.8	V
V_{CCPGM}	Supplies power to the configuration pins	-0.5	3.75	V
V_{CCAUX}	Auxiliary supply	-0.5	3.75	V
V_{CCBAT}	Supplies battery back-up power for design security volatile key register	-0.5	3.75	V
V_{CCPD}	Supplies power to the I/O pre-drivers, differential input buffers, and MSEL circuitry	-0.5	3.75	V
V_{CCIO}	Supplies power to the I/O banks	-0.5	3.9	V
V_{CC_CLKIN}	Supplies power to the differential clock input	-0.5	3.75	V
V_{CCD_PLL}	Supplies power to the digital portions of the PLL	-0.5	1.35	V
V_{CCA_PLL}	Supplies power to the analog portions of the PLL and device-wide power management circuitry	-0.5	3.75	V
V_I	DC input voltage	-0.5	4.0	V
I_{OUT}	DC output current, per pin	-25	40	mA

Table 1–2. Absolute Maximum Ratings for Arria II GZ Devices (Part 2 of 2)

Symbol	Description	Minimum	Maximum	Unit
V _{CCA_L}	Supplies transceiver high voltage power (left side)	-0.5	3.75	V
V _{CCA_R}	Supplies transceiver high voltage power (right side)	-0.5	3.75	V
V _{CCHIP_L}	Supplies transceiver HIP digital power (left side)	-0.5	1.35	V
V _{CCR_L}	Supplies receiver power (left side)	-0.5	1.35	V
V _{CCR_R}	Supplies receiver power (right side)	-0.5	1.35	V
V _{CCT_L}	Supplies transmitter power (left side)	-0.5	1.35	V
V _{CCT_R}	Supplies transmitter power (right side)	-0.5	1.35	V
V _{CCL_GXBLn} (1)	Supplies power to the transceiver PMA TX, PMA RX, and clocking (left side)	-0.5	1.35	V
V _{CCL_GXBRn} (1)	Supplies power to the transceiver PMA TX, PMA RX, and clocking (right side)	-0.5	1.35	V
V _{CCH_GXBLn} (1)	Supplies power to the transceiver PMA output (TX) buffer (left side)	-0.5	1.8	V
V _{CCH_GXBRn} (1)	Supplies power to the transceiver PMA output (TX) buffer (right side)	-0.5	1.8	V
T _J	Operating junction temperature	-55	125	°C
T _{STG}	Storage temperature (no bias)	-65	150	°C

Note to Table 1–2:

(1) n = 0, 1, or 2.

Maximum Allowed Overshoot and Undershoot Voltage

During transitions, input signals may overshoot to the voltage shown in Table 1–3 and undershoot to –2.0 V for magnitude of currents less than 100 mA and periods shorter than 20 ns.

Table 1–3 lists the Arria II GX and GZ maximum allowed input overshoot voltage and the duration of the overshoot voltage as a percentage over the device lifetime. The maximum allowed overshoot duration is specified as a percentage of high-time over the lifetime of the device. A DC signal is equivalent to 100% duty cycle. For example, a signal that overshoots to 4.3 V can only be at 4.3 V for 5.41% over the lifetime of the device; for a device lifetime of 10 years, this amounts to 5.41/10ths of a year.

Table 1-11. OCT With and Without Calibration Specification for Arria II GX Device I/Os (Note 1) (Part 2 of 2)

Symbol	Description	Conditions (V)	Calibration Accuracy		Unit
			Commercial	Industrial	
50- Ω R_S 3.0, 2.5, 1.8, 1.5, 1.2	50- Ω series OCT with calibration	$V_{CCIO} = 3.0, 2.5,$ 1.8, 1.5, 1.2	± 10	± 10	%
100- Ω R_D 2.5	100- Ω differential OCT without calibration	$V_{CCIO} = 2.5$	± 30	± 30	%

Note to Table 1-11:

(1) OCT with calibration accuracy is valid at the time of calibration only.

Table 1-12 lists the OCT termination calibration accuracy specifications for Arria II GZ devices.

Table 1-12. OCT with Calibration Accuracy Specifications for Arria II GZ Devices (Note 1)

Symbol	Description	Conditions (V)	Calibration Accuracy			Unit
			C2	C3,I3	C4,I4	
25- Ω R_S 3.0, 2.5, 1.8, 1.5, 1.2 (2)	25- Ω series OCT with calibration	$V_{CCIO} = 3.0, 2.5,$ 1.8, 1.5, 1.2	± 8	± 8	± 8	%
50- Ω R_S 3.0, 2.5, 1.8, 1.5, 1.2	50- Ω internal series OCT with calibration	$V_{CCIO} = 3.0, 2.5,$ 1.8, 1.5, 1.2	± 8	± 8	± 8	%
50- Ω R_T 2.5, 1.8, 1.5, 1.2	50- Ω internal parallel OCT with calibration	$V_{CCIO} = 2.5, 1.8,$ 1.5, 1.2	± 10	± 10	± 10	%
20- Ω , 40- Ω , and 60- Ω R_S 3.0, 2.5, 1.8, 1.5, 1.2 (3)	20- Ω , 40- Ω and 60- Ω R_S expanded range for internal series OCT with calibration	$V_{CCIO} = 3.0, 2.5,$ 1.8, 1.5, 1.2	± 10	± 10	± 10	%
25- Ω $R_{S_left_shift}$ 3.0, 2.5, 1.8, 1.5, 1.2	25- Ω $R_{S_left_shift}$ internal left shift series OCT with calibration	$V_{CCIO} = 3.0, 2.5,$ 1.8, 1.5, 1.2	± 10	± 10	± 10	%

Notes to Table 1-12:

- (1) OCT calibration accuracy is valid at the time of calibration only.
 (2) 25- Ω R_S is not supported for 1.5 V and 1.2 V in Row I/O.
 (3) 20- Ω R_S is not supported for 1.5 V and 1.2 V in Row I/O.

The calibration accuracy for calibrated series and parallel OCTs are applicable at the moment of calibration. When process, voltage, and temperature (PVT) conditions change after calibration, the tolerance may change.

Table 1-13 lists the Arria II GZ OCT without calibration resistance tolerance to PVT changes.

Table 1-13. OCT Without Calibration Resistance Tolerance Specifications for Arria II GZ Devices

Symbol	Description	Conditions (V)	Resistance Tolerance		Unit
			C3,I3	C4,I4	
25-Ω R _S 3.0 and 2.5	25-Ω internal series OCT without calibration	V _{CCIO} = 3.0, 2.5	± 40	± 40	%
25-Ω R _S 1.8 and 1.5	25-Ω internal series OCT without calibration	V _{CCIO} = 1.8, 1.5	± 40	± 40	%
25-Ω R _S 1.2	25-Ω internal series OCT without calibration	V _{CCIO} = 1.2	± 50	± 50	%
50-Ω R _S 3.0 and 2.5	50-Ω internal series OCT without calibration	V _{CCIO} = 3.0, 2.5	± 40	± 40	%
50-Ω R _S 1.8 and 1.5	50-Ω internal series OCT without calibration	V _{CCIO} = 1.8, 1.5	± 40	± 40	%
50-Ω R _S 1.2	50-Ω internal series OCT without calibration	V _{CCIO} = 1.2	± 50	± 50	%
100-Ω R _D 2.5	100-Ω internal differential OCT	V _{CCIO} = 2.5	± 25	± 25	%

OCT calibration is automatically performed at power up for OCT-enabled I/Os. When voltage and temperature conditions change after calibration, the resistance may change. Use Equation 1-1 and Table 1-14 to determine the OCT variation when voltage and temperature vary after power-up calibration for Arria II GX and GZ devices.

Equation 1-1. OCT Variation (Note 1)

$$R_{OCT} = R_{SCAL} \left(1 + \left\langle \frac{dR}{dT} \times \Delta T \right\rangle \pm \left\langle \frac{dR}{dV} \times \Delta V \right\rangle \right)$$

Notes to Equation 1-1:

- (1) R_{OCT} value calculated from Equation 1-1 shows the range of OCT resistance with the variation of temperature and V_{CCIO}.

Table 1-19 lists the weak pull-up resistor values for Arria II GZ devices.

Table 1-19. Internal Weak Pull-Up Resistor for Arria II GZ Devices (Note 1), (2)

Symbol	Description	Conditions	Min	Typ	Max	Unit
R_{PU}	Value of the I/O pin pull-up resistor before and during configuration, as well as user mode if the programmable pull-up resistor option is enabled.	$V_{CCIO} = 3.0\text{ V} \pm 5\%$ (3)	—	25	—	$k\Omega$
		$V_{CCIO} = 2.5\text{ V} \pm 5\%$ (3)	—	25	—	$k\Omega$
		$V_{CCIO} = 1.8\text{ V} \pm 5\%$ (3)	—	25	—	$k\Omega$
		$V_{CCIO} = 1.5\text{ V} \pm 5\%$ (3)	—	25	—	$k\Omega$
		$V_{CCIO} = 1.2\text{ V} \pm 5\%$ (3)	—	25	—	$k\Omega$

Notes to Table 1-19:

- (1) All I/O pins have an option to enable weak pull-up except configuration, test, and JTAG pins.
- (2) The internal weak pull-down feature is only available for the JTAG TCK pin. The typical value for this internal weak pull-down resistor is approximately $25\text{ k}\Omega$.
- (3) Pin pull-up resistance values may be lower if an external source drives the pin higher than V_{CCIO} .

Hot Socketing

Table 1-20 lists the hot-socketing specification for Arria II GX and GZ devices.

Table 1-20. Hot Socketing Specifications for Arria II Devices

Symbol	Description	Maximum
$I_{IOPIN(DC)}$	DC current per I/O pin	$300\text{ }\mu\text{A}$
$I_{IOPIN(AC)}$	AC current per I/O pin	8 mA (1)
$I_{XCVR TX(DC)}$	DC current per transceiver TX pin	100 mA
$I_{XCVR RX(DC)}$	DC current per transceiver RX pin	50 mA

Note to Table 1-20:

- (1) The I/O ramp rate is 10 ns or more. For ramp rates faster than 10 ns , $|I_{IOPIN}| = C\text{ dv/dt}$, in which “C” is I/O pin capacitance and “dv/dt” is slew rate.

Schmitt Trigger Input

The Arria II GX device supports Schmitt trigger input on the TDI, TMS, TCK, nSTATUS, nCONFIG, nCE, CONF_DONE, and DCLK pins. A Schmitt trigger feature introduces hysteresis to the input signal for improved noise immunity, especially for signals with slow edge rates.

Table 1-21 lists the hysteresis specifications across the supported V_{CCIO} range for Schmitt trigger inputs in Arria II GX devices.

Table 1-21. Schmitt Trigger Input Hysteresis Specifications for Arria II GX Devices

Symbol	Description	Condition (V)	Minimum	Unit
$V_{Schmitt}$	Hysteresis for Schmitt trigger input	$V_{CCIO} = 3.3$	220	mV
		$V_{CCIO} = 2.5$	180	mV
		$V_{CCIO} = 1.8$	110	mV
		$V_{CCIO} = 1.5$	70	mV

I/O Standard Specifications

Table 1-22 through Table 1-35 list input voltage (V_{IH} and V_{IL}), output voltage (V_{OH} and V_{OL}), and current drive characteristics (I_{OH} and I_{OL}) for various I/O standards supported by the Arria II device family. They also show the Arria II device family I/O standard specifications. V_{OL} and V_{OH} values are valid at the corresponding I_{OH} and I_{OL} , respectively.



For an explanation of terms used in Table 1-22 through Table 1-35, refer to “Glossary” on page 1-74.

Table 1-22 lists the single-ended I/O standards for Arria II GX devices.

Table 1-22. Single-Ended I/O Standards for Arria II GX Devices

I/O Standard	V_{CCIO} (V)			V_{IL} (V)		V_{IH} (V)		V_{OL} (V)	V_{OH} (V)	I_{OL} (mA)	I_{OH} (mA)
	Min	Typ	Max	Min	Max	Min	Max	Max	Min		
3.3 V LVTTTL	3.135	3.3	3.465	-0.3	0.8	1.7	3.6	0.45	2.4	4	-4
3.3 V LVCMOS	3.135	3.3	3.465	-0.3	0.8	1.7	3.6	0.2	$V_{CCIO} - 0.2$	2	-2
3.0 V LVTTTL	2.85	3	3.15	-0.3	0.8	1.7	$V_{CCIO} + 0.3$	0.45	2.4	4	-4
3.0 V LVCMOS	2.85	3	3.15	-0.3	0.8	1.7	$V_{CCIO} + 0.3$	0.2	$V_{CCIO} - 0.2$	0.1	-0.1
2.5 V LVCMOS	2.375	2.5	2.625	-0.3	0.7	1.7	$V_{CCIO} + 0.3$	0.4	2	1	-1
1.8 V LVCMOS	1.71	1.8	1.89	-0.3	$0.35 \times V_{CCIO}$	$0.65 \times V_{CCIO}$	$V_{CCIO} + 0.3$	0.45	$V_{CCIO} - 0.45$	2	-2
1.5 V LVCMOS	1.425	1.5	1.575	-0.3	$0.35 \times V_{CCIO}$	$0.65 \times V_{CCIO}$	$V_{CCIO} + 0.3$	$0.25 \times V_{CCIO}$	$0.75 \times V_{CCIO}$	2	-2
1.2 V LVCMOS	1.14	1.2	1.26	-0.3	$0.35 \times V_{CCIO}$	$0.65 \times V_{CCIO}$	$V_{CCIO} + 0.3$	$0.25 \times V_{CCIO}$	$0.75 \times V_{CCIO}$	2	-2
3.0-V PCI	2.85	3	3.15	—	$0.3 \times V_{CCIO}$	$0.5 \times V_{CCIO}$	$V_{CCIO} + 0.3$	$0.1 \times V_{CCIO}$	$0.9 \times V_{CCIO}$	1.5	-0.5
3.0-V PCI-X	2.85	3	3.15	—	$0.35 \times V_{CCIO}$	$0.5 \times V_{CCIO}$	$V_{CCIO} + 0.3$	$0.1 \times V_{CCIO}$	$0.9 \times V_{CCIO}$	1.5	-0.5

Table 1-23 lists the single-ended I/O standards for Arria II GZ devices.

Table 1-23. Single-Ended I/O Standards for Arria II GZ Devices (Part 1 of 2)

I/O Standard	V_{CCIO} (V)			V_{IL} (V)		V_{IH} (V)		V_{OL} (V)	V_{OH} (V)	I_{OL} (mA)	I_{OH} (mA)
	Min	Typ	Max	Min	Max	Min	Max	Max	Min		
LVTTTL	2.85	3	3.15	-0.3	0.8	1.7	3.6	0.4	2.4	2	-2
LVCMOS	2.85	3	3.15	-0.3	0.8	1.7	3.6	0.2	$V_{CCIO} - 0.2$	0.1	-0.1
2.5 V	2.375	2.5	2.625	-0.3	0.7	1.7	3.6	0.4	2	1	-1
1.8 V	1.71	1.8	1.89	-0.3	$0.35 \times V_{CCIO}$	$0.65 \times V_{CCIO}$	$V_{CCIO} + 0.3$	0.45	$V_{CCIO} - 0.45$	2	-2
1.5 V	1.425	1.5	1.575	-0.3	$0.35 \times V_{CCIO}$	$0.65 \times V_{CCIO}$	$V_{CCIO} + 0.3$	$0.25 \times V_{CCIO}$	$0.75 \times V_{CCIO}$	2	-2

Table 1–35. Transceiver Specifications for Arria II GZ Devices (Part 4 of 5)

Symbol/ Description	Conditions	–C3 and –I3 (1)			–C4 and –I4			Unit
		Min	Typ	Max	Min	Typ	Max	
Transmitter								
Supported I/O Standards	1.5-V PCML							
Data rate (14)	—	600	—	6375	600	—	3750	Mbps
V _{OCM}	0.65 V setting	—	650	—	—	650	—	mV
Differential on-chip termination resistors	85–Ω setting	85 ± 15%			85 ± 15%			Ω
	100–Ω setting	100 ± 15%			100 ± 15%			Ω
	120–Ω setting	120 ± 15%			120 ± 15%			Ω
	150–Ω setting	150 ± 15%			150 ± 15%			Ω
Differential and common mode return loss	PCIe Gen1 and Gen2 (TX V _{OD} =4), XAUI (TX V _{OD} =6), HiGig+ (TX V _{OD} =6), CEI SR/LR (TX V _{OD} =8), SRIO SR (V _{OD} =6), SRIO LR (V _{OD} =8), CPRI LV (V _{OD} =6), CPRI HV (V _{OD} =2), OBSAI (V _{OD} =6), SATA (V _{OD} =4),	Compliant						—
Rise time (15)	—	50	—	200	50	—	200	ps
Fall time (15)	—	50	—	200	50	—	200	ps
Intra-differential pair skew	—	—	—	15	—	—	15	ps
Intra-transceiver block transmitter channel-to-channel skew	×4 PMA and PCS bonded mode Example: XAUI, PCIe ×4, Basic ×4	—	—	120	—	—	120	ps
Inter-transceiver block transmitter channel-to-channel skew	×8 PMA and PCS bonded mode Example: PCIe ×8, Basic ×8	—	—	500	—	—	500	ps
CMU0 PLL and CMU1 PLL								
Supported Data Range	—	600	—	6375	600	—	3750	Mbps
pll_powerdown minimum pulse width (tpll_powerdown)	—	1			1			μs
CMU PLL lock time from pll_powerdown de-assertion	—	—	—	100	—	—	100	μs

Table 1–37 lists the typical V_{OD} for TX term that equals $100\ \Omega$ for Arria II GX and GZ devices.

Table 1–37. Typical V_{OD} Setting, TX Termination = $100\ \Omega$ for Arria II Devices

Quartus II Setting	V_{OD} Setting (mV)
1	400
2	600
3 (Arria II GZ)	700
4	800
5	900
6	1000
7	1200

Table 1–38 lists the typical transmitter pre-emphasis levels in dB for the first post tap under the following conditions: low-frequency data pattern (five 1s and five 0s) at 6.375 Gbps. The levels listed in Table 1–38 are a representation of possible pre-emphasis levels under these specified conditions only, the pre-emphasis levels may change with data pattern and data rate.

To predict the pre-emphasis level for your specific data rate and pattern, run simulations using the Arria II GX HSSI HSPICE models.

Table 1–38. Transmitter Pre-Emphasis Levels for Arria II GX Devices

Arria II GX (Quartus II Software) First Post Tap Setting	Arria II GX (Quartus II Software) VOD Setting						Unit
	1	2	4	5	6	7	
0 (off)	0	0	0	0	0	0	—
1	0.7	0	0	0	0	0	dB
2	2.7	1.2	0.3	0	0	0	dB
3	4.9	2.4	1.2	0.8	0.5	0.2	dB
4	7.5	3.8	2.1	1.6	1.2	0.6	dB
5	—	5.3	3.1	2.4	1.8	1.1	dB
6	—	7	4.3	3.3	2.7	1.7	dB

Table 1–40. Transceiver Block Jitter Specifications for Arria II GX Devices (Note 1) (Part 3 of 10)

Symbol/ Description	Conditions	I3			C4			C5, I5			C6			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
PCIe Receiver Jitter Tolerance (4)														
Total jitter at 2.5 Gbps (Gen1)	Compliance pattern	> 0.6			> 0.6			> 0.6			> 0.6			UI
PCIe (Gen 1) Electrical Idle Detect Threshold (9)														
VRX-IDLE-DETDIFF (p-p)	Compliance pattern	65	—	175	65	—	175	65	—	175	65	—	175	mV
Serial RapidIO® (SRIO) Transmit Jitter Generation (5)														
Deterministic jitter (peak-to-peak)	Data Rate = 1.25, 2.5, 3.125 Gbps Pattern = CJPAT	—	—	0.17	—	—	0.17	—	—	0.17	—	—	0.17	UI
Total jitter (peak-to-peak)	Data Rate = 1.25, 2.5, 3.125 Gbps Pattern = CJPAT	—	—	0.35	—	—	0.35	—	—	0.35	—	—	0.35	UI
SRIO Receiver Jitter Tolerance (5)														
Deterministic jitter tolerance (peak-to-peak)	Data Rate = 1.25, 2.5, 3.125 Gbps Pattern = CJPAT	> 0.37			> 0.37			> 0.37			> 0.37			UI
Combined deterministic and random jitter tolerance (peak-to-peak)	Data Rate = 1.25, 2.5, 3.125 Gbps Pattern = CJPAT	> 0.55			> 0.55			> 0.55			> 0.55			UI
Sinusoidal jitter tolerance (peak-to-peak)	Jitter frequency = 22.1 KHz Data rate = 1.25, 2.5, 3.125 Gbps Pattern = CJPAT	> 8.5			> 8.5			> 8.5			> 8.5			UI
	Jitter frequency = 1.875 MHz Data rate = 1.25, 2.5, 3.125 Gbps Pattern = CJPAT	> 0.1			> 0.1			> 0.1			> 0.1			UI
	Jitter frequency = 20 MHz Data rate = 1.25, 2.5, 3.125 Gbps Pattern = CJPAT	> 0.1			> 0.1			> 0.1			> 0.1			UI
GIGE Transmit Jitter Generation (6)														
Deterministic jitter (peak-to-peak)	Pattern = CRPAT	—	—	0.14	—	—	0.14	—	—	0.14	—	—	0.14	UI

Table 1–41. Transceiver Block Jitter Specifications for Arria II GZ Devices (Note 1), (2) (Part 2 of 7)

Symbol/ Description	Conditions	–C3 and –I3			–C4 and –I4			Unit
		Min	Typ	Max	Min	Typ	Max	
Jitter tolerance at 2488.32 Mbps	Jitter frequency = 0.06 KHz Pattern = PRBS15	> 15			> 15			UI
	Jitter frequency = 100 KHZ Pattern = PRBS15	> 1.5			> 1.5			UI
	Jitter frequency = 1 MHz Pattern = PRBS15	> 0.15			> 0.15			UI
	Jitter frequency = 10 MHz Pattern = PRBS15	> 0.15			> 0.15			UI
Fibre Channel Transmit Jitter Generation (4), (5)								
Total jitter FC-1	Pattern = CRPAT	—	—	0.23	—	—	0.23	UI
Deterministic jitter FC-1	Pattern = CRPAT	—	—	0.11	—	—	0.11	UI
Total jitter FC-2	Pattern = CRPAT	—	—	0.33	—	—	0.33	UI
Deterministic jitter FC-2	Pattern = CRPAT	—	—	0.2	—	—	0.2	UI
Total jitter FC-4	Pattern = CRPAT	—	—	0.52	—	—	0.52	UI
Deterministic jitter FC-4	Pattern = CRPAT	—	—	0.33	—	—	0.33	UI
Fibre Channel Receiver Jitter Tolerance (4), (6)								
Deterministic jitter FC-1	Pattern = CJTPAT	> 0.37			> 0.37			UI
Random jitter FC-1	Pattern = CJTPAT	> 0.31			> 0.31			UI
Sinusoidal jitter FC-1	Fc/25000	> 1.5			> 1.5			UI
	Fc/1667	> 0.1			> 0.1			UI
Deterministic jitter FC-2	Pattern = CJTPAT	> 0.33			> 0.33			UI
Random jitter FC-2	Pattern = CJTPAT	> 0.29			> 0.29			UI
Sinusoidal jitter FC-2	Fc/25000	> 1.5			> 1.5			UI
	Fc/1667	> 0.1			> 0.1			UI
Deterministic jitter FC-4	Pattern = CJTPAT	> 0.33			> 0.33			UI
Random jitter FC-4	Pattern = CJTPAT	> 0.29			> 0.29			UI
Sinusoidal jitter FC-4	Fc/25000	> 1.5			> 1.5			UI
	Fc/1667	> 0.1			> 0.1			UI
XAUI Transmit Jitter Generation (7)								
Total jitter at 3.125 Gbps	Pattern = CJPAT	—	—	0.3	—	—	0.3	UI
Deterministic jitter at 3.125 Gbps	Pattern = CJPAT	—	—	0.17	—	—	0.17	UI
XAUI Receiver Jitter Tolerance (7)								
Total jitter	—	> 0.65			> 0.65			UI
Deterministic jitter	—	> 0.37			> 0.37			UI

Table 1–41. Transceiver Block Jitter Specifications for Arria II GZ Devices (Note 1), (2) (Part 3 of 7)

Symbol/ Description	Conditions	–C3 and –I3			–C4 and –I4			Unit
		Min	Typ	Max	Min	Typ	Max	
Peak-to-peak jitter	Jitter frequency = 22.1 KHz	> 8.5			> 8.5			UI
Peak-to-peak jitter	Jitter frequency = 1.875 MHz	> 0.1			> 0.1			UI
Peak-to-peak jitter	Jitter frequency = 20 MHz	> 0.1			> 0.1			UI
PCIe Transmit Jitter Generation (8)								
Total jitter at 2.5 Gbps (Gen1)— x1, x4, and x8	Compliance pattern	—	—	0.25	—	—	0.25	UI
Total jitter at 5 Gbps (Gen2)— x1, x4, and x8	Compliance pattern	—	—	0.25	—	—	—	UI
PCIe Receiver Jitter Tolerance (8)								
Total jitter at 2.5 Gbps (Gen1)	Compliance pattern	> 0.6			> 0.6			UI
Total jitter at 5 Gbps (Gen2)	Compliance pattern	Not supported			Not supported			UI
PCIe (Gen 1) Electrical Idle Detect Threshold								
V _{RX-IDLE-DETDIFFp-p} (9)	Compliance pattern	65	—	175	65	—	175	UI
SRIO Transmit Jitter Generation (10)								
Deterministic jitter (peak-to-peak)	Data rate = 1.25, 2.5, 3.125 Gbps Pattern = CJPAT	—	—	0.17	—	—	0.17	UI
Total jitter (peak-to-peak)	Data rate = 1.25, 2.5, 3.125 Gbps Pattern = CJPAT	—	—	0.35	—	—	0.35	UI
SRIO Receiver Jitter Tolerance (10)								
Deterministic jitter tolerance (peak-to-peak)	Data rate = 1.25, 2.5, 3.125 Gbps Pattern = CJPAT	> 0.37			> 0.37			UI
Combined deterministic and random jitter tolerance (peak-to- peak)	Data rate = 1.25, 2.5, 3.125 Gbps Pattern = CJPAT	> 0.55			> 0.55			UI
Sinusoidal jitter tolerance (peak- to-peak)	Jitter frequency = 22.1 KHz Data rate = 1.25, 2.5, 3.125 Gbps Pattern = CJPAT	> 8.5			> 8.5			UI
	Jitter frequency = 1.875 MHz Data rate = 1.25, 2.5, 3.125 Gbps Pattern = CJPAT	> 0.1			> 0.1			UI
	Jitter frequency = 20 MHz Data rate = 1.25, 2.5, 3.125 Gbps Pattern = CJPAT	> 0.1			> 0.1			UI
GIGE Transmit Jitter Generation (11)								
Deterministic jitter (peak-to-peak)	Pattern = CRPAT	—	—	0.14	—	—	0.14	UI
Total jitter (peak-to-peak)	Pattern = CRPAT	—	—	0.279	—	—	0.279	UI

Table 1–41. Transceiver Block Jitter Specifications for Arria II GZ Devices (Note 1), (2) (Part 6 of 7)

Symbol/ Description	Conditions	–C3 and –I3			–C4 and –I4			Unit
		Min	Typ	Max	Min	Typ	Max	
Deterministic jitter at 3.0 Gbps (G2)	Pattern = CJPAT	—	—	0.35	—	—	0.35	UI
Total jitter at 6.0 Gbps (G3)	Pattern = CJPAT	—	—	0.25	—	—	0.25	UI
Random jitter at 6.0 Gbps (G3)	Pattern = CJPAT	—	—	0.15	—	—	0.15	UI
SAS Receiver Jitter Tolerance (13)								
Total jitter tolerance at 1.5 Gbps (G1)	Pattern = CJPAT	—	—	0.65	—	—	0.65	UI
Deterministic jitter tolerance at 1.5 Gbps (G1)	Pattern = CJPAT	—	—	0.35	—	—	0.35	UI
Sinusoidal jitter tolerance at 1.5 Gbps (G1)	Jitter frequency = 900 KHz to 5 MHz Pattern = CJTPAT BER = 1E-12	> 0.1			> 0.1			UI
CPRI Transmit Jitter Generation (14)								
Total jitter	E.6.HV, E.12.HV Pattern = CJPAT	—	—	0.279	—	—	0.279	UI
	E.6.LV, E.12.LV, E.24.LV, E.30.LV Pattern = CJPAT	—	—	0.35	—	—	0.35	UI
Deterministic jitter	E.6.HV, E.12.HV Pattern = CJPAT	—	—	0.14	—	—	0.14	UI
	E.6.LV, E.12.LV, E.24.LV, E.30.LV Pattern = CJPAT	—	—	0.17	—	—	0.17	UI
CPRI Receiver Jitter Tolerance (14)								
Total jitter tolerance	E.6.HV, E.12.HV Pattern = CJPAT	> 0.66			> 0.66			UI
Deterministic jitter tolerance	E.6.HV, E.12.HV Pattern = CJPAT	> 0.4			> 0.4			UI
Total jitter tolerance	E.6.LV, E.12.LV, E.24.LV, E.30.LV Pattern = CJPAT	> 0.65			> 0.65			UI
Deterministic jitter tolerance	E.6.LV, E.12.LV, E.24.LV, E.30.LV Pattern = CJPAT	> 0.37			> 0.37			UI
Combined deterministic and random jitter tolerance	E.6.LV, E.12.LV, E.24.LV, E.30.LV Pattern = CJPAT	> 0.55			> 0.55			UI
OBSAI Transmit Jitter Generation (15)								
Total jitter at 768 Mbps, 1536 Mbps, and 3072 Mbps	REFCLK = 153.6 MHz Pattern CJPAT	—	—	0.35	—	—	0.35	UI
Deterministic jitter at 768 MBps, 1536 Mbps, and 3072 Mbps	REFCLK = 153.6 MHz Pattern CJPAT	—	—	0.17	—	—	0.17	UI

Table 1–41. Transceiver Block Jitter Specifications for Arria II GZ Devices (Note 1), (2) (Part 7 of 7)

Symbol/ Description	Conditions	–C3 and –I3			–C4 and –I4			Unit
		Min	Typ	Max	Min	Typ	Max	
OBSAI Receiver Jitter Tolerance (15)								
Deterministic jitter tolerance at 768 Mbps, 1536 Mbps, and 3072 Mbps	Pattern = CJPAT	> 0.37			> 0.37			UI
Combined deterministic and random jitter tolerance at 768 Mbps, 1536 Mbps, and 3072 Mbps	Pattern = CJPAT	> 0.55			> 0.55			UI
Sinusoidal jitter tolerance at 768 Mbps	Jitter frequency = 5.4 KHz Pattern = CJPAT	> 8.5			> 8.5			UI
	Jitter frequency = 460 MHz to 20 MHz Pattern = CJPAT	> 0.1			> 0.1			UI
Sinusoidal jitter tolerance at 1536 Mbps	Jitter frequency = 10.9 KHz Pattern = CJPAT	> 8.5			> 8.5			UI
	Jitter frequency = 921.6 MHz to 20 MHz Pattern = CJPAT	> 0.1			> 0.1			UI
Sinusoidal jitter tolerance at 3072 Mbps	Jitter frequency = 21.8 KHz Pattern = CJPAT	> 8.5			> 8.5			UI
	Jitter frequency = 1843.2 MHz to 20 MHz Pattern = CJPAT	> 0.1			> 0.1			UI

Notes to Table 1–41:

- (1) Dedicated `refclk` pins were used to drive the input reference clocks.
- (2) The jitter numbers are valid for the stated conditions only.
- (3) The jitter numbers for SONET/SDH are compliant to the GR-253-CORE Issue 3 Specification.
- (4) The jitter numbers for Fibre Channel are compliant to the FC-P1-4 Specification revision 6.10.
- (5) The Fibre Channel transmitter jitter generation numbers are compliant to the specification at the δ_T inter operability point.
- (6) The Fibre Channel receiver jitter tolerance numbers are compliant to the specification at the δ_R interpretability point.
- (7) The jitter numbers for XAUI are compliant to the IEEE802.3ae-2002 Specification.
- (8) The jitter numbers for PCIe are compliant to the PCIe Base Specification 2.0.
- (9) Arria II GZ PCIe receivers are compliant to this specification provided the $V_{TX-CM-DC-ACTIVEIDLE-DELTA}$ of the upstream transmitter is less than 50 mV.
- (10) The jitter numbers for SRIO are compliant to the RapidIO Specification 1.3.
- (11) The jitter numbers for GIGE are compliant to the IEEE802.3-2002 Specification.
- (12) The HD-SDI and 3G-SDI jitter numbers are compliant to the SMPTE292M and SMPTE424M Specifications.
- (13) The jitter numbers for Serial Attached SCSI (SAS) are compliant to the SAS-2.1 Specification.
- (14) The jitter numbers for CPRI are compliant to the CPRI Specification V3.0.
- (15) The jitter numbers for OBSAI are compliant to the OBSAI RP3 Specification V4.1.

Core Performance Specifications for the Arria II Device Family

This section describes the clock tree, phase-locked loop (PLL), digital signal processing (DSP), embedded memory, configuration, and JTAG specifications for Arria II GX and GZ devices.

Clock Tree Specifications

Table 1-42 lists the clock tree specifications for Arria II GX devices.

Table 1-42. Clock Tree Performance for Arria II GX Devices

Clock Network	Performance			Unit
	I3, C4	C5,I5	C6	
GCLK and RCLK	500	500	400	MHz
PCLK	420	350	280	MHz

Table 1-43 lists the clock tree specifications for Arria II GZ devices.

Table 1-43. Clock Tree Performance for Arria II GZ Devices

Clock Network	Performance		Unit
	-C3 and -I3	-C4 and -I4	
GCLK and RCLK	700	500	MHz
PCLK	500	450	MHz

PLL Specifications

Table 1-44 lists the PLL specifications for Arria II GX devices.

Table 1-44. PLL Specifications for Arria II GX Devices (Part 1 of 3)

Symbol	Description	Min	Typ	Max	Unit
f_{IN}	Input clock frequency (from clock input pins residing in right/top/bottom banks) (-4 Speed Grade)	5	—	670 (1)	MHz
	Input clock frequency (from clock input pins residing in right/top/bottom banks) (-5 Speed Grade)	5	—	622 (1)	MHz
	Input clock frequency (from clock input pins residing in right/top/bottom banks) (-6 Speed Grade)	5	—	500 (1)	MHz
f_{INPFD}	Input frequency to the PFD	5	—	325	MHz
f_{VCO}	PLL VCO operating Range (2)	600	—	1,400	MHz
f_{INDUTY}	Input clock duty cycle	40	—	60	%
$f_{EINDUTY}$	External feedback clock input duty cycle	40	—	60	%
t_{INCCJ} (3), (4)	Input clock cycle-to-cycle jitter (Frequency ≥ 100 MHz)	—	—	0.15	UI (p-p)
	Input clock cycle-to-cycle jitter (Frequency ≤ 100 MHz)	—	—	± 750	ps (p-p)

Table 1-55. DPA Lock Time Specifications for Arria II Devices (Note 1), (2), (3)

Standard	Training Pattern	Number of Data Transitions in One Repetition of the Training Pattern	Number of Repetitions per 256 Data Transitions (4)	Maximum
SPI-4	00000000001111111111	2	128	640 data transitions
Parallel Rapid I/O	00001111	2	128	640 data transitions
	10010000	4	64	640 data transitions
Miscellaneous	10101010	8	32	640 data transitions
	01010101	8	32	640 data transitions

Notes to Table 1-55:

- (1) The DPA lock time is for one channel.
- (2) One data transition is defined as a 0-to-1 or 1-to-0 transition.
- (3) The DPA lock time stated in the table applies to both commercial and industrial grade.
- (4) This is the number of repetitions for the stated training pattern to achieve the 256 data transitions.

Figure 1-5 shows the LVDS soft-CDR/DPA sinusoidal jitter tolerance specification for Arria II GZ devices at a data rate less than 1.25 Gbps and all the Arria II GX devices.

Figure 1-5. LVDS Soft-CDR/DPA Sinusoidal Jitter Tolerance Specification for All Arria II GX Devices and for Arria II GZ Devices at a Data Rate less than 1.25 Gbps

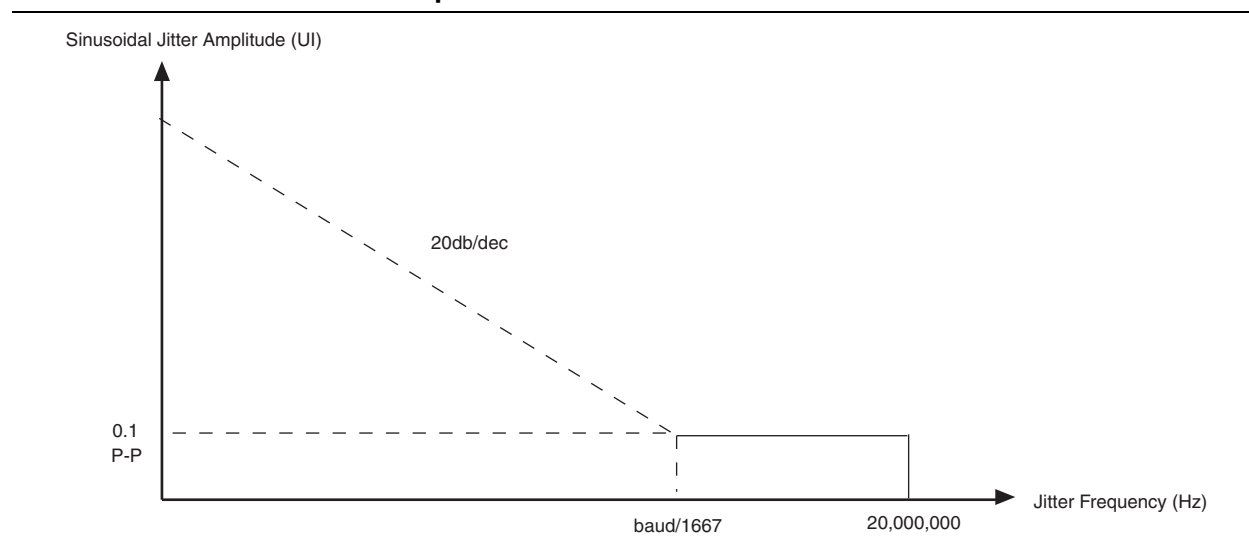


Figure 1-6 shows the LVDS soft-CDR/DPA sinusoidal jitter tolerance specification for Arria II GZ devices at 1.25 Gbps data rate.

Figure 1-6. LVDS Soft-CDR/DPA Sinusoidal Jitter Tolerance Specification for Arria II GZ Devices at a 1.25 Gbps Data Rate

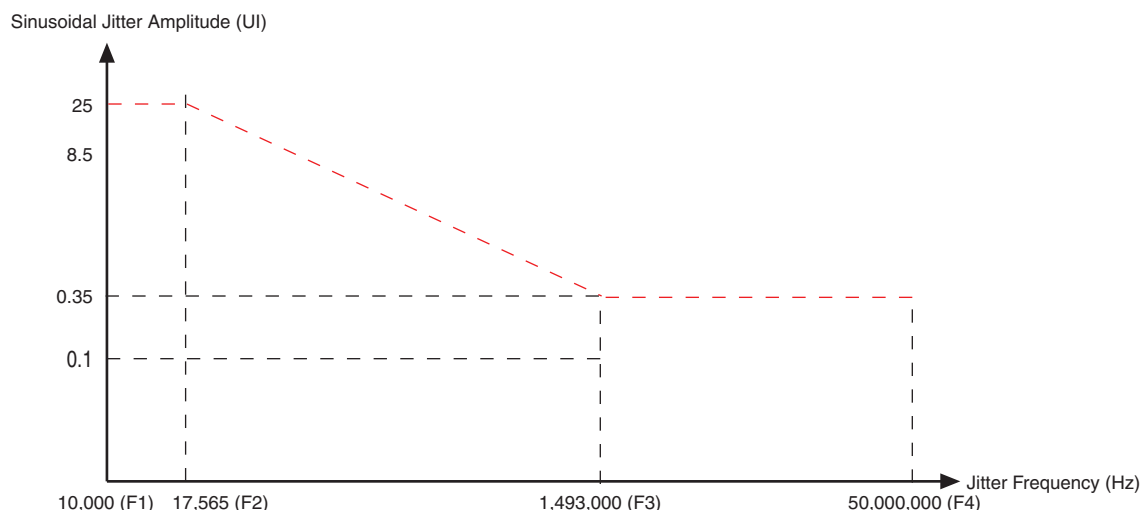


Table 1-56 lists the LVDS soft-CDR/DPA sinusoidal jitter tolerance specification for Arria II GZ devices at 1.25 Gbps data rate.

Table 1-56. LVDS Soft-CDR/DPA Sinusoidal Jitter Mask Values for Arria II GZ Devices at 1.25 Gbps Data Rate

Jitter Frequency (Hz)		Sinusoidal Jitter (UI)
F1	10,000	25.000
F2	17,565	25.000
F3	1,493,000	0.350
F4	50,000,000	0.350

External Memory Interface Specifications

 For the maximum clock rate supported for Arria II GX and GZ device family, refer to the [External Memory Interface Spec Estimator](#) page on the Altera website.

Table 1-57 lists the external memory interface specifications for Arria II GX devices.

Table 1-57. External Memory Interface Specifications for Arria II GX Devices (Part 1 of 2)

Frequency Mode	Frequency Range (MHz)			Resolution (°)	DQS Delay Buffer Mode ⁽¹⁾	Number of Delay Chains
	C4	I3, C5, I5	C6			
0	90-140	90-130	90-110	22.5	Low	16
1	110-180	110-170	110-150	30	Low	12
2	140-220	140-210	140-180	36	Low	10
3	170-270	170-260	170-220	45	Low	8
4	220-340	220-310	220-270	30	High	12

Table 1-63 lists the memory output clock jitter specifications for Arria II GZ devices.

Table 1-63. Memory Output Clock Jitter Specification for Arria II GZ Devices (Note 1), (2), (3)

Parameter	Clock Network	Symbol	-3		-4		Unit
			Min	Max	Min	Max	
Clock period jitter	Regional	$t_{JIT(per)}$	-55	55	-55	55	ps
Cycle-to-cycle period jitter	Regional	$t_{JIT(cc)}$	-110	110	-110	110	ps
Duty cycle jitter	Regional	$t_{JIT(duty)}$	-82.5	82.5	-82.5	82.5	ps
Clock period jitter	Global	$t_{JIT(per)}$	-82.5	82.5	-82.5	82.5	ps
Cycle-to-cycle period jitter	Global	$t_{JIT(cc)}$	-165	165	-165	165	ps
Duty cycle jitter	Global	$t_{JIT(duty)}$	-90	90	-90	90	ps

Notes to Table 1-63:

- (1) The memory output clock jitter measurements are for 200 consecutive clock cycles, as specified in the JEDEC DDR2/DDR3 SDRAM standard.
- (2) The clock jitter specification applies to memory output clock pins generated using differential signal-splitter and DDIO circuits clocked by a PLL output routed on a regional or global clock network as specified. Altera recommends using regional clock networks whenever possible.
- (3) The memory output clock jitter stated in Table 1-63 is applicable when an input jitter of 30 ps is applied.

Duty Cycle Distortion (DCD) Specifications

Table 1-64 lists the worst-case DCD specifications for Arria II GX devices.

Table 1-64. Duty Cycle Distortion on I/O Pins for Arria II GX Devices (Note 1)

Symbol	C4		I3, C5, I5		C6		Unit
	Min	Max	Min	Max	Min	Max	
Output Duty Cycle	45	55	45	55	45	55	%

Note to Table 1-64:

- (1) The DCD specification applies to clock outputs from the PLL, global clock tree, IOE driving dedicated, and general purpose I/O pins.

Table 1-65 lists the worst-case DCD specifications for Arria II GZ devices.

Table 1-65. Duty Cycle Distortion on I/O Pins for Arria II GZ Devices (Note 1)

Symbol	C3, I3		C4, I4		Unit
	Min	Max	Min	Max	
Output Duty Cycle	45	55	45	55	%

Note to Table 1-65:

- (1) The DCD specification applies to clock outputs from the PLL, global clock tree, IOE driving dedicated, and general purpose I/O pins.

IOE Programmable Delay

Table 1–66 lists the delay associated with each supported IOE programmable delay chain for Arria II GX devices.

Table 1–66. IOE Programmable Delay for Arria II GX Devices

Parameter	Available Settings (1)	Minimum Offset (2)	Maximum Offset								Unit
			Fast Model			Slow Model					
			I3	C4	I5	I3	C4	C5	I5	C6	
Output enable pin delay	7	0	0.413	0.442	0.413	0.814	0.713	0.796	0.801	0.873	ns
Delay from output register to output pin	7	0	0.339	0.362	0.339	0.671	0.585	0.654	0.661	0.722	ns
Input delay from pin to internal cell	52	0	1.494	1.607	1.494	2.895	2.520	2.733	2.775	2.944	ns
Input delay from pin to input register	52	0	1.493	1.607	1.493	2.896	2.503	2.732	2.774	2.944	ns
DQS bus to input register delay	4	0	0.074	0.076	0.074	0.140	0.124	0.147	0.147	0.167	ns

Notes to Table 1–66:

- (1) The available setting for every delay chain starts with zero and ends with the specified maximum number of settings.
- (2) The minimum offset represented in the table does not include intrinsic delay.

Table 1–67 lists the IOE programmable delay settings for Arria II GZ devices.

Table 1–67. IOE Programmable Delay for Arria II GZ Devices

Parameter	Available Settings <i>(1)</i>	Minimum Offset <i>(2)</i>	Maximum Offset						Unit
			Fast Model		Slow Model				
			Industrial	Commercial	C3	I3	C4	I4	
D1	15	0	0.462	0.505	0.795	0.801	0.857	0.864	ns
D2	7	0	0.234	0.232	0.372	0.371	0.407	0.405	ns
D3	7	0	1.700	1.769	2.927	2.948	3.157	3.178	ns
D4	15	0	0.508	0.554	0.882	0.889	0.952	0.959	ns
D5	15	0	0.472	0.500	0.799	0.817	0.875	0.882	ns
D6	6	0	0.186	0.195	0.319	0.321	0.345	0.347	ns

Notes to Table 1–67:

- (1) You can set this value in the Quartus II software by selecting **D1**, **D2**, **D3**, **D4**, **D5**, and **D6** in the **Assignment Name** column.
- (2) Minimum offset does not include the intrinsic delay.

Table 1-68. Glossary (Part 3 of 4)

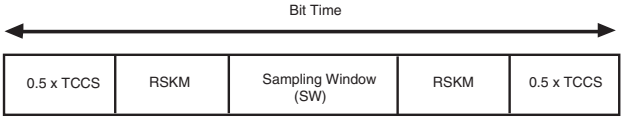
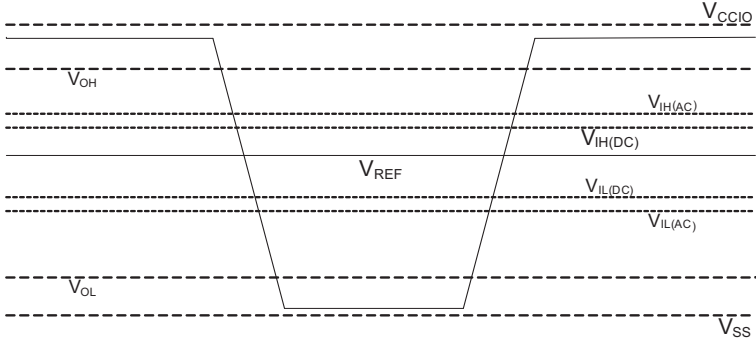
Letter	Subject	Definitions
S	SW (sampling window)	The period of time during which the data must be valid in order to capture it correctly. The setup and hold times determine the ideal strobe position within the sampling window: <i>Timing Diagram</i> 
	Single-ended Voltage Referenced I/O Standard	The JEDEC standard for SSTL and HSTL I/O standards define both the AC and DC input signal values. The AC values indicate the voltage levels at which the receiver must meet its timing specifications. The DC values indicate the voltage levels at which the final logic state of the receiver is unambiguously defined. After the receiver input has crossed the AC value, the receiver changes to the new logic state. The new logic state is then maintained as long as the input stays beyond the AC threshold. This approach is intended to provide predictable receiver timing in the presence of input waveform ringing: <i>Single-Ended Voltage Referenced I/O Standard</i> 
T	t_c	High-speed receiver and transmitter input and output clock period.
	TCCS (channel-to-channel-skew)	The timing difference between the fastest and slowest output edges, including t_{CO} variation and clock skew, across channels driven by the same PLL. The clock is included in the TCCS measurement (refer to the <i>Timing Diagram</i> figure under S in this table).
	t_{DUTY}	High-speed I/O block: Duty cycle on the high-speed transmitter output clock. Timing Unit Interval (TUI) The timing budget allowed for skew, propagation delays, and data sampling window. (TUI = $1/(\text{Receiver Input Clock Frequency Multiplication Factor}) = t_c/w$)
	t_{FALL}	Signal high-to-low transition time (80-20%)
	t_{INCCJ}	Cycle-to-cycle jitter tolerance on the PLL clock input.
	t_{OUTPJ_IO}	Period jitter on the general purpose I/O driven by a PLL.
	t_{OUTPJ_DC}	Period jitter on the dedicated clock output driven by a PLL.
	t_{RISE}	Signal low-to-high transition time (20-80%).

Table 1-69. Document Revision History (Part 2 of 2)

Date	Version	Changes
December 2010	4.0	■ Added Arria II GZ information. ■ Added Table 1-61 with Arria II GX information. ■ Updated Table 1-1, Table 1-2, Table 1-5, Table 1-6, Table 1-7, Table 1-11, Table 1-35, Table 1-37, Table 1-40, Table 1-42, Table 1-44, Table 1-45, Table 1-57, Table 1-61, and Table 1-63. ■ Updated Figure 1-5. ■ Updated for the Quartus II version 10.0 release. ■ Updated the first paragraph for searchability. ■ Minor text edits.
July 2010	3.0	■ Updated Table 1-1, Table 1-4, Table 1-16, Table 1-19, Table 1-21, Table 1-23, Table 1-25, Table 1-26, Table 1-30, and Table 1-35 ■ Added Table 1-27 and Table 1-29. ■ Added I3 speed grade information to Table 1-19, Table 1-21, Table 1-22, Table 1-24, Table 1-25, Table 1-30, Table 1-32, Table 1-33, Table 1-34, and Table 1-35. ■ Updated the “Operating Conditions” section. ■ Removed “Preliminary” from Table 1-19, Table 1-21, Table 1-22, Table 1-23, Table 1-24, Table 1-25, Table 1-26, Table 1-28, Table 1-30, Table 1-32, Table 1-33, Table 1-34, and Figure 1-4. ■ Minor text edits.
March 2010	2.3	Updated for the Quartus II version 9.1 SP2 release: ■ Updated Table 1-3, Table 1-7, Table 1-19, Table 1-21, Table 1-22, Table 1-24, Table 1-25 and Table 1-33. ■ Updated “Recommended Operating Conditions” section. ■ Minor text edits.
February 2010	2.2	Updated Table 1-19.
February 2010	2.1	Updated for Arria II GX v9.1 SP1 release: ■ Updated Table 1-19, Table 1-23, Table 1-28, Table 1-30, and Table 1-33. ■ Added Figure 1-5. ■ Minor text edits.
November 2009	2.0	Updated for Arria II GX v9.1 release: ■ Updated Table 1-1, Table 1-4, Table 1-13, Table 1-14, Table 1-19, Table 1-15, Table 1-22, Table 1-24, and Table 1-28. ■ Added Table 1-6 and Table 1-33. ■ Added “Bus Hold” on page 1-5. ■ Added “IOE Programmable Delay” section. ■ Minor text edit.
June 2009	1.2	■ Updated Table 1-1, Table 1-3, Table 1-7, Table 1-8, Table 1-18, Table 1-23, Table 1-25, Table 1-26, Table 1-29, Table 1-30, Table 1-31, Table 1-32, and Table 1-33. ■ Added Table 1-32. ■ Updated Equation 1-1.
March 2009	1.1	Added “I/O Timing” section.
February 2009	1.0	Initial release.