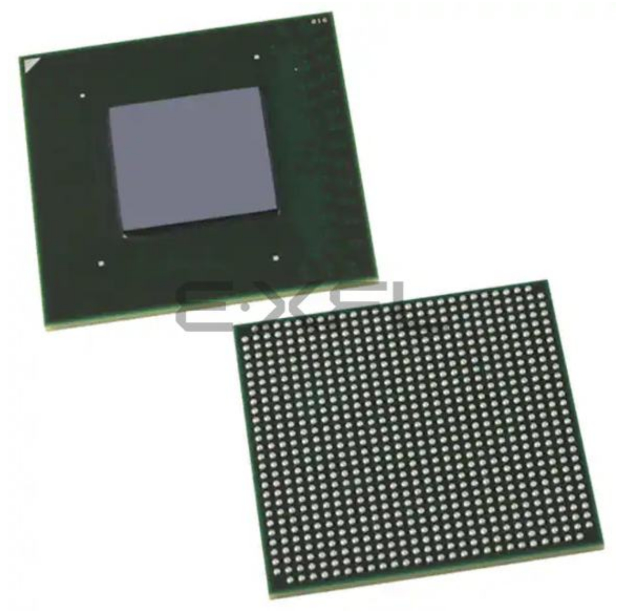
# Intel - EP2AGX95EF29I3N Datasheet



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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

| **Details** | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | 3747 |
| Number of Logic Elements/Cells | 89178 |
| Total RAM Bits | 6839296 |
| Number of I/O | 372 |
| Number of Gates | - |
| Voltage - Supply | 0.87V ~ 0.93V |
| Mounting Type | Surface Mount |
| Operating Temperature | -40°C ~ 100°C (TJ) |
| Package / Case | 780-BBGA, FCBGA |
| Supplier Device Package | 780-FBGA (29x29) |
| Purchase URL | https://www.e-xfl.com/product-detail/intel/ep2agx95ef29i3n |

Email: info@E-XFL.COM
Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

**Table 1–2. Absolute Maximum Ratings for Arria II GZ Devices (Part 2 of 2)**

| Symbol | Description | Minimum | Maximum | Unit |
|---|---|---|---|---|
| $V_{CCA\_L}$ | Supplies transceiver high voltage power (left side) | -0.5 | 3.75 | V |
| $V_{CCA\_R}$ | Supplies transceiver high voltage power (right side) | -0.5 | 3.75 | V |
| $V_{CCHIP\_L}$ | Supplies transceiver HIP digital power (left side) | -0.5 | 1.35 | V |
| $V_{CCR\_L}$ | Supplies receiver power (left side) | -0.5 | 1.35 | V |
| $V_{CCR\_R}$ | Supplies receiver power (right side) | -0.5 | 1.35 | V |
| $V_{CCT\_L}$ | Supplies transmitter power (left side) | -0.5 | 1.35 | V |
| $V_{CCT\_R}$ | Supplies transmitter power (right side) | -0.5 | 1.35 | V |
| $V_{CCL\_GXBLn}$ *(1)* | Supplies power to the transceiver PMA TX, PMA RX, and clocking (left side) | -0.5 | 1.35 | V |
| $V_{CCL\_GXBRn}$ *(1)* | Supplies power to the transceiver PMA TX, PMA RX, and clocking (right side) | -0.5 | 1.35 | V |
| $V_{CCH\_GXBLn}$ *(1)* | Supplies power to the transceiver PMA output (TX) buffer (left side) | -0.5 | 1.8 | V |
| $V_{CCH\_GXBRn}$ *(1)* | Supplies power to the transceiver PMA output (TX) buffer (right side) | -0.5 | 1.8 | V |
| $T_J$ | Operating junction temperature | -55 | 125 | °C |
| $T_{STG}$ | Storage temperature (no bias) | -65 | 150 | °C |

**Note to Table 1–2:**

(1) n = 0, 1, or 2.

### Maximum Allowed Overshoot and Undershoot Voltage

During transitions, input signals may overshoot to the voltage shown in Table 1–3 and undershoot to –2.0 V for magnitude of currents less than 100 mA and periods shorter than 20 ns.

Table 1–3 lists the Arria II GX and GZ maximum allowed input overshoot voltage and the duration of the overshoot voltage as a percentage over the device lifetime. The maximum allowed overshoot duration is specified as a percentage of high-time over the lifetime of the device. A DC signal is equivalent to 100% duty cycle. For example, a signal that overshoots to 4.3 V can only be at 4.3 V for 5.41% over the lifetime of the device; for a device lifetime of 10 years, this amounts to 5.41/10ths of a year.

### I/O Pin Leakage Current

Table 1–7 lists the Arria II GX I/O pin leakage current specifications.

**Table 1–7. I/O Pin Leakage Current for Arria II GX Devices**

| Symbol | Description | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $I_I$ | Input pin | $V_I$ = 0 V to $V_{CCIOMAX}$ | –10 | — | 10 | µA |
| $I_{OZ}$ | Tri-stated I/O pin | $V_O$ = 0 V to $V_{CCIOMAX}$ | –10 | — | 10 | µA |

Table 1–8 lists the Arria II GZ I/O pin leakage current specifications.

**Table 1–8. I/O Pin Leakage Current for Arria II GZ Devices**

| Symbol | Description | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $I_I$ | Input pin | $V_I$ = 0 V to $V_{CCIOMAX}$ | –20 | — | 20 | µA |
| $I_{OZ}$ | Tri-stated I/O pin | $V_O$ = 0 V to $V_{CCIOMAX}$ | –20 | — | 20 | µA |

### Bus Hold

Bus hold retains the last valid logic state after the source driving it either enters the high impedance state or is removed. Each I/O pin has an option to enable bus hold in user mode. Bus hold is always disabled in configuration mode.

Table 1–9 lists bus hold specifications for Arria II GX devices.

**Table 1–9. Bus Hold Parameters for Arria II GX Devices** *(Note 1)*

| Parameter | Symbol | Cond. | $V_{CCIO}$ (V) | | | | | | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 1.2 | | 1.5 | | 1.8 | | 2.5 | | 3.0 | | 3.3 | | |
| | | | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | |
| Bus-hold low, sustaining current | $I_{SUSL}$ | $V_{IN} > V_{IL}$ (max.) | 8 | — | 12 | — | 30 | — | 50 | — | 70 | — | 70 | — | µA |
| Bus-hold high, sustaining current | $I_{SUSH}$ | $V_{IN} < V_{IL}$ (min.) | –8 | — | –12 | — | –30 | — | –50 | — | –70 | — | –70 | — | µA |
| Bus-hold low, overdrive current | $I_{ODL}$ | $0 V < V_{IN} < V_{CCIO}$ | — | 125 | — | 175 | — | 200 | — | 300 | — | 500 | — | 500 | µA |
| Bus-hold high, overdrive current | $I_{ODH}$ | $0 V < V_{IN} < V_{CCIO}$ | — | –125 | — | –175 | — | –200 | — | –300 | — | –500 | — | –500 | µA |
| Bus-hold trip point | $V_{TRIP}$ | — | 0.3 | 0.9 | 0.375 | 1.125 | 0.68 | 1.07 | 0.7 | 1.7 | 0.8 | 2 | 0.8 | 2 | V |

**Note to Table 1–9:**

(1) The bus-hold trip points are based on calculated input voltages from the JEDEC standard.

Table 1–19 lists the weak pull-up resistor values for Arria II GZ devices.

**Table 1–19. Internal Weak Pull-Up Resistor for Arria II GZ Devices** *(Note 1)*, *(2)*

| Symbol | Description | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $R_{PU}$ | Value of the I/O pin pull-up resistor before and during configuration, as well as user mode if the programmable pull-up resistor option is enabled. | $V_{CCIO}$ = 3.0 V ±5% *(3)* | — | 25 | — | kΩ |
| | | $V_{CCIO}$ = 2.5 V ±5% *(3)* | — | 25 | — | kΩ |
| | | $V_{CCIO}$ = 1.8 V ±5% *(3)* | — | 25 | — | kΩ |
| | | $V_{CCIO}$ = 1.5 V ±5% *(3)* | — | 25 | — | kΩ |
| | | $V_{CCIO}$ = 1.2 V ±5% *(3)* | — | 25 | — | kΩ |

**Notes to Table 1–19:**

(1) All I/O pins have an option to enable weak pull-up except configuration, test, and JTAG pins.

(2) The internal weak pull-down feature is only available for the JTAG `TCK` pin. The typical value for this internal weak pull-down resistor is approximately 25 kΩ .

(3) Pin pull-up resistance values may be lower if an external source drives the pin higher than $V_{CCIO}$.

### Hot Socketing

Table 1–20 lists the hot-socketing specification for Arria II GX and GZ devices.

**Table 1–20. Hot Socketing Specifications for Arria II Devices**

| Symbol | Description | Maximum |
|---|---|---|
| $I_{IIOPIN(DC)}$ | DC current per I/O pin | 300 μA |
| $I_{IOPIN(AC)}$ | AC current per I/O pin | 8 mA *(1)* |
| $I_{XCVRTX(DC)}$ | DC current per transceiver TX pin | 100 mA |
| $I_{XCVRRX(DC)}$ | DC current per transceiver RX pin | 50 mA |

**Note to Table 1–20:**

(1) The I/O ramp rate is 10 ns or more. For ramp rates faster than 10 ns, $|I_{IOPIN}|$ = C dv/dt, in which “C” is I/O pin capacitance and “dv/dt” is slew rate.

## Schmitt Trigger Input

The Arria II GX device supports Schmitt trigger input on the `TDI`, `TMS`, `TCK`, `nSTATUS`, `nCONFIG`, `nCE`, `CONF_DONE`, and `DCLK` pins. A Schmitt trigger feature introduces hysteresis to the input signal for improved noise immunity, especially for signals with slow edge rates.

Table 1–21 lists the hysteresis specifications across the supported $V_{CCIO}$ range for Schmitt trigger inputs in Arria II GX devices.

**Table 1–21. Schmitt Trigger Input Hysteresis Specifications for Arria II GX Devices**

| Symbol | Description | Condition (V) | Minimum | Unit |
|---|---|---|---|---|
| $V_{Schmitt}$ | Hysteresis for Schmitt trigger input | $V_{CCIO}$ = 3.3 | 220 | mV |
| | | $V_{CCIO}$ = 2.5 | 180 | mV |
| | | $V_{CCIO}$ = 1.8 | 110 | mV |
| | | $V_{CCIO}$ = 1.5 | 70 | mV |

## I/O Standard Specifications

Table 1–22 through Table 1–35 list input voltage ($V_{IH}$ and $V_{IL}$), output voltage ($V_{OH}$ and $V_{OL}$), and current drive characteristics ($I_{OH}$ and $I_{OL}$) for various I/O standards supported by the Arria II device family. They also show the Arria II device family I/O standard specifications. $V_{OL}$ and $V_{OH}$ values are valid at the corresponding $I_{OH}$ and $I_{OL}$, respectively.

For an explanation of terms used in Table 1–22 through Table 1–35, refer to "Glossary" on page 1–74.

Table 1–22 lists the single-ended I/O standards for Arria II GX devices.

**Table 1–22. Single-Ended I/O Standards for Arria II GX Devices**

| I/O Standard | $V_{CCIO}$ (V) | | | $V_{IL}$ (V) | | $V_{IH}$ (V) | | $V_{OL}$ (V) | $V_{OH}$ (V) | $I_{OL}$ (mA) | $I_{OH}$ (mA) |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Max | Min | Max | Max | Min | | |
| 3.3 V LVTTL | 3.135 | 3.3 | 3.465 | –0.3 | 0.8 | 1.7 | 3.6 | 0.45 | 2.4 | 4 | –4 |
| 3.3 V LVCMOS | 3.135 | 3.3 | 3.465 | –0.3 | 0.8 | 1.7 | 3.6 | 0.2 | $V_{CCIO}$ -0.2 | 2 | –2 |
| 3.0 V LVTTL | 2.85 | 3 | 3.15 | –0.3 | 0.8 | 1.7 | $V_{CCIO}$ + 0.3 | 0.45 | 2.4 | 4 | –4 |
| 3.0 V LVCMOS | 2.85 | 3 | 3.15 | –0.3 | 0.8 | 1.7 | $V_{CCIO}$ + 0.3 | 0.2 | $V_{CCIO}$ - 0.2 | 0.1 | –0.1 |
| 2.5 V LVCMOS | 2.375 | 2.5 | 2.625 | –0.3 | 0.7 | 1.7 | $V_{CCIO}$ + 0.3 | 0.4 | 2 | 1 | –1 |
| 1.8 V LVCMOS | 1.71 | 1.8 | 1.89 | –0.3 | 0.35 × $V_{CCIO}$ | 0.65 × $V_{CCIO}$ | $V_{CCIO}$ + 0.3 | 0.45 | $V_{CCIO}$ - 0.45 | 2 | –2 |
| 1.5 V LVCMOS | 1.425 | 1.5 | 1.575 | –0.3 | 0.35 × $V_{CCIO}$ | 0.65 × $V_{CCIO}$ | $V_{CCIO}$ + 0.3 | 0.25 × $V_{CCIO}$ | 0.75 × $V_{CCIO}$ | 2 | –2 |
| 1.2 V LVCMOS | 1.14 | 1.2 | 1.26 | –0.3 | 0.35 × $V_{CCIO}$ | 0.65 × $V_{CCIO}$ | $V_{CCIO}$ + 0.3 | 0.25 × $V_{CCIO}$ | 0.75 × $V_{CCIO}$ | 2 | –2 |
| 3.0-V PCI | 2.85 | 3 | 3.15 | — | 0.3 × $V_{CCIO}$ | 0.5 × $V_{CCIO}$ | $V_{CCIO}$ + 0.3 | 0.1 × $V_{CCIO}$ | 0.9 × $V_{CCIO}$ | 1.5 | –0.5 |
| 3.0-V PCI-X | 2.85 | 3 | 3.15 | — | 0.35 × $V_{CCIO}$ | 0.5 × $V_{CCIO}$ | $V_{CCIO}$ + 0.3 | 0.1 × $V_{CCIO}$ | 0.9 × $V_{CCIO}$ | 1.5 | –0.5 |

Table 1–23 lists the single-ended I/O standards for Arria II GZ devices.

**Table 1–23. Single-Ended I/O Standards for Arria II GZ Devices (Part 1 of 2)**

| I/O Standard | $V_{CCIO}$ (V) | | | $V_{IL}$ (V) | | $V_{IH}$ (V) | | $V_{OL}$ (V) | $V_{OH}$ (V) | $I_{OL}$ (mA) | $I_{OH}$ (mA) |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Max | Min | Max | Max | Min | | |
| LVTTL | 2.85 | 3 | 3.15 | -0.3 | 0.8 | 1.7 | 3.6 | 0.4 | 2.4 | 2 | -2 |
| LVCMOS | 2.85 | 3 | 3.15 | -0.3 | 0.8 | 1.7 | 3.6 | 0.2 | $V_{CCIO}$ - 0.2 | 0.1 | -0.1 |
| 2.5 V | 2.375 | 2.5 | 2.625 | -0.3 | 0.7 | 1.7 | 3.6 | 0.4 | 2 | 1 | -1 |
| 1.8 V | 1.71 | 1.8 | 1.89 | -0.3 | 0.35 × $V_{CCIO}$ | 0.65 × $V_{CCIO}$ | $V_{CCIO}$ + 0.3 | 0.45 | $V_{CCIO}$ - 0.45 | 2 | -2 |
| 1.5 V | 1.425 | 1.5 | 1.575 | -0.3 | 0.35 × $V_{CCIO}$ | 0.65 × $V_{CCIO}$ | $V_{CCIO}$ + 0.3 | 0.25 × $V_{CCIO}$ | 0.75 × $V_{CCIO}$ | 2 | -2 |

Table 1–30 lists the HSTL I/O standards for Arria II GX devices.

**Table 1–30. Differential HSTL I/O Standards for Arria II GX Devices**

| I/O Standard | $V_{CCIO}$ (V) | | | $V_{DIF(DC)}$ (V) | | $V_{X(AC)}$ (V) | | | $V_{CM(DC)}$ (V) | | | $V_{DIF(AC)}$ (V) | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Max | Min | Typ | Max | Min | Typ | Max | Min | Max |
| HSTL-18 Class I | 1.71 | 1.8 | 1.89 | 0.2 | — | 0.85 | — | 0.95 | 0.88 | — | 0.95 | 0.4 | — |
| HSTL-15 Class I, II | 1.425 | 1.5 | 1.575 | 0.2 | — | 0.71 | — | 0.79 | 0.71 | — | 0.79 | 0.4 | — |
| HSTL-12 Class I, II | 1.14 | 1.2 | 1.26 | 0.16 | — | — | 0.5 × $V_{CCIO}$ | — | 0.48 × $V_{CCIO}$ | 0.5 × $V_{CCIO}$ | 0.52 × $V_{CCIO}$ | 0.3 | — |

Table 1–31 lists the HSTL I/O standards for Arria II GZ devices.

**Table 1–31. Differential HSTL I/O Standards for Arria II GZ Devices**

| I/O Standard | $V_{CCIO}$ (V) | | | $V_{DIF(DC)}$ (V) | | $V_{X(AC)}$ (V) | | | $V_{CM(DC)}$ (V) | | | $V_{DIF(AC)}$ (V) | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Max | Min | Typ | Max | Min | Typ | Max | Min | Max |
| HSTL-18 Class I | 1.71 | 1.8 | 1.89 | 0.2 | — | 0.78 | — | 1.12 | 0.78 | — | 1.12 | 0.4 | — |
| HSTL-15 Class I, II | 1.425 | 1.5 | 1.575 | 0.2 | — | 0.68 | — | 0.9 | 0.68 | — | 0.9 | 0.4 | — |
| HSTL-12 Class I, II | 1.14 | 1.2 | 1.26 | 0.16 | $V_{CCIO}$ + 0.3 | — | 0.5 × $V_{CCIO}$ | — | 0.4 × $V_{CCIO}$ | 0.5 × $V_{CCIO}$ | 0.6 × $V_{CCIO}$ | 0.3 | $V_{CCIO}$ + 0.48 |

Table 1–32 lists the differential I/O standard specifications for Arria II GX devices.

**Table 1–32. Differential I/O Standard Specifications for Arria II GX Devices** *(Note 1)*

| I/O Standard | $V_{CCIO}$ (V) | | | $V_{ID}$ (mV) | | | $V_{ICM}$ (V) *(2)* | | $V_{OD}$ (V) *(3)* | | | $V_{OCM}$ (V) | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Cond. | Max | Min | Max | Min | Typ | Max | Min | Typ | Max |
| 2.5 V LVDS | 2.375 | 2.5 | 2.625 | 100 | $V_{CM}$ = 1.25 V | — | 0.05 | 1.80 | 0.247 | — | 0.6 | 1.125 | 1.25 | 1.375 |
| RSDS *(4)* | 2.375 | 2.5 | 2.625 | — | — | — | — | — | 0.1 | 0.2 | 0.6 | 0.5 | 1.2 | 1.4 |
| Mini-LVDS *(4)* | 2.375 | 2.5 | 2.625 | — | — | — | — | — | 0.25 | — | 0.6 | 1 | 1.2 | 1.4 |
| LVPECL *(5)* | 2.375 | 2.5 | 2.625 | 300 | — | — | 0.6 | 1.8 | — | — | — | — | — | — |
| BLVDS *(6)* | 2.375 | 2.5 | 2.625 | 100 | — | — | — | — | — | — | — | — | — | — |

**Notes to Table 1–32:**

(1) The 1.5 V PCML transceiver I/O standard specifications are described in "Transceiver Performance Specifications" on page 1–21.

(2) $V_{IN}$ range: $0 <= V_{IN} <= 1.85$ V.

(3) $R_L$ range: $90 <= RL <= 110\ \Omega$.

(4) The RSDS and mini-LVDS I/O standards are only supported for differential outputs.

(5) The LVPECL input standard is supported at the dedicated clock input pins (GCLK) only.

(6) There are no fixed $V_{ICM}$, $V_{OD}$, and $V_{OCM}$ specifications for BLVDS. These specifications depend on the system topology.

**Table 1–34. Transceiver Specifications for Arria II GX Devices** ***(Note 1)*** **(Part 7 of 7)**

| Symbol/ Description | Condition | I3 | | | C4 | | | C5 and I5 | | | C6 | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Digital reset pulse width | — | Minimum is 2 parallel clock cycles | | | | | | | | | | | | |

**Notes to Table 1–34:**

(1) For AC-coupled links, the on-chip biasing circuit is switched off before and during configuration. Ensure that input specifications are not violated during this period.

(2) The rise/fall time is specified from 20% to 80%.

(3) To calculate the REFCLK rms phase jitter requirement at reference clock frequencies other than 100 MHz, use the following formula:
REFCLK rms phase jitter at f (MHz) = REFCLK rms phase jitter at 100 MHz * 100/f.

(4) The minimum `reconfig_clk` frequency is 2.5 MHz if the transceiver channel is configured in **Transmitter only** mode. The minimum `reconfig_clk` frequency is 37.5 MHz if the transceiver channel is configured in **Receiver only** or **Receiver and Transmitter** mode. For more information, refer to *AN 558: Implementing Dynamic Reconfiguration in Arria II Devices*.

(5) If your design uses more than one dynamic reconfiguration controller instances (`altgx_reconfig`) to control the transceiver channels (`altgx`) physically located on the same side of the device, and if you use different `reconfig_clk` sources for these `altgx_reconfig` instances, the delta time between any two of these `reconfig_clk` sources becoming stable must not exceed the maximum specification listed.

(6) The device cannot tolerate prolonged operation at this absolute maximum.

(7) You must use the 1.1-V RX $V_{ICM}$ setting if the input serial data standard is LVDS and the link is DC-coupled.

(8) The rate matcher supports only up to ±300 parts per million (ppm).

(9) Time taken to `rx_pll_locked` goes high from `rx_analogreset` de-assertion. Refer to Figure 1–1.

(10) The time in which the CDR must be kept in lock-to-reference mode after `rx_pll_locked` goes high and before `rx_locktodata` is asserted in manual mode. Refer to Figure 1–1.

(11) The time taken to recover valid data after the `rx_locktodata` signal is asserted in manual mode. Refer to Figure 1–1.

(12) The time taken to recover valid data after the `rx_freqlocked` signal goes high in automatic mode. Refer to Figure 1–2.

(13) To support data rates lower than the minimum specification through oversampling, use the CDR in LTR mode only.

Table 1–35 lists the transceiver specifications for Arria II GZ devices.

**Table 1–35. Transceiver Specifications for Arria II GZ Devices (Part 1 of 5)**

| Symbol/ Description | Conditions | –C3 and –I3 *(1)* | | | –C4 and –I4 | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| **Reference Clock** | | | | | | | | |
| Supported I/O Standards | 1.2-V PCML, 1.5-V PCML, 2.5-V PCML, Differential LVPECL, LVDS, and HCSL | | | | | | | |
| Input frequency from `REFCLK` input pins | — | 50 | — | 697 | 50 | — | 637.5 | MHz |
| Phase frequency detector (CMU PLL and receiver CDR) | — | 50 | — | 325 | 50 | — | 325 | MHz |
| Absolute $V_{MAX}$ for a `REFCLK` pin | — | — | — | 1.6 | — | — | 1.6 | V |
| Operational $V_{MAX}$ for a `REFCLK` pin | — | — | — | 1.5 | — | — | 1.5 | V |
| Absolute $V_{MIN}$ for a `REFCLK` pin | — | -0.4 | — | — | -0.4 | — | — | V |
| Rise/fall time *(2)* | — | — | — | 0.2 | — | — | 0.2 | UI |
| Duty cycle | — | 45 | — | 55 | 45 | — | 55 | % |
| Peak-to-peak differential input voltage | — | 200 | — | 1600 | 200 | — | 1600 | mV |
| Spread-spectrum modulating clock frequency | PCIe | 30 | — | 33 | 30 | — | 33 | kHz |
| Spread-spectrum downspread | PCIe | — | 0 to -0.5% | — | — | 0 to -0.5% | — | — |
| On-chip termination resistors | — | — | 100 | — | — | 100 | — | Ω |
| $V_{ICM}$ (AC coupled) | — | 1100 ± 10% | | | 1100 ± 10% | | | mV |
| $V_{ICM}$ (DC coupled) | HCSL I/O standard for PCIe reference clock | 250 | — | 550 | 250 | — | 550 | mV |
| Transmitter REFCLK Phase Noise | 10 Hz | — | — | -50 | — | — | -50 | dBc/Hz |
| | 100 Hz | — | — | -80 | — | — | -80 | dBc/Hz |
| | 1 KHz | — | — | -110 | — | — | -110 | dBc/Hz |
| | 10 KHz | — | — | -120 | — | — | -120 | dBc/Hz |
| | 100 KHz | — | — | -120 | — | — | -120 | dBc/Hz |
| | ≥ 1 MHz | — | — | -130 | — | — | -130 | dBc/Hz |
| Transmitter REFCLK Phase Jitter (rms) for 100 MHz REFCLK *(3)* | 10 KHz to 20 MHz | — | — | 3 | — | — | 3 | ps |
| $R_{REF}$ | — | — | 2000 ± 1% | — | — | 2000 ± 1% | — | Ω |

**Table 1–35. Transceiver Specifications for Arria II GZ Devices (Part 3 of 5)**

| Symbol/ Description | Conditions | –C3 and –I3 *(1)* | | | –C4 and –I4 | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| Receiver DC Coupling Support | — | For more information about receiver DC coupling support, refer to the “DC-Coupled Links” section in the *Transceiver Architecture for Arria II Devices* chapter. | | | | | | |
| Differential on-chip termination resistors | 85–Ω setting | 85 ± 20% | | | 85 ± 20% | | | Ω |
| | 100–Ω setting | 100 ± 20% | | | 100 ± 20% | | | Ω |
| | 120–Ω setting | 120 ± 20% | | | 120 ± 20% | | | Ω |
| | 150-Ω setting | 150 ± 20% | | | 150 ± 20% | | | Ω |
| Differential and common mode return loss | PCIe (Gen 1 and Gen 2),<br>XAUI,<br>HiGig+,<br>CEI SR/LR,<br>SRIO SR/LR,<br>CPRI LV/HV,<br>OBSAI,<br>SATA | Compliant | | | | | | — |
| Programmable PPM detector *(9)* | — | ± 62.5, 100, 125, 200, 250, 300, 500, 1,000 | | | | | | ppm |
| Run length | — | — | — | 200 | — | — | 200 | UI |
| Programmable equalization | — | — | — | 16 | — | — | 16 | dB |
| $t_{LTR}$ *(10)* | — | — | — | 75 | — | — | 75 | µs |
| $t_{LTR\_LTD\_Manual}$ *(11)* | — | 15 | — | — | 15 | — | — | µs |
| $t_{LTD\_Manual}$ *(12)* | — | — | — | 4000 | — | — | 4000 | ns |
| $t_{LTD\_Auto}$ *(13)* | — | — | — | 4000 | — | — | 4000 | ns |
| Receiver CDR 3 dB Bandwidth in lock-to-data (LTD) mode | PCIe Gen1 | 2.0 - 3.5 | | | | | | MHz |
| | PCIe Gen2 | 40 - 65 | | | | | | MHz |
| | (OIF) CEI PHY at 6.375 Gbps | 20 - 35 | | | | | | MHz |
| | XAUI | 10 - 18 | | | | | | MHz |
| | SRIO 1.25 Gbps | 10 - 18 | | | | | | MHz |
| | SRIO 2.5 Gbps | 10 - 18 | | | | | | MHz |
| | SRIO 3.125 Gbps | 6 - 10 | | | | | | MHz |
| | GIGE | 6 - 10 | | | | | | MHz |
| | SONET OC12 | 3 - 6 | | | | | | MHz |
| | SONET OC48 | 14 - 19 | | | | | | MHz |
| Receiver buffer and CDR offset cancellation time (per channel) | — | — | — | 17000 | — | — | 17000 | `reconfig_clk` cycles |
| Programmable DC gain | DC Gain Setting = 0 | — | 0 | — | — | 0 | — | dB |
| | DC Gain Setting = 1 | — | 3 | — | — | 3 | — | dB |
| | DC Gain Setting = 2 | — | 6 | — | — | 6 | — | dB |

Figure 1–1 shows the lock time parameters in manual mode.

☞ LTD = lock-to-data. LTR = lock-to-reference.

**Figure 1–1. Lock Time Parameters for Manual Mode**

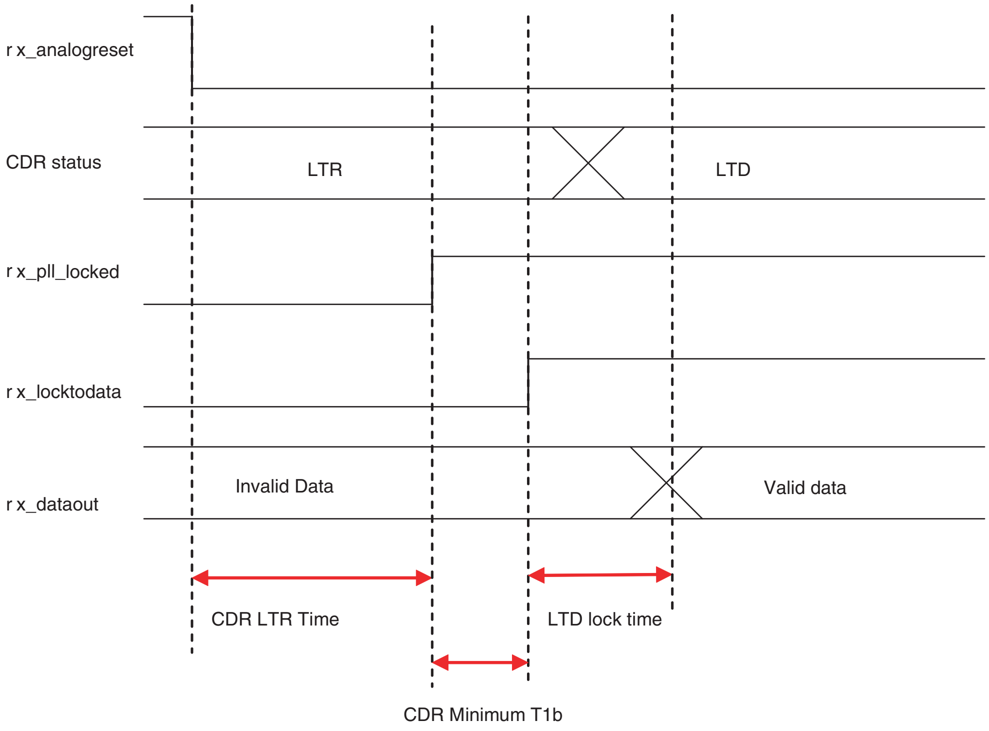


Figure 1–2 shows the lock time parameters in automatic mode.

**Figure 1–2. Lock Time Parameters for Automatic Mode**

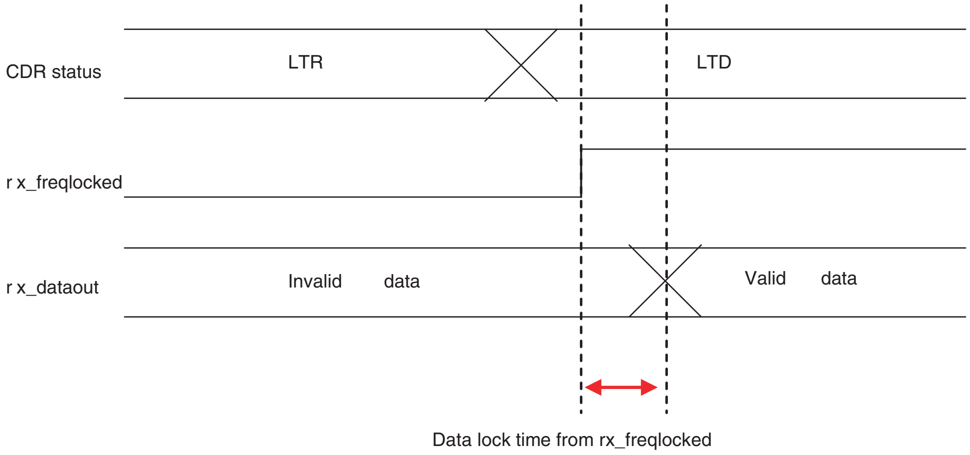


Figure 1–3 shows the differential receiver input waveform.

**Figure 1–3. Receiver Input Waveform**

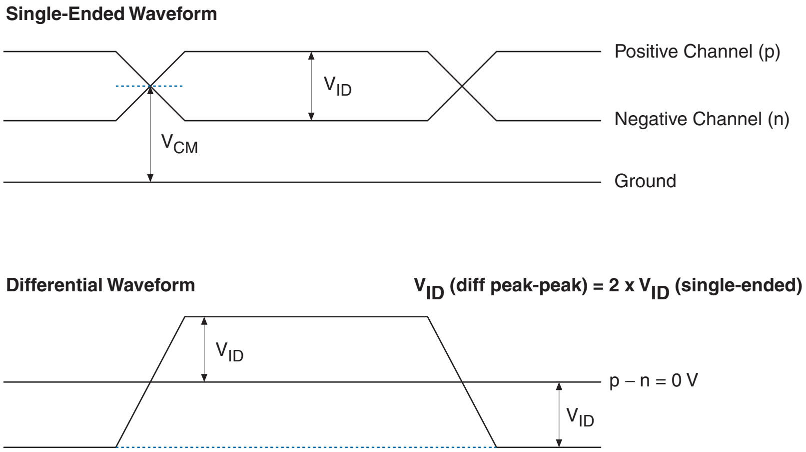


Figure 1–4 shows the transmitter output waveform.

**Figure 1–4. Transmitter Output Waveform**

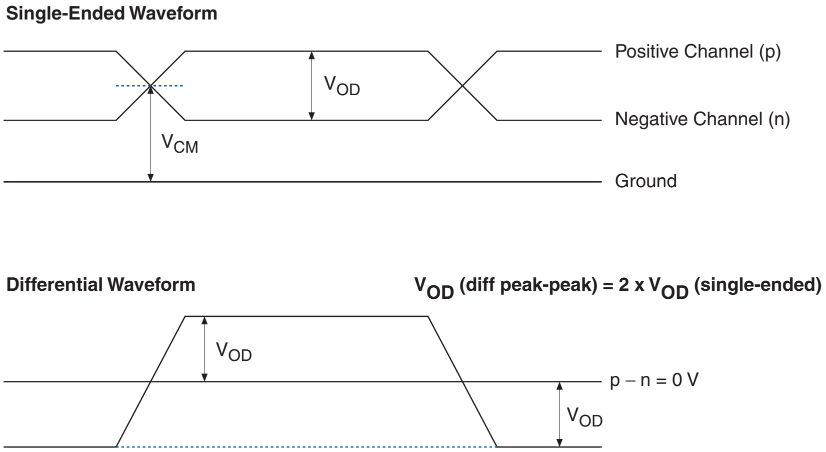


Table 1–36 lists the typical $V_{OD}$ for TX term that equals 85 Ω for Arria II GZ devices.

**Table 1–36. Typical $V_{OD}$ Setting, TX Term = 85 Ω for Arria II GZ Devices**

| Symbol | $V_{OD}$ Setting (mV) | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| $V_{OD}$ differential peak-to-peak Typical (mV) | 170 ± 20% | 340 ± 20% | 510 ± 20% | 595 ± 20% | 680 ± 20% | 765 ± 20% | 850 ± 20% | 1020± 20% |

Table 1–37 lists the typical $V_{OD}$ for TX term that equals 100 Ω for Arria II GX and GZ devices.

Table 1–37. Typical $V_{OD}$ Setting, TX Termination = 100 Ω for Arria II Devices

| Quartus II Setting | $V_{OD}$ Setting (mV) |
|---|---|
| 1 | 400 |
| 2 | 600 |
| 3 (Arria II GZ) | 700 |
| 4 | 800 |
| 5 | 900 |
| 6 | 1000 |
| 7 | 1200 |

Table 1–38 lists the typical transmitter pre-emphasis levels in dB for the first post tap under the following conditions: low-frequency data pattern (five 1s and five 0s) at 6.375 Gbps. The levels listed in Table 1–38 are a representation of possible pre-emphasis levels under these specified conditions only, the pre-emphasis levels may change with data pattern and data rate.

To predict the pre-emphasis level for your specific data rate and pattern, run simulations using the Arria II GX HSSI HSPICE models.

Table 1–38. Transmitter Pre-Emphasis Levels for Arria II GX Devices

| Arria II GX (Quartus II Software) First Post Tap Setting | Arria II GX (Quartus II Software) VOD Setting | | | | | | |
|---|---|---|---|---|---|---|---|
| | 1 | 2 | 4 | 5 | 6 | 7 | Unit |
| 0 (off) | 0 | 0 | 0 | 0 | 0 | 0 | — |
| 1 | 0.7 | 0 | 0 | 0 | 0 | 0 | dB |
| 2 | 2.7 | 1.2 | 0.3 | 0 | 0 | 0 | dB |
| 3 | 4.9 | 2.4 | 1.2 | 0.8 | 0.5 | 0.2 | dB |
| 4 | 7.5 | 3.8 | 2.1 | 1.6 | 1.2 | 0.6 | dB |
| 5 | — | 5.3 | 3.1 | 2.4 | 1.8 | 1.1 | dB |
| 6 | — | 7 | 4.3 | 3.3 | 2.7 | 1.7 | dB |

**Table 1–39. Transmitter Pre-Emphasis Levels for Arria II GZ Devices (Part 2 of 2)**

| Pre-Emphasis 1st Post-Tap Setting | $V_{OD}$ Setting | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| 29 | N/A | N/A | N/A | 12.5 | 9.6 | 7.7 | 6.3 | 4.3 |
| 30 | N/A | N/A | N/A | N/A | 11.4 | 9 | 7.4 | N/A |
| 31 | N/A | N/A | N/A | N/A | 12.9 | 10 | 8.2 | N/A |

Table 1–40 lists the transceiver jitter specifications for all supported protocols for Arria II GX devices.

**Table 1–40. Transceiver Block Jitter Specifications for Arria II GX Devices *(Note 1)* (Part 1 of 10)**

| Symbol/ Description | Conditions | I3 | | | C4 | | | C5, I5 | | | C6 | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| **SONET/SDH Transmit Jitter Generation *(2)*** | | | | | | | | | | | | | | |
| Peak-to-peak jitter at 622.08 Mbps | Pattern = PRBS15 | — | — | 0.1 | — | — | 0.1 | — | — | 0.1 | — | — | 0.1 | UI |
| RMS jitter at 622.08 Mbps | Pattern = PRBS15 | — | — | 0.01 | — | — | 0.01 | — | — | 0.01 | — | — | 0.01 | UI |
| Peak-to-peak jitter at 2488.32 Mbps | Pattern = PRBS15 | — | — | 0.1 | — | — | 0.1 | — | — | 0.1 | — | — | 0.1 | UI |
| RMS jitter at 2488.32 Mbps | Pattern = PRBS15 | — | — | 0.01 | — | — | 0.01 | — | — | 0.01 | — | — | 0.01 | UI |
| **SONET/SDH Receiver Jitter Tolerance *(2)*** | | | | | | | | | | | | | | |
| Jitter tolerance at 622.08 Mbps | Jitter frequency = 0.03 KHz<br>Pattern = PRBS15 | > 15 | | | > 15 | | | > 15 | | | > 15 | | | UI |
| | Jitter frequency = 25 KHZ<br>Pattern = PRBS15 | > 1.5 | | | > 1.5 | | | > 1.5 | | | > 1.5 | | | UI |
| | Jitter frequency = 250 KHz<br>Pattern = PRBS15 | > 0.15 | | | > 0.15 | | | > 0.15 | | | > 0.15 | | | UI |

**Table 1–40. Transceiver Block Jitter Specifications for Arria II GX Devices** *(Note 1)* **(Part 4 of 10)**

| Symbol/ Description | Conditions | I3 | | | C4 | | | C5, I5 | | | C6 | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Total jitter (peak-to-peak) | Pattern = CRPAT | — | — | 0.279 | — | — | 0.279 | — | — | 0.279 | — | — | 0.279 | UI |
| **GIGE Receiver Jitter Tolerance** *(6)* | | | | | | | | | | | | | | |
| Deterministic jitter tolerance (peak-to-peak) | Pattern = CJPAT | > 0.4 | | | > 0.4 | | | > 0.4 | | | > 0.4 | | | UI |
| Combined deterministic and random jitter tolerance (peak-to-peak) | Pattern = CJPAT | > 0.66 | | | > 0.66 | | | > 0.66 | | | > 0.66 | | | UI |
| **HiGig Transmit Jitter Generation** *(7)* | | | | | | | | | | | | | | |
| Deterministic jitter (peak-to-peak) | Data rate = 3.75 Gbps<br>Pattern = CJPAT | — | — | 0.17 | — | — | 0.17 | — | — | — | — | — | — | UI |
| Total jitter (peak-to-peak) | Data rate = 3.75 Gbps<br>Pattern = CJPAT | — | — | 0.35 | — | — | 0.35 | — | — | — | — | — | — | UI |
| **HiGig Receiver Jitter Tolerance** *(7)* | | | | | | | | | | | | | | |
| Deterministic jitter tolerance (peak-to-peak) | Data rate = 3.75 Gbps<br>Pattern = CJPAT | > 0.37 | | | > 0.37 | | | — | — | — | — | — | — | UI |
| Combined deterministic and random jitter tolerance (peak-to-peak) | Data rate = 3.75 Gbps<br>Pattern = CJPAT | > 0.65 | | | > 0.65 | | | — | — | — | — | — | — | UI |
| Sinusoidal jitter tolerance (peak-to-peak) | Jitter frequency = 22.1 KHz<br>Data rate = 3.75 Gbps<br>Pattern = CJPAT | > 8.5 | | | > 8.5 | | | — | — | — | — | — | — | UI |
| | Jitter frequency = 1.875MHz<br>Data rate = 3.75 Gbps<br>Pattern = CJPAT | > 0.1 | | | > 0.1 | | | — | — | — | — | — | — | UI |
| | Jitter frequency = 20 MHz<br>Data rate = 3.75 Gbps<br>Pattern = CJPAT | > 0.1 | | | > 0.1 | | | — | — | — | — | — | — | UI |

**Table 1–40. Transceiver Block Jitter Specifications for Arria II GX Devices *(Note 1)* (Part 5 of 10)**

| Symbol/ Description | Conditions | I3 | | | C4 | | | C5, I5 | | | C6 | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| **SDI Transmitter Jitter Generation *(8)*** | | | | | | | | | | | | | | |
| Alignment jitter (peak-to-peak) | Data rate = 1.485 Gbps (HD) pattern = Color Bar Low-frequency Roll-off = 100 KHz | 0.2 | — | — | 0.2 | — | — | 0.2 | — | — | 0.2 | — | — | UI |
| | Data rate = 2.97 Gbps (3G) pattern = Color bar Low-frequency Roll-off = 100 KHz | 0.3 | — | — | 0.3 | — | — | 0.3 | — | — | 0.3 | — | — | UI |
| **SDI Receiver Jitter Tolerance *(8)*** | | | | | | | | | | | | | | |
| Sinusoidal jitter tolerance (peak-to-peak) | Jitter frequency = 15 KHz<br>Data rate = 2.97 Gbps (3G) Pattern = single line scramble color bar | > 2 | | | > 2 | | | > 2 | | | > 2 | | | UI |
| | Jitter frequency = 100 KHz<br>Data rate = 2.97 Gbps (3G) Pattern = single line scramble color bar | > 0.3 | | | > 0.3 | | | > 0.3 | | | > 0.3 | | | UI |
| | Jitter frequency = 148.5 MHz<br>Data rate = 2.97 Gbps (3G) Pattern = single line scramble color bar | > 0.3 | | | > 0.3 | | | > 0.3 | | | > 0.3 | | | UI |

**Table 1–40. Transceiver Block Jitter Specifications for Arria II GX Devices** ***(Note 1)*** **(Part 8 of 10)**

| Symbol/ Description | Conditions | I3 | | | C4 | | | C5, I5 | | | C6 | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| **CPRI Transmit Jitter Generation** *(11)* | | | | | | | | | | | | | | |
| Total jitter | E.6.HV, E.12.HV<br>Pattern = CJPAT | — | — | 0.279 | — | — | 0.279 | — | — | 0.279 | — | — | 0.279 | UI |
| | E.6.LV, E.12.LV, E.24.LV, E.30.LV<br>Pattern = CJTPAT | — | — | 0.35 | — | — | 0.35 | — | — | 0.35 | — | — | 0.35 | UI |
| Deterministic jitter | E.6.HV, E.12.HV<br>Pattern = CJPAT | — | — | 0.14 | — | — | 0.14 | — | — | 0.14 | — | — | 0.14 | UI |
| | E.6.LV, E.12.LV, E.24.LV, E.30.LV<br>Pattern = CJTPAT | — | — | 0.17 | — | — | 0.17 | — | — | 0.17 | — | — | 0.17 | UI |
| **CPRI Receiver Jitter Tolerance** *(11)* | | | | | | | | | | | | | | |
| Total jitter tolerance | E.6.HV, E.12.HV<br>Pattern = CJPAT | > 0.66 | | | > 0.66 | | | > 0.66 | | | > 0.66 | | | UI |
| Deterministic jitter tolerance | E.6.HV, E.12.HV<br>Pattern = CJPAT | > 0.4 | | | > 0.4 | | | > 0.4 | | | > 0.4 | | | UI |
| Total jitter tolerance | E.6.LV, E.12.LV, E.24.LV, E.30.LV<br>Pattern = CJTPAT | > 0.65 | | | > 0.65 | | | > 0.65 | | | > 0.65 | | | UI |
| | E.60.LV<br>Pattern = PRBS31 | > 0.6 | | | — | | | — | | | — | | | UI |
| Deterministic jitter tolerance | E.6.LV, E.12.LV, E.24.LV, E.30.LV<br>Pattern = CJTPAT | > 0.37 | | | > 0.37 | | | > 0.37 | | | > 0.37 | | | UI |
| | E.60.LV<br>Pattern = PRBS31 | > 0.45 | | | — | | | — | | | — | | | UI |
| Combined deterministic and random jitter tolerance | E.6.LV, E.12.LV, E.24.LV, E.30.LV<br>Pattern = CJTPAT | > 0.55 | | | > 0.55 | | | > 0.55 | | | > 0.55 | | | UI |
| **OBSAI Transmit Jitter Generation** *(12)* | | | | | | | | | | | | | | |
| Total jitter at 768 Mbps, 1536 Mbps, and 3072 Mbps | REFCLK = 153.6 MHz<br>Pattern = CJPAT | — | — | 0.35 | — | — | 0.35 | — | — | 0.35 | — | — | 0.35 | UI |
| Deterministic jitter at 768 Mbps, 1536 Mbps, and 3072 Mbps | REFCLK = 153.6 MHz<br>Pattern = CJPAT | — | — | 0.17 | — | — | 0.17 | — | — | 0.17 | — | — | 0.17 | UI |

**Table 1–44. PLL Specifications for Arria II GX Devices (Part 3 of 3)**

| Symbol | Description | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $t_{CASC\_OUTJITTER\_PERIOD\_DEDCLK}$ (6), (7) | Period Jitter for dedicated clock output in cascaded PLLs (FOUT ≥ 100 MHz) | — | — | 425 | ps (p-p) |
| | Period Jitter for dedicated clock output in cascaded PLLs (FOUT ≤ 100 MHz) | — | — | 42.5 | mUI (p-p) |

**Notes to Table 1–44:**

(1) $f_{IN}$ is limited by the I/O $f_{MAX}$.

(2) The VCO frequency reported by the Quartus II software in the PLL summary section of the compilation report takes into consideration the VCO post-scale counter K value. Therefore, if the counter K has a value of 2, the frequency reported can be lower than the $f_{VCO}$ specification.

(3) A high-input jitter directly affects the PLL output jitter. To have low PLL output clock jitter, you must provide a clean-clock source, which is less than 200 ps.

(4) $F_{REF}$ is fIN/N when N = 1.

(5) This specification is limited by the lower of the two: I/O $f_{MAX}$ or $f_{OUT}$ of the PLL.

(6) Peak-to-peak jitter with a probability level of $10^{-12}$ (14 sigma, 99.99999999974404% confidence level). The output jitter specification applies to the intrinsic jitter of the PLL, when an input jitter of 30 ps is applied. The external memory interface clock output jitter specifications use a different measurement method and are available in Table 1–62 on page 1–70.

(7) The cascaded PLL specification is only applicable with the following condition:
a. Upstream PLL: 0.59 Mhz ≤ Upstream PLL BW < 1 MHz
b. Downstream PLL: Downstream PLL BW > 2 MHz

Table 1–45 lists the PLL specifications for Arria II GZ devices when operating in both the commercial junction temperature range (0° to 85°C) and the industrial junction temperature range (-40° to 100°C).

**Table 1–45. PLL Specifications for Arria II GZ Devices (Part 1 of 2)**

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $f_{IN}$ | Input clock frequency (–3 speed grade) | 5 | — | 717 (1) | MHz |
| | Input clock frequency (–4 speed grade) | 5 | — | 717 (1) | MHz |
| $f_{INPFD}$ | Input frequency to the PFD | 5 | — | 325 | MHz |
| $f_{VCO}$ | PLL VCO operating range (–3 speed grade) | 600 | — | 1,300 | MHz |
| | PLL VCO operating range (–4 speed grade) | 600 | — | 1,300 | MHz |
| $t_{EINDUTY}$ | Input clock or external feedback clock input duty cycle | 40 | — | 60 | % |
| $f_{OUT}$ | Output frequency for internal global or regional clock (–3 speed grade) | — | — | 700 (2) | MHz |
| | Output frequency for internal global or regional clock (–4 speed grade) | — | — | 500 (2) | MHz |
| $f_{OUT\_EXT}$ | Output frequency for external clock output (–3 speed grade) | — | — | 717 (2) | MHz |
| | Output frequency for external clock output (–4 speed grade) | — | — | 717 (2) | MHz |
| $t_{OUTDUTY}$ | Duty cycle for external clock output (when set to 50%) | 45 | 50 | 55 | % |
| $t_{FCOMP}$ | External feedback clock compensation time | — | — | 10 | ns |
| $t_{CONFIGPLL}$ | Time required to reconfigure scan chain | — | 3.5 | — | scanclk cycles |
| $t_{CONFIGPHASE}$ | Time required to reconfigure phase shift | — | 1 | — | scanclk cycles |
| $f_{SCANCLK}$ | scanclk frequency | — | — | 100 | MHz |
| $t_{LOCK}$ | Time required to lock from end-of-device configuration or de-assertion of areset | — | — | 1 | ms |

**Table 1–53. High-Speed I/O Specifications for Arria II GX Devices (Part 4 of 4)**

| Symbol | Conditions | I3 |  | C4 |  | C5,I5 |  | C6 |  | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
|  |  | Min | Max | Min | Max | Min | Max | Min | Max |  |
| $f_{HSDR}$ (data rate) | SERDES factor J = 3 to 10 | *(3)* | 945 *(7)* | *(3)* | 945 *(7)* | *(3)* | 740 *(7)* | *(3)* | 640 *(7)* | Mbps |
|  | SERDES factor J = 2 (using DDR registers) | *(3)* | *(7)* | *(3)* | *(7)* | *(3)* | *(7)* | *(3)* | *(7)* | Mbps |
|  | SERDES factor J = 1 (using SDR registers) | *(3)* | *(7)* | *(3)* | *(7)* | *(3)* | *(7)* | *(3)* | *(7)* | Mbps |
| Soft-CDR PPM tolerance | Soft-CDR mode | — | 300 | — | 300 | — | 300 | — | 300 | ±PPM |
| DPA run length | DPA mode | — | 10,000 | — | 10,000 | — | 10,000 | — | 10,000 | UI |
| Sampling window (SW) | Non-DPA mode *(5)* | — | 300 | — | 300 | — | 350 | — | 400 | ps |

**Notes to Table 1–53:**

(1) $f_{HSCLK\_IN} = f_{HSDR}$ / W. Use W to determine the supported selection of input reference clock frequencies for the desired data rate.

(2) Applicable for interfacing with DPA receivers only. For interfacing with non-DPA receivers, you must calculate the leftover timing margin in the receiver by performing link timing closure analysis. For Arria II GX transmitter to Arria II GX non-DPA receiver, the maximum supported data rate is 945 Mbps. For data rates above 840 Mbps, perform PCB trace compensation by adjusting the PCB trace length for LVDS channels to improve channel-to-channel skews.

(3) The minimum and maximum specification depends on the clock source (for example, PLL and clock pin) and the clock routing resource you use (global, regional, or local). The I/O differential buffer and input register do not have a minimum toggle rate.

(4) The specification is only applicable under the influence of core noise.

(5) Applicable for true LVDS using dedicated SERDES only.

(6) Dedicated SERDES and DPA features are only available on the right banks.

(7) You must calculate the leftover timing margin in the receiver by performing link timing closure analysis. You must consider the board skew margin, transmitter channel-to-channel skew, and the receiver sampling margin to determine the leftover timing margin.

Table 1–54 lists the high-speed I/O timing for Arria II GZ devices.

**Table 1–54. High-Speed I/O Specifications for Arria II GZ Devices *(Note 1), (2), (10)* (Part 1 of 3)**

| Symbol | Conditions | C3, I3 |  |  | C4, I4 |  |  | Unit |
|---|---|---|---|---|---|---|---|---|
|  |  | Min | Typ | Max | Min | Typ | Max |  |
| **Clock** |  |  |  |  |  |  |  |  |
| $f_{HSCLK\_in}$ (input clock frequency) true differential I/O standards | Clock boost factor W = 1 to 40 *(3)* | 5 | — | 717 | 5 | — | 717 | MHz |
| $f_{HSCLK\_in}$ (input clock frequency) single ended I/O standards *(9)* | Clock boost factor W = 1 to 40 *(3)* | 5 | — | 717 | 5 | — | 717 | MHz |
| $f_{HSCLK\_in}$ (input clock frequency) single ended I/O standards *(10)* | Clock boost factor W = 1 to 40 *(3)* | 5 | — | 420 | 5 | — | 420 | MHz |

Figure 1–6 shows the LVDS soft-CDR/DPA sinusoidal jitter tolerance specification for Arria II GZ devices at 1.25 Gbps data rate.

**Figure 1–6. LVDS Soft-CDR/DPA Sinusoidal Jitter Tolerance Specification for Arria II GZ Devices at a 1.25 Gbps Data Rate**

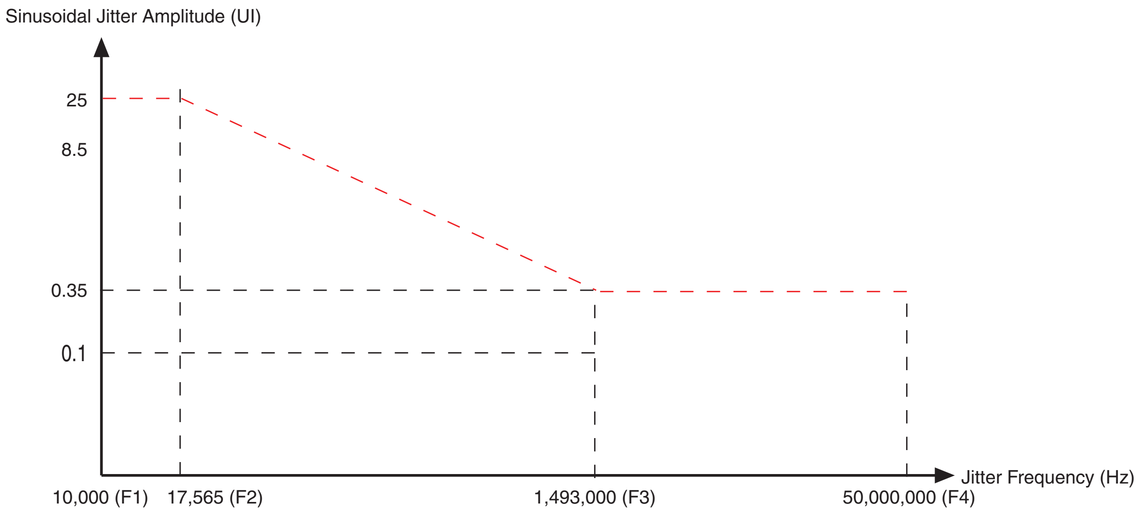


Table 1–56 lists the LVDS soft-CDR/DPA sinusoidal jitter tolerance specification for Arria II GZ devices at 1.25 Gbps data rate.

**Table 1–56. LVDS Soft-CDR/DPA Sinusoidal Jitter Mask Values for Arria II GZ Devices at 1.25 Gbps Data Rate**

| Jitter Frequency (Hz) | | Sinusoidal Jitter (UI) |
|---|---|---|
| F1 | 10,000 | 25.000 |
| F2 | 17,565 | 25.000 |
| F3 | 1,493,000 | 0.350 |
| F4 | 50,000,000 | 0.350 |

## External Memory Interface Specifications

For the maximum clock rate supported for Arria II GX and GZ device family, refer to the External Memory Interface Spec Estimator page on the Altera website.

Table 1–57 lists the external memory interface specifications for Arria II GX devices.

**Table 1–57. External Memory Interface Specifications for Arria II GX Devices (Part 1 of 2)**

| Frequency Mode | Frequency Range (MHz) | | | Resolution (°) | DQS Delay Buffer Mode *(1)* | Number of Delay Chains |
|---|---|---|---|---|---|---|
| | C4 | I3, C5, I5 | C6 | | | |
| 0 | 90-140 | 90-130 | 90-110 | 22.5 | Low | 16 |
| 1 | 110-180 | 110-170 | 110-150 | 30 | Low | 12 |
| 2 | 140-220 | 140-210 | 140-180 | 36 | Low | 10 |
| 3 | 170-270 | 170-260 | 170-220 | 45 | Low | 8 |
| 4 | 220-340 | 220-310 | 220-270 | 30 | High | 12 |

# I/O Timing

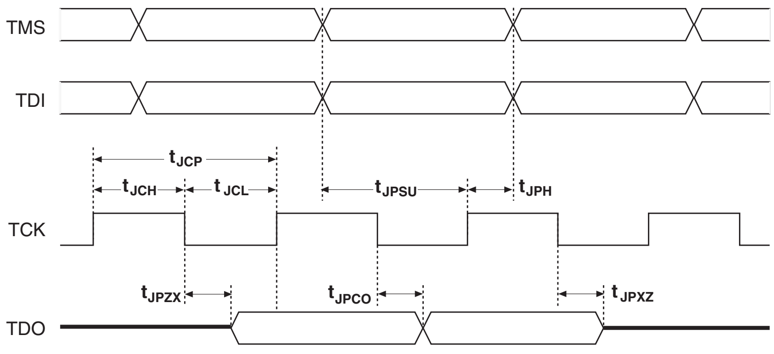
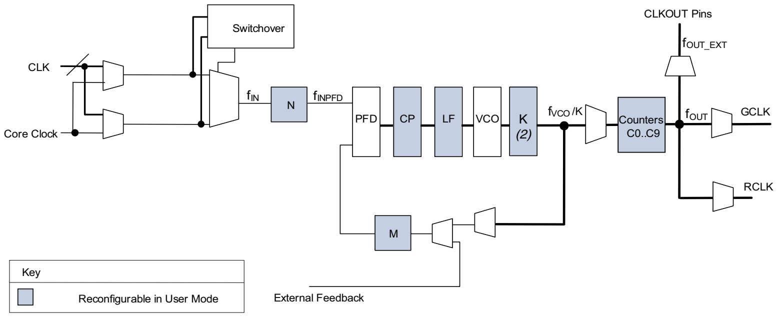
Altera offers two ways to determine I/O timing:

- Using the Microsoft Excel-based I/O Timing.
- Using the Quartus II Timing Analyzer.

The Microsoft Excel-based I/O Timing provides pin timing performance for each device density and speed grade. The data is typically used prior to designing the FPGA to get an estimate of the timing budget as part of the link timing analysis. The Quartus II timing analyzer provides a more accurate and precise I/O timing data based on the specifics of the design after place-and-route is complete.

The Microsoft Excel-based I/O Timing spreadsheet is downloadable from the Literature: Arria II Devices web page.

**Table 1–68. Glossary (Part 2 of 4)**

| Letter | Subject | Definitions |
|---|---|---|
| **G,<br>H,<br>I,<br>J** | J | High-speed I/O block: Deserialization factor (width of parallel data bus). |
| | JTAG Timing Specifications | JTAG Timing Specifications:<br><br> |
| **K,<br>L,<br>M,<br>N,<br>O,<br>P** | PLL Specifications | PLL Specification parameters:<br>**Diagram of PLL Specifications** *(1)*<br><br> <br>**Notes:**<br>(1) CoreClock can only be fed by dedicated clock input pins or PLL outputs.<br>(2) This is the VCO post-scale counter K. |
| **Q,<br>R** | **$R_L$** | Receiver differential input discrete resistor (external to the Arria II device). |