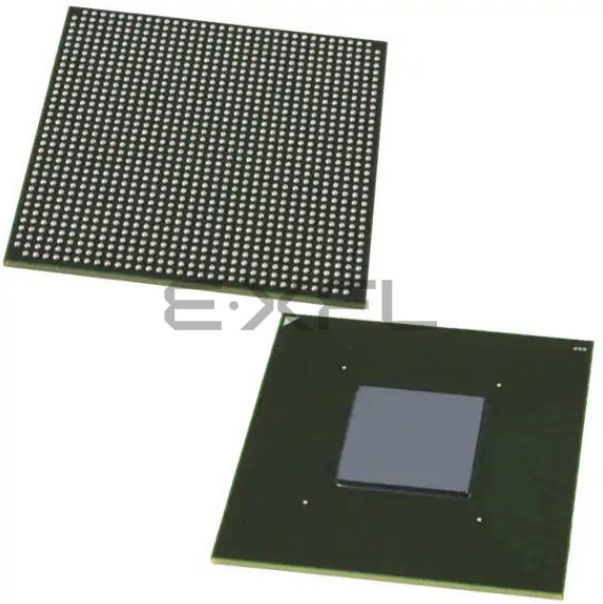

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Details	
Product Status	Obsolete
Number of LABs/CLBs	3747
Number of Logic Elements/Cells	89178
Total RAM Bits	6839296
Number of I/O	452
Number of Gates	-
Voltage - Supply	0.87V ~ 0.93V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	1152-BBGA, FCBGA
Supplier Device Package	1152-FBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep2agx95ef35i5es

Recommended Operating Conditions

This section lists the functional operation limits for AC and DC parameters for Arria II GX and GZ devices. All supplies are required to monotonically reach their full-rail values without plateaus within t_{RAMP}.

Table 1–5 lists the recommended operating conditions for Arria II GX devices.

Table 1–5. Recommended Operating Conditions for Arria II GX Devices *(Note 1)* (Part 1 of 2)

Symbol	Description	Condition	Minimum	Typical	Maximum	Unit
V_{CC}	Supplies power to the core, periphery, I/O registers, PCIe HIP block, and transceiver PCS	—	0.87	0.90	0.93	V
V_{CCCB}	Supplies power to the configuration RAM bits	—	1.425	1.50	1.575	V
V_{CCBAT} *(2)*	Battery back-up power supply for design security volatile key registers	—	1.2	—	3.3	V
V_{CCPD} *(3)*	Supplies power to the I/O pre-drivers, differential input buffers, and MSEL circuitry	—	3.135	3.3	3.465	V
		—	2.85	3.0	3.15	V
		—	2.375	2.5	2.625	V
V_{CCIO}	Supplies power to the I/O banks *(4)*	—	3.135	3.3	3.465	V
		—	2.85	3.0	3.15	V
		—	2.375	2.5	2.625	V
		—	1.71	1.8	1.89	V
		—	1.425	1.5	1.575	V
		—	1.14	1.2	1.26	V
V_{CCD_PLL}	Supplies power to the digital portions of the PLL	—	0.87	0.90	0.93	V
V_{CCA_PLL}	Supplies power to the analog portions of the PLL and device-wide power management circuitry	—	2.375	2.5	2.625	V
V_I	DC Input voltage	—	–0.5	—	3.6	V
V_O	Output voltage	—	0	—	V_{CCIO}	V
V_{CCA}	Supplies power to the transceiver PMA regulator	—	2.375	2.5	2.625	V
V_{CCL_GXB}	Supplies power to the transceiver PMA TX, PMA RX, and clocking	—	1.045	1.1	1.155	V
V_{CCH_GXB}	Supplies power to the transceiver PMA output (TX) buffer	—	1.425	1.5	1.575	V
T_J	Operating junction temperature	Commercial	0	—	85	°C
		Industrial	–40	—	100	°C

Table 1–10 lists the bus hold specifications for Arria II GZ devices.

Table 1–10. Bus Hold Parameters for Arria II GZ Devices

Parameter	Symbol	Cond.	V_{CCIO} (V)										Unit
			1.2		1.5		1.8		2.5		3.0		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Bus-hold Low sustaining current	I_{SUSL}	$V_{IN} > V_{IL}$ (max.)	22.5	—	25.0	—	30.0	—	50.0	—	70.0	—	µA
Bus-hold High sustaining current	I_{SUSH}	$V_{IN} < V_{IH}$ (min.)	-22.5	—	-25.0	—	-30.0	—	-50.0	—	-70.0	—	µA
Bus-hold Low overdrive current	I_{ODL}	$0V < V_{IN} < V_{CCIO}$	—	120	—	160	—	200	—	300	—	500	µA
Bus-hold High overdrive current	I_{ODH}	$0V < V_{IN} < V_{CCIO}$	—	-120	—	-160	—	-200	—	-300	—	-500	µA
Bus-hold trip point	V_{TRIP}	—	0.45	0.95	0.50	1.00	0.68	1.07	0.70	1.70	0.80	2.00	V

OCT Specifications

Table 1–11 lists the Arria II GX device and differential OCT with and without calibration accuracy.

Table 1–11. OCT With and Without Calibration Specification for Arria II GX Device I/Os *(Note 1)* (Part 1 of 2)

Symbol	Description	Conditions (V)	Calibration Accuracy		Unit
			Commercial	Industrial	
25-Ω R_S 3.0, 2.5	25-Ω series OCT without calibration	V_{CCIO} = 3.0, 2.5	± 30	± 40	%
50-Ω R_S 3.0, 2.5	50-Ω series OCT without calibration	V_{CCIO} = 3.0, 2.5	± 30	± 40	%
25-Ω R_S 1.8	25-Ω series OCT without calibration	V_{CCIO} = 1.8	± 40	± 50	%
50-Ω R_S 1.8	50-Ω series OCT without calibration	V_{CCIO} = 1.8	± 40	± 50	%
25-Ω R_S 1.5, 1.2	25-Ω series OCT without calibration	V_{CCIO} = 1.5, 1.2	± 50	± 50	%
50-Ω R_S 1.5, 1.2	50-Ω series OCT without calibration	V_{CCIO} = 1.5, 1.2	± 50	± 50	%
25-Ω R_S 3.0, 2.5, 1.8, 1.5, 1.2	25-Ω series OCT with calibration	V_{CCIO} = 3.0, 2.5, 1.8, 1.5, 1.2	± 10	± 10	%

Table 1–33 lists the differential I/O standard specifications for Arria II GZ devices.

Table 1–33. Differential I/O Standard Specifications for Arria II GZ Devices *(Note 1)*

I/O Standard *(2)*	V_{CCIO} (V)			V_{ID} (mV)			$V_{ICM(DC)}$ (V)		V_{OD} (V) *(3)*			V_{OCM} (V) *(3)*		
	Min	Typ	Max	Min	Cond.	Max	Min	Max	Min	Typ	Max	Min	Typ	Max
2.5 V LVDS (HIO)	2.375	2.5	2.625	100	V_{CM} = 1.25 V	—	0.05	1.8	0.247	—	0.6	1.125	1.25	1.375
2.5 V LVDS (VIO)	2.375	2.5	2.625	100	V_{CM} = 1.25 V	—	0.05	1.8	0.247	—	0.6	1	1.25	1.5
RSDS (HIO)	2.375	2.5	2.625	100	V_{CM} = 1.25 V	—	0.3	1.4	0.1	0.2	0.6	0.5	1.2	1.4
RSDS (VIO)	2.375	2.5	2.625	100	V_{CM} = 1.25 V	—	0.3	1.4	0.1	0.2	0.6	0.5	1.2	1.5
Mini-LVDS (HIO)	2.375	2.5	2.625	200	—	600	0.4	1.325	0.25	—	0.6	1	1.2	1.4
Mini-LVDS (VIO)	2.375	2.5	2.625	200	—	600	0.4	1.325	0.25	—	0.6	1	1.2	1.5
LVPECL	2.375	2.5	2.625	300	—	—	0.6	1.8	—	—	—	—	—	—
BLVDS *(4)*	2.375	2.5	2.625	100	—	—	—	—	—	—	—	—	—	—

Notes to Table 1–33:

(1) 1.4-V/1.5-V PCML transceiver I/O standard specifications are described in "Transceiver Performance Specifications" on page 1–21.
(2) Vertical I/O (VIO) is top and bottom I/Os; horizontal I/O (HIO) is left and right I/Os.
(3) R_L range: $90 \leq RL \leq 110\ \Omega$.
(4) There are no fixed V_{ICM}, V_{OD}, and V_{OCM} specifications for BLVDS. These specifications depend on the system topology.

Power Consumption for the Arria II Device Family

Altera offers two ways to estimate power for a design:

- Using the Microsoft Excel-based Early Power Estimator
- Using the Quartus® II PowerPlay Power Analyzer feature

The interactive Microsoft Excel-based Early Power Estimator is typically used prior to designing the FPGA in order to get a magnitude estimate of the device power. The Quartus II PowerPlay Power Analyzer provides better quality estimates based on the specifics of the design after place-and-route is complete. The PowerPlay Power Analyzer can apply a combination of user-entered, simulation-derived, and estimated signal activities which, when combined with detailed circuit models, can yield very accurate power estimates.

For more information about power estimation tools, refer to the *PowerPlay Early Power Estimator User Guide* and the *PowerPlay Power Analysis* chapter in volume 3 of the *Quartus II Handbook*.

Switching Characteristics

This section provides performance characteristics of the Arria II GX and GZ core and periphery blocks for commercial grade devices. The following tables are considered final and are based on actual silicon characterization and testing. These numbers reflect the actual performance of the device under worst-case silicon process, voltage, and junction temperature conditions.

Transceiver Performance Specifications

Table 1–34 lists the Arria II GX transceiver specifications.

Table 1–34. Transceiver Specifications for Arria II GX Devices *(Note 1)* (Part 1 of 7)

Symbol/ Description	Condition	I3			C4			C5 and I5			C6			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Reference Clock														
Supported I/O Standards	1.2-V PCML, 1.5-V PCML, 2.5-V PCML, Differential LVPECL, LVDS, and HCSL													
Input frequency from REFCLK input pins	—	50	—	622.08	50	—	622.08	50	—	622.08	50	—	622.08	MHz
Input frequency from PLD input	—	50	—	200	50	—	200	50	—	200	50	—	200	MHz
Absolute V_{MAX} for a REFCLK pin	—	—	—	2.2	—	—	2.2	—	—	2.2	—	—	2.2	V
Absolute V_{MIN} for a REFCLK pin	—	–0.3	—	—	–0.3	—	—	–0.3	—	—	–0.3	—	—	V
Rise/fall time *(2)*	—	—	—	0.2	—	—	0.2	—	—	0.2	—	—	0.2	UI
Duty cycle	—	45	—	55	45	—	55	45	—	55	45	—	55	%
Peak-to-peak differential input voltage	—	200	—	2000	200	—	2000	200	—	2000	200	—	2000	mV
Spread-spectrum modulating clock frequency	PCIe	30	—	33	30	—	33	30	—	33	30	—	33	kHz

Table 1–34. Transceiver Specifications for Arria II GX Devices *(Note 1)* (Part 4 of 7)

Symbol/ Description	Condition	I3			C4			C5 and I5			C6			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Minimum peak-to-peak differential input voltage V_{ID} (diff p-p)	—	100	—	—	100	—	—	100	—	—	100	—	—	mV
V_{ICM}	V_{ICM} = 0.82 V setting	—	820	—	—	820	—	—	820	—	—	820	—	mV
	V_{ICM} =1.1 V setting *(7)*	—	1100	—	—	1100	—	—	1100	—	—	1100	—	mV
Differential on-chip termination resistors	100–Ω setting	—	100	—	—	100	—	—	100	—	—	100	—	Ω
Return loss differential mode	PCIe				50 MHz to 1.25 GHz: –10dB									
	XAUI				100 MHz to 2.5 GHz: –10dB									
Return loss common mode	PCIe				50 MHz to 1.25 GHz: –6dB									
	XAUI				100 MHz to 2.5 GHz: –6dB									
Programmable PPM detector *(8)*	—	± 62.5, 100, 125, 200, 250, 300, 500, 1000												ppm
Run length	—	—	80	—	—	80	—	—	80	—	—	80	—	UI
Programmable equalization	—	—	—	7	—	—	7	—	—	7	—	—	7	dB
Signal detect/loss threshold	PCIe Mode	65	—	175	65	—	175	65	—	175	65	—	175	mV
CDR LTR time *(9)*	—	—	—	75	—	—	75	—	—	75	—	—	75	µs
CDR minimum T1b *(10)*	—	15	—	—	15	—		15	—	—	15	—	—	µs

Table 1–34. Transceiver Specifications for Arria II GX Devices *(Note 1)* (Part 6 of 7)

Symbol/ Description	Condition	I3			C4			C5 and I5			C6			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Intra-differential pair skew	—	—	—	15	—	—	15	—	—	15	—	—	15	ps
Intra-transceiver block skew	PCIe ×4	—	—	120	—	—	120	—	—	120	—	—	120	ps
Inter-transceiver block skew	PCIe ×8	—	—	300	—	—	300	—	—	300	—	—	300	ps
CMU PLL0 and CMU PLL1														
CMU PLL lock time from `CMUPLL_reset` deassertion	—	—	—	100	—	—	100	—	—	100	—	—	100	µs
PLD-Transceiver Interface														
Interface speed	—	25	—	320	25	—	240	25	—	240	25	—	200	MHz

Table 1–34. Transceiver Specifications for Arria II GX Devices *(Note 1)* (Part 7 of 7)

Symbol/ Description	Condition	I3			C4			C5 and I5			C6			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Digital reset pulse width	—	Minimum is 2 parallel clock cycles												

Notes to Table 1–34:

(1) For AC-coupled links, the on-chip biasing circuit is switched off before and during configuration. Ensure that input specifications are not violated during this period.

(2) The rise/fall time is specified from 20% to 80%.

(3) To calculate the REFCLK rms phase jitter requirement at reference clock frequencies other than 100 MHz, use the following formula:
REFCLK rms phase jitter at f (MHz) = REFCLK rms phase jitter at 100 MHz * 100/f.

(4) The minimum `reconfig_clk` frequency is 2.5 MHz if the transceiver channel is configured in **Transmitter only** mode. The minimum `reconfig_clk` frequency is 37.5 MHz if the transceiver channel is configured in **Receiver only** or **Receiver and Transmitter** mode. For more information, refer to *AN 558: Implementing Dynamic Reconfiguration in Arria II Devices*.

(5) If your design uses more than one dynamic reconfiguration controller instances (`altgx_reconfig`) to control the transceiver channels (`altgx`) physically located on the same side of the device, and if you use different `reconfig_clk` sources for these `altgx_reconfig` instances, the delta time between any two of these `reconfig_clk` sources becoming stable must not exceed the maximum specification listed.

(6) The device cannot tolerate prolonged operation at this absolute maximum.

(7) You must use the 1.1-V RX V_{ICM} setting if the input serial data standard is LVDS and the link is DC-coupled.

(8) The rate matcher supports only up to ±300 parts per million (ppm).

(9) Time taken to `rx_pll_locked` goes high from `rx_analogreset` de-assertion. Refer to Figure 1–1.

(10) The time in which the CDR must be kept in lock-to-reference mode after `rx_pll_locked` goes high and before `rx_locktodata` is asserted in manual mode. Refer to Figure 1–1.

(11) The time taken to recover valid data after the `rx_locktodata` signal is asserted in manual mode. Refer to Figure 1–1.

(12) The time taken to recover valid data after the `rx_freqlocked` signal goes high in automatic mode. Refer to Figure 1–2.

(13) To support data rates lower than the minimum specification through oversampling, use the CDR in LTR mode only.

Table 1–35. Transceiver Specifications for Arria II GZ Devices (Part 3 of 5)

Symbol/ Description	Conditions	–C3 and –I3 *(1)*			–C4 and –I4			Unit
		Min	Typ	Max	Min	Typ	Max	
Receiver DC Coupling Support	—	For more information about receiver DC coupling support, refer to the "DC-Coupled Links" section in the *Transceiver Architecture for Arria II Devices* chapter.						
Differential on-chip termination resistors	85–Ω setting	85 ± 20%			85 ± 20%			Ω
	100–Ω setting	100 ± 20%			100 ± 20%			Ω
	120–Ω setting	120 ± 20%			120 ± 20%			Ω
	150-Ω setting	150 ± 20%			150 ± 20%			Ω
Differential and common mode return loss	PCIe (Gen 1 and Gen 2), XAUI, HiGig+, CEI SR/LR, SRIO SR/LR, CPRI LV/HV, OBSAI, SATA	Compliant						—
Programmable PPM detector *(9)*	—	± 62.5, 100, 125, 200, 250, 300, 500, 1,000						ppm
Run length	—	—	—	200	—	—	200	UI
Programmable equalization	—	—	—	16	—	—	16	dB
t_{LTR} *(10)*	—	—	—	75	—	—	75	µs
$t_{LTR\_LTD\_Manual}$ *(11)*	—	15	—	—	15	—	—	µs
t_{LTD_Manual} *(12)*	—	—	—	4000	—	—	4000	ns
t_{LTD_Auto} *(13)*	—	—	—	4000	—	—	4000	ns
Receiver CDR 3 dB Bandwidth in lock-to-data (LTD) mode	PCIe Gen1	2.0 - 3.5						MHz
	PCIe Gen2	40 - 65						MHz
	(OIF) CEI PHY at 6.375 Gbps	20 - 35						MHz
	XAUI	10 - 18						MHz
	SRIO 1.25 Gbps	10 - 18						MHz
	SRIO 2.5 Gbps	10 - 18						MHz
	SRIO 3.125 Gbps	6 - 10						MHz
	GIGE	6 - 10						MHz
	SONET OC12	3 - 6						MHz
	SONET OC48	14 - 19						MHz
Receiver buffer and CDR offset cancellation time (per channel)	—	—	—	17000	—	—	17000	reconfig_clk cycles
Programmable DC gain	DC Gain Setting = 0	—	0	—	—	0	—	dB
	DC Gain Setting = 1	—	3	—	—	3	—	dB
	DC Gain Setting = 2	—	6	—	—	6	—	dB

Table 1–35. Transceiver Specifications for Arria II GZ Devices (Part 4 of 5)

Symbol/ Description	Conditions	–C3 and –I3 *(1)*			–C4 and –I4			Unit
		Min	Typ	Max	Min	Typ	Max	
Transmitter								
Supported I/O Standards	1.5-V PCML							
Data rate *(14)*	—	600	—	6375	600	—	3750	Mbps
V_{OCM}	0.65 V setting	—	650	—	—	650	—	mV
Differential on-chip termination resistors	85–Ω setting	85 ± 15%			85 ± 15%			Ω
	100–Ω setting	100 ± 15%			100 ± 15%			Ω
	120–Ω setting	120 ± 15%			120 ± 15%			Ω
	150-Ω setting	150 ± 15%			150 ± 15%			Ω
Differential and common mode return loss	PCIe Gen1 and Gen2 (TX V_{OD}=4), XAUI (TX V_{OD}=6), HiGig+ (TX V_{OD}=6), CEI SR/LR (TX V_{OD}=8), SRIO SR (V_{OD}=6), SRIO LR (V_{OD}=8), CPRI LV (V_{OD}=6), CPRI HV (V_{OD}=2), OBSAI (V_{OD}=6), SATA (V_{OD}=4),	Compliant						—
Rise time *(15)*	—	50	—	200	50	—	200	ps
Fall time *(15)*	—	50	—	200	50	—	200	ps
Intra-differential pair skew	—	—	—	15	—	—	15	ps
Intra-transceiver block transmitter channel-to-channel skew	×4 PMA and PCS bonded mode Example: XAUI, PCIe ×4, Basic ×4	—	—	120	—	—	120	ps
Inter-transceiver block transmitter channel-to-channel skew	×8 PMA and PCS bonded mode Example: PCIe ×8, Basic ×8	—	—	500	—	—	500	ps
CMU0 PLL and CMU1 PLL								
Supported Data Range	—	600	—	6375	600	—	3750	Mbps
`pll_powerdown` minimum pulse width (`tpll_powerdown`)	—	1			1			µs
CMU PLL lock time from `pll_powerdown` de-assertion	—	—	—	100	—	—	100	µs

Figure 1–3 shows the differential receiver input waveform.

Figure 1–3. Receiver Input Waveform

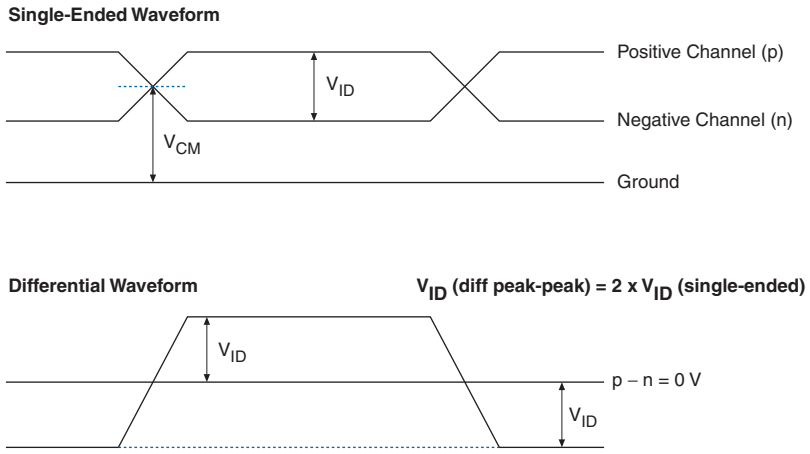

Figure 1–4 shows the transmitter output waveform.

Figure 1–4. Transmitter Output Waveform

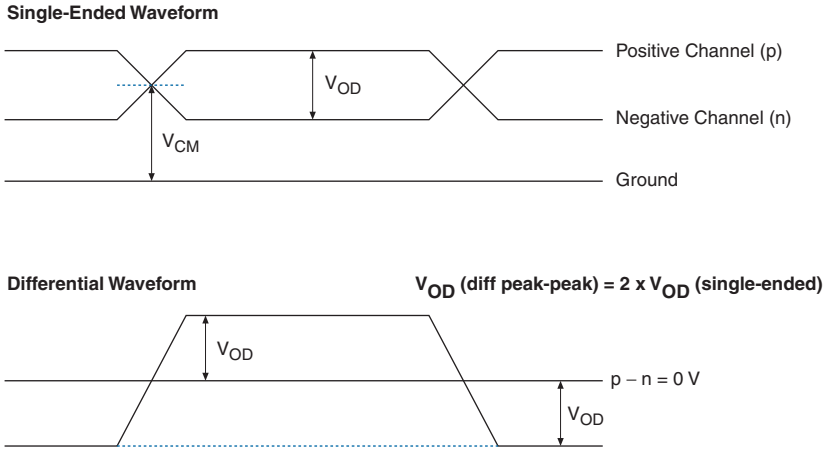

Table 1–36 lists the typical V_{OD} for TX term that equals 85 Ω for Arria II GZ devices.

Table 1–36. Typical V_{OD} Setting, TX Term = 85 Ω for Arria II GZ Devices

Symbol	V_{OD} Setting (mV)							
	0	1	2	3	4	5	6	7
V_{OD} differential peak-to-peak Typical (mV)	170 ± 20%	340 ± 20%	510 ± 20%	595 ± 20%	680 ± 20%	765 ± 20%	850 ± 20%	1020 ± 20%

Table 1–39 lists typical transmitter pre-emphasis levels for Arria II GZ devices (in dB) for the first post tap under the following conditions (low-frequency data pattern [five 1s and five 0s] at 6.25 Gbps). The levels listed in Table 1–39 are a representation of possible pre-emphasis levels under the specified conditions only and that the pre-emphasis levels may change with data pattern and data rate.

To predict the pre-emphasis level for your specific data rate and pattern, run simulations using the Arria II HSSI HSPICE models.

Table 1–39. Transmitter Pre-Emphasis Levels for Arria II GZ Devices (Part 1 of 2)

Pre-Emphasis 1st Post-Tap Setting	V_{OD} Setting							
	0	1	2	3	4	5	6	7
0	0	0	0	0	0	0	0	0
1	N/A	0.7	0	0	0	0	0	0
2	N/A	1	0.3	0	0	0	0	0
3	N/A	1.5	0.6	0	0	0	0	0
4	N/A	2	0.7	0.3	0	0	0	0
5	N/A	2.7	1.2	0.5	0.3	0	0	0
6	N/A	3.1	1.3	0.8	0.5	0.2	0	0
7	N/A	3.7	1.8	1.1	0.7	0.4	0.2	0
8	N/A	4.2	2.1	1.3	0.9	0.6	0.3	0
9	N/A	4.9	2.4	1.6	1.2	0.8	0.5	0.2
10	N/A	5.4	2.8	1.9	1.4	1	0.7	0.3
11	N/A	6	3.2	2.2	1.7	1.2	0.9	0.4
12	N/A	6.8	3.5	2.6	1.9	1.4	1.1	0.6
13	N/A	7.5	3.8	2.8	2.1	1.6	1.2	0.6
14	N/A	8.1	4.2	3.1	2.3	1.7	1.3	0.7
15	N/A	8.8	4.5	3.4	2.6	1.9	1.5	0.8
16	N/A	N/A	4.9	3.7	2.9	2.2	1.7	0.9
17	N/A	N/A	5.3	4	3.1	2.4	1.8	1.1
18	N/A	N/A	5.7	4.4	3.4	2.6	2	1.2
19	N/A	N/A	6.1	4.7	3.6	2.8	2.2	1.4
20	N/A	N/A	6.6	5.1	4	3.1	2.4	1.5
21	N/A	N/A	7	5.4	4.3	3.3	2.7	1.7
22	N/A	N/A	8	6.1	4.8	3.8	3	2
23	N/A	N/A	9	6.8	5.4	4.3	3.4	2.3
24	N/A	N/A	10	7.6	6	4.8	3.9	2.6
25	N/A	N/A	11.4	8.4	6.8	5.4	4.4	3
26	N/A	N/A	12.6	9.4	7.4	5.9	4.9	3.3
27	N/A	N/A	N/A	10.3	8.1	6.4	5.3	3.6
28	N/A	N/A	N/A	11.3	8.8	7.1	5.8	4

Table 1–40. Transceiver Block Jitter Specifications for Arria II GX Devices *(Note 1)* (Part 8 of 10)

Symbol/ Description	Conditions	I3			C4			C5, I5			C6			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
CPRI Transmit Jitter Generation *(11)*														
Total jitter	E.6.HV, E.12.HV Pattern = CJPAT	—	—	0.279	—	—	0.279	—	—	0.279	—	—	0.279	UI
	E.6.LV, E.12.LV, E.24.LV, E.30.LV Pattern = CJTPAT	—	—	0.35	—	—	0.35	—	—	0.35	—	—	0.35	UI
Deterministic jitter	E.6.HV, E.12.HV Pattern = CJPAT	—	—	0.14	—	—	0.14	—	—	0.14	—	—	0.14	UI
	E.6.LV, E.12.LV, E.24.LV, E.30.LV Pattern = CJTPAT	—	—	0.17	—	—	0.17	—	—	0.17	—	—	0.17	UI
CPRI Receiver Jitter Tolerance *(11)*														
Total jitter tolerance	E.6.HV, E.12.HV Pattern = CJPAT	> 0.66			> 0.66			> 0.66			> 0.66			UI
Deterministic jitter tolerance	E.6.HV, E.12.HV Pattern = CJPAT	> 0.4			> 0.4			> 0.4			> 0.4			UI
Total jitter tolerance	E.6.LV, E.12.LV, E.24.LV, E.30.LV Pattern = CJTPAT	> 0.65			> 0.65			> 0.65			> 0.65			UI
	E.60.LV Pattern = PRBS31	> 0.6			—			—			—			UI
Deterministic jitter tolerance	E.6.LV, E.12.LV, E.24.LV, E.30.LV Pattern = CJTPAT	> 0.37			> 0.37			> 0.37			> 0.37			UI
	E.60.LV Pattern = PRBS31	> 0.45			—			—			—			UI
Combined deterministic and random jitter tolerance	E.6.LV, E.12.LV, E.24.LV, E.30.LV Pattern = CJTPAT	> 0.55			> 0.55			> 0.55			> 0.55			UI
OBSAI Transmit Jitter Generation *(12)*														
Total jitter at 768 Mbps, 1536 Mbps, and 3072 Mbps	REFCLK = 153.6 MHz Pattern = CJPAT	—	—	0.35	—	—	0.35	—	—	0.35	—	—	0.35	UI
Deterministic jitter at 768 Mbps, 1536 Mbps, and 3072 Mbps	REFCLK = 153.6 MHz Pattern = CJPAT	—	—	0.17	—	—	0.17	—	—	0.17	—	—	0.17	UI

Table 1–40. Transceiver Block Jitter Specifications for Arria II GX Devices *(Note 1)* (Part 9 of 10)

Symbol/ Description	Conditions	I3			C4			C5, I5			C6			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
OBSAI Receiver Jitter Tolerance *(12)*														
Deterministic jitter tolerance at 768 Mbps, 1536 Mbps, and 3072 Mbps	Pattern = CJPAT	> 0.37			> 0.37			> 0.37			> 0.37			UI
Combined deterministic and random jitter tolerance at 768 Mbps, 1536 Mbps, and 3072 Mbps	Pattern = CJPAT	> 0.55			> 0.55			> 0.55			> 0.55			UI
Sinusoidal jitter tolerance at 768 Mbps	Jitter frequency = 5.4 KHz Pattern = CJPAT	> 8.5			> 8.5			> 8.5			> 8.5			UI
	Jitter frequency = 460.8 KHz to 20 MHz Pattern = CJPAT	> 0.1			> 0.1			> 0.1			> 0.1			UI
Sinusoidal jitter tolerance at 1536 Mbps	Jitter frequency = 10.9 KHz Pattern = CJPAT	> 8.5			> 8.5			> 8.5			> 8.5			UI
	Jitter frequency = 921.6 KHz to 20 MHz Pattern = CJPAT	> 0.1			> 0.1			> 0.1			> 0.1			UI

Table 1–41. Transceiver Block Jitter Specifications for Arria II GZ Devices *(Note 1)*, *(2)* (Part 4 of 7)

Symbol/ Description	Conditions	–C3 and –I3			–C4 and –I4			Unit
		Min	Typ	Max	Min	Typ	Max	
GIGE Receiver Jitter Tolerance *(11)*								
Deterministic jitter tolerance (peak-to-peak)	Pattern = CJPAT		> 0.4			> 0.4		UI
Combined deterministic and random jitter tolerance (peak-to-peak)	Pattern = CJPAT		> 0.66			> 0.66		UI
HiGig Transmit Jitter Generation								
Deterministic jitter (peak-to-peak)	Data rate = 3.75 Gbps Pattern = CJPAT	—	—	0.17	—	—	—	UI
Total jitter (peak-to-peak)	Data rate = 3.75 Gbps Pattern = CJPAT	—	—	0.35	—	—	—	UI
HiGig Receiver Jitter Tolerance								
Deterministic jitter tolerance (peak-to-peak)	Data rate = 3.75 Gbps Pattern = CJPAT		> 0.37		—	—	—	UI
Combined deterministic and random jitter tolerance (peak-to-peak)	Data rate = 3.75 Gbps Pattern = CJPAT		> 0.65		—	—	—	UI
Sinusoidal jitter tolerance (peak-to-peak)	Jitter frequency = 22.1 KHz Data rate = 3.75 Gbps Pattern = CJPAT		> 8.5		—	—	—	UI
	Jitter frequency = 22.1 KHz Data rate = 3.75 Gbps Pattern = CJPAT		> 0.1		—	—	—	UI
	Jitter frequency = 22.1 KHz Data rate = 3.75 Gbps Pattern = CJPAT		> 0.1		—	—	—	UI
(OIF) CEI Transmitter Jitter Generation								
Total jitter (peak-to-peak)	Data rate = 6.375 Gbps Pattern = PRBS15 BER = 10^{-12}	—	—	0.3	—	—	0.3	UI
(OIF) CEI Receiver Jitter Tolerance								
Deterministic jitter tolerance (peak-to-peak)	Data rate = 6.375 Gbps Pattern = PRBS31 BER = 10^{-12}		> 0.675		—	—	—	UI
Combined deterministic and random jitter tolerance (peak-to-peak)	Data rate = 6.375 Gbps Pattern = PRBS31 BER = 10^{-12}		> 0.988		—	—	—	UI

Table 1–41. Transceiver Block Jitter Specifications for Arria II GZ Devices *(Note 1)*, *(2)* (Part 7 of 7)

Symbol/ Description	Conditions	–C3 and –I3			–C4 and –I4			Unit
		Min	Typ	Max	Min	Typ	Max	
OBSAI Receiver Jitter Tolerance *(15)*								
Deterministic jitter tolerance at 768 Mbps, 1536 Mbps, and 3072 Mbps	Pattern = CJPAT		> 0.37			> 0.37		UI
Combined deterministic and random jitter tolerance at 768 Mbps, 1536 Mbps, and 3072 Mbps	Pattern = CJPAT		> 0.55			> 0.55		UI
Sinusoidal jitter tolerance at 768 Mbps	Jitter frequency = 5.4 KHz Pattern = CJPAT		> 8.5			> 8.5		UI
	Jitter frequency = 460 MHz to 20 MHz Pattern = CJPAT		> 0.1			> 0.1		UI
Sinusoidal jitter tolerance at 1536 Mbps	Jitter frequency = 10.9 KHz Pattern = CJPAT		> 8.5			> 8.5		UI
	Jitter frequency = 921.6 MHz to 20 MHz Pattern = CJPAT		> 0.1			> 0.1		UI
Sinusoidal jitter tolerance at 3072 Mbps	Jitter frequency = 21.8 KHz Pattern = CJPAT		> 8.5			> 8.5		UI
	Jitter frequency = 1843.2 MHz to 20 MHz Pattern = CJPAT		> 0.1			> 0.1		UI

Notes to Table 1–41:

(1) Dedicated `refclk` pins were used to drive the input reference clocks.
(2) The jitter numbers are valid for the stated conditions only.
(3) The jitter numbers for SONET/SDH are compliant to the GR-253-CORE Issue 3 Specification.
(4) The jitter numbers for Fibre Channel are compliant to the FC-PI-4 Specification revision 6.10.
(5) The Fibre Channel transmitter jitter generation numbers are compliant to the specification at the δ_T inter operability point.
(6) The Fibre Channel receiver jitter tolerance numbers are compliant to the specification at the δ_R interpretability point.
(7) The jitter numbers for XAUI are compliant to the IEEE802.3ae-2002 Specification.
(8) The jitter numbers for PCIe are compliant to the PCIe Base Specification 2.0.
(9) Arria II GZ PCIe receivers are compliant to this specification provided the $V_{TX-CM-DC-ACTIVEIDLE-DELTA}$ of the upstream transmitter is less than 50 mV.
(10) The jitter numbers for SRIO are compliant to the RapidIO Specification 1.3.
(11) The jitter numbers for GIGE are compliant to the IEEE802.3-2002 Specification.
(12) The HD-SDI and 3G-SDI jitter numbers are compliant to the SMPTE292M and SMPTE424M Specifications.
(13) The jitter numbers for Serial Attached SCSI (SAS) are compliant to the SAS-2.1 Specification.
(14) The jitter numbers for CPRI are compliant to the CPRI Specification V3.0.
(15) The jitter numbers for OBSAI are compliant to the OBSAI RP3 Specification V4.1.

Core Performance Specifications for the Arria II Device Family

This section describes the clock tree, phase-locked loop (PLL), digital signal processing (DSP), embedded memory, configuration, and JTAG specifications for Arria II GX and GZ devices.

Clock Tree Specifications

Table 1–42 lists the clock tree specifications for Arria II GX devices.

Table 1–42. Clock Tree Performance for Arria II GX Devices

Clock Network	Performance			Unit
	I3, C4	C5,I5	C6	
GCLK and RCLK	500	500	400	MHz
PCLK	420	350	280	MHz

Table 1–43 lists the clock tree specifications for Arria II GZ devices.

Table 1–43. Clock Tree Performance for Arria II GZ Devices

Clock Network	Performance		Unit
	–C3 and –I3	–C4 and –I4	
GCLK and RCLK	700	500	MHz
PCLK	500	450	MHz

PLL Specifications

Table 1–44 lists the PLL specifications for Arria II GX devices.

Table 1–44. PLL Specifications for Arria II GX Devices (Part 1 of 3)

Symbol	Description	Min	Typ	Max	Unit
f_{IN}	Input clock frequency (from clock input pins residing in right/top/bottom banks) (–4 Speed Grade)	5	—	670 *(1)*	MHz
	Input clock frequency (from clock input pins residing in right/top/bottom banks) (–5 Speed Grade)	5	—	622 *(1)*	MHz
	Input clock frequency (from clock input pins residing in right/top/bottom banks) (–6 Speed Grade)	5	—	500 *(1)*	MHz
f_{INPFD}	Input frequency to the PFD	5	—	325	MHz
f_{VCO}	PLL VCO operating Range *(2)*	600	—	1,400	MHz
f_{INDUTY}	Input clock duty cycle	40	—	60	%
$f_{EINDUTY}$	External feedback clock input duty cycle	40	—	60	%
t_{INCCJ} *(3)*, *(4)*	Input clock cycle-to-cycle jitter (Frequency ≥ 100 MHz)	—	—	0.15	UI (p–p)
	Input clock cycle-to-cycle jitter (Frequency ≤ 100 MHz)	—	—	±750	ps (p–p)

Table 1–53. High-Speed I/O Specifications for Arria II GX Devices (Part 4 of 4)

Symbol	Conditions	I3		C4		C5,I5		C6		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
f_{HSDR} (data rate)	SERDES factor J = 3 to 10	*(3)*	945 *(7)*	*(3)*	945 *(7)*	*(3)*	740 *(7)*	*(3)*	640 *(7)*	Mbps
	SERDES factor J = 2 (using DDR registers)	*(3)*	*(7)*	*(3)*	*(7)*	*(3)*	*(7)*	*(3)*	*(7)*	Mbps
	SERDES factor J = 1 (using SDR registers)	*(3)*	*(7)*	*(3)*	*(7)*	*(3)*	*(7)*	*(3)*	*(7)*	Mbps
Soft-CDR PPM tolerance	Soft-CDR mode	—	300	—	300	—	300	—	300	±PPM
DPA run length	DPA mode	—	10,000	—	10,000	—	10,000	—	10,000	UI
Sampling window (SW)	Non-DPA mode *(5)*	—	300	—	300	—	350	—	400	ps

Notes to Table 1–53:

(1) $f_{HSCLK\_IN} = f_{HSDR} / W$. Use W to determine the supported selection of input reference clock frequencies for the desired data rate.

(2) Applicable for interfacing with DPA receivers only. For interfacing with non-DPA receivers, you must calculate the leftover timing margin in the receiver by performing link timing closure analysis. For Arria II GX transmitter to Arria II GX non-DPA receiver, the maximum supported data rate is 945 Mbps. For data rates above 840 Mbps, perform PCB trace compensation by adjusting the PCB trace length for LVDS channels to improve channel-to-channel skews.

(3) The minimum and maximum specification depends on the clock source (for example, PLL and clock pin) and the clock routing resource you use (global, regional, or local). The I/O differential buffer and input register do not have a minimum toggle rate.

(4) The specification is only applicable under the influence of core noise.

(5) Applicable for true LVDS using dedicated SERDES only.

(6) Dedicated SERDES and DPA features are only available on the right banks.

(7) You must calculate the leftover timing margin in the receiver by performing link timing closure analysis. You must consider the board skew margin, transmitter channel-to-channel skew, and the receiver sampling margin to determine the leftover timing margin.

Table 1–54 lists the high-speed I/O timing for Arria II GZ devices.

Table 1–54. High-Speed I/O Specifications for Arria II GZ Devices *(Note 1), (2), (10)* (Part 1 of 3)

Symbol	Conditions	C3, I3			C4, I4			Unit
		Min	Typ	Max	Min	Typ	Max	
Clock								
f_{HSCLK_in} (input clock frequency) true differential I/O standards	Clock boost factor W = 1 to 40 *(3)*	5	—	717	5	—	717	MHz
f_{HSCLK_in} (input clock frequency) single ended I/O standards *(9)*	Clock boost factor W = 1 to 40 *(3)*	5	—	717	5	—	717	MHz
f_{HSCLK_in} (input clock frequency) single ended I/O standards *(10)*	Clock boost factor W = 1 to 40 *(3)*	5	—	420	5	—	420	MHz

Table 1–57. External Memory Interface Specifications for Arria II GX Devices (Part 2 of 2)

Frequency Mode	Frequency Range (MHz)			Resolution (°)	DQS Delay Buffer Mode *(1)*	Number of Delay Chains
	C4	I3, C5, I5	C6			
5	270-410	270-380	270-320	36	High	10
6	320-450	320-410	320-370	45	High	8

Note to Table 1–57:

(1) Low indicates a 6-bit DQS delay setting; high indicates a 5-bit DQS delay setting.

Table 1–58 lists the DLL frequency range specifications for Arria II GZ devices.

Table 1–58. DLL Frequency Range Specifications for Arria II GZ Devices

Frequency Mode	Frequency Range (MHz)		Available Phase Shift	DQS Delay Buffer Mode *(1)*	Number of Delay Chains
	–3	–4			
0	90-130	90-120	22.5°, 45°, 67.5°, 90°	Low	16
1	120-170	120-160	30°, 60°, 90°, 120°	Low	12
2	150-210	150-200	36°, 72°, 108°, 144°	Low	10
3	180-260	180-240	45°, 90°,135°, 180°	Low	8
4	240-320	240-290	30°, 60°, 90°, 120°	High	12
5	290-380	290-360	36°, 72°, 108°, 144°	High	10
6	360-450	360-450	45°, 90°, 135°, 180°	High	8
7	470-630	470-590	60°, 120°, 180°, 240°	High	6

Note to Table 1–58:

(1) Low indicates a 6-bit DQS delay setting; high indicates a 5-bit DQS delay setting.

Table 1–59 lists the DQS phase offset delay per stage for Arria II GX devices.

Table 1–59. DQS Phase Offset Delay Per Setting for Arria II GX Devices *(Note 1)*, *(2)*, *(3)*

Speed Grade	Min	Max	Unit
C4	7.0	13.0	ps
I3, C5, I5	7.0	15.0	ps
C6	8.5	18.0	ps

Notes to Table 1–59:

(1) The valid settings for phase offset are -64 to +63 for frequency modes 0 to 3 and -32 to +31 for frequency modes 4 to 5.

(2) The typical value equals the average of the minimum and maximum values.

(3) The delay settings are linear.

Table 1–63 lists the memory output clock jitter specifications for Arria II GZ devices.

Table 1–63. Memory Output Clock Jitter Specification for Arria II GZ Devices *(Note 1)*, *(2)*, *(3)*

Parameter	Clock Network	Symbol	–3		–4		Unit
			Min	Max	Min	Max	
Clock period jitter	Regional	$t_{JIT(per)}$	-55	55	-55	55	ps
Cycle-to-cycle period jitter	Regional	$t_{JIT(cc)}$	-110	110	-110	110	ps
Duty cycle jitter	Regional	$t_{JIT(duty)}$	-82.5	82.5	-82.5	82.5	ps
Clock period jitter	Global	$t_{JIT(per)}$	-82.5	82.5	-82.5	82.5	ps
Cycle-to-cycle period jitter	Global	$t_{JIT(cc)}$	-165	165	-165	165	ps
Duty cycle jitter	Global	$t_{JIT(duty)}$	-90	90	-90	90	ps

Notes to Table 1–63:

(1) The memory output clock jitter measurements are for 200 consecutive clock cycles, as specified in the JEDEC DDR2/DDR3 SDRAM standard.

(2) The clock jitter specification applies to memory output clock pins generated using differential signal-splitter and DDIO circuits clocked by a PLL output routed on a regional or global clock network as specified. Altera recommends using regional clock networks whenever possible.

(3) The memory output clock jitter stated in Table 1–63 is applicable when an input jitter of 30 ps is applied.

Duty Cycle Distortion (DCD) Specifications

Table 1–64 lists the worst-case DCD specifications for Arria II GX devices.

Table 1–64. Duty Cycle Distortion on I/O Pins for Arria II GX Devices *(Note 1)*

Symbol	C4		I3, C5, I5		C6		Unit
	Min	Max	Min	Max	Min	Max	
Output Duty Cycle	45	55	45	55	45	55	%

Note to Table 1–64:

(1) The DCD specification applies to clock outputs from the PLL, global clock tree, IOE driving dedicated, and general purpose I/O pins.

Table 1–65 lists the worst-case DCD specifications for Arria II GZ devices.

Table 1–65. Duty Cycle Distortion on I/O Pins for Arria II GZ Devices *(Note 1)*

Symbol	C3, I3		C4, I4		Unit
	Min	Max	Min	Max	
Output Duty Cycle	45	55	45	55	%

Note to Table 1–65:

(1) The DCD specification applies to clock outputs from the PLL, global clock tree, IOE driving dedicated, and general purpose I/O pins.

Table 1–68. Glossary (Part 4 of 4)

Letter	Subject	Definitions
U, V	$V_{CM(DC)}$	DC common mode input voltage.
	V_{ICM}	Input common mode voltage: The common mode of the differential signal at the receiver.
	V_{ID}	Input differential voltage swing: The difference in voltage between the positive and complementary conductors of a differential transmission at the receiver.
	$V_{DIF(AC)}$	AC differential input voltage: Minimum AC input differential voltage required for switching.
	$V_{DIF(DC)}$	DC differential input voltage: Minimum DC input differential voltage required for switching.
	V_{IH}	Voltage input high: The minimum positive voltage applied to the input which is accepted by the device as a logic high.
	$V_{IH(AC)}$	High-level AC input voltage.
	$V_{IH(DC)}$	High-level DC input voltage.
	V_{IL}	Voltage input low: The maximum positive voltage applied to the input which is accepted by the device as a logic low.
	$V_{IL(AC)}$	Low-level AC input voltage.
	$V_{IL(DC)}$	Low-level DC input voltage.
	V_{OCM}	Output common mode voltage: The common mode of the differential signal at the transmitter.
	V_{OD}	Output differential voltage swing: The difference in voltage between the positive and complementary conductors of a differential transmission at the transmitter.
W, X, Y, Z	W	High-speed I/O block: The clock boost factor.

Document Revision History

Table 1–69 lists the revision history for this chapter.

Table 1–69. Document Revision History (Part 1 of 2)

Date	Version	Changes
December 2013	4.4	Updated Table 1–34 and Table 1–35.
July 2012	4.3	■ Updated the $V_{CCH\_GXBL/R}$ operating conditions in Table 1–6. ■ Finalized Arria II GZ information in Table 1–20. ■ Added BLVDS specification in Table 1–32 and Table 1–33. ■ Updated input and output waveforms in Table 1–68.
December 2011	4.2	■ Updated Table 1–32, Table 1–33, Table 1–34, Table 1–35, Table 1–40, Table 1–41, Table 1–54, and Table 1–67. ■ Minor text edits.
June 2011	4.1	■ Added Table 1–60. ■ Updated Table 1–32, Table 1–33, Table 1–38, Table 1–41, and Table 1–61. ■ Updated the “Switching Characteristics” section introduction. ■ Minor text edits.