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### Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

|                                |                                                                                                                                       |
|--------------------------------|---------------------------------------------------------------------------------------------------------------------------------------|
| Product Status                 | Obsolete                                                                                                                              |
| Number of LABs/CLBs            | 11920                                                                                                                                 |
| Number of Logic Elements/Cells | 298000                                                                                                                                |
| Total RAM Bits                 | 18854912                                                                                                                              |
| Number of I/O                  | 281                                                                                                                                   |
| Number of Gates                | -                                                                                                                                     |
| Voltage - Supply               | 0.87V ~ 0.93V                                                                                                                         |
| Mounting Type                  | Surface Mount                                                                                                                         |
| Operating Temperature          | -40°C ~ 100°C (TJ)                                                                                                                    |
| Package / Case                 | 780-BBGA, FCBGA                                                                                                                       |
| Supplier Device Package        | 780-HBGA (33x33)                                                                                                                      |
| Purchase URL                   | <a href="https://www.e-xfl.com/product-detail/intel/ep2agz300fh29i4n">https://www.e-xfl.com/product-detail/intel/ep2agz300fh29i4n</a> |



Conditions beyond those listed in [Table 1-1](#) and [Table 1-2](#) may cause permanent damage to the device. Additionally, device operation at the absolute maximum ratings for extended periods of time may have adverse effects on the device.

[Table 1-1](#) lists the absolute maximum ratings for Arria II GX devices.

**Table 1-1. Absolute Maximum Ratings for Arria II GX Devices**

| Symbol         | Description                                                                                                     | Minimum | Maximum | Unit |
|----------------|-----------------------------------------------------------------------------------------------------------------|---------|---------|------|
| $V_{CC}$       | Supplies power to the core, periphery, I/O registers, PCI Express® (PIPE) (PCIe) HIP block, and transceiver PCS | -0.5    | 1.35    | V    |
| $V_{CCCB}$     | Supplies power for the configuration RAM bits                                                                   | -0.5    | 1.8     | V    |
| $V_{CCBAT}$    | Battery back-up power supply for design security volatile key register                                          | -0.5    | 3.75    | V    |
| $V_{CCPD}$     | Supplies power to the I/O pre-drivers, differential input buffers, and MSEL circuitry                           | -0.5    | 3.75    | V    |
| $V_{CCIO}$     | Supplies power to the I/O banks                                                                                 | -0.5    | 3.9     | V    |
| $V_{CCD\_PLL}$ | Supplies power to the digital portions of the PLL                                                               | -0.5    | 1.35    | V    |
| $V_{CCA\_PLL}$ | Supplies power to the analog portions of the PLL and device-wide power management circuitry                     | -0.5    | 3.75    | V    |
| $V_I$          | DC input voltage                                                                                                | -0.5    | 4.0     | V    |
| $I_{OUT}$      | DC output current, per pin                                                                                      | -25     | 40      | mA   |
| $V_{CCA}$      | Supplies power to the transceiver PMA regulator                                                                 | —       | 3.75    | V    |
| $V_{CCL\_GXB}$ | Supplies power to the transceiver PMA TX, PMA RX, and clocking                                                  | —       | 1.21    | V    |
| $V_{CCH\_GXB}$ | Supplies power to the transceiver PMA output (TX) buffer                                                        | —       | 1.8     | V    |
| $T_J$          | Operating junction temperature                                                                                  | -55     | 125     | °C   |
| $T_{STG}$      | Storage temperature (no bias)                                                                                   | -65     | 150     | °C   |

[Table 1-2](#) lists the absolute maximum ratings for Arria II GZ devices.

**Table 1-2. Absolute Maximum Ratings for Arria II GZ Devices (Part 1 of 2)**

| Symbol          | Description                                                                                 | Minimum | Maximum | Unit |
|-----------------|---------------------------------------------------------------------------------------------|---------|---------|------|
| $V_{CC}$        | Supplies power to the core, periphery, I/O registers, PCIe HIP block, and transceiver PCS   | -0.5    | 1.35    | V    |
| $V_{CCCB}$      | Power supply to the configuration RAM bits                                                  | -0.5    | 1.8     | V    |
| $V_{CCPGM}$     | Supplies power to the configuration pins                                                    | -0.5    | 3.75    | V    |
| $V_{CCAUX}$     | Auxiliary supply                                                                            | -0.5    | 3.75    | V    |
| $V_{CCBAT}$     | Supplies battery back-up power for design security volatile key register                    | -0.5    | 3.75    | V    |
| $V_{CCPD}$      | Supplies power to the I/O pre-drivers, differential input buffers, and MSEL circuitry       | -0.5    | 3.75    | V    |
| $V_{CCIO}$      | Supplies power to the I/O banks                                                             | -0.5    | 3.9     | V    |
| $V_{CC\_CLKIN}$ | Supplies power to the differential clock input                                              | -0.5    | 3.75    | V    |
| $V_{CCD\_PLL}$  | Supplies power to the digital portions of the PLL                                           | -0.5    | 1.35    | V    |
| $V_{CCA\_PLL}$  | Supplies power to the analog portions of the PLL and device-wide power management circuitry | -0.5    | 3.75    | V    |
| $V_I$           | DC input voltage                                                                            | -0.5    | 4.0     | V    |
| $I_{OUT}$       | DC output current, per pin                                                                  | -25     | 40      | mA   |

## Recommended Operating Conditions

This section lists the functional operation limits for AC and DC parameters for Arria II GX and GZ devices. All supplies are required to monotonically reach their full-rail values without plateaus within  $t_{RAMP}$ .

Table 1–5 lists the recommended operating conditions for Arria II GX devices.

**Table 1–5. Recommended Operating Conditions for Arria II GX Devices (Note 1) (Part 1 of 2)**

| Symbol             | Description                                                                                 | Condition  | Minimum | Typical | Maximum    | Unit |
|--------------------|---------------------------------------------------------------------------------------------|------------|---------|---------|------------|------|
| $V_{CC}$           | Supplies power to the core, periphery, I/O registers, PCIe HIP block, and transceiver PCS   | —          | 0.87    | 0.90    | 0.93       | V    |
| $V_{CCCB}$         | Supplies power to the configuration RAM bits                                                | —          | 1.425   | 1.50    | 1.575      | V    |
| $V_{CCBAT}$<br>(2) | Battery back-up power supply for design security volatile key registers                     | —          | 1.2     | —       | 3.3        | V    |
| $V_{CCPD}$<br>(3)  | Supplies power to the I/O pre-drivers, differential input buffers, and MSEL circuitry       | —          | 3.135   | 3.3     | 3.465      | V    |
|                    |                                                                                             | —          | 2.85    | 3.0     | 3.15       | V    |
|                    |                                                                                             | —          | 2.375   | 2.5     | 2.625      | V    |
| $V_{CCIO}$         | Supplies power to the I/O banks (4)                                                         | —          | 3.135   | 3.3     | 3.465      | V    |
|                    |                                                                                             | —          | 2.85    | 3.0     | 3.15       | V    |
|                    |                                                                                             | —          | 2.375   | 2.5     | 2.625      | V    |
|                    |                                                                                             | —          | 1.71    | 1.8     | 1.89       | V    |
|                    |                                                                                             | —          | 1.425   | 1.5     | 1.575      | V    |
|                    |                                                                                             | —          | 1.14    | 1.2     | 1.26       | V    |
| $V_{CCD\_PLL}$     | Supplies power to the digital portions of the PLL                                           | —          | 0.87    | 0.90    | 0.93       | V    |
| $V_{CCA\_PLL}$     | Supplies power to the analog portions of the PLL and device-wide power management circuitry | —          | 2.375   | 2.5     | 2.625      | V    |
| $V_I$              | DC Input voltage                                                                            | —          | –0.5    | —       | 3.6        | V    |
| $V_O$              | Output voltage                                                                              | —          | 0       | —       | $V_{CCIO}$ | V    |
| $V_{CCA}$          | Supplies power to the transceiver PMA regulator                                             | —          | 2.375   | 2.5     | 2.625      | V    |
| $V_{CCL\_GXB}$     | Supplies power to the transceiver PMA TX, PMA RX, and clocking                              | —          | 1.045   | 1.1     | 1.155      | V    |
| $V_{CCH\_GXB}$     | Supplies power to the transceiver PMA output (TX) buffer                                    | —          | 1.425   | 1.5     | 1.575      | V    |
| $T_J$              | Operating junction temperature                                                              | Commercial | 0       | —       | 85         | °C   |
|                    |                                                                                             | Industrial | –40     | —       | 100        | °C   |

Table 1-17 lists the pin capacitance for Arria II GZ devices.

**Table 1-17. Pin Capacitance for Arria II GZ Devices**

| Symbol                                                    | Description                                                            | Typical | Unit |
|-----------------------------------------------------------|------------------------------------------------------------------------|---------|------|
| $C_{IOTB}$                                                | Input capacitance on the top and bottom I/O pins                       | 4       | pF   |
| $C_{IOLR}$                                                | Input capacitance on the left and right I/O pins                       | 4       | pF   |
| $C_{CLKTB}$                                               | Input capacitance on the top and bottom non-dedicated clock input pins | 4       | pF   |
| $C_{CLKLR}$                                               | Input capacitance on the left and right non-dedicated clock input pins | 4       | pF   |
| $C_{OUTFB}$                                               | Input capacitance on the dual-purpose clock output and feedback pins   | 5       | pF   |
| $C_{CLK1}$ , $C_{CLK3}$ , $C_{CLK8}$ ,<br>and $C_{CLK10}$ | Input capacitance for dedicated clock input pins                       | 2       | pF   |

### Internal Weak Pull-Up and Weak Pull-Down Resistors

Table 1-18 lists the weak pull-up and pull-down resistor values for Arria II GX devices.

**Table 1-18. Internal Weak Pull-up and Weak Pull-Down Resistors for Arria II GX Devices (Note 1)**

| Symbol   | Description                                                                                                                                     | Conditions                             | Min | Typ | Max | Unit       |
|----------|-------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------|-----|-----|-----|------------|
| $R_{PU}$ | Value of I/O pin pull-up resistor before and during configuration, as well as user mode if the programmable pull-up resistor option is enabled. | $V_{CCIO} = 3.3 \text{ V} \pm 5\%$ (2) | 7   | 25  | 41  | k $\Omega$ |
|          |                                                                                                                                                 | $V_{CCIO} = 3.0 \text{ V} \pm 5\%$ (2) | 7   | 28  | 47  | k $\Omega$ |
|          |                                                                                                                                                 | $V_{CCIO} = 2.5 \text{ V} \pm 5\%$ (2) | 8   | 35  | 61  | k $\Omega$ |
|          |                                                                                                                                                 | $V_{CCIO} = 1.8 \text{ V} \pm 5\%$ (2) | 10  | 57  | 108 | k $\Omega$ |
|          |                                                                                                                                                 | $V_{CCIO} = 1.5 \text{ V} \pm 5\%$ (2) | 13  | 82  | 163 | k $\Omega$ |
|          |                                                                                                                                                 | $V_{CCIO} = 1.2 \text{ V} \pm 5\%$ (2) | 19  | 143 | 351 | k $\Omega$ |
| $R_{PD}$ | Value of TCK pin pull-down resistor                                                                                                             | $V_{CCIO} = 3.3 \text{ V} \pm 5\%$     | 6   | 19  | 29  | k $\Omega$ |
|          |                                                                                                                                                 | $V_{CCIO} = 3.0 \text{ V} \pm 5\%$     | 6   | 22  | 32  | k $\Omega$ |
|          |                                                                                                                                                 | $V_{CCIO} = 2.5 \text{ V} \pm 5\%$     | 6   | 25  | 42  | k $\Omega$ |
|          |                                                                                                                                                 | $V_{CCIO} = 1.8 \text{ V} \pm 5\%$     | 7   | 35  | 70  | k $\Omega$ |
|          |                                                                                                                                                 | $V_{CCIO} = 1.5 \text{ V} \pm 5\%$     | 8   | 50  | 112 | k $\Omega$ |

#### Notes to Table 1-18:

- (1) All I/O pins have an option to enable weak pull-up except configuration, test, and JTAG pins. The weak pull-down feature is only available for JTAG TCK.
- (2) Pin pull-up resistance values may be lower if an external source drives the pin higher than  $V_{CCIO}$ .

**Table 1–23. Single-Ended I/O Standards for Arria II GZ Devices (Part 2 of 2)**

| I/O Standard | $V_{CCIO}$ (V) |     |      | $V_{IL}$ (V) |                        | $V_{IH}$ (V)           |                  | $V_{OL}$ (V)           | $V_{OH}$ (V)           | $I_{OL}$ (mA) | $I_{OH}$ (mA) |
|--------------|----------------|-----|------|--------------|------------------------|------------------------|------------------|------------------------|------------------------|---------------|---------------|
|              | Min            | Typ | Max  | Min          | Max                    | Min                    | Max              | Max                    | Min                    |               |               |
| 1.2 V        | 1.14           | 1.2 | 1.26 | -0.3         | $0.35 \times V_{CCIO}$ | $0.65 \times V_{CCIO}$ | $V_{CCIO} + 0.3$ | $0.25 \times V_{CCIO}$ | $0.75 \times V_{CCIO}$ | 2             | -2            |
| 3.0-V PCI    | 2.85           | 3   | 3.15 | —            | $0.3 \times V_{CCIO}$  | $0.5 \times V_{CCIO}$  | 3.6              | $0.1 \times V_{CCIO}$  | $0.9 \times V_{CCIO}$  | 1.5           | -0.5          |
| 3.0-V PCI-X  | 2.85           | 3   | 3.15 | —            | $0.35 \times V_{CCIO}$ | $0.5 \times V_{CCIO}$  | —                | $0.1 \times V_{CCIO}$  | $0.9 \times V_{CCIO}$  | 1.5           | -0.5          |

Table 1–24 lists the single-ended SSTL and HSTL I/O reference voltage specifications for Arria II GX devices.

**Table 1–24. Single-Ended SSTL and HSTL I/O Reference Voltage Specifications for Arria II GX Devices**

| I/O Standard        | $V_{CCIO}$ (V) |     |       | $V_{REF}$ (V)          |                       |                        | $V_{TT}$ (V)           |                       |                        |
|---------------------|----------------|-----|-------|------------------------|-----------------------|------------------------|------------------------|-----------------------|------------------------|
|                     | Min            | Typ | Max   | Min                    | Typ                   | Max                    | Min                    | Typ                   | Max                    |
| SSTL-2 Class I, II  | 2.375          | 2.5 | 2.625 | $0.49 \times V_{CCIO}$ | $0.5 \times V_{CCIO}$ | $0.51 \times V_{CCIO}$ | $V_{REF} - 0.04$       | $V_{REF}$             | $V_{REF} + 0.04$       |
| SSTL-18 Class I, II | 1.71           | 1.8 | 1.89  | 0.833                  | 0.9                   | 0.969                  | $V_{REF} - 0.04$       | $V_{REF}$             | $V_{REF} + 0.04$       |
| SSTL-15 Class I, II | 1.425          | 1.5 | 1.575 | $0.47 \times V_{CCIO}$ | $0.5 \times V_{CCIO}$ | $0.53 \times V_{CCIO}$ | $0.47 \times V_{CCIO}$ | $0.5 \times V_{CCIO}$ | $0.53 \times V_{CCIO}$ |
| HSTL-18 Class I, II | 1.71           | 1.8 | 1.89  | 0.85                   | 0.9                   | 0.95                   | 0.85                   | 0.9                   | 0.95                   |
| HSTL-15 Class I, II | 1.425          | 1.5 | 1.575 | 0.71                   | 0.75                  | 0.79                   | 0.71                   | 0.75                  | 0.79                   |
| HSTL-12 Class I, II | 1.14           | 1.2 | 1.26  | $0.48 \times V_{CCIO}$ | $0.5 \times V_{CCIO}$ | $0.52 \times V_{CCIO}$ | —                      | $V_{CCIO}/2$          | —                      |

Table 1–25 lists the single-ended SSTL and HSTL I/O reference voltage specifications for Arria II GZ devices.

**Table 1–25. Single-Ended SSTL and HSTL I/O Reference Voltage Specifications for Arria II GZ Devices**

| I/O Standard        | $V_{CCIO}$ (V) |     |       | $V_{REF}$ (V)          |                       |                        | $V_{TT}$ (V)           |              |                        |
|---------------------|----------------|-----|-------|------------------------|-----------------------|------------------------|------------------------|--------------|------------------------|
|                     | Min            | Typ | Max   | Min                    | Typ                   | Max                    | Min                    | Typ          | Max                    |
| SSTL-2 Class I, II  | 2.375          | 2.5 | 2.625 | $0.49 \times V_{CCIO}$ | $0.5 \times V_{CCIO}$ | $0.51 \times V_{CCIO}$ | $V_{REF} - 0.04$       | $V_{REF}$    | $V_{REF} + 0.04$       |
| SSTL-18 Class I, II | 1.71           | 1.8 | 1.89  | 0.833                  | 0.9                   | 0.969                  | $V_{REF} - 0.04$       | $V_{REF}$    | $V_{REF} + 0.04$       |
| SSTL-15 Class I, II | 1.425          | 1.5 | 1.575 | $0.47 \times V_{CCIO}$ | $0.5 \times V_{CCIO}$ | $0.53 \times V_{CCIO}$ | $0.47 \times V_{CCIO}$ | $V_{REF}$    | $0.53 \times V_{CCIO}$ |
| HSTL-18 Class I, II | 1.71           | 1.8 | 1.89  | 0.85                   | 0.9                   | 0.95                   | —                      | $V_{CCIO}/2$ | —                      |
| HSTL-15 Class I, II | 1.425          | 1.5 | 1.575 | 0.68                   | 0.75                  | 0.9                    | —                      | $V_{CCIO}/2$ | —                      |
| HSTL-12 Class I, II | 1.14           | 1.2 | 1.26  | $0.47 \times V_{CCIO}$ | $0.5 \times V_{CCIO}$ | $0.53 \times V_{CCIO}$ | —                      | $V_{CCIO}/2$ | —                      |

**Table 1-27. Single-Ended SSTL and HSTL I/O Standards Signal Specifications for Arria II GZ Devices (Part 2 of 2)**

| I/O Standard     | $V_{IL(DC)} (V)$ |                  | $V_{IH(DC)} (V)$ |                   | $V_{IL(AC)} (V)$  | $V_{IH(AC)} (V)$  | $V_{OL} (V)$           | $V_{OH} (V)$           | $I_{OL} (mA)$ | $I_{OH} (mA)$ |
|------------------|------------------|------------------|------------------|-------------------|-------------------|-------------------|------------------------|------------------------|---------------|---------------|
|                  | Min              | Max              | Min              | Max               | Max               | Min               | Max                    | Min                    |               |               |
| SSTL-15 Class II | —                | $V_{REF} - 0.1$  | $V_{REF} + 0.1$  | —                 | $V_{REF} - 0.175$ | $V_{REF} + 0.175$ | $0.2 \times V_{CCIO}$  | $0.8 \times V_{CCIO}$  | 16            | -16           |
| HSTL-18 Class I  | —                | $V_{REF} - 0.1$  | $V_{REF} + 0.1$  | —                 | $V_{REF} - 0.2$   | $V_{REF} + 0.2$   | 0.4                    | $V_{CCIO} - 0.4$       | 8             | -8            |
| HSTL-18 Class II | —                | $V_{REF} - 0.1$  | $V_{REF} + 0.1$  | —                 | $V_{REF} - 0.2$   | $V_{REF} + 0.2$   | 0.4                    | $V_{CCIO} - 0.4$       | 16            | -16           |
| HSTL-15 Class I  | —                | $V_{REF} - 0.1$  | $V_{REF} + 0.1$  | —                 | $V_{REF} - 0.2$   | $V_{REF} + 0.2$   | 0.4                    | $V_{CCIO} - 0.4$       | 8             | -8            |
| HSTL-15 Class II | —                | $V_{REF} - 0.1$  | $V_{REF} + 0.1$  | —                 | $V_{REF} - 0.2$   | $V_{REF} + 0.2$   | 0.4                    | $V_{CCIO} - 0.4$       | 16            | -16           |
| HSTL-12 Class I  | -0.15            | $V_{REF} - 0.08$ | $V_{REF} + 0.08$ | $V_{CCIO} + 0.15$ | $V_{REF} - 0.15$  | $V_{REF} + 0.15$  | $0.25 \times V_{CCIO}$ | $0.75 \times V_{CCIO}$ | 8             | -8            |
| HSTL-12 Class II | -0.15            | $V_{REF} - 0.08$ | $V_{REF} + 0.08$ | $V_{CCIO} + 0.15$ | $V_{REF} - 0.15$  | $V_{REF} + 0.15$  | $0.25 \times V_{CCIO}$ | $0.75 \times V_{CCIO}$ | 16            | -16           |

Table 1-28 lists the differential SSTL I/O standards for Arria II GX devices.

**Table 1-28. Differential SSTL I/O Standards for Arria II GX Devices**

| I/O Standard        | $V_{CCIO} (V)$ |     |       | $V_{SWING(DC)} (V)$ |            | $V_{X(AC)} (V)$      |              |                      | $V_{SWING(AC)} (V)$ |            | $V_{OX(AC)} (V)$     |              |                      |
|---------------------|----------------|-----|-------|---------------------|------------|----------------------|--------------|----------------------|---------------------|------------|----------------------|--------------|----------------------|
|                     | Min            | Typ | Max   | Min                 | Max        | Min                  | Typ          | Max                  | Min                 | Max        | Min                  | Typ          | Max                  |
| SSTL-2 Class I, II  | 2.375          | 2.5 | 2.625 | 0.36                | $V_{CCIO}$ | $V_{CCIO}/2 - 0.2$   | —            | $V_{CCIO}/2 + 0.2$   | 0.7                 | $V_{CCIO}$ | $V_{CCIO}/2 - 0.15$  | —            | $V_{CCIO}/2 + 0.15$  |
| SSTL-18 Class I, II | 1.71           | 1.8 | 1.89  | 0.25                | $V_{CCIO}$ | $V_{CCIO}/2 - 0.175$ | —            | $V_{CCIO}/2 + 0.175$ | 0.5                 | $V_{CCIO}$ | $V_{CCIO}/2 - 0.125$ | —            | $V_{CCIO}/2 + 0.125$ |
| SSTL-15 Class I, II | 1.425          | 1.5 | 1.575 | 0.2                 | —          | —                    | $V_{CCIO}/2$ | —                    | 0.35                | —          | —                    | $V_{CCIO}/2$ | —                    |

Table 1-29 lists the differential SSTL I/O standards for Arria II GZ devices

**Table 1-29. Differential SSTL I/O Standards for Arria II GZ Devices**

| I/O Standard        | $V_{CCIO} (V)$ |     |       | $V_{SWING(DC)} (V)$ |                  | $V_{X(AC)} (V)$      |              |                      | $V_{SWING(AC)} (V)$ |                  | $V_{OX(AC)} (V)$     |              |                      |
|---------------------|----------------|-----|-------|---------------------|------------------|----------------------|--------------|----------------------|---------------------|------------------|----------------------|--------------|----------------------|
|                     | Min            | Typ | Max   | Min                 | Max              | Min                  | Typ          | Max                  | Min                 | Max              | Min                  | Typ          | Max                  |
| SSTL-2 Class I, II  | 2.375          | 2.5 | 2.625 | 0.3                 | $V_{CCIO} + 0.6$ | $V_{CCIO}/2 - 0.2$   | —            | $V_{CCIO}/2 + 0.2$   | 0.62                | $V_{CCIO} + 0.6$ | $V_{CCIO}/2 - 0.15$  | —            | $V_{CCIO}/2 + 0.15$  |
| SSTL-18 Class I, II | 1.71           | 1.8 | 1.89  | 0.25                | $V_{CCIO} + 0.6$ | $V_{CCIO}/2 - 0.175$ | —            | $V_{CCIO}/2 + 0.175$ | 0.5                 | $V_{CCIO} + 0.6$ | $V_{CCIO}/2 - 0.125$ | —            | $V_{CCIO}/2 + 0.125$ |
| SSTL-15 Class I, II | 1.425          | 1.5 | 1.575 | 0.2                 | —                | —                    | $V_{CCIO}/2$ | —                    | 0.35                | —                | —                    | $V_{CCIO}/2$ | —                    |

Table 1-30 lists the HSTL I/O standards for Arria II GX devices.

**Table 1-30. Differential HSTL I/O Standards for Arria II GX Devices**

| I/O Standard        | $V_{CCIO}$ (V) |     |       | $V_{DIF(DC)}$ (V) |     | $V_{X(AC)}$ (V) |                       |      | $V_{CM(DC)}$ (V)       |                       |                        | $V_{DIF(AC)}$ (V) |     |
|---------------------|----------------|-----|-------|-------------------|-----|-----------------|-----------------------|------|------------------------|-----------------------|------------------------|-------------------|-----|
|                     | Min            | Typ | Max   | Min               | Max | Min             | Typ                   | Max  | Min                    | Typ                   | Max                    | Min               | Max |
| HSTL-18 Class I     | 1.71           | 1.8 | 1.89  | 0.2               | —   | 0.85            | —                     | 0.95 | 0.88                   | —                     | 0.95                   | 0.4               | —   |
| HSTL-15 Class I, II | 1.425          | 1.5 | 1.575 | 0.2               | —   | 0.71            | —                     | 0.79 | 0.71                   | —                     | 0.79                   | 0.4               | —   |
| HSTL-12 Class I, II | 1.14           | 1.2 | 1.26  | 0.16              | —   | —               | $0.5 \times V_{CCIO}$ | —    | $0.48 \times V_{CCIO}$ | $0.5 \times V_{CCIO}$ | $0.52 \times V_{CCIO}$ | 0.3               | —   |

Table 1-31 lists the HSTL I/O standards for Arria II GZ devices.

**Table 1-31. Differential HSTL I/O Standards for Arria II GZ Devices**

| I/O Standard        | $V_{CCIO}$ (V) |     |       | $V_{DIF(DC)}$ (V) |                  | $V_{X(AC)}$ (V) |                       |      | $V_{CM(DC)}$ (V)      |                       |                       | $V_{DIF(AC)}$ (V) |                   |
|---------------------|----------------|-----|-------|-------------------|------------------|-----------------|-----------------------|------|-----------------------|-----------------------|-----------------------|-------------------|-------------------|
|                     | Min            | Typ | Max   | Min               | Max              | Min             | Typ                   | Max  | Min                   | Typ                   | Max                   | Min               | Max               |
| HSTL-18 Class I     | 1.71           | 1.8 | 1.89  | 0.2               | —                | 0.78            | —                     | 1.12 | 0.78                  | —                     | 1.12                  | 0.4               | —                 |
| HSTL-15 Class I, II | 1.425          | 1.5 | 1.575 | 0.2               | —                | 0.68            | —                     | 0.9  | 0.68                  | —                     | 0.9                   | 0.4               | —                 |
| HSTL-12 Class I, II | 1.14           | 1.2 | 1.26  | 0.16              | $V_{CCIO} + 0.3$ | —               | $0.5 \times V_{CCIO}$ | —    | $0.4 \times V_{CCIO}$ | $0.5 \times V_{CCIO}$ | $0.6 \times V_{CCIO}$ | 0.3               | $V_{CCIO} + 0.48$ |

Table 1-32 lists the differential I/O standard specifications for Arria II GX devices.

**Table 1-32. Differential I/O Standard Specifications for Arria II GX Devices (Note 1)**

| I/O Standard  | $V_{CCIO}$ (V) |     |       | $V_{ID}$ (mV) |                   |     | $V_{ICM}$ (V) (2) |      | $V_{OD}$ (V) (3) |     |     | $V_{OCM}$ (V) |      |       |
|---------------|----------------|-----|-------|---------------|-------------------|-----|-------------------|------|------------------|-----|-----|---------------|------|-------|
|               | Min            | Typ | Max   | Min           | Cond.             | Max | Min               | Max  | Min              | Typ | Max | Min           | Typ  | Max   |
| 2.5 V LVDS    | 2.375          | 2.5 | 2.625 | 100           | $V_{CM} = 1.25$ V | —   | 0.05              | 1.80 | 0.247            | —   | 0.6 | 1.125         | 1.25 | 1.375 |
| RSDS (4)      | 2.375          | 2.5 | 2.625 | —             | —                 | —   | —                 | —    | 0.1              | 0.2 | 0.6 | 0.5           | 1.2  | 1.4   |
| Mini-LVDS (4) | 2.375          | 2.5 | 2.625 | —             | —                 | —   | —                 | —    | 0.25             | —   | 0.6 | 1             | 1.2  | 1.4   |
| LVPECL (5)    | 2.375          | 2.5 | 2.625 | 300           | —                 | —   | 0.6               | 1.8  | —                | —   | —   | —             | —    | —     |
| BLVDS (6)     | 2.375          | 2.5 | 2.625 | 100           | —                 | —   | —                 | —    | —                | —   | —   | —             | —    | —     |

**Notes to Table 1-32:**

- (1) The 1.5 V PCML transceiver I/O standard specifications are described in “Transceiver Performance Specifications” on page 1-21.
- (2)  $V_{IN}$  range:  $0 \leq V_{IN} \leq 1.85$  V.
- (3)  $R_L$  range:  $90 \leq R_L \leq 110 \Omega$ .
- (4) The RSDS and mini-LVDS I/O standards are only supported for differential outputs.
- (5) The LVPECL input standard is supported at the dedicated clock input pins (GCLK) only.
- (6) There are no fixed  $V_{ICM}$ ,  $V_{OD}$ , and  $V_{OCM}$  specifications for BLVDS. These specifications depend on the system topology.

**Table 1–34. Transceiver Specifications for Arria II GX Devices (Note 1) (Part 2 of 7)**

| Symbol/<br>Description                                       | Condition                                  | I3        |            |      | C4        |            |      | C5 and I5 |            |      | C6        |            |      | Unit   |
|--------------------------------------------------------------|--------------------------------------------|-----------|------------|------|-----------|------------|------|-----------|------------|------|-----------|------------|------|--------|
|                                                              |                                            | Min       | Typ        | Max  | Min       | Typ        | Max  | Min       | Typ        | Max  | Min       | Typ        | Max  |        |
| Spread-spectrum downspread                                   | PCIe                                       | —         | 0 to –0.5% | —    | —         | 0 to –0.5% | —    | —         | 0 to –0.5% | —    | —         | 0 to –0.5% | —    | —      |
| On-chip termination resistors                                | —                                          | —         | 100        | —    | —         | 100        | —    | —         | 100        | —    | —         | 100        | —    | Ω      |
| V <sub>ICM</sub> (AC coupled)                                | —                                          | 1100 ± 5% |            |      | 1100 ± 5% |            |      | 1100 ± 5% |            |      | 1100 ± 5% |            |      | mV     |
| V <sub>ICM</sub> (DC coupled)                                | HCSL I/O standard for PCIe reference clock | 250       | —          | 550  | 250       | —          | 550  | 250       | —          | 550  | 250       | —          | 550  | mV     |
| Transmitter REFCLK Phase Noise                               | 10 Hz                                      | —         | —          | -50  | —         | —          | -50  | —         | —          | -50  | —         | —          | -50  | dBc/Hz |
|                                                              | 100 Hz                                     | —         | —          | -80  | —         | —          | -80  | —         | —          | -80  | —         | —          | -80  | dBc/Hz |
|                                                              | 1 KHz                                      | —         | —          | -110 | —         | —          | -110 | —         | —          | -110 | —         | —          | -110 | dBc/Hz |
|                                                              | 10 KHz                                     | —         | —          | -120 | —         | —          | -120 | —         | —          | -120 | —         | —          | -120 | dBc/Hz |
|                                                              | 100 KHz                                    | —         | —          | -120 | —         | —          | -120 | —         | —          | -120 | —         | —          | -120 | dBc/Hz |
|                                                              | ≥ 1 MHz                                    | —         | —          | -130 | —         | —          | -130 | —         | —          | -130 | —         | —          | -130 | dBc/Hz |
| Transmitter REFCLK Phase Jitter (rms) for 100 MHz REFCLK (3) | 10 KHz to 20 MHz                           | —         | —          | 3    | —         | —          | 3    | —         | —          | 3    | —         | —          | 3    | ps     |
| R <sub>ref</sub>                                             | —                                          | —         | 2000 ± 1%  | —    | —         | 2000 ± 1%  | —    | —         | 2000 ± 1%  | —    | —         | 2000 ± 1%  | —    | Ω      |
| <b>Transceiver Clocks</b>                                    |                                            |           |            |      |           |            |      |           |            |      |           |            |      |        |
| Calibration block clock frequency (cal_blk_clk)              | —                                          | 10        | —          | 125  | 10        | —          | 125  | 10        | —          | 125  | 10        | —          | 125  | MHz    |

Table 1–35 lists the transceiver specifications for Arria II GZ devices.

**Table 1–35. Transceiver Specifications for Arria II GZ Devices (Part 1 of 5)**

| Symbol/<br>Description                                       | Conditions                                                              | –C3 and –I3 (1) |            |      | –C4 and –I4 |            |       | Unit   |
|--------------------------------------------------------------|-------------------------------------------------------------------------|-----------------|------------|------|-------------|------------|-------|--------|
|                                                              |                                                                         | Min             | Typ        | Max  | Min         | Typ        | Max   |        |
| Reference Clock                                              |                                                                         |                 |            |      |             |            |       |        |
| Supported I/O Standards                                      | 1.2-V PCML, 1.5-V PCML, 2.5-V PCML, Differential LVPECL, LVDS, and HCSL |                 |            |      |             |            |       |        |
| Input frequency from REFCLK input pins                       | —                                                                       | 50              | —          | 697  | 50          | —          | 637.5 | MHz    |
| Phase frequency detector (CMU PLL and receiver CDR)          | —                                                                       | 50              | —          | 325  | 50          | —          | 325   | MHz    |
| Absolute V <sub>MAX</sub> for a REFCLK pin                   | —                                                                       | —               | —          | 1.6  | —           | —          | 1.6   | V      |
| Operational V <sub>MAX</sub> for a REFCLK pin                | —                                                                       | —               | —          | 1.5  | —           | —          | 1.5   | V      |
| Absolute V <sub>MIN</sub> for a REFCLK pin                   | —                                                                       | -0.4            | —          | —    | -0.4        | —          | —     | V      |
| Rise/fall time (2)                                           | —                                                                       | —               | —          | 0.2  | —           | —          | 0.2   | UI     |
| Duty cycle                                                   | —                                                                       | 45              | —          | 55   | 45          | —          | 55    | %      |
| Peak-to-peak differential input voltage                      | —                                                                       | 200             | —          | 1600 | 200         | —          | 1600  | mV     |
| Spread-spectrum modulating clock frequency                   | PCIe                                                                    | 30              | —          | 33   | 30          | —          | 33    | kHz    |
| Spread-spectrum downspread                                   | PCIe                                                                    | —               | 0 to -0.5% | —    | —           | 0 to -0.5% | —     | —      |
| On-chip termination resistors                                | —                                                                       | —               | 100        | —    | —           | 100        | —     | Ω      |
| V <sub>ICM</sub> (AC coupled)                                | —                                                                       | 1100 ± 10%      |            |      | 1100 ± 10%  |            |       | mV     |
| V <sub>ICM</sub> (DC coupled)                                | HCSL I/O standard for PCIe reference clock                              | 250             | —          | 550  | 250         | —          | 550   | mV     |
| Transmitter REFCLK Phase Noise                               | 10 Hz                                                                   | —               | —          | -50  | —           | —          | -50   | dBc/Hz |
|                                                              | 100 Hz                                                                  | —               | —          | -80  | —           | —          | -80   | dBc/Hz |
|                                                              | 1 KHz                                                                   | —               | —          | -110 | —           | —          | -110  | dBc/Hz |
|                                                              | 10 KHz                                                                  | —               | —          | -120 | —           | —          | -120  | dBc/Hz |
|                                                              | 100 KHz                                                                 | —               | —          | -120 | —           | —          | -120  | dBc/Hz |
|                                                              | ≥ 1 MHz                                                                 | —               | —          | -130 | —           | —          | -130  | dBc/Hz |
| Transmitter REFCLK Phase Jitter (rms) for 100 MHz REFCLK (3) | 10 KHz to 20 MHz                                                        | —               | —          | 3    | —           | —          | 3     | ps     |
| R <sub>REF</sub>                                             | —                                                                       | —               | 2000 ± 1%  | —    | —           | 2000 ± 1%  | —     | Ω      |

**Table 1–35. Transceiver Specifications for Arria II GZ Devices (Part 5 of 5)**

| Symbol/<br>Description            | Conditions                  | –C3 and –I3 (1)                      |     |     | –C4 and –I4 |     |     | Unit |
|-----------------------------------|-----------------------------|--------------------------------------|-----|-----|-------------|-----|-----|------|
|                                   |                             | Min                                  | Typ | Max | Min         | Typ | Max |      |
| -3 dB Bandwidth                   | PCIe Gen1                   | 2.5 - 3.5                            |     |     |             |     |     | MHz  |
|                                   | PCIe Gen2                   | 6 - 8                                |     |     |             |     |     | MHz  |
|                                   | (OIF) CEI PHY at 4.976 Gbps | 7 - 11                               |     |     |             |     |     | MHz  |
|                                   | (OIF) CEI PHY at 6.375 Gbps | 5 - 10                               |     |     |             |     |     | MHz  |
|                                   | XAUI                        | 2 - 4                                |     |     |             |     |     | MHz  |
|                                   | SRIO 1.25 Gbps              | 3 - 5.5                              |     |     |             |     |     | MHz  |
|                                   | SRIO 2.5 Gbps               | 3 - 5.5                              |     |     |             |     |     | MHz  |
|                                   | SRIO 3.125 Gbps             | 2 - 4                                |     |     |             |     |     | MHz  |
|                                   | GIGE                        | 2.5 - 4.5                            |     |     |             |     |     | MHz  |
|                                   | SONET OC12                  | 1.5 - 2.5                            |     |     |             |     |     | MHz  |
|                                   | SONET OC48                  | 3.5 - 6                              |     |     |             |     |     | MHz  |
| Transceiver-FPGA Fabric Interface |                             |                                      |     |     |             |     |     |      |
| Interface speed                   | —                           | 25                                   | —   | 325 | 25          | —   | 250 | MHz  |
| Digital reset pulse width         | —                           | Minimum is two parallel clock cycles |     |     |             |     |     | —    |

**Notes to Table 1–35:**

- (1) The 3x speed grade is the fastest speed grade offered in the following Arria II GZ devices: EP2AGZ225, EP2AGZ300, and EP2AGZ350.
- (2) The rise and fall time transition is specified from 20% to 80%.
- (3) To calculate the REFCLK rms phase jitter requirement at reference clock frequencies other than 100 MHz, use the following formula:  
REFCLK rms phase jitter at f (MHz) = REFCLK rms phase jitter at 100 MHz \* 100/f.
- (4) The minimum `reconfig_clk` frequency is 2.5 MHz if the transceiver channel is configured in **Transmitter only** mode. The minimum `reconfig_clk` frequency is 37.5 MHz if the transceiver channel is configured in **Receiver only** or **Receiver and Transmitter** mode.
- (5) If your design uses more than one dynamic reconfiguration controller (`altgx_reconfig`) instances to control the transceiver (`altgx`) channels physically located on the same side of the device AND if you use different `reconfig_clk` sources for these `altgx_reconfig` instances, the delta time between any two of these `reconfig_clk` sources becoming stable must not exceed the maximum specification listed.
- (6) The device cannot tolerate prolonged operation at this absolute maximum.
- (7) You must use the 1.1-V RX  $V_{ICM}$  setting if the input serial data standard is LVDS.
- (8) The differential eye opening specification at the receiver input pins assumes that Receiver Equalization is disabled. If you enable Receiver Equalization, the receiver circuitry can tolerate a lower minimum eye opening, depending on the equalization level. Use H-Spice simulation to derive the minimum eye opening requirement with Receiver Equalization enabled.
- (9) The rate matcher supports only up to  $\pm 300$  ppm.
- (10) Time taken to `rx_pll_locked` goes high from `rx_analogreset` de-assertion. Refer to [Figure 1–1 on page 1–33](#).
- (11) Time for which the CDR must be kept in lock-to-reference mode after `rx_pll_locked` goes high and before `rx_locktodata` is asserted in manual mode. Refer to [Figure 1–1 on page 1–33](#).
- (12) Time taken to recover valid data after the `rx_locktodata` signal is asserted in manual mode. Refer to [Figure 1–1 on page 1–33](#).
- (13) Time taken to recover valid data after the `rx_freqlocked` signal goes high in automatic mode. Refer to [Figure 1–2 on page 1–33](#).
- (14) A GPLL may be required to meet the PMA-FPGA fabric interface timing above certain data rates. For more information, refer to the [Transceiver Clocking for Arria II Devices](#) chapter.
- (15) The Quartus II software automatically selects the appropriate slew rate depending on the configured data rate or functional mode.
- (16) To support data rates lower than the minimum specification through oversampling, use the CDR in LTR mode only.

Figure 1-3 shows the differential receiver input waveform.

**Figure 1-3. Receiver Input Waveform**

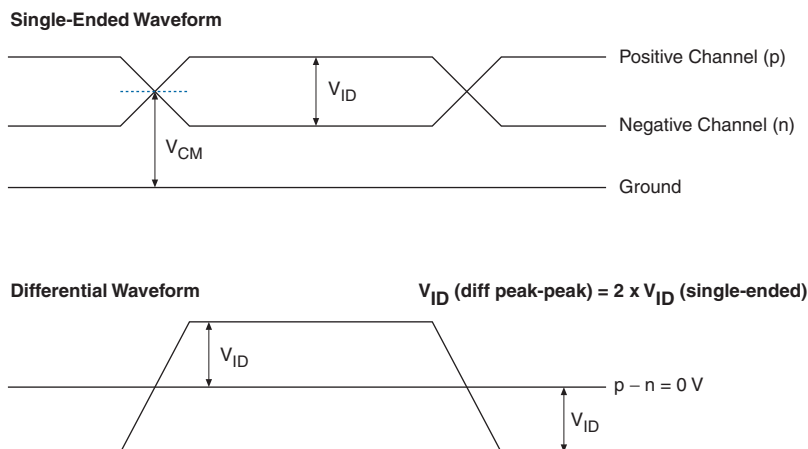


Figure 1-4 shows the transmitter output waveform.

**Figure 1-4. Transmitter Output Waveform**

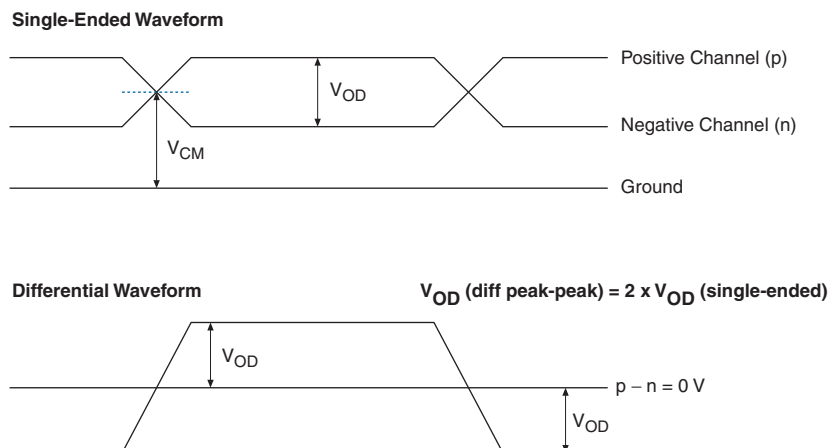


Table 1-36 lists the typical  $V_{OD}$  for TX term that equals  $85\ \Omega$  for Arria II GZ devices.

**Table 1-36. Typical  $V_{OD}$  Setting, TX Term =  $85\ \Omega$  for Arria II GZ Devices**

| Symbol                                          | $V_{OD}$ Setting (mV) |                |                |                |                |                |                |                 |
|-------------------------------------------------|-----------------------|----------------|----------------|----------------|----------------|----------------|----------------|-----------------|
|                                                 | 0                     | 1              | 2              | 3              | 4              | 5              | 6              | 7               |
| $V_{OD}$ differential peak-to-peak Typical (mV) | $170 \pm 20\%$        | $340 \pm 20\%$ | $510 \pm 20\%$ | $595 \pm 20\%$ | $680 \pm 20\%$ | $765 \pm 20\%$ | $850 \pm 20\%$ | $1020 \pm 20\%$ |

**Table 1–39. Transmitter Pre-Emphasis Levels for Arria II GZ Devices (Part 2 of 2)**

| Pre-Emphasis<br>1st<br>Post-Tap<br>Setting | V <sub>DD</sub> Setting |     |     |      |      |     |     |     |
|--------------------------------------------|-------------------------|-----|-----|------|------|-----|-----|-----|
|                                            | 0                       | 1   | 2   | 3    | 4    | 5   | 6   | 7   |
| 29                                         | N/A                     | N/A | N/A | 12.5 | 9.6  | 7.7 | 6.3 | 4.3 |
| 30                                         | N/A                     | N/A | N/A | N/A  | 11.4 | 9   | 7.4 | N/A |
| 31                                         | N/A                     | N/A | N/A | N/A  | 12.9 | 10  | 8.2 | N/A |

Table 1–40 lists the transceiver jitter specifications for all supported protocols for Arria II GX devices.

**Table 1–40. Transceiver Block Jitter Specifications for Arria II GX Devices (Note 1) (Part 1 of 10)**

| Symbol/<br>Description                   | Conditions                                      | I3     |     |      | C4     |     |      | C5, I5 |     |      | C6     |     |      | Unit |
|------------------------------------------|-------------------------------------------------|--------|-----|------|--------|-----|------|--------|-----|------|--------|-----|------|------|
|                                          |                                                 | Min    | Typ | Max  | Min    | Typ | Max  | Min    | Typ | Max  | Min    | Typ | Max  |      |
| SONET/SDH Transmit Jitter Generation (2) |                                                 |        |     |      |        |     |      |        |     |      |        |     |      |      |
| Peak-to-peak jitter at 622.08 Mbps       | Pattern = PRBS15                                | —      | —   | 0.1  | —      | —   | 0.1  | —      | —   | 0.1  | —      | —   | 0.1  | UI   |
| RMS jitter at 622.08 Mbps                | Pattern = PRBS15                                | —      | —   | 0.01 | —      | —   | 0.01 | —      | —   | 0.01 | —      | —   | 0.01 | UI   |
| Peak-to-peak jitter at 2488.32 Mbps      | Pattern = PRBS15                                | —      | —   | 0.1  | —      | —   | 0.1  | —      | —   | 0.1  | —      | —   | 0.1  | UI   |
| RMS jitter at 2488.32 Mbps               | Pattern = PRBS15                                | —      | —   | 0.01 | —      | —   | 0.01 | —      | —   | 0.01 | —      | —   | 0.01 | UI   |
| SONET/SDH Receiver Jitter Tolerance (2)  |                                                 |        |     |      |        |     |      |        |     |      |        |     |      |      |
| Jitter tolerance at 622.08 Mbps          | Jitter frequency = 0.03 KHz<br>Pattern = PRBS15 | > 15   |     |      | > 15   |     |      | > 15   |     |      | > 15   |     |      | UI   |
|                                          | Jitter frequency = 25 KHZ<br>Pattern = PRBS15   | > 1.5  |     |      | > 1.5  |     |      | > 1.5  |     |      | > 1.5  |     |      | UI   |
|                                          | Jitter frequency = 250 KHz<br>Pattern = PRBS15  | > 0.15 |     |      | > 0.15 |     |      | > 0.15 |     |      | > 0.15 |     |      | UI   |

**Table 1–40. Transceiver Block Jitter Specifications for Arria II GX Devices (Note 1) (Part 2 of 10)**

| Symbol/<br>Description                   | Conditions                                         | I3     |     |      | C4     |     |      | C5, I5 |     |      | C6     |     |      | Unit |
|------------------------------------------|----------------------------------------------------|--------|-----|------|--------|-----|------|--------|-----|------|--------|-----|------|------|
|                                          |                                                    | Min    | Typ | Max  | Min    | Typ | Max  | Min    | Typ | Max  | Min    | Typ | Max  |      |
| Jitter tolerance at<br>2488.32 Mbps      | Jitter frequency =<br>0.06 KHz<br>Pattern = PRBS15 | > 15   |     |      | > 15   |     |      | > 15   |     |      | > 15   |     |      | UI   |
|                                          | Jitter frequency =<br>100 KHz<br>Pattern = PRBS15  | > 1.5  |     |      | > 1.5  |     |      | > 1.5  |     |      | > 1.5  |     |      | UI   |
|                                          | Jitter frequency =<br>1 MHz<br>Pattern = PRBS15    | > 0.15 |     |      | > 0.15 |     |      | > 0.15 |     |      | > 0.15 |     |      | UI   |
|                                          | Jitter frequency =<br>10 MHz<br>Pattern = PRBS15   | > 0.15 |     |      | > 0.15 |     |      | > 0.15 |     |      | > 0.15 |     |      | UI   |
| XAUI Transmit Jitter Generation (3)      |                                                    |        |     |      |        |     |      |        |     |      |        |     |      |      |
| Total jitter at<br>3.125 Gbps            | Pattern = CJPAT                                    | —      | —   | 0.3  | —      | —   | 0.3  | —      | —   | 0.3  | —      | —   | 0.3  | UI   |
| Deterministic<br>jitter at<br>3.125 Gbps | Pattern = CJPAT                                    | —      | —   | 0.17 | —      | —   | 0.17 | —      | —   | 0.17 | —      | —   | 0.17 | UI   |
| XAUI Receiver Jitter Tolerance (3)       |                                                    |        |     |      |        |     |      |        |     |      |        |     |      |      |
| Total jitter                             | —                                                  | > 0.65 |     |      | > 0.65 |     |      | > 0.65 |     |      | > 0.65 |     |      | UI   |
| Deterministic<br>jitter                  | —                                                  | > 0.37 |     |      | > 0.37 |     |      | > 0.37 |     |      | > 0.37 |     |      | UI   |
| Peak-to-peak<br>jitter                   | Jitter frequency =<br>22.1 KHz                     | > 8.5  |     |      | > 8.5  |     |      | > 8.5  |     |      | > 8.5  |     |      | UI   |
| Peak-to-peak<br>jitter                   | Jitter frequency =<br>1.875 MHz                    | > 0.1  |     |      | > 0.1  |     |      | > 0.1  |     |      | > 0.1  |     |      | UI   |
| Peak-to-peak<br>jitter                   | Jitter frequency =<br>20 MHz                       | > 0.1  |     |      | > 0.1  |     |      | > 0.1  |     |      | > 0.1  |     |      | UI   |
| PCIe Transmit Jitter Generation (4)      |                                                    |        |     |      |        |     |      |        |     |      |        |     |      |      |
| Total jitter at<br>2.5 Gbps (Gen1)       | Compliance<br>pattern                              | —      | —   | 0.25 | —      | —   | 0.25 | —      | —   | 0.25 | —      | —   | 0.25 | UI   |

**Table 1–40. Transceiver Block Jitter Specifications for Arria II GX Devices (Note 1) (Part 5 of 10)**

| Symbol/<br>Description                           | Conditions                                                                                                             | I3    |     |     | C4    |     |     | C5, I5 |     |     | C6    |     |     | Unit |
|--------------------------------------------------|------------------------------------------------------------------------------------------------------------------------|-------|-----|-----|-------|-----|-----|--------|-----|-----|-------|-----|-----|------|
|                                                  |                                                                                                                        | Min   | Typ | Max | Min   | Typ | Max | Min    | Typ | Max | Min   | Typ | Max |      |
| SDI Transmitter Jitter Generation (8)            |                                                                                                                        |       |     |     |       |     |     |        |     |     |       |     |     |      |
| Alignment jitter<br>(peak-to-peak)               | Data rate =<br>1.485 Gbps (HD)<br>pattern = Color<br>Bar Low-<br>frequency Roll-off<br>= 100 KHz                       | 0.2   | —   | —   | 0.2   | —   | —   | 0.2    | —   | —   | 0.2   | —   | —   | UI   |
|                                                  | Data rate =<br>2.97 Gbps (3G)<br>pattern = Color<br>bar Low-<br>frequency Roll-off<br>= 100 KHz                        | 0.3   | —   | —   | 0.3   | —   | —   | 0.3    | —   | —   | 0.3   | —   | —   | UI   |
| SDI Receiver Jitter Tolerance (8)                |                                                                                                                        |       |     |     |       |     |     |        |     |     |       |     |     |      |
| Sinusoidal jitter<br>tolerance<br>(peak-to-peak) | Jitter frequency =<br>15 KHz<br><br>Data rate =<br>2.97 Gbps (3G)<br>Pattern = single<br>line scramble<br>color bar    | > 2   |     |     | > 2   |     |     | > 2    |     |     | > 2   |     |     | UI   |
|                                                  | Jitter frequency =<br>100 KHz<br><br>Data rate =<br>2.97 Gbps (3G)<br>Pattern = single<br>line scramble<br>color bar   | > 0.3 |     |     | > 0.3 |     |     | > 0.3  |     |     | > 0.3 |     |     | UI   |
|                                                  | Jitter frequency =<br>148.5 MHz<br><br>Data rate =<br>2.97 Gbps (3G)<br>Pattern = single<br>line scramble<br>color bar | > 0.3 |     |     | > 0.3 |     |     | > 0.3  |     |     | > 0.3 |     |     | UI   |

**Table 1–40. Transceiver Block Jitter Specifications for Arria II GX Devices (Note 1) (Part 8 of 10)**

| Symbol/<br>Description                                     | Conditions                                               | I3     |     |           | C4     |     |       | C5, I5 |     |       | C6     |     |       | Unit |
|------------------------------------------------------------|----------------------------------------------------------|--------|-----|-----------|--------|-----|-------|--------|-----|-------|--------|-----|-------|------|
|                                                            |                                                          | Min    | Typ | Max       | Min    | Typ | Max   | Min    | Typ | Max   | Min    | Typ | Max   |      |
| CPRI Transmit Jitter Generation (11)                       |                                                          |        |     |           |        |     |       |        |     |       |        |     |       |      |
| Total jitter                                               | E.6.HV, E.12.HV<br>Pattern = CJPAT                       | —      | —   | 0.27<br>9 | —      | —   | 0.279 | —      | —   | 0.279 | —      | —   | 0.279 | UI   |
|                                                            | E.6.LV, E.12.LV,<br>E.24.LV, E.30.LV<br>Pattern = CJTPAT | —      | —   | 0.35      | —      | —   | 0.35  | —      | —   | 0.35  | —      | —   | 0.35  | UI   |
| Deterministic jitter                                       | E.6.HV, E.12.HV<br>Pattern = CJPAT                       | —      | —   | 0.14      | —      | —   | 0.14  | —      | —   | 0.14  | —      | —   | 0.14  | UI   |
|                                                            | E.6.LV, E.12.LV,<br>E.24.LV, E.30.LV<br>Pattern = CJTPAT | —      | —   | 0.17      | —      | —   | 0.17  | —      | —   | 0.17  | —      | —   | 0.17  | UI   |
| CPRI Receiver Jitter Tolerance (11)                        |                                                          |        |     |           |        |     |       |        |     |       |        |     |       |      |
| Total jitter tolerance                                     | E.6.HV, E.12.HV<br>Pattern = CJPAT                       | > 0.66 |     |           | > 0.66 |     |       | > 0.66 |     |       | > 0.66 |     |       | UI   |
| Deterministic jitter tolerance                             | E.6.HV, E.12.HV<br>Pattern = CJPAT                       | > 0.4  |     |           | > 0.4  |     |       | > 0.4  |     |       | > 0.4  |     |       | UI   |
| Total jitter tolerance                                     | E.6.LV, E.12.LV,<br>E.24.LV, E.30.LV<br>Pattern = CJTPAT | > 0.65 |     |           | > 0.65 |     |       | > 0.65 |     |       | > 0.65 |     |       | UI   |
|                                                            | E.60.LV<br>Pattern = PRBS31                              | > 0.6  |     |           | —      |     |       | —      |     |       | —      |     |       | UI   |
| Deterministic jitter tolerance                             | E.6.LV, E.12.LV,<br>E.24.LV, E.30.LV<br>Pattern = CJTPAT | > 0.37 |     |           | > 0.37 |     |       | > 0.37 |     |       | > 0.37 |     |       | UI   |
|                                                            | E.60.LV<br>Pattern = PRBS31                              | > 0.45 |     |           | —      |     |       | —      |     |       | —      |     |       | UI   |
| Combined deterministic and random jitter tolerance         | E.6.LV, E.12.LV,<br>E.24.LV, E.30.LV<br>Pattern = CJTPAT | > 0.55 |     |           | > 0.55 |     |       | > 0.55 |     |       | > 0.55 |     |       | UI   |
| OBSAI Transmit Jitter Generation (12)                      |                                                          |        |     |           |        |     |       |        |     |       |        |     |       |      |
| Total jitter at 768 Mbps, 1536 Mbps, and 3072 Mbps         | REFCLK = 153.6 MHz<br>Pattern = CJPAT                    | —      | —   | 0.35      | —      | —   | 0.35  | —      | —   | 0.35  | —      | —   | 0.35  | UI   |
| Deterministic jitter at 768 Mbps, 1536 Mbps, and 3072 Mbps | REFCLK = 153.6 MHz<br>Pattern = CJPAT                    | —      | —   | 0.17      | —      | —   | 0.17  | —      | —   | 0.17  | —      | —   | 0.17  | UI   |

**Table 1–41. Transceiver Block Jitter Specifications for Arria II GZ Devices (Note 1), (2) (Part 2 of 7)**

| Symbol/<br>Description                            | Conditions                                      | –C3 and –I3 |     |      | –C4 and –I4 |     |      | Unit |
|---------------------------------------------------|-------------------------------------------------|-------------|-----|------|-------------|-----|------|------|
|                                                   |                                                 | Min         | Typ | Max  | Min         | Typ | Max  |      |
| Jitter tolerance at 2488.32 Mbps                  | Jitter frequency = 0.06 KHz<br>Pattern = PRBS15 | > 15        |     |      | > 15        |     |      | UI   |
|                                                   | Jitter frequency = 100 KHZ<br>Pattern = PRBS15  | > 1.5       |     |      | > 1.5       |     |      | UI   |
|                                                   | Jitter frequency = 1 MHz<br>Pattern = PRBS15    | > 0.15      |     |      | > 0.15      |     |      | UI   |
|                                                   | Jitter frequency = 10 MHz<br>Pattern = PRBS15   | > 0.15      |     |      | > 0.15      |     |      | UI   |
| Fibre Channel Transmit Jitter Generation (4), (5) |                                                 |             |     |      |             |     |      |      |
| Total jitter FC-1                                 | Pattern = CRPAT                                 | —           | —   | 0.23 | —           | —   | 0.23 | UI   |
| Deterministic jitter FC-1                         | Pattern = CRPAT                                 | —           | —   | 0.11 | —           | —   | 0.11 | UI   |
| Total jitter FC-2                                 | Pattern = CRPAT                                 | —           | —   | 0.33 | —           | —   | 0.33 | UI   |
| Deterministic jitter FC-2                         | Pattern = CRPAT                                 | —           | —   | 0.2  | —           | —   | 0.2  | UI   |
| Total jitter FC-4                                 | Pattern = CRPAT                                 | —           | —   | 0.52 | —           | —   | 0.52 | UI   |
| Deterministic jitter FC-4                         | Pattern = CRPAT                                 | —           | —   | 0.33 | —           | —   | 0.33 | UI   |
| Fibre Channel Receiver Jitter Tolerance (4), (6)  |                                                 |             |     |      |             |     |      |      |
| Deterministic jitter FC-1                         | Pattern = CJTPAT                                | > 0.37      |     |      | > 0.37      |     |      | UI   |
| Random jitter FC-1                                | Pattern = CJTPAT                                | > 0.31      |     |      | > 0.31      |     |      | UI   |
| Sinusoidal jitter FC-1                            | Fc/25000                                        | > 1.5       |     |      | > 1.5       |     |      | UI   |
|                                                   | Fc/1667                                         | > 0.1       |     |      | > 0.1       |     |      | UI   |
| Deterministic jitter FC-2                         | Pattern = CJTPAT                                | > 0.33      |     |      | > 0.33      |     |      | UI   |
| Random jitter FC-2                                | Pattern = CJTPAT                                | > 0.29      |     |      | > 0.29      |     |      | UI   |
| Sinusoidal jitter FC-2                            | Fc/25000                                        | > 1.5       |     |      | > 1.5       |     |      | UI   |
|                                                   | Fc/1667                                         | > 0.1       |     |      | > 0.1       |     |      | UI   |
| Deterministic jitter FC-4                         | Pattern = CJTPAT                                | > 0.33      |     |      | > 0.33      |     |      | UI   |
| Random jitter FC-4                                | Pattern = CJTPAT                                | > 0.29      |     |      | > 0.29      |     |      | UI   |
| Sinusoidal jitter FC-4                            | Fc/25000                                        | > 1.5       |     |      | > 1.5       |     |      | UI   |
|                                                   | Fc/1667                                         | > 0.1       |     |      | > 0.1       |     |      | UI   |
| XAUI Transmit Jitter Generation (7)               |                                                 |             |     |      |             |     |      |      |
| Total jitter at 3.125 Gbps                        | Pattern = CJPAT                                 | —           | —   | 0.3  | —           | —   | 0.3  | UI   |
| Deterministic jitter at 3.125 Gbps                | Pattern = CJPAT                                 | —           | —   | 0.17 | —           | —   | 0.17 | UI   |
| XAUI Receiver Jitter Tolerance (7)                |                                                 |             |     |      |             |     |      |      |
| Total jitter                                      | —                                               | > 0.65      |     |      | > 0.65      |     |      | UI   |
| Deterministic jitter                              | —                                               | > 0.37      |     |      | > 0.37      |     |      | UI   |

**Table 1–41. Transceiver Block Jitter Specifications for Arria II GZ Devices (Note 1), (2) (Part 3 of 7)**

| Symbol/<br>Description                                                   | Conditions                                                                           | –C3 and –I3   |     |       | –C4 and –I4   |     |       | Unit |
|--------------------------------------------------------------------------|--------------------------------------------------------------------------------------|---------------|-----|-------|---------------|-----|-------|------|
|                                                                          |                                                                                      | Min           | Typ | Max   | Min           | Typ | Max   |      |
| Peak-to-peak jitter                                                      | Jitter frequency = 22.1 KHz                                                          | > 8.5         |     |       | > 8.5         |     |       | UI   |
| Peak-to-peak jitter                                                      | Jitter frequency = 1.875 MHz                                                         | > 0.1         |     |       | > 0.1         |     |       | UI   |
| Peak-to-peak jitter                                                      | Jitter frequency = 20 MHz                                                            | > 0.1         |     |       | > 0.1         |     |       | UI   |
| PCIe Transmit Jitter Generation (8)                                      |                                                                                      |               |     |       |               |     |       |      |
| Total jitter at 2.5 Gbps (Gen1)—<br>x1, x4, and x8                       | Compliance pattern                                                                   | —             | —   | 0.25  | —             | —   | 0.25  | UI   |
| Total jitter at 5 Gbps (Gen2)—<br>x1, x4, and x8                         | Compliance pattern                                                                   | —             | —   | 0.25  | —             | —   | —     | UI   |
| PCIe Receiver Jitter Tolerance (8)                                       |                                                                                      |               |     |       |               |     |       |      |
| Total jitter at 2.5 Gbps (Gen1)                                          | Compliance pattern                                                                   | > 0.6         |     |       | > 0.6         |     |       | UI   |
| Total jitter at 5 Gbps (Gen2)                                            | Compliance pattern                                                                   | Not supported |     |       | Not supported |     |       | UI   |
| PCIe (Gen 1) Electrical Idle Detect Threshold                            |                                                                                      |               |     |       |               |     |       |      |
| V <sub>RX-IDLE-DETDIFFp-p</sub> (9)                                      | Compliance pattern                                                                   | 65            | —   | 175   | 65            | —   | 175   | UI   |
| SRIO Transmit Jitter Generation (10)                                     |                                                                                      |               |     |       |               |     |       |      |
| Deterministic jitter<br>(peak-to-peak)                                   | Data rate = 1.25, 2.5, 3.125 Gbps<br>Pattern = CJPAT                                 | —             | —   | 0.17  | —             | —   | 0.17  | UI   |
| Total jitter (peak-to-peak)                                              | Data rate = 1.25, 2.5, 3.125 Gbps<br>Pattern = CJPAT                                 | —             | —   | 0.35  | —             | —   | 0.35  | UI   |
| SRIO Receiver Jitter Tolerance (10)                                      |                                                                                      |               |     |       |               |     |       |      |
| Deterministic jitter tolerance<br>(peak-to-peak)                         | Data rate = 1.25, 2.5, 3.125 Gbps<br>Pattern = CJPAT                                 | > 0.37        |     |       | > 0.37        |     |       | UI   |
| Combined deterministic and<br>random jitter tolerance (peak-to-<br>peak) | Data rate = 1.25, 2.5, 3.125 Gbps<br>Pattern = CJPAT                                 | > 0.55        |     |       | > 0.55        |     |       | UI   |
| Sinusoidal jitter tolerance (peak-<br>to-peak)                           | Jitter frequency = 22.1 KHz<br>Data rate = 1.25, 2.5, 3.125 Gbps<br>Pattern = CJPAT  | > 8.5         |     |       | > 8.5         |     |       | UI   |
|                                                                          | Jitter frequency = 1.875 MHz<br>Data rate = 1.25, 2.5, 3.125 Gbps<br>Pattern = CJPAT | > 0.1         |     |       | > 0.1         |     |       | UI   |
|                                                                          | Jitter frequency = 20 MHz<br>Data rate = 1.25, 2.5, 3.125 Gbps<br>Pattern = CJPAT    | > 0.1         |     |       | > 0.1         |     |       | UI   |
| GIGE Transmit Jitter Generation (11)                                     |                                                                                      |               |     |       |               |     |       |      |
| Deterministic jitter<br>(peak-to-peak)                                   | Pattern = CRPAT                                                                      | —             | —   | 0.14  | —             | —   | 0.14  | UI   |
| Total jitter (peak-to-peak)                                              | Pattern = CRPAT                                                                      | —             | —   | 0.279 | —             | —   | 0.279 | UI   |

**Table 1-44. PLL Specifications for Arria II GX Devices (Part 3 of 3)**

| Symbol                                            | Description                                                                         | Min | Typ | Max  | Unit      |
|---------------------------------------------------|-------------------------------------------------------------------------------------|-----|-----|------|-----------|
| $t_{CASC\_OUTJITTER\_PERIOD\_DEDCLK}$<br>(6), (7) | Period jitter for dedicated clock output in cascaded PLLs ( $F_{OUT} \geq 100$ MHz) | —   | —   | 425  | ps (p-p)  |
|                                                   | Period jitter for dedicated clock output in cascaded PLLs ( $F_{OUT} \leq 100$ MHz) | —   | —   | 42.5 | mUI (p-p) |

**Notes to Table 1-44:**

- (1)  $f_{IN}$  is limited by the I/O  $f_{MAX}$ .
- (2) The VCO frequency reported by the Quartus II software in the PLL summary section of the compilation report takes into consideration the VCO post-scale counter K value. Therefore, if the counter K has a value of 2, the frequency reported can be lower than the  $f_{VCO}$  specification.
- (3) A high-input jitter directly affects the PLL output jitter. To have low PLL output clock jitter, you must provide a clean-clock source, which is less than 200 ps.
- (4)  $F_{REF}$  is  $f_{IN}/N$  when  $N = 1$ .
- (5) This specification is limited by the lower of the two: I/O  $f_{MAX}$  or  $f_{OUT}$  of the PLL.
- (6) Peak-to-peak jitter with a probability level of  $10^{-12}$  (14 sigma, 99.9999999974404% confidence level). The output jitter specification applies to the intrinsic jitter of the PLL, when an input jitter of 30 ps is applied. The external memory interface clock output jitter specifications use a different measurement method and are available in Table 1-62 on page 1-70.
- (7) The cascaded PLL specification is only applicable with the following condition:
  - a. Upstream PLL:  $0.59 \text{ MHz} \leq \text{Upstream PLL BW} < 1 \text{ MHz}$
  - b. Downstream PLL:  $\text{Downstream PLL BW} > 2 \text{ MHz}$

Table 1-45 lists the PLL specifications for Arria II GZ devices when operating in both the commercial junction temperature range (0° to 85°C) and the industrial junction temperature range (-40° to 100°C).

**Table 1-45. PLL Specifications for Arria II GZ Devices (Part 1 of 2)**

| Symbol            | Parameter                                                                        | Min | Typ | Max     | Unit           |
|-------------------|----------------------------------------------------------------------------------|-----|-----|---------|----------------|
| $f_{IN}$          | Input clock frequency (-3 speed grade)                                           | 5   | —   | 717 (1) | MHz            |
|                   | Input clock frequency (-4 speed grade)                                           | 5   | —   | 717 (1) | MHz            |
| $f_{INPFD}$       | Input frequency to the PFD                                                       | 5   | —   | 325     | MHz            |
| $f_{VCO}$         | PLL VCO operating range (-3 speed grade)                                         | 600 | —   | 1,300   | MHz            |
|                   | PLL VCO operating range (-4 speed grade)                                         | 600 | —   | 1,300   | MHz            |
| $t_{EINDUTY}$     | Input clock or external feedback clock input duty cycle                          | 40  | —   | 60      | %              |
| $f_{OUT}$         | Output frequency for internal global or regional clock (-3 speed grade)          | —   | —   | 700 (2) | MHz            |
|                   | Output frequency for internal global or regional clock (-4 speed grade)          | —   | —   | 500 (2) | MHz            |
| $f_{OUT\_EXT}$    | Output frequency for external clock output (-3 speed grade)                      | —   | —   | 717 (2) | MHz            |
|                   | Output frequency for external clock output (-4 speed grade)                      | —   | —   | 717 (2) | MHz            |
| $t_{OUTDUTY}$     | Duty cycle for external clock output (when set to 50%)                           | 45  | 50  | 55      | %              |
| $t_{FCOMP}$       | External feedback clock compensation time                                        | —   | —   | 10      | ns             |
| $t_{CONFIGPLL}$   | Time required to reconfigure scan chain                                          | —   | 3.5 | —       | scanclk cycles |
| $t_{CONFIGPHASE}$ | Time required to reconfigure phase shift                                         | —   | 1   | —       | scanclk cycles |
| $f_{SCANCLK}$     | scanclk frequency                                                                | —   | —   | 100     | MHz            |
| $t_{LOCK}$        | Time required to lock from end-of-device configuration or de-assertion of areset | —   | —   | 1       | ms             |

## Configuration

Table 1–50 lists the configuration mode specifications for Arria II GX and GZ devices.

**Table 1–50. Configuration Mode Specifications for Arria II Devices**

| Programming Mode                   | DCLK Frequency |     |     | Unit |
|------------------------------------|----------------|-----|-----|------|
|                                    | Min            | Typ | Max |      |
| Passive serial                     | —              | —   | 125 | MHz  |
| Fast passive parallel              | —              | —   | 125 | MHz  |
| Fast active serial (fast clock)    | 17             | 26  | 40  | MHz  |
| Fast active serial (slow clock)    | 8.5            | 13  | 20  | MHz  |
| Remote update only in fast AS mode | —              | —   | 10  | MHz  |

## JTAG Specifications

Table 1–51 lists the JTAG timing parameters and values for Arria II GX and GZ devices.

**Table 1–51. JTAG Timing Parameters and Values for Arria II Devices**

| Symbol          | Description                              | Min | Max | Unit |
|-----------------|------------------------------------------|-----|-----|------|
| $t_{JCP}$       | TCK clock period                         | 30  | —   | ns   |
| $t_{JCH}$       | TCK clock high time                      | 14  | —   | ns   |
| $t_{JCL}$       | TCK clock low time                       | 14  | —   | ns   |
| $t_{JPSU(TDI)}$ | TDI JTAG port setup time                 | 1   | —   | ns   |
| $t_{JPSU(TMS)}$ | TMS JTAG port setup time                 | 3   | —   | ns   |
| $t_{JPH}$       | JTAG port hold time                      | 5   | —   | ns   |
| $t_{JPCO}$      | JTAG port clock to output                | —   | 11  | ns   |
| $t_{JPZX}$      | JTAG port high impedance to valid output | —   | 14  | ns   |
| $t_{JPXZ}$      | JTAG port valid output to high impedance | —   | 14  | ns   |

## Chip-Wide Reset (Dev\_CLRn) Specifications

Table 1–52 lists the specifications for the chip-wide reset (Dev\_CLRn) for Arria II GX and GZ devices.

**Table 1–52. Chip-Wide Reset (Dev\_CLRn) Specifications for Arria II Devices**

| Description | Min | Typ | Max | Unit |
|-------------|-----|-----|-----|------|
| Dev_CLRn    | 500 | —   | —   | μs   |

Figure 1-6 shows the LVDS soft-CDR/DPA sinusoidal jitter tolerance specification for Arria II GZ devices at 1.25 Gbps data rate.

**Figure 1-6. LVDS Soft-CDR/DPA Sinusoidal Jitter Tolerance Specification for Arria II GZ Devices at a 1.25 Gbps Data Rate**

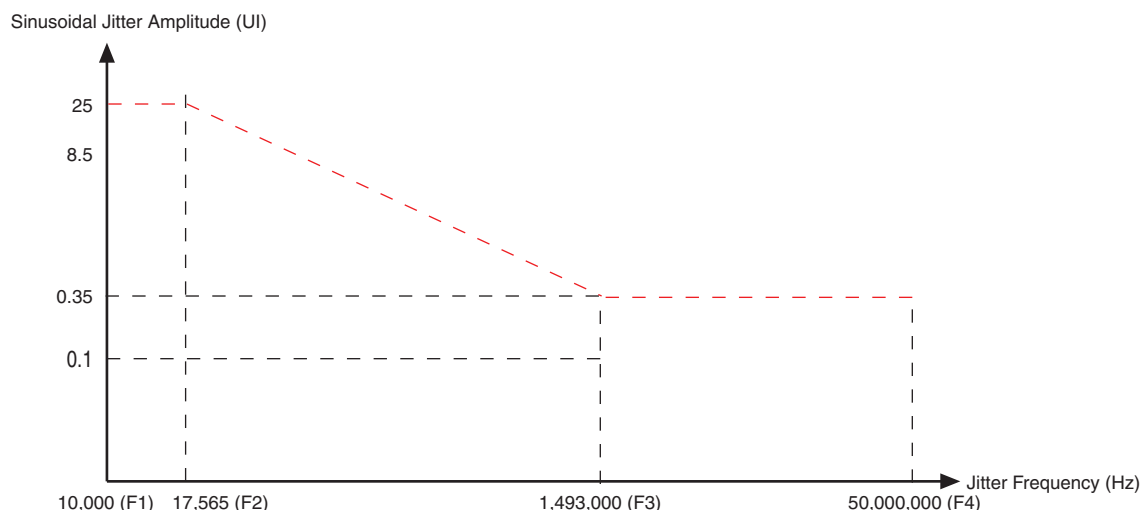


Table 1-56 lists the LVDS soft-CDR/DPA sinusoidal jitter tolerance specification for Arria II GZ devices at 1.25 Gbps data rate.

**Table 1-56. LVDS Soft-CDR/DPA Sinusoidal Jitter Mask Values for Arria II GZ Devices at 1.25 Gbps Data Rate**

| Jitter Frequency (Hz) |            | Sinusoidal Jitter (UI) |
|-----------------------|------------|------------------------|
| F1                    | 10,000     | 25.000                 |
| F2                    | 17,565     | 25.000                 |
| F3                    | 1,493,000  | 0.350                  |
| F4                    | 50,000,000 | 0.350                  |

## External Memory Interface Specifications

 For the maximum clock rate supported for Arria II GX and GZ device family, refer to the [External Memory Interface Spec Estimator](#) page on the Altera website.

Table 1-57 lists the external memory interface specifications for Arria II GX devices.

**Table 1-57. External Memory Interface Specifications for Arria II GX Devices (Part 1 of 2)**

| Frequency Mode | Frequency Range (MHz) |            |         | Resolution (°) | DQS Delay Buffer Mode <sup>(1)</sup> | Number of Delay Chains |
|----------------|-----------------------|------------|---------|----------------|--------------------------------------|------------------------|
|                | C4                    | I3, C5, I5 | C6      |                |                                      |                        |
| 0              | 90-140                | 90-130     | 90-110  | 22.5           | Low                                  | 16                     |
| 1              | 110-180               | 110-170    | 110-150 | 30             | Low                                  | 12                     |
| 2              | 140-220               | 140-210    | 140-180 | 36             | Low                                  | 10                     |
| 3              | 170-270               | 170-260    | 170-220 | 45             | Low                                  | 8                      |
| 4              | 220-340               | 220-310    | 220-270 | 30             | High                                 | 12                     |

