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Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	13940
Number of Logic Elements/Cells	348500
Total RAM Bits	21270528
Number of I/O	281
Number of Gates	-
Voltage - Supply	0.87V ~ 0.93V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	780-BBGA, FCBGA
Supplier Device Package	780-HBGA (33x33)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep2agz350fh29c4n

CAUTION

Conditions beyond those listed in Table 1–1 and Table 1–2 may cause permanent damage to the device. Additionally, device operation at the absolute maximum ratings for extended periods of time may have adverse effects on the device.

Table 1–1 lists the absolute maximum ratings for Arria II GX devices.

Table 1–1. Absolute Maximum Ratings for Arria II GX Devices

Symbol	Description	Minimum	Maximum	Unit
V_{CC}	Supplies power to the core, periphery, I/O registers, PCI Express® (PIPE) (PCIe) HIP block, and transceiver PCS	–0.5	1.35	V
V_{CCCB}	Supplies power for the configuration RAM bits	–0.5	1.8	V
V_{CCBAT}	Battery back-up power supply for design security volatile key register	–0.5	3.75	V
V_{CCPD}	Supplies power to the I/O pre-drivers, differential input buffers, and MSEL circuitry	–0.5	3.75	V
V_{CCIO}	Supplies power to the I/O banks	–0.5	3.9	V
V_{CCD_PLL}	Supplies power to the digital portions of the PLL	–0.5	1.35	V
V_{CCA_PLL}	Supplies power to the analog portions of the PLL and device-wide power management circuitry	–0.5	3.75	V
V_I	DC input voltage	–0.5	4.0	V
I_{OUT}	DC output current, per pin	–25	40	mA
V_{CCA}	Supplies power to the transceiver PMA regulator	—	3.75	V
V_{CCL_GXB}	Supplies power to the transceiver PMA TX, PMA RX, and clocking	—	1.21	V
V_{CCH_GXB}	Supplies power to the transceiver PMA output (TX) buffer	—	1.8	V
T_J	Operating junction temperature	–55	125	°C
T_{STG}	Storage temperature (no bias)	–65	150	°C

Table 1–2 lists the absolute maximum ratings for Arria II GZ devices.

Table 1–2. Absolute Maximum Ratings for Arria II GZ Devices (Part 1 of 2)

Symbol	Description	Minimum	Maximum	Unit
V_{CC}	Supplies power to the core, periphery, I/O registers, PCIe HIP block, and transceiver PCS	-0.5	1.35	V
V_{CCCB}	Power supply to the configuration RAM bits	-0.5	1.8	V
V_{CCPGM}	Supplies power to the configuration pins	-0.5	3.75	V
V_{CCAUX}	Auxiliary supply	-0.5	3.75	V
V_{CCBAT}	Supplies battery back-up power for design security volatile key register	-0.5	3.75	V
V_{CCPD}	Supplies power to the I/O pre-drivers, differential input buffers, and MSEL circuitry	-0.5	3.75	V
V_{CCIO}	Supplies power to the I/O banks	-0.5	3.9	V
V_{CC_CLKIN}	Supplies power to the differential clock input	-0.5	3.75	V
V_{CCD_PLL}	Supplies power to the digital portions of the PLL	-0.5	1.35	V
V_{CCA_PLL}	Supplies power to the analog portions of the PLL and device-wide power management circuitry	-0.5	3.75	V
V_I	DC input voltage	-0.5	4.0	V
I_{OUT}	DC output current, per pin	-25	40	mA

Table 1–17 lists the pin capacitance for Arria II GZ devices.

Table 1–17. Pin Capacitance for Arria II GZ Devices

Symbol	Description	Typical	Unit
C_{IOTB}	Input capacitance on the top and bottom I/O pins	4	pF
C_{IOLR}	Input capacitance on the left and right I/O pins	4	pF
C_{CLKTB}	Input capacitance on the top and bottom non-dedicated clock input pins	4	pF
C_{CLKLR}	Input capacitance on the left and right non-dedicated clock input pins	4	pF
C_{OUTFB}	Input capacitance on the dual-purpose clock output and feedback pins	5	pF
C_{CLK1}, C_{CLK3}, C_{CLK8}, and C_{CLK10}	Input capacitance for dedicated clock input pins	2	pF

Internal Weak Pull-Up and Weak Pull-Down Resistors

Table 1–18 lists the weak pull-up and pull-down resistor values for Arria II GX devices.

Table 1–18. Internal Weak Pull-up and Weak Pull-Down Resistors for Arria II GX Devices *(Note 1)*

Symbol	Description	Conditions	Min	Typ	Max	Unit
R_{PU}	Value of I/O pin pull-up resistor before and during configuration, as well as user mode if the programmable pull-up resistor option is enabled.	V_{CCIO} = 3.3 V ±5% *(2)*	7	25	41	kΩ
		V_{CCIO} = 3.0 V ±5% *(2)*	7	28	47	kΩ
		V_{CCIO} = 2.5 V ±5% *(2)*	8	35	61	kΩ
		V_{CCIO} = 1.8 V ±5% *(2)*	10	57	108	kΩ
		V_{CCIO} = 1.5 V ±5% *(2)*	13	82	163	kΩ
		V_{CCIO} = 1.2 V ±5% *(2)*	19	143	351	kΩ
R_{PD}	Value of TCK pin pull-down resistor	V_{CCIO} = 3.3 V ±5%	6	19	29	kΩ
		V_{CCIO} = 3.0 V ±5%	6	22	32	kΩ
		V_{CCIO} = 2.5 V ±5%	6	25	42	kΩ
		V_{CCIO} = 1.8 V ±5%	7	35	70	kΩ
		V_{CCIO} = 1.5 V ±5%	8	50	112	kΩ

Notes to Table 1–18:

(1) All I/O pins have an option to enable weak pull-up except configuration, test, and JTAG pins. The weak pull-down feature is only available for JTAG TCK.

(2) Pin pull-up resistance values may be lower if an external source drives the pin higher than V_{CCIO}.

Table 1–23. Single-Ended I/O Standards for Arria II GZ Devices (Part 2 of 2)

I/O Standard	V_{CCIO} (V)			V_{IL} (V)		V_{IH} (V)		V_{OL} (V)	V_{OH} (V)	I_{OL} (mA)	I_{OH} (mA)
	Min	Typ	Max	Min	Max	Min	Max	Max	Min		
1.2 V	1.14	1.2	1.26	-0.3	0.35 × V_{CCIO}	0.65 × V_{CCIO}	V_{CCIO} + 0.3	0.25 × V_{CCIO}	0.75 × V_{CCIO}	2	-2
3.0-V PCI	2.85	3	3.15	—	0.3 × V_{CCIO}	0.5 × V_{CCIO}	3.6	0.1 × V_{CCIO}	0.9 × V_{CCIO}	1.5	-0.5
3.0-V PCI-X	2.85	3	3.15	—	0.35 × V_{CCIO}	0.5 × V_{CCIO}	—	0.1 × V_{CCIO}	0.9 × V_{CCIO}	1.5	-0.5

Table 1–24 lists the single-ended SSTL and HSTL I/O reference voltage specifications for Arria II GX devices.

Table 1–24. Single-Ended SSTL and HSTL I/O Reference Voltage Specifications for Arria II GX Devices

I/O Standard	V_{CCIO} (V)			V_{REF} (V)			V_{TT} (V)		
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max
SSTL-2 Class I, II	2.375	2.5	2.625	0.49 × V_{CCIO}	0.5 × V_{CCIO}	0.51 × V_{CCIO}	V_{REF} - 0.04	V_{REF}	V_{REF} + 0.04
SSTL-18 Class I, II	1.71	1.8	1.89	0.833	0.9	0.969	V_{REF} - 0.04	V_{REF}	V_{REF} + 0.04
SSTL-15 Class I, II	1.425	1.5	1.575	0.47 × V_{CCIO}	0.5 × V_{CCIO}	0.53 × V_{CCIO}	0.47 × V_{CCIO}	0.5 × V_{CCIO}	0.53 × V_{CCIO}
HSTL-18 Class I, II	1.71	1.8	1.89	0.85	0.9	0.95	0.85	0.9	0.95
HSTL-15 Class I, II	1.425	1.5	1.575	0.71	0.75	0.79	0.71	0.75	0.79
HSTL-12 Class I, II	1.14	1.2	1.26	0.48 × V_{CCIO}	0.5 × V_{CCIO}	0.52 × V_{CCIO}	—	V_{CCIO}/2	—

Table 1–25 lists the single-ended SSTL and HSTL I/O reference voltage specifications for Arria II GZ devices.

Table 1–25. Single-Ended SSTL and HSTL I/O Reference Voltage Specifications for Arria II GZ Devices

I/O Standard	V_{CCIO} (V)			V_{REF} (V)			V_{TT} (V)		
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max
SSTL-2 Class I, II	2.375	2.5	2.625	0.49 × V_{CCIO}	0.5 × V_{CCIO}	0.51 × V_{CCIO}	V_{REF} - 0.04	V_{REF}	V_{REF} + 0.04
SSTL-18 Class I, II	1.71	1.8	1.89	0.833	0.9	0.969	V_{REF} - 0.04	V_{REF}	V_{REF} + 0.04
SSTL-15 Class I, II	1.425	1.5	1.575	0.47 × V_{CCIO}	0.5 × V_{CCIO}	0.53 × V_{CCIO}	0.47 × V_{CCIO}	V_{REF}	0.53 × V_{CCIO}
HSTL-18 Class I, II	1.71	1.8	1.89	0.85	0.9	0.95	—	V_{CCIO}/2	—
HSTL-15 Class I, II	1.425	1.5	1.575	0.68	0.75	0.9	—	V_{CCIO}/2	—
HSTL-12 Class I, II	1.14	1.2	1.26	0.47 × V_{CCIO}	0.5 × V_{CCIO}	0.53 × V_{CCIO}	—	V_{CCIO}/2	—

Table 1–30 lists the HSTL I/O standards for Arria II GX devices.

Table 1–30. Differential HSTL I/O Standards for Arria II GX Devices

I/O Standard	V_{CCIO} (V)			$V_{DIF(DC)}$ (V)		$V_{X(AC)}$ (V)			$V_{CM(DC)}$ (V)			$V_{DIF(AC)}$ (V)	
	Min	Typ	Max	Min	Max	Min	Typ	Max	Min	Typ	Max	Min	Max
HSTL-18 Class I	1.71	1.8	1.89	0.2	—	0.85	—	0.95	0.88	—	0.95	0.4	—
HSTL-15 Class I, II	1.425	1.5	1.575	0.2	—	0.71	—	0.79	0.71	—	0.79	0.4	—
HSTL-12 Class I, II	1.14	1.2	1.26	0.16	—	—	0.5 × V_{CCIO}	—	0.48 × V_{CCIO}	0.5 × V_{CCIO}	0.52 × V_{CCIO}	0.3	—

Table 1–31 lists the HSTL I/O standards for Arria II GZ devices.

Table 1–31. Differential HSTL I/O Standards for Arria II GZ Devices

I/O Standard	V_{CCIO} (V)			$V_{DIF(DC)}$ (V)		$V_{X(AC)}$ (V)			$V_{CM(DC)}$ (V)			$V_{DIF(AC)}$ (V)	
	Min	Typ	Max	Min	Max	Min	Typ	Max	Min	Typ	Max	Min	Max
HSTL-18 Class I	1.71	1.8	1.89	0.2	—	0.78	—	1.12	0.78	—	1.12	0.4	—
HSTL-15 Class I, II	1.425	1.5	1.575	0.2	—	0.68	—	0.9	0.68	—	0.9	0.4	—
HSTL-12 Class I, II	1.14	1.2	1.26	0.16	V_{CCIO} + 0.3	—	0.5 × V_{CCIO}	—	0.4 × V_{CCIO}	0.5 × V_{CCIO}	0.6 × V_{CCIO}	0.3	V_{CCIO} + 0.48

Table 1–32 lists the differential I/O standard specifications for Arria II GX devices.

Table 1–32. Differential I/O Standard Specifications for Arria II GX Devices *(Note 1)*

I/O Standard	V_{CCIO} (V)			V_{ID} (mV)			V_{ICM} (V) *(2)*		V_{OD} (V) *(3)*			V_{OCM} (V)		
	Min	Typ	Max	Min	Cond.	Max	Min	Max	Min	Typ	Max	Min	Typ	Max
2.5 V LVDS	2.375	2.5	2.625	100	V_{CM} = 1.25 V	—	0.05	1.80	0.247	—	0.6	1.125	1.25	1.375
RSDS *(4)*	2.375	2.5	2.625	—	—	—	—	—	0.1	0.2	0.6	0.5	1.2	1.4
Mini-LVDS *(4)*	2.375	2.5	2.625	—	—	—	—	—	0.25	—	0.6	1	1.2	1.4
LVPECL *(5)*	2.375	2.5	2.625	300	—	—	0.6	1.8	—	—	—	—	—	—
BLVDS *(6)*	2.375	2.5	2.625	100	—	—	—	—	—	—	—	—	—	—

Notes to Table 1–32:

(1) The 1.5 V PCML transceiver I/O standard specifications are described in "Transceiver Performance Specifications" on page 1–21.
(2) V_{IN} range: 0 <= V_{IN} <= 1.85 V.
(3) R_L range: 90 <= RL <= 110 Ω.
(4) The RSDS and mini-LVDS I/O standards are only supported for differential outputs.
(5) The LVPECL input standard is supported at the dedicated clock input pins (GCLK) only.
(6) There are no fixed V_{ICM}, V_{OD}, and V_{OCM} specifications for BLVDS. These specifications depend on the system topology.

Table 1–34. Transceiver Specifications for Arria II GX Devices *(Note 1)* (Part 4 of 7)

Symbol/ Description	Condition	I3			C4			C5 and I5			C6			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Minimum peak-to-peak differential input voltage V_{ID} (diff p-p)	—	100	—	—	100	—	—	100	—	—	100	—	—	mV
V_{ICM}	V_{ICM} = 0.82 V setting	—	820	—	—	820	—	—	820	—	—	820	—	mV
	V_{ICM} =1.1 V setting *(7)*	—	1100	—	—	1100	—	—	1100	—	—	1100	—	mV
Differential on-chip termination resistors	100–Ω setting	—	100	—	—	100	—	—	100	—	—	100	—	Ω
Return loss differential mode	PCIe				50 MHz to 1.25 GHz: –10dB									
	XAUI				100 MHz to 2.5 GHz: –10dB									
Return loss common mode	PCIe				50 MHz to 1.25 GHz: –6dB									
	XAUI				100 MHz to 2.5 GHz: –6dB									
Programmable PPM detector *(8)*	—	± 62.5, 100, 125, 200, 250, 300, 500, 1000												ppm
Run length	—	—	80	—	—	80	—	—	80	—	—	80	—	UI
Programmable equalization	—	—	—	7	—	—	7	—	—	7	—	—	7	dB
Signal detect/loss threshold	PCIe Mode	65	—	175	65	—	175	65	—	175	65	—	175	mV
CDR LTR time *(9)*	—	—	—	75	—	—	75	—	—	75	—	—	75	µs
CDR minimum T1b *(10)*	—	15	—	—	15	—		15	—	—	15	—	—	µs

Table 1–34. Transceiver Specifications for Arria II GX Devices *(Note 1)* (Part 6 of 7)

Symbol/ Description	Condition	I3			C4			C5 and I5			C6			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Intra-differential pair skew	—	—	—	15	—	—	15	—	—	15	—	—	15	ps
Intra-transceiver block skew	PCIe ×4	—	—	120	—	—	120	—	—	120	—	—	120	ps
Inter-transceiver block skew	PCIe ×8	—	—	300	—	—	300	—	—	300	—	—	300	ps
CMU PLL0 and CMU PLL1														
CMU PLL lock time from `CMUPLL_reset` deassertion	—	—	—	100	—	—	100	—	—	100	—	—	100	µs
PLD-Transceiver Interface														
Interface speed	—	25	—	320	25	—	240	25	—	240	25	—	200	MHz

Table 1–35. Transceiver Specifications for Arria II GZ Devices (Part 5 of 5)

Symbol/ Description	Conditions	–C3 and –I3 *(1)*			–C4 and –I4			Unit
		Min	Typ	Max	Min	Typ	Max	
-3 dB Bandwidth	PCIe Gen1	2.5 - 3.5						MHz
	PCIe Gen2	6 - 8						MHz
	(OIF) CEI PHY at 4.976 Gbps	7 - 11						MHz
	(OIF) CEI PHY at 6.375 Gbps	5 - 10						MHz
	XAUI	2 - 4						MHz
	SRIO 1.25 Gbps	3 - 5.5						MHz
	SRIO 2.5 Gbps	3 - 5.5						MHz
	SRIO 3.125 Gbps	2 - 4						MHz
	GIGE	2.5 - 4.5						MHz
	SONET OC12	1.5 - 2.5						MHz
	SONET OC48	3.5 - 6						MHz
Transceiver-FPGA Fabric Interface								
Interface speed	—	25	—	325	25	—	250	MHz
Digital reset pulse width	—	Minimum is two parallel clock cycles						—

Notes to Table 1–35:

(1) The 3x speed grade is the fastest speed grade offered in the following Arria II GZ devices: EP2AGZ225, EP2AGZ300, and EP2AGZ350.

(2) The rise and fall time transition is specified from 20% to 80%.

(3) To calculate the REFCLK rms phase jitter requirement at reference clock frequencies other than 100 MHz, use the following formula: REFCLK rms phase jitter at f (MHz) = REFCLK rms phase jitter at 100 MHz * 100/f.

(4) The minimum `reconfig_clk` frequency is 2.5 MHz if the transceiver channel is configured in **Transmitter only** mode. The minimum `reconfig_clk` frequency is 37.5 MHz if the transceiver channel is configured in **Receiver only** or **Receiver and Transmitter** mode.

(5) If your design uses more than one dynamic reconfiguration controller (`altgx_reconfig`) instances to control the transceiver (`altgx`) channels physically located on the same side of the device AND if you use different `reconfig_clk` sources for these `altgx_reconfig` instances, the delta time between any two of these `reconfig_clk` sources becoming stable must not exceed the maximum specification listed.

(6) The device cannot tolerate prolonged operation at this absolute maximum.

(7) You must use the 1.1-V RX V_{ICM} setting if the input serial data standard is LVDS.

(8) The differential eye opening specification at the receiver input pins assumes that Receiver Equalization is disabled. If you enable Receiver Equalization, the receiver circuitry can tolerate a lower minimum eye opening, depending on the equalization level. Use H-Spice simulation to derive the minimum eye opening requirement with Receiver Equalization enabled.

(9) The rate matcher supports only up to ± 300 ppm.

(10) Time taken to `rx_pll_locked` goes high from `rx_analogreset` de-assertion. Refer to Figure 1–1 on page 1–33.

(11) Time for which the CDR must be kept in lock-to-reference mode after `rx_pll_locked` goes high and before `rx_locktodata` is asserted in manual mode. Refer to Figure 1–1 on page 1–33.

(12) Time taken to recover valid data after the `rx_locktodata` signal is asserted in manual mode. Refer to Figure 1–1 on page 1–33.

(13) Time taken to recover valid data after the `rx_freqlocked` signal goes high in automatic mode. Refer to Figure 1–2 on page 1–33.

(14) A GPLL may be required to meet the PMA-FPGA fabric interface timing above certain data rates. For more information, refer to the *Transceiver Clocking for Arria II Devices* chapter.

(15) The Quartus II software automatically selects the appropriate slew rate depending on the configured data rate or functional mode.

(16) To support data rates lower than the minimum specification through oversampling, use the CDR in LTR mode only.

Table 1–39. Transmitter Pre-Emphasis Levels for Arria II GZ Devices (Part 2 of 2)

Pre-Emphasis 1st Post-Tap Setting	V_{OD} Setting							
	0	1	2	3	4	5	6	7
29	N/A	N/A	N/A	12.5	9.6	7.7	6.3	4.3
30	N/A	N/A	N/A	N/A	11.4	9	7.4	N/A
31	N/A	N/A	N/A	N/A	12.9	10	8.2	N/A

Table 1–40 lists the transceiver jitter specifications for all supported protocols for Arria II GX devices.

Table 1–40. Transceiver Block Jitter Specifications for Arria II GX Devices *(Note 1)* (Part 1 of 10)

Symbol/ Description	Conditions	I3			C4			C5, I5			C6			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
SONET/SDH Transmit Jitter Generation *(2)*														
Peak-to-peak jitter at 622.08 Mbps	Pattern = PRBS15	—	—	0.1	—	—	0.1	—	—	0.1	—	—	0.1	UI
RMS jitter at 622.08 Mbps	Pattern = PRBS15	—	—	0.01	—	—	0.01	—	—	0.01	—	—	0.01	UI
Peak-to-peak jitter at 2488.32 Mbps	Pattern = PRBS15	—	—	0.1	—	—	0.1	—	—	0.1	—	—	0.1	UI
RMS jitter at 2488.32 Mbps	Pattern = PRBS15	—	—	0.01	—	—	0.01	—	—	0.01	—	—	0.01	UI
SONET/SDH Receiver Jitter Tolerance *(2)*														
Jitter tolerance at 622.08 Mbps	Jitter frequency = 0.03 KHz Pattern = PRBS15	> 15			> 15			> 15			> 15			UI
	Jitter frequency = 25 KHZ Pattern = PRBS15	> 1.5			> 1.5			> 1.5			> 1.5			UI
	Jitter frequency = 250 KHz Pattern = PRBS15	> 0.15			> 0.15			> 0.15			> 0.15			UI

Table 1–40. Transceiver Block Jitter Specifications for Arria II GX Devices *(Note 1)* (Part 6 of 10)

Symbol/ Description	Conditions	I3			C4			C5, I5			C6			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Sinusoidal jitter tolerance (peak-to-peak)	Jitter frequency = 20 KHz Data rate = 1.485 Gbps (HD) Pattern = 75% color bar		> 1			> 1			> 1			> 1		UI
	Jitter frequency = 100 KHz Data rate = 1.485 Gbps (HD) Pattern = 75% color bar		> 0.2			> 0.2			> 0.2			> 0.2		UI
	Jitter frequency = 148.5 MHz Data rate = 1.485 Gbps (HD) Pattern =75% color bar		> 0.2			> 0.2			> 0.2			> 0.2		UI
SATA Transmit Jitter Generation *(10)*														
Total jitter at 1.5 Gbps (G1)	Compliance pattern	—	—	0.55	—	—	0.55	—	—	0.55	—	—	0.55	UI
Deterministic jitter at 1.5 Gbps (G1)	Compliance pattern	—	—	0.35	—	—	0.35	—	—	0.35	—	—	0.35	UI
Total jitter at 3.0 Gbps (G2)	Compliance pattern	—	—	0.55	—	—	0.55	—	—	0.55	—	—	0.55	UI
Deterministic jitter at 3.0 Gbps (G2)	Compliance pattern	—	—	0.35	—	—	0.35	—	—	0.35	—	—	0.35	UI
Total jitter at 6.0 Gbps (G3)	Compliance pattern	—	—	0.52	—	—	—	—	—	—	—	—	—	UI
Random jitter at 6.0 Gbps (G3)	Compliance pattern	—	—	0.18	—	—	—	—	—	—	—	—	—	UI
SATA Receiver Jitter Tolerance *(10)*														
Total jitter tolerance at 1.5 Gbps (G1)	Compliance pattern		> 0.65			> 0.65			> 0.65			> 0.65		UI
Deterministic jitter tolerance at 1.5 Gbps (G1)	Compliance pattern		> 0.35			> 0.35			> 0.35			> 0.35		UI
SSC modulation frequency at 1.5 Gbps (G1)	Compliance pattern		33			33			33			33		kHz

Table 1–41. Transceiver Block Jitter Specifications for Arria II GZ Devices *(Note 1)*, *(2)* (Part 3 of 7)

Symbol/ Description	Conditions	–C3 and –I3			–C4 and –I4			Unit
		Min	Typ	Max	Min	Typ	Max	
Peak-to-peak jitter	Jitter frequency = 22.1 KHz		> 8.5			> 8.5		UI
Peak-to-peak jitter	Jitter frequency = 1.875 MHz		> 0.1			> 0.1		UI
Peak-to-peak jitter	Jitter frequency = 20 MHz		> 0.1			> 0.1		UI
PCIe Transmit Jitter Generation *(8)*								
Total jitter at 2.5 Gbps (Gen1)—x1, x4, and x8	Compliance pattern	—	—	0.25	—	—	0.25	UI
Total jitter at 5 Gbps (Gen2)—x1, x4, and x8	Compliance pattern	—	—	0.25	—	—	—	UI
PCIe Receiver Jitter Tolerance *(8)*								
Total jitter at 2.5 Gbps (Gen1)	Compliance pattern		> 0.6			> 0.6		UI
Total jitter at 5 Gbps (Gen2)	Compliance pattern		Not supported			Not supported		UI
PCIe (Gen 1) Electrical Idle Detect Threshold								
$V_{RX-IDLE-DETDIFFp-p}$ *(9)*	Compliance pattern	65	—	175	65	—	175	UI
SRIO Transmit Jitter Generation *(10)*								
Deterministic jitter (peak-to-peak)	Data rate = 1.25, 2.5, 3.125 Gbps Pattern = CJPAT	—	—	0.17	—	—	0.17	UI
Total jitter (peak-to-peak)	Data rate = 1.25, 2.5, 3.125 Gbps Pattern = CJPAT	—	—	0.35	—	—	0.35	UI
SRIO Receiver Jitter Tolerance *(10)*								
Deterministic jitter tolerance (peak-to-peak)	Data rate = 1.25, 2.5, 3.125 Gbps Pattern = CJPAT		> 0.37			> 0.37		UI
Combined deterministic and random jitter tolerance (peak-to-peak)	Data rate = 1.25, 2.5, 3.125 Gbps Pattern = CJPAT		> 0.55			> 0.55		UI
Sinusoidal jitter tolerance (peak-to-peak)	Jitter frequency = 22.1 KHz Data rate = 1.25, 2.5, 3.125 Gbps Pattern = CJPAT		> 8.5			> 8.5		UI
	Jitter frequency = 1.875 MHz Data rate = 1.25, 2.5, 3.125 Gbps Pattern = CJPAT		> 0.1			> 0.1		UI
	Jitter frequency = 20 MHz Data rate = 1.25, 2.5, 3.125 Gbps Pattern = CJPAT		> 0.1			> 0.1		UI
GIGE Transmit Jitter Generation *(11)*								
Deterministic jitter (peak-to-peak)	Pattern = CRPAT	—	—	0.14	—	—	0.14	UI
Total jitter (peak-to-peak)	Pattern = CRPAT	—	—	0.279	—	—	0.279	UI

Table 1–41. Transceiver Block Jitter Specifications for Arria II GZ Devices *(Note 1)*, *(2)* (Part 5 of 7)

Symbol/ Description	Conditions	–C3 and –I3			–C4 and –I4			Unit
		Min	Typ	Max	Min	Typ	Max	
Sinusoidal jitter tolerance (peak-to-peak)	Jitter Frequency = 38.2 KHz Data rate = 6.375 Gbps Pattern = PRBS31 BER = 10^{-12}	> 0.5			—	—	—	UI
	Jitter Frequency = 3.82 MHz Data rate = 6.375 Gbps Pattern = PRBS31 BER = 10^{-12}	> 0.05			—	—	—	UI
	Jitter Frequency = 20 MHz Data rate = 6.375 Gbps Pattern = PRBS31 BER = 10^{-12}	> 0.05			—	—	—	UI
SDI Transmitter Jitter Generation *(12)*								
Alignment jitter (peak-to-peak)	Data rate = 1.485 Gbps (HD) Pattern = color bar Low-frequency roll-off = 100 KHz	0.2	—	—	0.2	—	—	UI
	Data rate = 2.97 Gbps (3G) Pattern = color bar Low-frequency roll-off = 100 KHz	0.3	—	—	0.3	—	—	UI
SDI Receiver Jitter Tolerance *(12)*								
Sinusoidal jitter tolerance (peak-to-peak)	Jitter frequency = 15 KHz Data rate = 2.97 Gbps (3G) Pattern = single line scramble color bar	> 2			> 2			UI
	Jitter frequency = 100 KHz Data rate = 2.97 Gbps (3G) Pattern = single line scramble color bar	> 0.3			> 0.3			UI
	Jitter frequency = 148.5 MHz Data rate = 2.97 Gbps (3G) Pattern = single line scramble color bar	> 0.3			> 0.3			UI
Sinusoidal jitter tolerance (peak-to-peak)	Jitter frequency = 20 KHz Data rate = 1.485 Gbps (HD) pattern = 75% color bar	> 1			> 1			UI
	Jitter frequency = 100 KHz Data rate = 1.485 Gbps (HD) Pattern = 75% color bar	> 0.2			> 0.2			UI
	Jitter frequency = 148.5 MHz Data rate = 1.485 Gbps (HD) Pattern = 75% color bar	> 0.2			> 0.2			UI
SAS Transmit Jitter Generation *(13)*								
Total jitter at 1.5 Gbps (G1)	Pattern = CJPAT	—	—	0.55	—	—	0.55	UI
Deterministic jitter at 1.5 Gbps (G1)	Pattern = CJPAT	—	—	0.35	—	—	0.35	UI
Total jitter at 3.0 Gbps (G2)	Pattern = CJPAT	—	—	0.55	—	—	0.55	UI

Table 1–47. DSP Block Performance Specifications for Arria II GZ Devices *(Note 1)* (Part 2 of 2)

Mode	Resources Used	Performance		Unit
	Number of Multipliers	–3	–4	
Double mode	1	440	380	MHz

Notes to Table 1–47:

(1) Maximum is for fully pipelined block with **Round** and **Saturation** disabled.

(2) Maximum for loopback input registers disabled, **Round** and **Saturation** disabled, and pipeline and output registers enabled.

Embedded Memory Block Specifications

Table 1–48 lists the embedded memory block specifications for Arria II GX devices.

Table 1–48. Embedded Memory Block Performance Specifications for Arria II GX Devices

Memory	Mode	Resources Used		Performance				Unit
		ALUTs	Embedded Memory	I3	C4	C5,I5	C6	
Memory Logic Array Block (MLAB)	Single port 64 × 10	0	1	450	500	450	378	MHz
	Simple dual-port 32 × 20 single clock	0	1	270	500	450	378	MHz
	Simple dual-port 64 × 10 single clock	0	1	428	500	450	378	MHz
M9K Block	Single-port 256 × 36	0	1	360	400	360	310	MHz
	Single-port 256 × 36, with the **read-during-write** option set to **Old Data**	0	1	250	280	250	210	MHz
	Simple dual-port 256 × 36 single CLK	0	1	360	400	360	310	MHz
	Single-port 256 × 36 single CLK, with the **read-during-write** option set to **Old Data**	0	1	250	280	250	210	MHz
	True dual port 512 × 18 single CLK	0	1	360	400	360	310	MHz
	True dual-port 512 × 18 single CLK, with the **read-during-write** option set to **Old Data**	0	1	250	280	250	210	MHz
	Min Pulse Width (clock high time)	—	—	900	850	950	1130	ps
	Min Pulse Width (clock low time)	—	—	730	690	770	920	ps

Periphery Performance

This section describes periphery performance, including high-speed I/O, external memory interface, and IOE programmable delay.

I/O performance supports several system interfaces, for example the high-speed I/O interface, external memory interface, and the PCI/PCI-X bus interface. I/O using SSTL-18 Class I termination standard can achieve up to the stated DDR2 SDRAM interfacing speed with typical DDR2 SDRAM memory interface setup. I/O using general purpose I/O (GPIO) standards such as 3.0, 2.5, 1.8, or 1.5 LVTTL/LVCMOS are capable of typical 200 MHz interfacing frequency with 10pF load.

☞ Actual achievable frequency depends on design- and system-specific factors. You should perform HSPICE/IBIS simulations based on your specific design and system setup to determine the maximum achievable frequency in your system.

High-Speed I/O Specification

Table 1–53 lists the high-speed I/O timing for Arria II GX devices.

Table 1–53. High-Speed I/O Specifications for Arria II GX Devices (Part 1 of 4)

Symbol	Conditions	I3		C4		C5,I5		C6		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Clock										
f_{HSCLK_IN} (input clock frequency)–Row I/O	Clock boost factor, W = 1 to 40 *(1)*	5	670	5	670	5	622	5	500	MHz
f_{HSCLK_IN} (input clock frequency)–Column I/O	Clock boost factor, W = 1 to 40 *(1)*	5	500	5	500	5	472.5	5	472.5	MHz
f_{HSCLK_OUT} (output clock frequency)–Row I/O	—	5	670	5	670	5	622	5	500	MHz
f_{HSCLK_OUT} (output clock frequency)–Column I/O	—	5	500	5	500	5	472.5	5	472.5	MHz

Table 1–53. High-Speed I/O Specifications for Arria II GX Devices (Part 2 of 4)

Symbol	Conditions	I3		C4		C5,I5		C6		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Transmitter										
f_{HSDR_TX} (true LVDS output data rate)	SERDES factor, J = 3 to 10 (using dedicated SERDES)	150	1250 *(2)*	150	1250 *(2)*	150	1050 *(2)*	150	840	Mbps
	SERDES factor, J = 4 to 10 (using logic elements as SERDES)	*(3)*	945	*(3)*	945	*(3)*	840	*(3)*	740	Mbps
	SERDES factor, J = 2 (using DDR registers) and J = 1 (using SDR register)	*(3)*	*(3)*	*(3)*	*(3)*	*(3)*	*(3)*	*(3)*	*(3)*	Mbps
$f_{HSDR\_TX\_E3R}$ (emulated LVDS_E_3R output data rate) *(7)*	SERDES factor, J = 4 to 10	*(3)*	945	*(3)*	945	*(3)*	840	*(3)*	740	Mbps

Table 1–54. High-Speed I/O Specifications for Arria II GZ Devices *(Note 1), (2), (10)* (Part 2 of 3)

Symbol	Conditions	C3, I3			C4, I4			Unit
		Min	Typ	Max	Min	Typ	Max	
f_{HSCLK_OUT} (output clock frequency)	—	5	—	717 *(7)*	5	—	717 *(7)*	MHz
Transmitter								
f_{HSDR} (true LVDS output data rate)	SERDES factor, J = 3 to 10 (using dedicated SERDES) *(8)*	*(4)*	—	1250	*(4)*	—	1250	Mbps
	SERDES factor J = 2, (using DDR registers)	*(4)*	—	*(5)*	*(4)*	—	*(5)*	Mbps
	SERDES factor J = 1, (uses an SDR register)	*(4)*	—	*(5)*	*(4)*	—	*(5)*	Mbps
f_{HSDR} (emulated LVDS_E_3R output data rate) *(5)*	SERDES factor J = 4 to 10	*(4)*	—	1152	*(4)*	—	800	Mbps
f_{HSDR} (emulated LVDS_E_1R output data rate)		*(4)*	—	200	*(4)*	—	200	Mbps
$t_{x\ Jitter}$	Total jitter for data rate, 600 Mbps to 1.6 Gbps	—	—	160	—	—	160	ps
	Total jitter for data rate, < 600 Mbps	—	—	0.1	—	—	0.1	UI
$t_{x\ Jitter}$ - emulated differential I/O standards with three external output resistor network	Total jitter for data rate, 600 Mbps to 1.25 Gbps	—	—	300	—	—	325	ps
	Total jitter for data rate < 600 Mbps	—	—	0.2	—	—	0.25	UI
$t_{x\ Jitter}$ - emulated differential I/O standards with one external output resistor network	—	—	—	0.15	—	—	0.15	UI
t_{DUTY}	TX output clock duty cycle for both True and emulated differential I/O standards	45	50	55	45	50	55	%

Table 1–54. High-Speed I/O Specifications for Arria II GZ Devices *(Note 1), (2), (10)* (Part 3 of 3)

Symbol	Conditions	C3, I3			C4, I4			Unit
		Min	Typ	Max	Min	Typ	Max	
t_{RISE} & t_{FALL}	True differential I/O standards	—	—	200	—	—	200	ps
	Emulated differential I/O standards with three external output resistor networks	—	—	250	—	—	300	ps
	Emulated differential I/O standards with one external output resistor	—	—	500	—	—	500	ps
TCCS	True LVDS	—	—	100	—	—	100	ps
	Emulated LVDS_E_3R	—	—	250	—	—	250	ps
Receiver								
True differential I/O standards - $f_{HSDRDPA}$ (data rate)	SERDES factor J = 3 to 10	150	—	1250	150	—	1250	Mbps
f_{HSDR} (data rate)	SERDES factor J = 3 to 10	*(4)*	—	*(6)*	*(4)*	—	*(6)*	Mbps
	SERDES factor J = 2, uses DDR registers	*(4)*	—	*(5)*	*(4)*	—	*(5)*	Mbps
	SERDES factor J = 1, uses an SDR register	*(4)*	—	*(5)*	*(4)*	—	*(5)*	Mbps
DPA run length	DPA mode	—	—	10000	—	—	10000	UI
Soft-CDR PPM tolerance	Soft-CDR mode	—	—	300	—	—	300	± PPM
Sampling Window (SW)	Non-DPA mode	—	—	300	—	—	300	ps

Notes to Table 1–54:

(1) When J = 3 to 10, use the SERDES block.

(2) When J = 1 or 2, bypass the SERDES block.

(3) Clock Boost Factor (W) is the ratio between input data rate to the input clock rate.

(4) The minimum specification depends on the clock source (for example, the PLL and clock pin) and the clock routing resource (global, regional, or local) that you use. The I/O differential buffer and input register do not have a minimum toggle rate.

(5) You must calculate the leftover timing margin in the receiver by performing link timing closure analysis. You must consider the board skew margin, transmitter channel-to-channel skew, and receiver sampling margin to determine leftover timing margin.

(6) You can estimate the achievable maximum data rate for non-DPA mode by performing link timing closure analysis. You must consider the board skew margin, transmitter delay margin, and the receiver sampling margin to determine the maximum data rate supported.

(7) This is achieved by using the LVDS and DPA clock network.

(8) If the receiver with DPA enabled and transmitter are using shared PLLs, the minimum data rate is 150 Mbps.

(9) This only applies to DPA and soft-CDR modes.

(10) This only applies to LVDS source synchronous mode.

Table 1–55 lists DPA lock time specifications for Arria II GX and GZ devices.

Table 1–55. DPA Lock Time Specifications for Arria II Devices *(Note 1)*, *(2)*, *(3)*

Standard	Training Pattern	Number of Data Transitions in One Repetition of the Training Pattern	Number of Repetitions per 256 Data Transitions *(4)*	Maximum
SPI-4	00000000001111111111	2	128	640 data transitions
Parallel Rapid I/O	00001111	2	128	640 data transitions
	10010000	4	64	640 data transitions
Miscellaneous	10101010	8	32	640 data transitions
	01010101	8	32	640 data transitions

Notes to Table 1–55:

(1) The DPA lock time is for one channel.
(2) One data transition is defined as a 0-to-1 or 1-to-0 transition.
(3) The DPA lock time stated in the table applies to both commercial and industrial grade.
(4) This is the number of repetitions for the stated training pattern to achieve the 256 data transitions.

Figure 1–5 shows the LVDS soft-CDR/DPA sinusoidal jitter tolerance specification for Arria II GZ devices at a data rate less than 1.25 Gbps and all the Arria II GX devices.

Figure 1–5. LVDS Soft-CDR/DPA Sinusoidal Jitter Tolerance Specification for All Arria II GX Devices and for Arria II GZ Devices at a Data Rate less than 1.25 Gbps

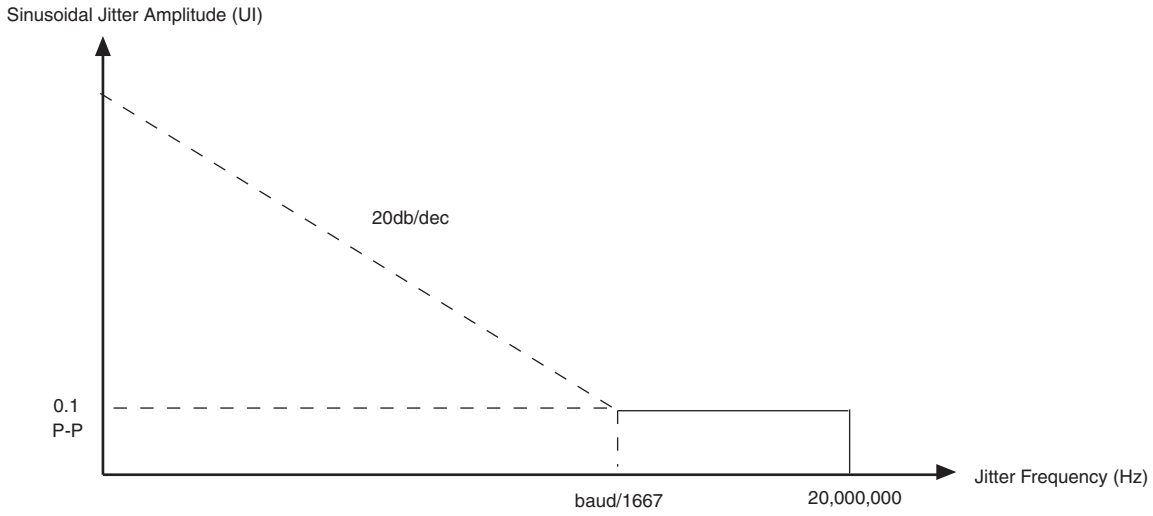


Table 1–60 lists the DQS phase shift error for Arria II GX devices.

Table 1–60. DQS Phase Shift Error Specification for DLL-Delayed Clock (t_{DQS_PSERR}) for Arria II GX Devices *(Note 1)*

Number of DQS Delay Buffer	C4	I3, C5, I5	C6	Unit
1	26	30	36	ps
2	52	60	72	ps
3	78	90	108	ps
4	104	120	144	ps

Note to Table 1–60:

(1) This error specification is the absolute maximum and minimum error. For example, skew on three DQS delay buffers in a C4 speed grade is ± 78 ps or ± 39 ps.

Table 1–61 lists the DQS phase shift error for Arria II GZ devices.

Table 1–61. DQS Phase Shift Error Specification for DLL-Delayed Clock (t_{DQS_PSERR}) for Arria II GZ Devices *(Note 1)*

Number of DQS Delay Buffer	–3	–4	Unit
1	28	30	ps
2	56	60	ps
3	84	90	ps
4	112	120	ps

Note to Table 1–61:

(1) This error specification is the absolute maximum and minimum error. For example, skew on three DQS delay buffers in a 3 speed grade is ± 84 ps or ± 42 ps.

Table 1–62 lists the memory output clock jitter specifications for Arria II GX devices.

Table 1–62. Memory Output Clock Jitter Specification for Arria II GX Devices *(Note 1)*, *(2)*, *(3)*

Parameter	Clock Network	Symbol	–4		–5		–6		Unit
			Min	Max	Min	Max	Min	Max	
Clock period jitter	Global	$t_{JIT(per)}$	-100	100	-125	125	-125	125	ps
Cycle-to-cycle period jitter	Global	$t_{JIT(cc)}$	-200	200	-250	250	-250	250	ps
Duty cycle jitter	Global	$t_{JIT(duty)}$	-100	100	-125	125	-125	125	ps

Notes to Table 1–62:

(1) The memory output clock jitter measurements are for 200 consecutive clock cycles, as specified in the JEDEC DDR2/DDR3 SDRAM standard.

(2) The clock jitter specification applies to memory output clock pins generated using DDIO circuits clocked by a PLL output routed on a global clock network.

(3) The memory output clock jitter stated in Table 1–62 is applicable when an input jitter of 30 ps is applied.

Table 1–68. Glossary (Part 3 of 4)

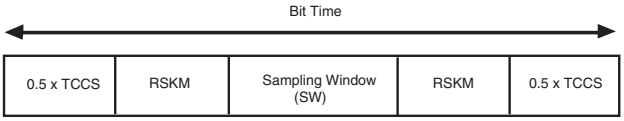
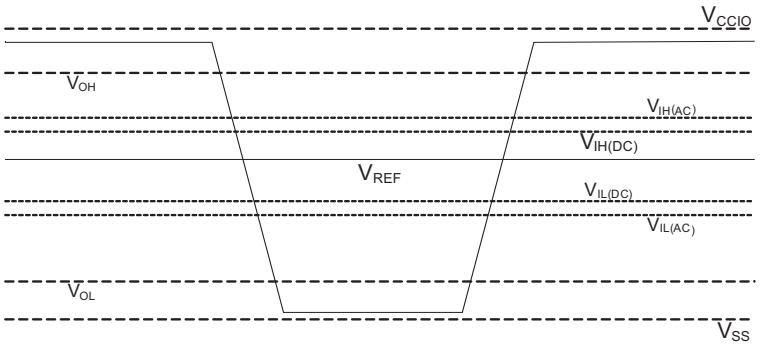
Letter	Subject	Definitions
S	**SW (sampling window)**	The period of time during which the data must be valid in order to capture it correctly. The setup and hold times determine the ideal strobe position within the sampling window: *Timing Diagram* 
	Single-ended Voltage Referenced I/O Standard	The JEDEC standard for SSTL and HSTL I/O standards define both the AC and DC input signal values. The AC values indicate the voltage levels at which the receiver must meet its timing specifications. The DC values indicate the voltage levels at which the final logic state of the receiver is unambiguously defined. After the receiver input has crossed the AC value, the receiver changes to the new logic state. The new logic state is then maintained as long as the input stays beyond the AC threshold. This approach is intended to provide predictable receiver timing in the presence of input waveform ringing: *Single-Ended Voltage Referenced I/O Standard* 
T	t_C	High-speed receiver and transmitter input and output clock period.
	TCCS (channel-to-channel-skew)	The timing difference between the fastest and slowest output edges, including t_{CO} variation and clock skew, across channels driven by the same PLL. The clock is included in the TCCS measurement (refer to the *Timing Diagram* figure under **S** in this table).
	t_{DUTY}	High-speed I/O block: Duty cycle on the high-speed transmitter output clock.
		Timing Unit Interval (TUI) The timing budget allowed for skew, propagation delays, and data sampling window. (TUI = 1/(Receiver Input Clock Frequency Multiplication Factor) = t_C/w)
	t_{FALL}	Signal high-to-low transition time (80-20%)
	t_{INCCJ}	Cycle-to-cycle jitter tolerance on the PLL clock input.
	t_{OUTPJ_IO}	Period jitter on the general purpose I/O driven by a PLL.
	t_{OUTPJ_DC}	Period jitter on the dedicated clock output driven by a PLL.
	t_{RISE}	Signal low-to-high transition time (20-80%).

Table 1–69. Document Revision History (Part 2 of 2)

Date	Version	Changes
December 2010	4.0	■ Added Arria II GZ information. ■ Added Table 1–61 with Arria II GX information. ■ Updated Table 1–1, Table 1–2, Table 1–5, Table 1–6, Table 1–7, Table 1–11, Table 1–35, Table 1–37, Table 1–40, Table 1–42, Table 1–44, Table 1–45, Table 1–57, Table 1–61, and Table 1–63. ■ Updated Figure 1–5. ■ Updated for the Quartus II version 10.0 release. ■ Updated the first paragraph for searchability. ■ Minor text edits.
July 2010	3.0	■ Updated Table 1–1, Table 1–4, Table 1–16, Table 1–19, Table 1–21, Table 1–23, Table 1–25, Table 1–26, Table 1–30, and Table 1–35 ■ Added Table 1–27 and Table 1–29. ■ Added I3 speed grade information to Table 1–19, Table 1–21, Table 1–22, Table 1–24, Table 1–25, Table 1–30, Table 1–32, Table 1–33, Table 1–34, and Table 1–35. ■ Updated the "Operating Conditions" section. ■ Removed "Preliminary" from Table 1–19, Table 1–21, Table 1–22, Table 1–23, Table 1–24, Table 1–25, Table 1–26, Table 1–28, Table 1–30, Table 1–32, Table 1–33, Table 1–34, and Figure 1–4. ■ Minor text edits.
March 2010	2.3	Updated for the Quartus II version 9.1 SP2 release: ■ Updated Table 1–3, Table 1–7, Table 1–19, Table 1–21, Table 1–22, Table 1–24, Table 1–25 and Table 1–33. ■ Updated "Recommended Operating Conditions" section. ■ Minor text edits.
February 2010	2.2	Updated Table 1–19.
February 2010	2.1	Updated for Arria II GX v9.1 SP1 release: ■ Updated Table 1–19, Table 1–23, Table 1–28, Table 1–30, and Table 1–33. ■ Added Figure 1–5. ■ Minor text edits.
November 2009	2.0	Updated for Arria II GX v9.1 release: ■ Updated Table 1–1, Table 1–4, Table 1–13, Table 1–14, Table 1–19, Table 1–15, Table 1–22, Table 1–24, and Table 1–28. ■ Added Table 1–6 and Table 1–33. ■ Added "Bus Hold" on page 1–5. ■ Added "IOE Programmable Delay" section. ■ Minor text edit.
June 2009	1.2	■ Updated Table 1–1, Table 1–3, Table 1–7, Table 1–8, Table 1–18, Table 1–23, Table 1–25, Table 1–26, Table 1–29, Table 1–30, Table 1–31, Table 1–32, and Table 1–33. ■ Added Table 1–32. ■ Updated Equation 1–1.
March 2009	1.1	Added "I/O Timing" section.
February 2009	1.0	Initial release.