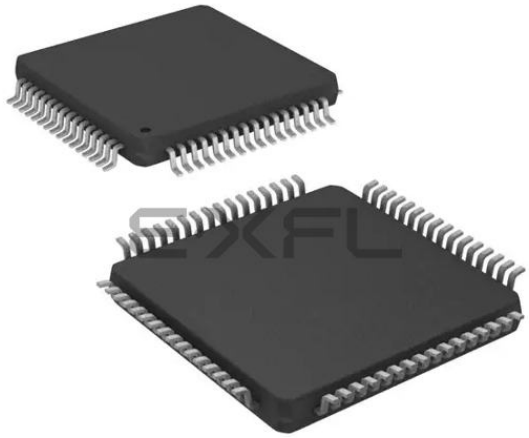


Welcome to E-XFL.COM

Understanding Embedded - CPLDs (Complex Programmable Logic Devices)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details	
Product Status	Active
Programmable Type	In System Programmable (min 10K program/erase cycles)
Delay Time tpd(1) Max	7.5 ns
Voltage Supply - Internal	3V ~ 3.6V
Number of Logic Elements/Blocks	2
Number of Macrocells	36
Number of Gates	800
Number of I/O	36
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-VQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc9536xl-7vqg64i

XC9536XL High Performance CPLD

DS058 (v1.9) April 3, 2007

Product Specification

Features

- 5 ns pin-to-pin logic delays
- System frequency up to 178 MHz
- 36 macrocells with 800 usable gates
- Available in small footprint packages
  - 44-pin PLCC (34 user I/O pins)
  - 44-pin VQFP (34 user I/O pins)
  - 48-pin CSP (36 user I/O pins)
  - 64-pin VQFP (36 user I/O pins)
  - Pb-free available for all packages
- Optimized for high-performance 3.3V systems
  - Low power operation
  - 5V tolerant I/O pins accept 5 V, 3.3V, and 2.5V signals
  - 3.3V or 2.5V output capability
  - Advanced 0.35 micron feature size CMOS Fast FLASH™ technology
- Advanced system features
  - In-system programmable
  - Superior pin-locking and routability with Fast CONNECT™ II switch matrix
  - Extra wide 54-input Function Blocks
  - Up to 90 product-terms per macrocell with individual product-term allocation
  - Local clock inversion with three global and one product-term clocks
  - Individual output enable per output pin
  - Input hysteresis on all user and boundary-scan pin inputs
  - Bus-hold circuitry on all user pin inputs
  - Full IEEE Standard 1149.1 boundary-scan (JTAG)
- Fast concurrent programming
- Slew rate control on individual outputs
- Enhanced data security features
- Excellent quality and reliability
  - Endurance exceeding 10,000 program/erase cycles
  - 20 year data retention
  - ESD protection exceeding 2,000V
- Pin-compatible with 5V-core XC9536 device in the 44-pin PLCC package and the 48-pin CSP package

WARNING: Programming temperature range of T_A = 0° C to +70° C

Description

The XC9536XL is a 3.3V CPLD targeted for high-performance, low-voltage applications in leading-edge communications and computing systems. It is comprised of two 54V18 Function Blocks, providing 800 usable gates with propagation delays of 5 ns. See Figure 2 for architecture overview.

Power Estimation

Power dissipation in CPLDs can vary substantially depending on the system frequency, design application and output loading. To help reduce power dissipation, each macrocell in a XC9500XL device may be configured for low-power mode (from the default high-performance mode). In addition, unused product-terms and macrocells are automatically deactivated by the software to further conserve power.

For a general estimate of I_{CC}, the following equation may be used:

$$I_{CC}(mA) = MC_{HS}(0.175*PT_{HS} + 0.345) + MC_{LP}(0.052*PT_{LP} + 0.272) + 0.04 * MC_{TOG}(MC_{HS} + MC_{LP})* f$$

where:

MC_{HS} = # macrocells in high-speed configuration

PT_{HS} = average number of high-speed product terms per macrocell

MC_{LP} = # macrocells in low power configuration

PT_{LP} = average number of low power product terms per macrocell

f = maximum clock frequency

MCTOG = average % of flip-flops toggling per clock (~12%)

This calculation was derived from laboratory measurements of an XC9500XL part filled with 16-bit counters and allowing a single output (the LSB) to be enabled. The actual I_{CC} value varies with the design application and should be verified during normal system operation. Figure 1 shows the above estimation in a graphical form. For a more detailed discussion of power consumption in this device, see Xilinx

application note **XAPP114, "Understanding XC9500XL CPLD Power."**

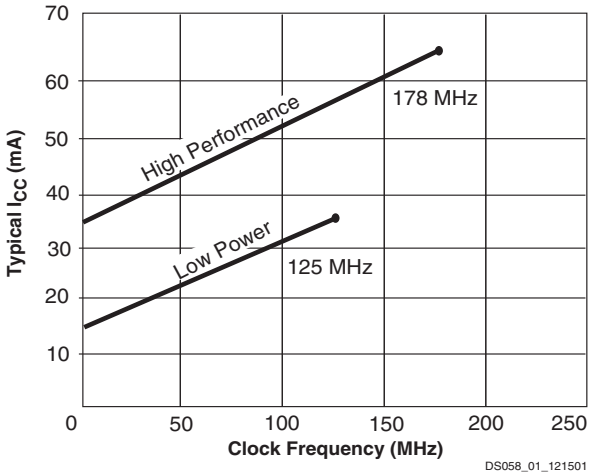


Figure 1: **Typical I_{CC} vs. Frequency for XC9536XL**

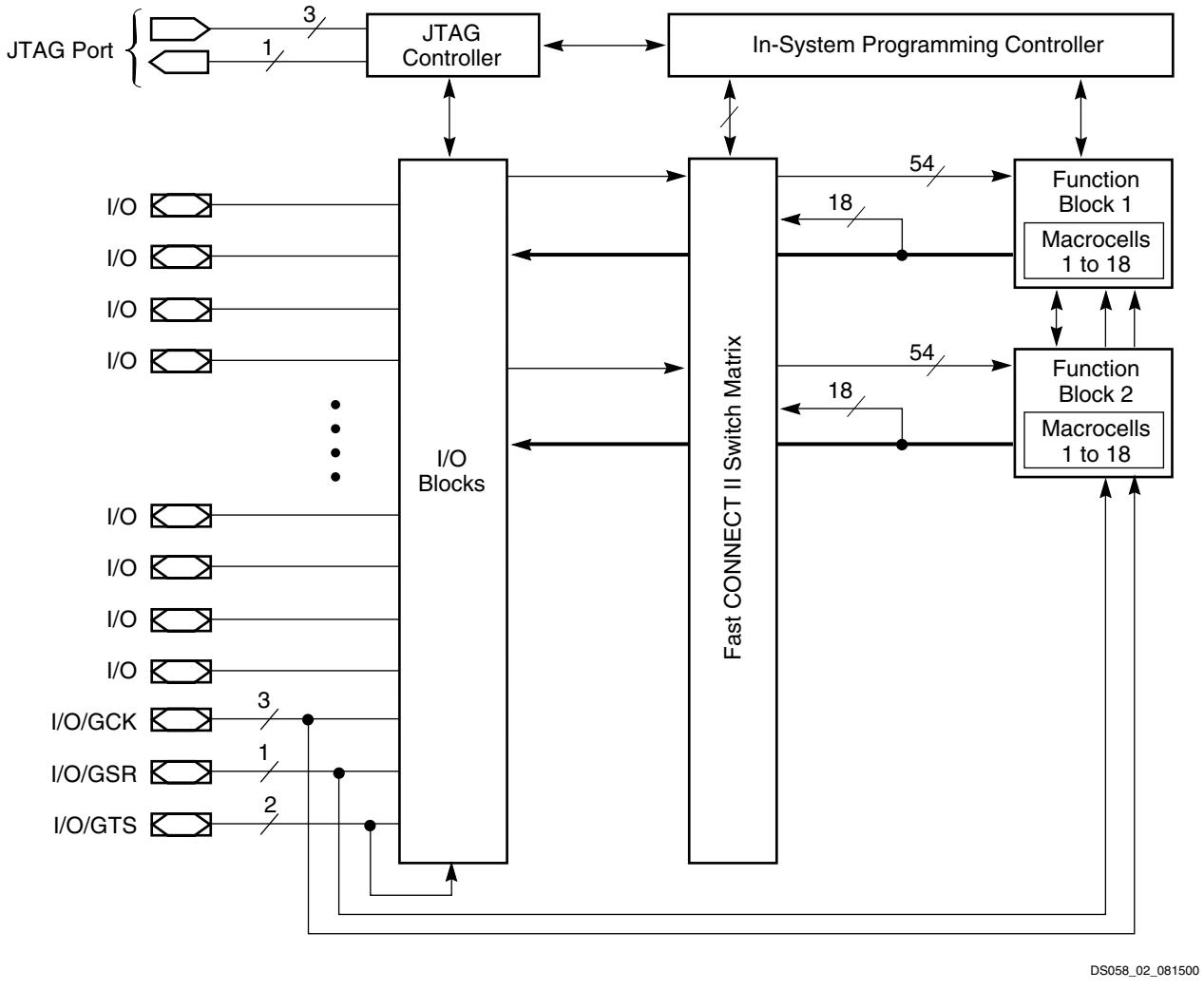


Figure 2: **XC9536XL Architecture**
Function Block outputs (indicated by the bold line) drive the I/O Blocks directly.

Absolute Maximum Ratings(2)

Symbol	Description	Value	Units
V_{CC}	Supply voltage relative to GND	–0.5 to 4.0	V
V_{IN}	Input voltage relative to GND(1)	–0.5 to 5.5	V
V_{TS}	Voltage applied to 3-state output(1)	–0.5 to 5.5	V
T_{STG}	Storage temperature (ambient)(3)	–65 to +150	°C
T_J	Junction temperature	+150	°C

Notes:

1. Maximum DC undershoot below GND must be limited to either 0.5V or 10 mA, whichever is easier to achieve. During transitions, the device pins may undershoot to –2.0 V or overshoot to +7.0V, provided this over- or undershoot lasts less than 10 ns and with the forcing current being limited to 200 mA. External I/O voltage may not exceed V_{CCINT} by 4.0V.
2. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.
3. For soldering guidelines and thermal considerations, see the Device Packaging information on the Xilinx website. For Pb-free packages, see XAPP427.

Recommended Operation Conditions

Symbol	Parameter		Min	Max	Units
V_{CCINT}	Supply voltage for internal logic and input buffers	Commercial T_A = 0°C to 70°C	3.0	3.6	V
		Industrial T_A = –40°C to +85°C	3.0	3.6	V
V_{CCIO}	Supply voltage for output drivers for 3.3V operation		3.0	3.6	V
	Supply voltage for output drivers for 2.5V operation		2.3	2.7	V
V_{IL}	Low-level input voltage		0	0.80	V
V_{IH}	High-level input voltage		2.0	5.5	V
V_O	Output voltage		0	V_{CCIO}	V

Quality and Reliability Characteristics

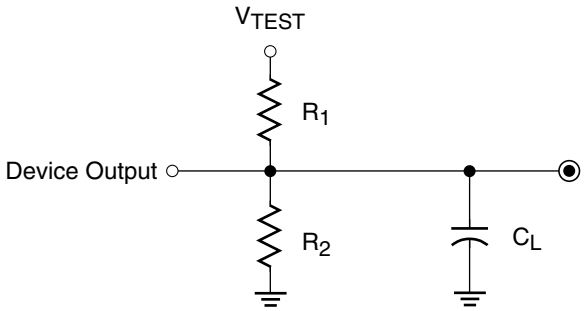
Symbol	Parameter	Min	Max	Units
T_{DR}	Data Retention	20	-	Years
N_{PE}	Program/Erase Cycles (Endurance)	10,000	-	Cycles
V_{ESD}	Electrostatic Discharge (ESD)	2,000	-	Volts

DC Characteristic Over Recommended Operating Conditions

Symbol	Parameter	Test Conditions	Min	Max	Units
V_{OH}	Output high voltage for 3.3V outputs	I_{OH} = –4.0 mA	2.4	-	V
	Output high voltage for 2.5V outputs	I_{OH} = –500 µA	90% V_{CCIO}	-	V
V_{OL}	Output low voltage for 3.3V outputs	I_{OL} = 8.0 mA	-	0.4	V
	Output low voltage for 2.5V outputs	I_{OL} = 500 µA	-	0.4	V
I_{IL}	Input leakage current	V_{CC} = Max; V_{IN} = GND or V_{CC}	-	±10	µA
I_{IH}	I/O high-Z leakage current	V_{CC} = Max; V_{IN} = GND or V_{CC}	-	±10	µA
I_{IH}	I/O high-Z leakage current	V_{CC} = Max; V_{CCIO} = Max; V_{IN} = GND or 3.6V	-	±10	µA
		V_{CC} Min < V_{IN} < 5.5V	-	±50	µA
C_{IN}	I/O capacitance	V_{IN} = GND; f = 1.0 MHz	-	10	pF
I_{CC}	Operating supply current (low power mode, active)	V_{IN} = GND, No load; f = 1.0 MHz	10 (Typical)		mA

AC Characteristics

Symbol	Parameter	XC9536XL-5		XC9536XL-7		XC9536XL-10		Units
		Min	Max	Min	Max	Min	Max	
T_{PD}	I/O to output valid	-	5.0	-	7.5	-	10.0	ns
T_{SU}	I/O setup time before GCK	3.7	-	4.8	-	6.5	-	ns
T_{H}	I/O hold time after GCK	0	-	0	-	0	-	ns
T_{CO}	GCK to output valid	-	3.5	-	4.5	-	5.8	ns
f_{SYSTEM}	Multiple FB internal operating frequency	-	178.6	-	125	-	100	MHz
T_{PSU}	I/O setup time before p-term clock input	1.7	-	1.6	-	2.1	-	ns
T_{PH}	I/O hold time after p-term clock input	2.0	-	3.2	-	4.4	-	ns
T_{PCO}	P-term clock output valid	-	5.5	-	7.7	-	10.2	ns
T_{OE}	GTS to output valid	-	4.0	-	5.0	-	7.0	ns
T_{OD}	GTS to output disable	-	4.0	-	5.0	-	7.0	ns
T_{POE}	Product term OE to output enabled	-	7.0	-	9.5	-	11.0	ns
T_{POD}	Product term OE to output disabled	-	7.0	-	9.5	-	11.0	ns
T_{AO}	GSR to output valid	-	10.0	-	12.0	-	14.5	ns
T_{PAO}	P-term S/R to output valid	-	10.5	-	12.6	-	15.3	ns
T_{WLH}	GCK pulse width (High or Low)	2.8	-	4.0	-	4.5	-	ns
T_{APRPW}	Asynchronous preset/reset pulse width (High or Low)	5.0	-	6.5	-	7.0	-	ns
T_{PLH}	P-term clock pulse width (High or Low)	5.0	-	6.5	-	7.0	-	ns



Output Type	V_{CCIO}	V_{TEST}	R_1	R_2	C_L
	3.3V	3.3V	320 Ω	360 Ω	35 pF
	2.5V	2.5V	250 Ω	660 Ω	35 pF

DS058_03_081500

Figure 3: **AC Load Circuit**

Internal Timing Parameters

Symbol	Parameter	XC9536XL-5		XC9536XL-7		XC9536XL-10		Units
		Min	Max	Min	Max	Min	Max	
Buffer Delays								
T_{IN}	Input buffer delay	-	1.5	-	2.3	-	3.5	ns
T_{GCK}	GCK buffer delay	-	1.1	-	1.5	-	1.8	ns
T_{GSR}	GSR buffer delay	-	2.0	-	3.1	-	4.5	ns
T_{GTS}	GTS buffer delay	-	4.0	-	5.0	-	7.0	ns
T_{OUT}	Output buffer delay	-	2.0	-	2.5	-	3.0	ns
T_{EN}	Output buffer enable/disable delay	-	0	-	0	-	0	ns
Product Term Control Delays								
T_{PTCK}	Product term clock delay	-	1.6	-	2.4	-	2.7	ns
T_{PTSR}	Product term set/reset delay	-	1.0	-	1.4	-	1.8	ns
T_{PTTS}	Product term 3-state delay	-	5.5	-	7.2	-	7.5	ns
Internal Register and Combinatorial Delays								
T_{PDI}	Combinatorial logic propagation delay	-	0.5	-	1.3	-	1.7	ns
T_{SUI}	Register setup time	2.3	-	2.6	-	3.0	-	ns
T_{HI}	Register hold time	1.4	-	2.2	-	3.5	-	ns
T_{ECSU}	Register clock enable setup time	2.3	-	2.6	-	3.0	-	ns
T_{ECHO}	Register clock enable hold time	1.4	-	2.2	-	3.5	-	ns
T_{COI}	Register clock to output valid time	-	0.4	-	0.5	-	1.0	ns
T_{AOI}	Register async. S/R to output delay	-	6.0	-	6.4	-	7.0	ns
T_{RAI}	Register async. S/R recover before clock	5.0		7.5		10.0		ns
T_{LOGI}	Internal logic delay	-	1.0	-	1.4	-	1.8	ns
T_{LOGILP}	Internal low power logic delay	-	5.0	-	6.4	-	7.3	ns
Feedback Delays								
T_F	Fast CONNECT II feedback delay	-	1.9	-	3.5	-	4.2	ns
Time Adders								
T_{PTA}	Incremental product term allocator delay	-	0.7	-	0.8	-	1.0	ns
T_{SLEW}	Slew-rate limited delay	-	3.0	-	4.0	-	4.5	ns

XC9536XL I/O Pins[2]

Function Block	Macro-cell	PC44	VQ44	CS48	VQ64	BScan Order	Function Block	Macro-cell	PC44	VQ44	CS48	VQ64	BScan Order
1	1	2	40	D6	9	105	2	1	1	39	D7	8	51
1	2	3	41	C7	10	102	2	2	44	38	E5	7	48
1	3	5[1]	43[1]	B7[1]	15[1]	99	2	3	42[1]	36[1]	E6[1]	5[1]	45
1	4	4	42	C6	11	96	2	4	43	37	E7	6	42
1	5	6[1]	44[1]	B6[1]	16[1]	93	2	5	40[1]	34[1]	F6[1]	2[1]	39
1	6	8	2	A6	19	90	2	6	39[1]	33[1]	G7[1]	64[1]	36
1	7	7[1]	1[1]	A7[1]	17[1]	87	2	7	38	32	G6	63	33
1	8	9	3	C5	20	84	2	8	37	31	F5	62	30
1	9	11	5	B5	22	81	2	9	36	30	G5	61	27
1	10	12	6	A4	24	78	2	10	35	29	F4	60	24
1	11	13	7	B4	25	75	2	11	34	28	G4	57	21
1	12	14	8	A3	27	72	2	12	33	27	E3	56	18
1	13	18	12	B2	33	69	2	13	29	23	F2	50	15
1	14	19	13	B1	35	66	2	14	28	22	G1	48	12
1	15	20	14	C2	36	63	2	15	27	21	F1	45	9
1	16	22	16	C3	38	60	2	16	26	20	E2	44	6
1	17	24	18	D2	42	57	2	17	25	19	E1	43	3
1	18	-	-	D3	39	54	2	18	-	-	E4	49	0

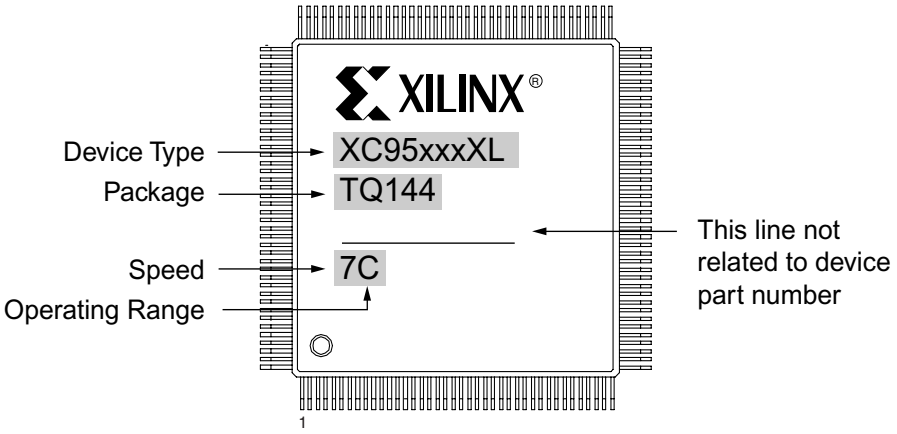
Notes:
1. Global control pin.
2. The pin-outs are the same for Pb-free versions of packages.

XC9536XL Global, JTAG and Power Pins[1]

Pin Type	PC44	VQ44	CS48	VQ64
I/O/GCK1	5	43	B7	15
I/O/GCK2	6	44	B6	16
I/O/GCK3	7	1	A7	17
I/O/GTS1	42	36	E6	5
I/O/GTS2	40	34	F6	2
I/O/GSR	39	33	G7	64
TCK	17	11	A1	30
TDI	15	9	B3	28
TDO	30	24	G2	53
TMS	16	10	A2	29
V_{CCINT} 3.3V	21, 41	15, 35	C1, F7	3, 37
V_{CCIO} 2.5V/3.3V	32	26	G3	55
GND	10, 23, 31	4, 17, 25	A5, D1, F3	21, 41, 54
No Connects	-	-	C4, D4	1, 4, 12, 13, 14, 18, 23, 26, 31, 32, 34, 40, 46, 47, 51, 52, 58, 59

Notes:
1. The pin-outs are the same for Pb-free versions of packages.

Device Part Marking and Ordering Combination Information



Sample package with part marking.

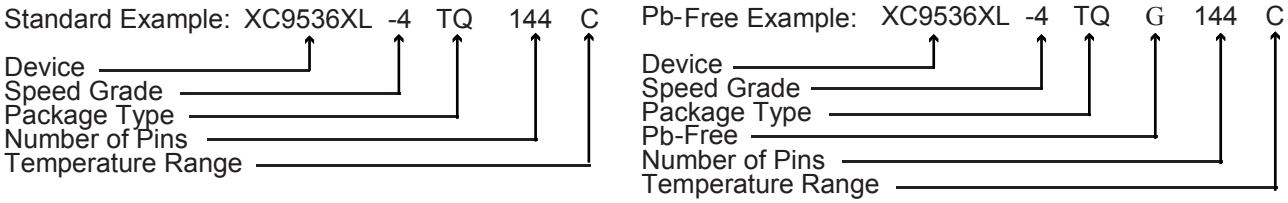
Notes:

1. Due to the small size of chip scale packages, part marking on these packages does not follow the above sample and the complete part number cannot be included in the marking. Part marking on chip scale packages by line:
   - Line 1 = X (Xilinx logo), then truncated part number (no XC), i.e., 95xxxXL.
   - Line 2 = Not related to device part number.
   - Line 3 = Not related to device part number.
   - Line 4 = Package code, speed, operating temperature, three digits not related to part number. Package codes: C1 = CS48, C2 = CSG48.

Device Ordering and Part Marking Number	Speed (pin-to-pin delay)	Pkg. Symbol	No. of Pins	Package Type	Operating Range(1)
XC9536XL-5PC44C	5 ns	PC44	44-pin	Plastic Lead Chip Carrier (PLCC)	C
XC9536XL-5VQ44C	5 ns	VQ44	44-pin	Quad Flat Pack (VQFP)	C
XC9536XL-5CS48C	5 ns	CS48	48-ball	Chip Scale Package (CSP)	C
XC9536XL-5VQ64C	5 ns	VQ64	64-pin	Quad Flat Pack (VQFP)	C
XC9536XL-7PC44C	7.5 ns	PC44	44-pin	Plastic Lead Chip Carrier (PLCC)	C
XC9536XL-7VQ44C	7.5 ns	VQ44	44-pin	Quad Flat Pack (VQFP)	C
XC9536XL-7CS48C	7.5 ns	CS48	48-ball	Chip Scale Package (CSP)	C
XC9536XL-7VQ64C	7.5 ns	VQ64	64-pin	Quad Flat Pack (VQFP)	C
XC9536XL-7PC44I	7.5 ns	PC44	44-pin	Plastic Lead Chip Carrier (PLCC)	I
XC9536XL-7VQ44I	7.5 ns	VQ44	44-pin	Quad Flat Pack (VQFP)	I
XC9536XL-7CS48I	7.5 ns	CS48	48-ball	Chip Scale Package (CSP)	I
XC9536XL-7VQ64I	7.5 ns	VQ64	64-pin	Quad Flat Pack (VQFP)	I
XC9536XL-10PC44C	10 ns	PC44	44-pin	Plastic Lead Chip Carrier (PLCC)	C
XC9536XL-10VQ44C	10 ns	VQ44	44-pin	Quad Flat Pack (VQFP)	C
XC9536XL-10CS48C	10 ns	CS48	48-ball	Chip Scale Package (CSP)	C
XC9536XL-10VQ64C	10 ns	VQ64	64-pin	Quad Flat Pack (VQFP)	C
XC9536XL-10PC44I	10 ns	PC44	44-pin	Plastic Lead Chip Carrier (PLCC)	I
XC9536XL-10VQ44I	10 ns	VQ44	44-pin	Quad Flat Pack (VQFP)	I
XC9536XL-10CS48I	10 ns	CS48	48-ball	Chip Scale Package (CSP)	I
XC9536XL-10VQ64I	10 ns	VQ64	64-pin	Quad Flat Pack (VQFP)	I
XC9536XL-5PCG44C	5 ns	PCG44	44-pin	Plastic Lead Chip Carrier (PLCC); Pb-free	C
XC9536XL-5VQG44C	5 ns	VQG44	44-pin	Quad Flat Pack (VQFP); Pb-free	C

Device Ordering and Part Marking Number	Speed (pin-to-pin delay)	Pkg. Symbol	No. of Pins	Package Type	Operating Range(1)
XC9536XL-5CSG48C	5 ns	CSG48	48-ball	Chip Scale Package (CSP); Pb-free	C
XC9536XL-5VQG64C	5 ns	VQG64	64-pin	Quad Flat Pack (VQFP); Pb-free	C
XC9536XL-7PCG44C	7.5 ns	PCG44	44-pin	Plastic Lead Chip Carrier (PLCC); Pb-free	C
XC9536XL-7VQG44C	7.5 ns	VQG44	44-pin	Quad Flat Pack (VQFP); Pb-free	C
XC9536XL-7CSG48C	7.5 ns	CSG48	48-ball	Chip Scale Package (CSP); Pb-free	C
XC9536XL-7VQG64C	7.5 ns	VQG64	64-pin	Quad Flat Pack (VQFP); Pb-free	C
XC9536XL-7PCG44I	7.5 ns	PCG44	44-pin	Plastic Lead Chip Carrier (PLCC); Pb-free	I
XC9536XL-7VQG44I	7.5 ns	VQG44	44-pin	Quad Flat Pack (VQFP); Pb-free	I
XC9536XL-7CSG48I	7.5 ns	CSG48	48-ball	Chip Scale Package (CSP); Pb-free	I
XC9536XL-7VQG64I	7.5 ns	VQG64	64-pin	Quad Flat Pack (VQFP); Pb-free	I
XC9536XL-10PCG44C	10 ns	PCG44	44-pin	Plastic Lead Chip Carrier (PLCC); Pb-free	C
XC9536XL-10VQG44C	10 ns	VQG44	44-pin	Quad Flat Pack (VQFP); Pb-free	C
XC9536XL-10CSG48C	10 ns	CSG48	48-ball	Chip Scale Package (CSP); Pb-free	C
XC9536XL-10VQG64C	10 ns	VQG64	64-pin	Quad Flat Pack (VQFP); Pb-free	C
XC9536XL-10PCG44I	10 ns	PCG44	44-pin	Plastic Lead Chip Carrier (PLCC); Pb-free	I
XC9536XL-10VQG44I	10 ns	VQG44	44-pin	Quad Flat Pack (VQFP); Pb-free	I
XC9536XL-10CSG48I	10 ns	CSG48	48-ball	Chip Scale Package (CSP); Pb-free	I
XC9536XL-10VQG64I	10 ns	VQG64	64-pin	Quad Flat Pack (VQFP); Pb-free	I

Notes:
1. C = Commercial: T_A = 0° to +70°C; I = Industrial: T_A = –40° to +85°C.



Warranty Disclaimer

THESE PRODUCTS ARE SUBJECT TO THE TERMS OF THE XILINX LIMITED WARRANTY WHICH CAN BE VIEWED AT http://www.xilinx.com/warranty.htm. THIS LIMITED WARRANTY DOES NOT EXTEND TO ANY USE OF THE PRODUCTS IN AN APPLICATION OR ENVIRONMENT THAT IS NOT WITHIN THE SPECIFICATIONS STATED ON THE THEN-CURRENT XILINX DATA SHEET FOR THE PRODUCTS. PRODUCTS ARE NOT DESIGNED TO BE FAIL-SAFE AND ARE NOT WARRANTED FOR USE IN APPLICATIONS THAT POSE A RISK OF PHYSICAL HARM OR LOSS OF LIFE. USE OF PRODUCTS IN SUCH APPLICATIONS IS FULLY AT THE RISK OF CUSTOMER SUBJECT TO APPLICABLE LAWS AND REGULATIONS.

Further Reading

The following Xilinx links go to relevant XC9500XL CPLD documentation, including XAPP111, Using the XC9500XL Timing Model, and XAPP784, Bulletproof CPLD Design Practices. Simply click on the link and scroll down.

Data Sheets, Application Notes, and White Papers.

Packaging

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
09/28/98	1.0	Initial Xilinx release.
08/28/00	1.1	Added VQ44 package.
06/20/02	1.2	Updated I_{CC} equation, page 1. Removed -4 device. Added industrial availability to -7 device. Added additional I_{IH} test conditions and measurements to DC Characteristics table.
06/18/03	1.3	Updated T_{SOL} from 260 to 220ºC. Added Device Part Marking and updated Ordering Information.
08/21/03	1.4	Updated Package Device Marking Pin 1 orientation.
07/15/04	1.5	Added Pb-free documentation
09/15/04	1.6	Added T_{APRPW} specification to AC Characteristics.
07/15/05	1.7	Move to Product Specification
03/22/06	1.8	Add Warranty Disclaimer.
04/03/07	1.9	Add programming temperature range warning on page 1.