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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

E·XFI

Product Status	Active
Core Processor	PIC
Core Size	16-Bit
Speed	32MHz
Connectivity	I ² C, PMP, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LVD, POR, PWM, WDT
Number of I/O	21
Program Memory Size	16KB (5.5K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 10x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	28-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24fj16ga002-i-so

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

1.1.4 EASY MIGRATION

Regardless of the memory size, all devices share the same rich set of peripherals, allowing for a smooth migration path as applications grow and evolve.

The consistent pinout scheme used throughout the entire family also aids in migrating to the next larger device. This is true when moving between devices with the same pin count, or even jumping from 28-pin to 44-pin devices.

The PIC24F family is pin-compatible with devices in the dsPIC33 family, and shares some compatibility with the pinout schema for PIC18 and dsPIC30. This extends the ability of applications to grow from the relatively simple, to the powerful and complex, yet still selecting a Microchip device.

1.2 Other Special Features

- **Communications:** The PIC24FJ64GA004 family incorporates a range of serial communication peripherals to handle a range of application requirements. There are two independent I²C modules that support both Master and Slave modes of operation. Devices also have, through the Peripheral Pin Select (PPS) feature, two independent UARTs with built-in IrDA encoder/decoders and two SPI modules.
- Peripheral Pin Select (PPS): The Peripheral Pin Select feature allows most digital peripherals to be mapped over a fixed set of digital I/O pins. Users may independently map the input and/or output of any one of the many digital peripherals to any one of the I/O pins.
- Parallel Master/Enhanced Parallel Slave Port: One of the general purpose I/O ports can be reconfigured for enhanced parallel data communications. In this mode, the port can be configured for both master and slave operations, and supports 8-bit and 16-bit data transfers with up to 16 external address lines in Master modes.
- Real-Time Clock/Calendar (RTCC): This module implements a full-featured clock and calendar with alarm functions in hardware, freeing up timer resources and program memory space for use of the core application.
- **10-Bit A/D Converter:** This module incorporates programmable acquisition time, allowing for a channel to be selected and a conversion to be initiated without waiting for a sampling period, as well as faster sampling speeds.

1.3 Details on Individual Family Members

Devices in the PIC24FJ64GA004 family are available in 28-pin and 44-pin packages. The general block diagram for all devices is shown in Figure 1-1.

The devices are differentiated from each other in two ways:

- Flash program memory (64 Kbytes for PIC24FJ64GA devices, 48 Kbytes for PIC24FJ48GA devices, 32 Kbytes for PIC24FJ32GA devices and 16 Kbytes for PIC24FJ16GA devices).
- 2. Internal SRAM memory (4k for PIC24FJ16GA devices, 8k for all other devices in the family).
- Available I/O pins and ports (21 pins on 2 ports for 28-pin devices and 35 pins on 3 ports for 44-pin devices).

All other features for devices in this family are identical. These are summarized in Table 1-1.

A list of the pin features that are available on the PIC24FJ64GA004 family devices, sorted by function, is shown in Table 1-2. Note that this table shows the pin location of individual peripheral features and not how they are multiplexed on the same pin. This information is provided in the pinout diagrams in the beginning of the data sheet. Multiplexed features are sorted by the priority given to a feature, with the highest priority peripheral being listed first.

6.0 RESETS

Note: This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information, refer to the *"PIC24F Family Reference Manual"*, **"Reset"** (DS39712).

The Reset module combines all Reset sources and controls the device Master Reset Signal, SYSRST. The following is a list of device Reset sources:

- · POR: Power-on Reset
- MCLR: Pin Reset
- SWR: RESET Instruction
- WDT: Watchdog Timer Reset
- BOR: Brown-out Reset
- CM: Configuration Mismatch Reset
- TRAPR: Trap Conflict Reset
- · IOPUWR: Illegal Opcode Reset
- · UWR: Uninitialized W Register Reset

A simplified block diagram of the Reset module is shown in Figure 6-1.

Any active source of Reset will make the SYSRST signal active. Many registers associated with the CPU and peripherals are forced to a known Reset state. Most registers are unaffected by a Reset; their status is unknown on POR and unchanged by all other Resets.

Note: Refer to the specific peripheral or CPU section of this manual for register Reset states.

All types of device Reset will set a corresponding status bit in the RCON register to indicate the type of Reset (see Register 6-1). A Power-on Reset will clear all bits except for the BOR and POR bits (RCON<1:0>) which are set. The user may set or clear any bit at any time during code execution. The RCON bits only serve as status bits. Setting a particular Reset status bit in software will not cause a device Reset to occur.

The RCON register also has other bits associated with the Watchdog Timer and device power-saving states. The function of these bits is discussed in other sections of this manual.

Note: The status bits in the RCON register should be cleared after they are read so that the next RCON register value after a device Reset will be meaningful.



REGISTER 10-19: RPOR4: PERIPHERAL PIN SELECT OUTPUT REGISTER 4

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—		RP9R4	RP9R3	RP9R2	RP9R1	RP9R0
bit 15							bit 8
U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	RP8R4	RP8R3	RP8R2	RP8R1	RP8R0
bit 7						•	bit 0
Logond							

Legena.			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	l as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-13 Unimplemented: Read as '0'

bit 12-8	RP9R<4:0>: Peripheral Output Function is Assigned to RP9 Output Pin bits
	(see Table 10-3 for peripheral function numbers)

bit 7-5 Unimplemented: Read as '0'

bit 4-0 **RP8R<4:0>:** Peripheral Output Function is Assigned to RP8 Output Pin bits (see Table 10-3 for peripheral function numbers)

REGISTER 10-20: RPOR5: PERIPHERAL PIN SELECT OUTPUT REGISTER 5

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	RP11R4	RP11R3	RP11R2	RP11R1	RP11R0
bit 15							bit 8

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	RP10R4	RP10R3	RP10R2	RP10R1	RP10R0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	1 as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-13 Unimplemented: Read as '0'

bit 12-8 **RP11R<4:0>:** Peripheral Output Function is Assigned to RP11 Output Pin bits (see Table 10-3 for peripheral function numbers)

bit 7-5 Unimplemented: Read as '0'

bit 4-0 **RP10R<4:0>:** Peripheral Output Function is Assigned to RP10 Output Pin bits (see Table 10-3 for peripheral function numbers)

14.3 Pulse-Width Modulation Mode

Note:	This peripheral contains input and output							
	functions that may need to be configured							
	by the Peripheral Pin Select. See							
	Section 10.4 "Peripheral Pin Select							
	(PPS)" for more information.							

The following steps should be taken when configuring the output compare module for PWM operation:

- 1. Set the PWM period by writing to the selected Timery Period register (PRy).
- 2. Set the PWM duty cycle by writing to the OCxRS register.
- 3. Write the OCxR register with the initial duty cycle.
- 4. Enable interrupts, if required, for the timer and output compare modules. The output compare interrupt is required for PWM Fault pin utilization.
- Configure the output compare module for one of two PWM Operation modes by writing to the Output Compare Mode bits, OCM<2:0> (OCxCON<2:0>).
- 6. Set the TMRy prescale value and enable the time base by setting TON (TyCON<15>) = 1.
 - Note: The OCxR register should be initialized before the output compare module is first enabled. The OCxR register becomes a read-only Duty Cycle register when the module is operated in the PWM modes. The value held in OCxR will become the PWM duty cycle for the first PWM period. The contents of the Output Compare x Secondary register, OCxRS, will not be transferred into OCxR until a time base period match occurs.

14.3.1 PWM PERIOD

The PWM period is specified by writing to PRy, the Timery Period register. The PWM period can be calculated using Equation 14-1.

EQUATION 14-1: CALCULATING THE PWM PERIOD⁽¹⁾

PWM Period = $[(PRy) + 1] \bullet TCY \bullet (Timer Prescale Value)$ Where:

PWM Frequency = 1/[PWM Period]

Note 1: Based on TCY = 2 * TOSC; Doze mode and PLL are disabled.

Note: A PRy value of N will produce a PWM period of N + 1 time base count cycles. For example, a value of 7 written into the PRy register will yield a period consisting of 8 time base cycles.

14.3.2 PWM DUTY CYCLE

The PWM duty cycle is specified by writing to the OCxRS register. The OCxRS register can be written to at any time, but the duty cycle value is not latched into OCxR until a match between PRy and TMRy occurs (i.e., the period is complete). This provides a double buffer for the PWM duty cycle and is essential for glitchless PWM operation. In the PWM mode, OCxR is a read-only register.

Some important boundary parameters of the PWM duty cycle include:

- If the Output Compare x register, OCxR, is loaded with 0000h, the OCx pin will remain low (0% duty cycle).
- If OCxR is greater than PRy (Timery Period register), the pin will remain high (100% duty cycle).
- If OCxR is equal to PRy, the OCx pin will be low for one time base count value and high for all other count values.

See Example 14-1 for PWM mode timing details. Table 14-1 and Table 14-2 show example PWM frequencies and resolutions for a device operating at 4 and 16 MIPS.

EQUATION 14-2: CALCULATION FOR MAXIMUM PWM RESOLUTION⁽¹⁾



REGISTER 16-1: I2CxCON: I2Cx CONTROL REGISTER (CONTINUED)

bit 5	ACKDT: Acknowledge Data bit (when operating as I ² C master, applicable during master receive) Value that will be transmitted when the software initiates an Acknowledge sequence. 1 = Sends a NACK during Acknowledge 0 = Sends an ACK during Acknowledge
bit 4	 ACKEN: Acknowledge Sequence Enable bit (when operating as I²C master, applicable during master receive) 1 = Initiates Acknowledge sequence on SDAx and SCLx pins and transmits the ACKDT data bit. Hardware is clear at the end of master Acknowledge sequence. 0 = Acknowledge sequence is not in progress
bit 3	RCEN: Receive Enable bit (when operating as I ² C master) 1 = Enables Receive mode for I ² C. Hardware is clear at the end of eighth bit of master receive data byte. 0 = Receive sequence is not in progress
bit 2	 PEN: Stop Condition Enable bit (when operating as I²C master) 1 = Initiates Stop condition on SDAx and SCLx pins. Hardware is clear at the end of master Stop sequence. 0 = Stop condition is not in progress
bit 1	 RSEN: Repeated Start Condition Enable bit (when operating as I²C master) 1 = Initiates Repeated Start condition on SDAx and SCLx pins. Hardware is clear at the end of master Repeated Start sequence. 0 = Repeated Start condition is not in progress
bit 0	 SEN: Start Condition Enable bit (when operating as I²C master) 1 = Initiates Start condition on SDAx and SCLx pins. Hardware is clear at the end of master Start sequence. 0 = Start condition is not in progress

Note 1: In Slave mode, the module will not automatically clock stretch after receiving the address byte.

R/W-0	U-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0 ⁽³⁾	R/W-0 ⁽³⁾
UARTEN ⁽	1)	USIDL	IREN ⁽²⁾	RTSMD	_	UEN1	UEN0
bit 15							bit 8
R/C-0, HC	C R/W-0	R/W-0, HC	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
WAKE	LPBACK	ABAUD	RXINV	BRGH	PDSEL1	PDSEL0	STSEL
bit 7							bit 0
· · ·							
Legend:		C = Clearable	bit	HC = Hardwa	re Clearable bi	t . (c)	
R = Reada	ble bit	W = Writable I	Dit		nented bit, read		
-n = Value	at POR	'1' = Bit is set		0° = Bit is clea	ared	x = Bit is unkn	own
bit 15		DTy Enable bit	(1)				
DIL 15	1 = 11	R IX Enabled: all LL	ΔRTx nins are	controlled by I	IARTy as defin	ed by LIEN<1.0)>
	0 = UARTx is minimal	s disabled; all U	ARTx pins are	controlled by F	PORT latches;	UARTx power c	onsumption is
bit 14	Unimplemen	ted: Read as 'o	,				
bit 13	USIDL: UAR	Tx Stop in Idle N	lode bit				
	1 = Discontin	ues module op	eration when o	device enters lo	lle mode		
	0 = Continue	s module opera	ition in Idle mo	ode			
bit 12	IREN: IrDA® I	Encoder and De	ecoder Enable	bit'~			
	1 = IrDA encoder0 = IrDA encoder	oder and decod	er are enable er are disable	d d			
bit 11	RTSMD: Mod	le Selection for	UxRTS Pin bi	t			
	$1 = \frac{UxRTS}{UxRTS} p$ 0 = UxRTS p	in in Simplex m in in Flow Cont	ode rol mode				
bit 10	Unimplemen	ted: Read as 'o	,				
bit 9-8	UEN<1:0>: U	ARTx Enable b	its ⁽³⁾				
	11 = UxTX, UxRX and BCLKx pins are enabled and used; $\overline{\text{UxCTS}}$ pin is controlled by PORT latches						
	10 = UxTX, UxRX, UxCTS and UxRTS pins are enabled and used						
	00 = UxTX ar	d UxRX pins are	enabled and u	used; UxCTS an	d UxRTS/BCL	CX pins are contr	olled by PORT
	latches	·					
bit 7	WAKE: Wake	e-up on Start Bit	Detect During	g Sleep Mode E	nable bit		
	1 = UARTx w	/ill continue to sa	ample the UxR	X pin; interrupt	is generated o	n falling edge, b	it is cleared in
	0 = No wake	-up is enabled	sing edge				
bit 6	LPBACK: UA	RTx Loopback	Mode Select I	bit			
	1 = Enables	Loopback mode	;				
	0 = Loopbac	k mode is disab	led				
bit 5	ABAUD: Auto	o-Baud Enable I	oit				
	1 = Enables	baud rate meas	urement on th	ne next characte	er – requires re	eception of a Sy	nc field (55h);
	0 = Baud rate	e measurement	is disabled or	completed			
					Course of the second		
NOTE 1:	IT UARIEN = 1, th Section 10.4 "Pe	ne peripheral in eripheral Pin Se	puts and outpo elect (PPS)" f	uts must be cor or more information	nigured to an a ation.	ivaliable RPh pi	in. See
2:	This feature is on	ly available for	the 16x BRG r	mode (BRGH =	0).		
	B., .,						

REGISTER 17-1: UXMODE: UARTX MODE REGISTER

3: Bit availability depends on pin availability.

18.0 PARALLEL MASTER PORT (PMP)

Note:	This data sheet summarizes the features of						
	this group of PIC24F devices. It is not						
	intended to be a comprehensive reference						
	source. For more information, refer to the						
	"PIC24F Family Reference Manual",						
	"Parallel Master Port (PMP)" (DS39713).						

The Parallel Master Port (PMP) module is a parallel 8-bit I/O module, specifically designed to communicate with a wide variety of parallel devices, such as communication peripherals, LCDs, external memory devices and microcontrollers. Because the interface to parallel peripherals varies significantly, the PMP is highly configurable.

Note: A number of the pins for the PMP are not present on PIC24FJ64GA004 devices. Refer to the specific device's pinout to determine which pins are available.

Key features of the PMP module include:

- Up to 16 Programmable Address Lines
- One Chip Select Line
- Programmable Strobe Options:
 - Individual Read and Write Strobes or;
 - Read/Write Strobe with Enable Strobe
- Address Auto-Increment/Auto-Decrement
- Programmable Address/Data Multiplexing
- · Programmable Polarity on Control Signals
- · Legacy Parallel Slave Port Support
- Enhanced Parallel Slave Support:
 - Address Support
 - 4-Byte Deep Auto-Incrementing Buffer
- · Programmable Wait States
- · Selectable Input Voltage Levels

FIGURE 18-1: PARALLEL MASTER PORT (PMP) MODULE OVERVIEW



FIGURE 18-2: LEGACY PARALLEL SLAVE PORT EXAMPLE



FIGURE 18-3: ADDRESSABLE PARALLEL SLAVE PORT EXAMPLE



TABLE 18-1: SLAVE MODE ADDRESS RESOLUTION

PMA<1:0>	Output Register (Buffer)	Input Register (Buffer)
00	PMDOUT1<7:0> (0)	PMDIN1<7:0> (0)
01	PMDOUT1<15:8> (1)	PMDIN1<15:8> (1)
10	PMDOUT2<7:0> (2)	PMDIN2<7:0> (2)
11	PMDOUT2<15:8> (3)	PMDIN2<15:8> (3)

FIGURE 18-4: MASTER MODE, DEMULTIPLEXED ADDRESSING (SEPARATE READ AND WRITE STROBES, SINGLE CHIP SELECT)



REGISTER 19-9: ALWDHR: ALARM WEEKDAY AND HOURS VALUE REGISTEI	REGISTER 19-9:
---	----------------

U-0	U-0	U-0	U-0	U-0	R/W-x	R/W-x	R/W-x	
_	—		_		WDAY2	WDAY1	WDAY0	
bit 15					•		bit 8	
U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	
_	—	HRTEN1	HRTEN0	HRONE3	HRONE2	HRONE1	HRONE0	
bit 7	÷	•			•	•	bit 0	
Legend:								
R = Readable bit W = Writable		W = Writable	oit	U = Unimplemented bit, read as '0'				
-n = Value a	It POR	'1' = Bit is set		'0' = Bit is cleared		x = Bit is unknown		
bit 15-11	Unimplemen	ted: Read as 'd)'					
bit 10-8	WDAY<2:0>:	Binary Coded	Decimal Value	of Weekday Di	git bits			
	Contains a value from 0 to 6.							
bit 7-6	Unimplemented: Read as '0'							
bit 5-4	HRTEN<1:0>	: Binary Coded	Decimal Value	e of Hour's Ten	s Digit bits			
	Contains a value from 0 to 2.							

- bit 3-0 **HRONE<3:0>:** Binary Coded Decimal Value of Hour's Ones Digit bits Contains a value from 0 to 9.
- **Note 1:** A write to this register is only allowed when RTCWREN = 1.

REGISTER 19-10: ALMINSEC: ALARM MINUTES AND SECONDS VALUE REGISTER

U-0	R/W-x						
—	MINTEN2	MINTEN1	MINTEN0	MINONE3	MINONE2	MINONE1	MINONE0
bit 15							bit 8

U-0	R/W-x						
—	SECTEN2	SECTEN1	SECTEN0	SECONE3	SECONE2	SECONE1	SECONE0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	d as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15	Unimplemented: Read as '0'
bit 14-12	MINTEN<2:0>: Binary Coded Decimal Value of Minute's Tens Digit bits
	Contains a value from 0 to 5.
bit 11-8	MINONE<3:0>: Binary Coded Decimal Value of Minute's Ones Digit bits
	Contains a value from 0 to 9.
bit 7	Unimplemented: Read as '0'
bit 6-4	SECTEN<2:0>: Binary Coded Decimal Value of Second's Tens Digit bits
	Contains a value from 0 to 5.
bit 3-0	SECONE<3:0>: Binary Coded Decimal Value of Second's Ones Digit bits
	Contains a value from 0 to 9.

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FIGURE 19-2	ALARM MASK SETTINGS
1100NL 13-2.	

Alarm Mask Setting (AMASK<3:0>)	Day of the Week	Month Day	Hours	Minutes Seconds
0000 – Every half second 0001 – Every second				:
0010 – Every 10 seconds				: S
0011 – Every minute				: : : : :
0100 – Every 10 minutes				: m : s s
0101 – Every hour				: m m : s s
0110 – Every day			h h	: m m : s s
0111 – Every week	d		h h	: m m : s s
1000 – Every month		/ d	h h	: m m : s s
1001 – Every year ⁽¹⁾		m m / d d	h h	: m m : s s
Note 1: Annually, except when co	nfigured fo	r February 29.		

REGISTER 21-2: AD1CON2: A/D CONTROL REGISTER 2

R/W-0	R/W-0	R/W-0	U-0	U-0	R/W-0	U-0	U-0
VCFG2	VCFG1	VCFG0	—	—	CSCNA	—	—
bit 15							bit 8

R-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
BUFS	—	SMPI3	SMPI2	SMPI1	SMPI0	BUFM	ALTS
bit 7							bit 0

Legend:R = Readable bitW = Writable bitU = Unimplemented bit, read as '0'-n = Value at POR'1' = Bit is set'0' = Bit is clearedx = Bit is unknown

bit 15-13 VCFG<2:0>: Voltage Reference Configuration bits

VCFG<2:0>	VR+	VR-
000	AVDD*	AVss*
001	External VREF+ Pin	AVss*
010	AVDD*	External VREF- Pin
011	External VREF+ Pin	External VREF- Pin
lxx	AVDD*	AVss*

* AVDD and AVSS inputs are tied to VDD and VSS on 28-pin devices.

bit 12-11 Unimplemented: Read as '0'

bit 10	CSCNA: Scan Input Selections for CH0+ S/H Input for MUX A Input Multiplexer Setting bit
	1 = Scans inputs
	0 = Does not scan inputs
bit 9-8	Unimplemented: Read as '0'
bit 7	BUFS: Buffer Fill Status bit (valid only when BUFM = 1)
	 1 = A/D is currently filling Buffer 08-0F, user should access data in 00-07 0 = A/D is currently filling Buffer 00-07, user should access data in 08-0F
bit 6	Unimplemented: Read as '0'
bit 5-2	SMPI<3:0>: Sample/Convert Sequences Per Interrupt Selection bits
	1111 = Interrupts at the completion of conversion for each 16th sample/convert sequence 1110 = Interrupts at the completion of conversion for each 15th sample/convert sequence
	· · · · · · · ·
	0001 = Interrupts at the completion of conversion for each 2nd sample/convert sequence
	0000 = Interrupts at the completion of conversion for each sample/convert sequence
bit 1	BUFM: Buffer Mode Select bit
	 1 = Buffer configured as two 8-word buffers (ADC1BUFn<15:8> and ADC1BUFn<7:0>) 0 = Buffer configured as one 16-word buffer (ADC1BUFn<15:0>)
bit 0	ALTS: Alternate Input Sample Mode Select bit
	1 = Uses MUX A input multiplexer settings for first sample, then alternates between MUX B and MUX A input multiplexer settings for all subsequent samples
	0 = Always uses MUX A input multiplexer settings

NOTES:

24.3.1 WINDOWED OPERATION

The Watchdog Timer has an optional Fixed Window mode of operation. In this Windowed mode, CLRWDT instructions can only reset the WDT during the last 1/4 of the programmed WDT period. A CLRWDT instruction executed before that window causes a WDT Reset, similar to a WDT time-out.

Windowed WDT mode is enabled by programming the WINDIS Configuration bit (CW1<6>) to '0'.

24.3.2 CONTROL REGISTER

The WDT is enabled or disabled by the FWDTEN Configuration bit. When the FWDTEN Configuration bit is set, the WDT is always enabled.

The WDT can be optionally controlled in software when the FWDTEN Configuration bit has been programmed to '0'. The WDT is enabled in software by setting the SWDTEN control bit (RCON<5>). The SWDTEN control bit is cleared on any device Reset. The software WDT option allows the user to enable the WDT for critical code segments and disable the WDT during non-critical segments for maximum power savings.



Assembly Mnemonic		Assembly Syntax	Description		# of Cycles	Status Flags Affected
BTSS	BTSS	f,#bit4	Bit Test f, Skip if Set	1	1 (2 or 3)	None
	BTSS	Ws,#bit4	Bit Test Ws, Skip if Set	1	1 (2 or 3)	None
BTST	BTST	f,#bit4	Bit Test f	1	1	Z
	BTST.C	Ws,#bit4	Bit Test Ws to C	1	1	С
	BTST.Z	Ws,#bit4	Bit Test Ws to Z	1	1	Z
	BTST.C	Ws,Wb	Bit Test Ws <wb> to C</wb>	1	1	С
	BTST.Z	Ws,Wb	Bit Test Ws <wb> to Z</wb>	1	1	Z
BTSTS	BTSTS	f,#bit4	Bit Test then Set f	1	1	Z
	BTSTS.C	Ws,#bit4	Bit Test Ws to C, then Set	1	1	С
	BTSTS.Z	Ws,#bit4	Bit Test Ws to Z, then Set	1	1	Z
CALL	CALL	lit23	Call Subroutine	2	2	None
	CALL	Wn	Call Indirect Subroutine	1	2	None
CLR	CLR	f	f = 0x0000	1	1	None
	CLR	WREG	WREG = 0x0000	1	1	None
	CLR	Ws	Ws = 0x0000	1	1	None
CLRWDT	CLRWDT		Clear Watchdog Timer	1	1	WDTO, Sleep
COM	СОМ	f	f = f	1	1	N, Z
	СОМ	f,WREG	WREG = \overline{f}	1	1	N. Z
	COM	We Wd	$Wd = \overline{Ws}$	1	1	N Z
CP	CP	f	Compare f with WREG	1	1	C DC N OV Z
01	CP	- Wb.#lit5	Compare Wb with lit5	1	1	C DC N OV Z
	CP	Wb.Ws	Compare Wb with Ws (Wb – Ws)	1	1	C, DC, N, OV, Z
CPO	CPO	f	Compare f with 0x0000	1	1	C DC N OV Z
	CP0	Ws	Compare Ws with 0x0000	1	1	C, DC, N, OV, Z
CPB	CPB	f	Compare f with WREG, with Borrow	1	1	C. DC. N. OV. Z
	CPB	Wb.#lit5	Compare Wb with lit5, with Borrow	1	1	C. DC. N. OV. Z
	CPB	Wb,Ws	Compare Wb with Ws, with Borrow $(Wb - Ws - \overline{C})$	1	1	C, DC, N, OV, Z
CPSEQ	CPSEQ	Wb,Wn	Compare Wb with Wn, Skip if =	1	1 (2 or 3)	None
CPSGT	CPSGT	Wb,Wn	Compare Wb with Wn, Skip if >	1	1 (2 or 3)	None
CPSLT	CPSLT	Wb,Wn	Compare Wb with Wn, Skip if <	1	1 (2 or 3)	None
CPSNE	CPSNE	Wb,Wn	Compare Wb with Wn, Skip if ≠	1	1 (2 or 3)	None
DAW	DAW.B	Wn	Wn = Decimal Adjust Wn	1	1	С
DEC	DEC	£	f = f -1	1	1	C, DC, N, OV, Z
	DEC	f,WREG	WREG = f-1	1	1	C, DC, N, OV, Z
	DEC	Ws,Wd	Wd = Ws - 1	1	1	C, DC, N, OV, Z
DEC2	DEC2	f	f = f - 2	1	1	C, DC, N, OV, Z
	DEC2	f,WREG	WREG = f – 2	1	1	C, DC, N, OV, Z
	DEC2	Ws,Wd	Wd = Ws - 2	1	1	C, DC, N, OV, Z
DISI	DISI	#lit14	Disable Interrupts for k Instruction Cycles	1	1	None
DIV	DIV.SW	Wm,Wn	Signed 16/16-bit Integer Divide	1	18	N, Z, C, OV
	DIV.SD	Wm,Wn	Signed 32/16-bit Integer Divide	1	18	N, Z, C, OV
	DIV.UW	Wm,Wn	Unsigned 16/16-bit Integer Divide	1	18	N, Z, C, OV
	DIV.UD	Wm,Wn	Unsigned 32/16-bit Integer Divide	1	18	N, Z, C, OV
EXCH	EXCH	Wns,Wnd	Swap Wns with Wnd	1	1	None
FBCL	FFBCL	Ws, Wnd	Find Bit Change from left (MSb) Side	1	1	None
FF1L	FF1L	Ws,Wnd	Find First One from Left (MSb) Side	1	1	С
FF1R	FF1R	Ws,Wnd	Find First One from Right (LSb) Side	1	1	С

TABLE 26-2: INSTRUCTION SET OVERVIEW (CONTINUED)

TABLE 26-2:	INSTRUCTION SET OVERVIEW (C	CONTINUED)
		, out into ED

Assembly Mnemonic	Assembly Syntax		Description	# of Words	# of Cycles	Status Flags Affected
PWRSAV	PWRSAV	#lit1	Go into Sleep or Idle mode	1	1	WDTO, Sleep
RCALL	RCALL	Expr	Relative Call	1	2	None
	RCALL	Wn	Computed Call	1	2	None
REPEAT	REPEAT	#lit14	Repeat Next Instruction lit14 + 1 times	1	1	None
	REPEAT	Wn	Repeat Next Instruction (Wn) + 1 times	1	1	None
RESET	RESET		Software Device Reset	1	1	None
RETFIE	RETFIE		Return from Interrupt	1	3 (2)	None
RETLW	RETLW	#lit10,Wn	Return with Literal in Wn	1	3 (2)	None
RETURN	RETURN		Return from Subroutine	1	3 (2)	None
RLC	RLC	f	f = Rotate Left through Carry f	1	1	C, N, Z
	RLC	f,WREG	WREG = Rotate Left through Carry f	1	1	C, N, Z
	RLC	Ws,Wd	Wd = Rotate Left through Carry Ws	1	1	C, N, Z
RLNC	RLNC	f	f = Rotate Left (No Carry) f	1	1	N, Z
	RLNC	f,WREG	WREG = Rotate Left (No Carry) f	1	1	N, Z
	RLNC	Ws,Wd	Wd = Rotate Left (No Carry) Ws	1	1	N, Z
RRC	RRC	f	f = Rotate Right through Carry f	1	1	C, N, Z
	RRC	f,WREG	WREG = Rotate Right through Carry f	1	1	C, N, Z
	RRC	Ws,Wd	Wd = Rotate Right through Carry Ws	1	1	C, N, Z
RRNC	RRNC	f	f = Rotate Right (No Carry) f	1	1	N, Z
	RRNC	f,WREG	WREG = Rotate Right (No Carry) f	1	1	N, Z
	RRNC	Ws,Wd	Wd = Rotate Right (No Carry) Ws	1	1	N, Z
SE	SE	Ws,Wnd	Wnd = Sign-Extended Ws	1	1	C, N, Z
SETM	SETM	f	f = FFFFh	1	1	None
	SETM	WREG	WREG = FFFFh	1	1	None
	SETM	Ws	Ws = FFFFh	1	1	None
SL	SL	f	f = Left Shift f	1	1	C, N, OV, Z
	SL	f,WREG	WREG = Left Shift f	1	1	C, N, OV, Z
	SL	Ws,Wd	Wd = Left Shift Ws	1	1	C, N, OV, Z
	SL	Wb,Wns,Wnd	Wnd = Left Shift Wb by Wns	1	1	N, Z
	SL	Wb,#lit4,Wnd	Wnd = Left Shift Wb by lit4	1	1	N, Z
SUB	SUB	f	f = f – WREG	1	1	C, DC, N, OV, Z
	SUB	f,WREG	WREG = f – WREG	1	1	C, DC, N, OV, Z
	SUB	#lit10,Wn	Wn = Wn - lit10	1	1	C, DC, N, OV, Z
	SUB	Wb,Ws,Wd	Wd = Wb – Ws	1	1	C, DC, N, OV, Z
	SUB	Wb,#lit5,Wd	Wd = Wb - lit5	1	1	C, DC, N, OV, Z
SUBB	SUBB	f	$f = f - WREG - (\overline{C})$	1	1	C, DC, N, OV, Z
	SUBB	f,WREG	WREG = $f - WREG - (\overline{C})$	1	1	C, DC, N, OV, Z
	SUBB	#lit10.Wn	$Wn = Wn - lit10 - (\overline{C})$	1	1	C. DC. N. OV. Z
	SUBB	Wh Ws Wd	$Wd = Wb - Ws - (\overline{C})$	1	1	C DC N OV Z
	CUDD		$Wd = Wb$ life $\overline{(C)}$	1	1	
CUDD	CUDD	4 f	$f = WPEC \qquad f$	1	1	
SUBR	CUDD		WPEG - WPEG f	1	1	
	CUDD	I, WREG	Wd - Wo Wb	1	1	
	CUDD	WD, WS, WQ	Wd - lit5 Wb	1	1	
GUDDD	SUBR	wb,#1105,wd		1	1	
SUBBR	SUBBR	Í.	f = WREG - f - (C)	1	1	C, DC, N, OV, Z
	SUBBR	f,WREG	WREG = WREG – † – (C) —	1	1	C, DC, N, OV, Z
	SUBBR	Wb,Ws,Wd	Wd = Ws - Wb - (C)	1	1	C, DC, N, OV, Z
	SUBBR	Wb,#lit5,Wd	Wd = lit5 - Wb - (C)	1	1	C, DC, N, OV, Z
SWAP	SWAP.b	Wn	Wn = Nibble Swap Wn	1	1	None
	SWAP	Wn	Wn = Byte Swap Wn	1	1	None

DC CHARACTERISTICS			$\begin{array}{llllllllllllllllllllllllllllllllllll$					
Param No.	Sym	Characteristic	Min	Typ ⁽¹⁾	Max	Units	Conditions	
DI31	IPU	Maximum Load Current	—	_	30	μA	VDD = 2.0V	
		for Digital High Detection with Internal Pull-up		—	100	μA	VDD = 3.3V	
	lı∟	Input Leakage Current ^(2,3)						
DI50		I/O Ports	—	-	<u>+</u> 1	μA	$\label{eq:VSS} \begin{split} &V{\sf SS} \leq V{\sf PIN} \leq V{\sf DD}, \\ &P{\rm in \ at \ high-impedance} \end{split}$	
DI51		Analog Input Pins	—	_	<u>+</u> 1	μA	$\label{eq:VSS} \begin{split} &V{\sf SS} \leq V{\sf PIN} \leq V{\sf DD}, \\ &P{\rm in \ at \ high-impedance} \end{split}$	
DI55		MCLR	—	—	<u>+</u> 1	μA	$Vss \leq V \text{PIN} \leq V \text{DD}$	
DI56		OSCI	—	—	<u>+</u> 1	μA	$\label{eq:VSS} \begin{array}{l} VSS \leq VPIN \leq VDD, \\ XT \text{ and } HS \text{ modes} \end{array}$	
DI60a	licl	Input Low Injection Current	0		₋₅ (5,8)	mA	All pins exce <u>pt VDD</u> , VSS, AVDD, AVSS, MCLR, VCAP, RB11, SOSCI, SOSCO, D+, D-, VUSB, and VBUS	
DI60b	lісн	Input High Injection Current	0		+5 ^(6,7,8)	mA	All pins except VDD, VSS, AVDD, AVSS, MCLR, VCAP, RB11, SOSCI, SOSCO, D+, D-, VUSB, and VBUS, and all 5V tolerant pins ⁽⁷⁾	
DI60c	∑lict	Total Input Injection Current (sum of all I/O and control pins)	-20(9)	_	+20 ⁽⁹⁾	mA	Absolute instantaneous sum of all ± input injection currents from all I/O pins (IICL + IICH) $\leq \sum$ IICT)	

TABLE 27-7: DC CHARACTERISTICS: I/O PIN INPUT SPECIFICATIONS (CONTINUED)

Note 1: Data in "Typ" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

- 2: The leakage current on the MCLR pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.
- **3:** Negative current is defined as current sourced by the pin.
- **4:** Refer to Table 1-2 for I/O pin buffer types.
- 5: Parameter is characterized but not tested.
- **6:** Non-5V tolerant pins, VIH source > (VDD + 0.3), 5V tolerant pins VIH source > 5.5V. Characterized but not tested.
- **7:** Digital 5V tolerant pins cannot tolerate any "positive" input injection current from input sources greater than 5.5V.
- 8: Injection currents > | 0 | can affect the performance of all analog peripherals (e.g., A/D, comparators, internal band gap reference, etc.)
- **9:** Any number and/or combination of I/O pins not excluded under IICL or IICH conditions are permitted provided the mathematical "absolute instantaneous" sum of the input injection currents from all pins do not exceed the specified limit. Characterized but not tested.

28.0 PACKAGING INFORMATION

28.1 Package Marking Information

28-Lead SPDIP (.300")



Example



28-Lead SSOP (5.30 mm)



Example



28-Lead SOIC (7.50 mm)



Example



Legend:	XXX	Customer-specific information					
	Y	Year code (last digit of calendar year)					
	ΥY	Year code (last 2 digits of calendar year)					
	WW	Week code (week of January 1 is week '01')					
	NNN	Alphanumeric traceability code					
		Pb-free JEDEC designator for Matte Tin (Sn)					
	*	This package is Pb-free. The Pb-free JEDEC designator ((e_3))					
		can be found on the outer packaging for this package.					
Note:	In the eve	nt the full Microchip part number cannot be marked on one line, it will					
	be carried over to the next line, thus limiting the number of available characters for customer-specific information.						

28.2 Package Details

The following sections give the technical details of the packages.

28-Lead Skinny Plastic Dual In-Line (SP) – 300 mil Body [SPDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units		INCHES		
Dimension	Dimension Limits		NOM	MAX	
Number of Pins	N	28			
Pitch	е	.100 BSC			
Top to Seating Plane	А	-	-	.200	
Molded Package Thickness	A2	.120	.135	.150	
Base to Seating Plane	A1	.015	-	-	
Shoulder to Shoulder Width	Е	.290	.310	.335	
Molded Package Width	E1	.240	.285	.295	
Overall Length	D	1.345	1.365	1.400	
Tip to Seating Plane	L	.110	.130	.150	
Lead Thickness	С	.008	.010	.015	
Upper Lead Width	b1	.040	.050	.070	
Lower Lead Width	b	.014	.018	.022	
Overall Row Spacing §	eB	_	-	.430	

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.

2. § Significant Characteristic.

3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.

4. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-070B

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44-Lead Plastic Quad Flat, No Lead Package (ML) - 8x8 mm Body [QFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	MILLIMETERS					
Dimension	MIN	NOM	MAX			
Number of Pins	N	44				
Pitch	е		0.65 BSC			
Overall Height	A	0.80 0.90 1.00				
Standoff	A1	0.00	0.02	0.05		
Terminal Thickness	A3	0.20 REF				
Overall Width	E	8.00 BSC				
Exposed Pad Width	E2	6.25	6.45	6.60		
Overall Length	D	8.00 BSC				
Exposed Pad Length D2		6.25	6.45	6.60		
Terminal Width	b	0.20	0.30	0.35		
Terminal Length	L	0.30	0.40	0.50		
Terminal-to-Exposed-Pad	K	0.20	-	-		

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.

2. Package is saw singulated

3. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension. usually without tolerance. for information purposes only.

Microchip Technology Drawing C04-103C Sheet 2 of 2

44-Lead Plastic Thin Quad Flatpack (PT) – 10x10x1 mm Body, 2.00 mm [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units	MILLIMETERS			
Dimensio	n Limits	MIN	NOM	MAX	
Number of Leads	Ν	44			
Lead Pitch	е	0.80 BSC			
Overall Height	А	-	-	1.20	
Molded Package Thickness	A2	0.95	1.00	1.05	
Standoff	A1	0.05	-	0.15	
Foot Length	L	0.45	0.60	0.75	
Footprint	L1	1.00 REF			
Foot Angle	φ	0°	3.5°	7°	
Overall Width	Е	12.00 BSC			
Overall Length	D	12.00 BSC			
Molded Package Width	E1	10.00 BSC			
Molded Package Length	D1	10.00 BSC			
Lead Thickness	с	0.09 – 0.20			
Lead Width	b	0.30	0.37	0.45	
Mold Draft Angle Top	α	11°	12°	13°	
Mold Draft Angle Bottom	β	11°	12°	13°	

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.

2. Chamfers at corners are optional; size may vary.

3. Dimensions D1 and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25 mm per side.

- 4. Dimensioning and tolerancing per ASME Y14.5M.
 - BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-076B