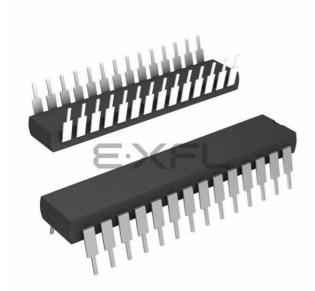
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Details	
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Connectivity	I ² C, PMP, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LVD, POR, PWM, WDT
Number of I/O	21
Program Memory Size	32KB (11K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 10x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
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TABLE 4-8: OUTPUT COMPARE REGISTER MAP

			•••••		LOIOI													
File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
OC1RS	0180							Output 0	Compare 1	Secondary	Register							FFFF
OC1R	0182							Οι	tput Comp	are 1 Regis	ter							FFFF
OC1CON	0184	_	—	OCSIDL	_	_	—	—	_	_	—	—	OCFLT	OCTSEL	OCM2	OCM1	OCM0	0000
OC2RS	0186							Output 0	Compare 2	Secondary	Register							FFFF
OC2R	0188							Οι	tput Comp	are 2 Regis	ter							FFFF
OC2CON	018A	_	_	OCSIDL	_	_	_	_	_	_	_	_	OCFLT	OCTSEL	OCM2	OCM1	OCM0	0000
OC3RS	018C							Output 0	Compare 3	Secondary	Register							FFFF
OC3R	018E							Οι	tput Comp	are 3 Regis	ter							FFFF
OC3CON	0190	_	_	OCSIDL	_	_	_	_	_	_	_	_	OCFLT	OCTSEL	OCM2	OCM1	OCM0	0000
OC4RS	0192							Output 0	Compare 4	Secondary	Register							FFFF
OC4R	0194							Οι	tput Comp	are 4 Regis	ter							FFFF
OC4CON	0196	_	_	OCSIDL	_	_	_	_	_	_	_	_	OCFLT	OCTSEL	OCM2	OCM1	OCM0	0000
OC5RS	0198							Output (Compare 5	Secondary	Register							FFFF
OC5R	019A							Οι	tput Comp	are 5 Regis	ter							FFFF
OC5CON	019C	_	_	OCSIDL	_	_	—	—	—	_	—	—	OCFLT	OCTSEL	OCM2	OCM1	OCM0	0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-9: I²C[™] REGISTER MAP

	-																	
File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
I2C1RCV	0200	_		—	_	_	_	—	—				I2C1 Recei	ve Register				0000
I2C1TRN	0202	_	_	_	_	_	_	_	_				I2C1 Transr	nit Register	r			OOFF
I2C1BRG	0204	_	_	_	_	_	_	_				Baud Rate	Generator	Register 1				0000
I2C1CON	0206	I2CEN	_	I2CSIDL	SCLREL	IPMIEN	A10M	DISSLW	SMEN	GCEN	STREN	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN	1000
I2C1STAT	0208	ACKSTAT	TRSTAT	_	_	_	BCL	GCSTAT	ADD10	IWCOL	I2COV	D/A	Р	S	R/W	RBF	TBF	0000
I2C1ADD	020A	_	_	_	_	_	_					I2C1 Addre	ss Register					0000
I2C1MSK	020C	_	_	_	_	_	_	AMSK9	AMSK8	AMSK7	AMSK6	AMSK5	AMSK4	AMSK3	AMSK2	AMSK1	AMSK0	0000
I2C2RCV	0210	_	—	_	_	_	_	_	_				I2C2 Receiv	ve Register				0000
I2C2TRN	0212	_	—	_	_	_	_	_	_				I2C2 Transr	nit Register	r			OOFF
I2C2BRG	0214	_	—	_	_	_	_	_				Baud Rate	Generator	Register 2				0000
I2C2CON	0216	I2CEN	—	I2CSIDL	SCLREL	IPMIEN	A10M	DISSLW	SMEN	GCEN	STREN	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN	1000
I2C2STAT	0218	ACKSTAT	TRSTAT	_	_	_	BCL	GCSTAT	ADD10	IWCOL	I2COV	D/A	Р	S	R/W	RBF	TBF	0000
I2C2ADD	021A	_		_	_	_	_		•		•	I2C2 Addre	ss Register		•	•	•	0000
I2C2MSK	021C	_		_	_	_	—	AMSK9	AMSK8	AMSK7	AMSK6	AMSK5	AMSK4	AMSK3	AMSK2	AMSK1	AMSK0	0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

R/SO-0	R/W-0	R/W-0	U-0	U-0	U-0	U-0	U-0
WR	WREN	WRERR	—	—	—	—	—
bit 15							bit 8
				DAALO	DAMA	DAMA	DAMO
U-0	R/W-0	U-0	U-0	R/W-0 NVMOP3 ⁽¹⁾	R/W-0 NVMOP2 ⁽¹⁾	R/W-0 NVMOP1 ⁽¹⁾	R/W-0 NVMOP0 ⁽¹⁾
	ERASE	—	—	NVMOP3	NVMOP207	NVMOP1**	
bit 7							bit
Legend:		SO = Settable	Only bit				
R = Reada	able bit	W = Writable	bit	U = Unimplem	nented bit, read	as '0'	
-n = Value	at POR	'1' = Bit is set		'0' = Bit is clea	ared	x = Bit is unkr	iown
bit 14 bit 13	0 = Program WREN: Write 1 = Enables 0 = Inhibits F WRERR: Writ 1 = An impro- automatic	Flash program/ lash program/e te Sequence E oper program cally on any se	tion is complet erase operation rror Flag bit or erase seq t attempt of the	e and inactive ns is uence attempt WR bit)	or terminatio	n has occurre	ed (bit is s
1 1 40 7		ram or erase o		leted normally			
bit 12-7 bit 6	=	ted: Read as ' e/Program Ena					
DIL O	1 = Performs	the erase ope	ration specified	l by the NVMOI fied by the NVM			
bit 5-4	Unimplemen	ted: Read as ')'				
bit 3-0	NVMOP<3:0>	-: NVM Operat	ion Select bits ⁽	1)			
	0011 = Memo 0010 = Memo	ory word progra	m operation (E operation (ER	SE = 1) or no o ERASE = 0) or 1 ASE = 1) or no RASE = 0) or no	no operation (E operation (ER/	RASE = 1) ASE = 0)	
Note 1:	All other combina	tions of NVMO	P<3:0> are uni	implemented.			
2:	Available in ICSP						

REGISTER 5-1: NVMCON: FLASH MEMORY CONTROL REGISTER

REGISTER 6-1: RCON: RESET CONTROL REGISTER⁽¹⁾ (CONTINUED)

- bit 2 IDLE: Wake-up from Idle Flag bit 1 = Device has been in Idle mode
 - 0 = Device has not been in Idle mode
- bit 1 BOR: Brown-out Reset Flag bit
 - 1 = A Brown-out Reset has occurred (note that BOR is also set after a Power-on Reset)
 - 0 = A Brown-out Reset has not occurred
- bit 0 **POR:** Power-on Reset Flag bit
 - 1 = A Power-on Reset has occurred
 - 0 = A Power-on Reset has not occurred
- **Note 1:** All of the Reset status bits may be set or cleared in software. Setting one of these bits in software does not cause a device Reset.
 - 2: If the FWDTEN Configuration bit is '1' (unprogrammed), the WDT is always enabled, regardless of the SWDTEN bit setting.

Flag Bit	Setting Event	Clearing Event
TRAPR (RCON<15>)	Trap Conflict Event	POR
IOPUWR (RCON<14>)	Illegal Opcode or Uninitialized W Register Access	POR
CM (RCON<9>)	Configuration Mismatch Reset	POR
EXTR (RCON<7>)	MCLR Reset	POR
SWR (RCON<6>)	RESET Instruction	POR
WDTO (RCON<4>)	WDT Time-out	PWRSAV Instruction, POR
SLEEP (RCON<3>)	PWRSAV #SLEEP Instruction	POR
IDLE (RCON<2>)	PWRSAV #IDLE Instruction	POR
BOR (RCON<1>)	POR, BOR	—
POR (RCON<0>)	POR	—

TABLE 6-1: RESET FLAG BIT OPERATION

Note: All Reset flag bits may be set or cleared by the user software.

NOTES:

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
_	—	AD1IF	U1TXIF	U1RXIF	SPI1IF	SPF1IF	T3IF
bit 15			•			·	bit 8
R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
T2IF	OC2IF	IC2IF	_	T1IF	OC1IF	IC1IF	INTOIF
bit 7	002li	10211			00111	10111	bit
Legend:							
R = Readab	le bit	W = Writable	bit	U = Unimplem	nented bit. rea	d as '0'	
-n = Value a	t POR	'1' = Bit is set		'0' = Bit is clea		x = Bit is unkn	iown
bit 15-14	Unimpleme	nted: Read as '	0'				
bit 13	AD1IF: A/D	Conversion Cor	nplete Interrup	t Flag Status bit			
	1 = Interrupt	request has oc request has no	curred	U			
bit 12	•	RT1 Transmitte		Status bit			
	1 = Interrupt	request has oc	curred				
L:1 4 4	•	request has no					
oit 11		RT1 Receiver li request has oc					
		request has no					
bit 10	-	1 Event Interrup		it			
	1 = Interrupt	request has oc request has no	curred				
bit 9		1 Fault Interrup		it			
bit 0		request has oc	•	it i			
	•	request has no					
bit 8	T3IF: Timer3	B Interrupt Flag	Status bit				
		request has oc request has no					
bit 7	T2IF: Timer2	2 Interrupt Flag	Status bit				
	•	request has oc					
hit C	•	request has no		nt Flag Status k	.:+		
bit 6	-	out Compare Ch request has oc		pi riag Status i	JIL		
	•	request has no					
bit 5	IC2IF: Input	Capture Chann	el 2 Interrupt F	lag Status bit			
	•	request has oc request has no					
bit 4	-	nted: Read as '					
bit 3	-	Interrupt Flag					
		request has oc					
		request has no					
bit 2	-	out Compare Ch		pt Flag Status b	pit		
		request has oc					
		request has no					

REGISTER 7-5: IFS0: INTERRUPT FLAG STATUS REGISTER 0

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
_	_	AD1IE	U1TXIE	U1RXIE	SPI1IE	SPF1IE	T3IE
bit 15				•			bit
R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
T2IE	OC2IE	IC2IE	—	T1IE	OC1IE	IC1IE	INT0IE ⁽¹⁾
bit 7							bit
Legend:							
R = Readable	e bit	W = Writable	bit	U = Unimplem	ented bit, read	l as '0'	
-n = Value at	POR	'1' = Bit is set		'0' = Bit is clea	red	x = Bit is unkn	iown
bit 15-14	-	ted: Read as '					
bit 13			nplete Interrup	t Enable bit			
	•	equest is enab equest is not e					
bit 12	-	-	r Interrupt Enal	hle hit			
		equest is enab	•				
		equest is not e					
bit 11	U1RXIE: UAR	RT1 Receiver In	nterrupt Enable	e bit			
		equest is enab equest is not e					
bit 10	-	-	olete Interrupt I	Enable bit			
		equest is enab	•				
	•	equest is not e					
bit 9		Fault Interrup					
		equest is enab equest is not e					
bit 8	-	Interrupt Enab					
		equest is enab					
	0 = Interrupt r	equest is not e	nabled				
bit 7		Interrupt Enab					
	•	equest is enab					
bit 6	•	equest is not e	annel 2 Interru	unt Enable bit			
	-	equest is enab					
		equest is not e					
bit 5	IC2IE: Input C	Capture Chann	el 2 Interrupt E	nable bit			
	•	equest is enab					
L:1 1	-	equest is not e					
bit 4 bit 3	-	ted: Read as '					
UIL J	I IIE. IIIIief I	Interrupt Enab					
	1 = Interrupt r	equest is enab	led				

REGISTER 7-10: IEC0: INTERRUPT ENABLE CONTROL REGISTER 0

Note 1: If INTxIE = 1, this external interrupt input must be configured to an available RPn pin. See Section 10.4 "Peripheral Pin Select (PPS)" for more information.

	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
	T4IP2	T4IP1	T4IP0	_	OC4IP2	OC4IP1	OC4IP0
bit 15							bit 8
U-0	R/W-1	R/W-0	R/W-0	U-0	U-0	U-0	U-0
 bit 7	OC3IP2	OC3IP1	OC3IP0	_	_	_	bit (
							Ditt
Legend:							
R = Readab	ole bit	W = Writable	bit	U = Unimplen	nented bit, read	d as '0'	
-n = Value a	at POR	'1' = Bit is set		'0' = Bit is clea	ared	x = Bit is unkr	nown
bit 15	Unimplemen	ted: Read as '	0'				
bit 14-12	T4IP<2:0>: ⊺i	imer4 Interrupt	Priority bits				
	111 = Interrup	pt is Priority 7 (highest priority	/ interrupt)			
	•						
	•						
	•						
	• 001 = Interrup	pt is Priority 1					
		pt is Priority 1 pt source is dis	abled				
bit 11	000 = Interru						
bit 11 bit 10-8	000 = Interrup Unimplemen	pt source is dis ted: Read as '	0'	Interrupt Priorit	/ bits		
	000 = Interru Unimplemen OC4IP<2:0>:	pt source is dis ted: Read as '	^{0'} are Channel 4	• •	/ bits		
	000 = Interru Unimplemen OC4IP<2:0>:	pt source is dis ted: Read as ' Output Compa	^{0'} are Channel 4	• •	/ bits		
	000 = Interru Unimplemen OC4IP<2:0>:	pt source is dis ted: Read as ' Output Compa	^{0'} are Channel 4	• •	/ bits		
	000 = Interru Unimplemen OC4IP<2:0>:	pt source is dis ted: Read as ' Output Compa pt is Priority 7 (^{0'} are Channel 4	• •	y bits		
	000 = Interrup Unimplement OC4IP<2:0>: 111 = Interrup	pt source is dis ted: Read as ' Output Compa pt is Priority 7 (^{0'} are Channel 4 highest priority	• •	/ bits		
	000 = Interrup Unimplemen OC4IP<2:0>: 111 = Interrup	pt source is dis ted: Read as ' Output Compa pt is Priority 7 (pt is Priority 1	₀ ' are Channel 4 highest priority abled	• •	/ bits		
bit 10-8	000 = Interrup Unimplement OC4IP<2:0>: 111 = Interrup	pt source is dis ted: Read as ' Output Compa pt is Priority 7 (pt is Priority 1 pt source is dis ted: Read as '	^{0'} are Channel 4 highest priority abled 0'	• •			
bit 10-8 bit 7	000 = Interrup Unimplement OC4IP<2:0>: 111 = Interrup 001 = Interrup 000 = Interrup Unimplement OC3IP<2:0>:	pt source is dis ted: Read as ' Output Compa pt is Priority 7 (pt is Priority 1 pt source is dis ted: Read as '	^{0'} are Channel 4 highest priority abled ^{0'} are Channel 3	y interrupt) Interrupt Priority			
bit 10-8 bit 7	000 = Interrup Unimplement OC4IP<2:0>: 111 = Interrup 001 = Interrup 000 = Interrup Unimplement OC3IP<2:0>:	pt source is dis ted: Read as ' Output Compa pt is Priority 7 (pt is Priority 1 pt source is dis ted: Read as ' Output Compa	^{0'} are Channel 4 highest priority abled ^{0'} are Channel 3	y interrupt) Interrupt Priority			
bit 10-8 bit 7	000 = Interrup Unimplement OC4IP<2:0>: 111 = Interrup 001 = Interrup 000 = Interrup Unimplement OC3IP<2:0>:	pt source is dis ted: Read as ' Output Compa pt is Priority 7 (pt is Priority 1 pt source is dis ted: Read as ' Output Compa	^{0'} are Channel 4 highest priority abled ^{0'} are Channel 3	y interrupt) Interrupt Priority			
bit 10-8 bit 7	000 = Interrup Unimplement OC4IP<2:0>: 111 = Interrup 001 = Interrup 000 = Interrup Unimplement OC3IP<2:0>:	pt source is dis ted: Read as ' Output Compa pt is Priority 7 (pt is Priority 1 pt source is dis ted: Read as ' Output Compa pt is Priority 7 (^{0'} are Channel 4 highest priority abled ^{0'} are Channel 3	y interrupt) Interrupt Priority			
bit 10-8 bit 7	000 = Interrup Unimplement OC4IP<2:0>: 111 = Interrup 001 = Interrup 000 = Interrup Unimplement OC3IP<2:0>: 111 = Interrup 001 = Interrup	pt source is dis ted: Read as ' Output Compa pt is Priority 7 (pt is Priority 1 pt source is dis ted: Read as ' Output Compa pt is Priority 7 (^{0'} are Channel 4 highest priority abled 0' are Channel 3 highest priority	y interrupt) Interrupt Priority			

REGISTER 7-21: IPC6: INTERRUPT PRIORITY CONTROL REGISTER 6

REGISTER 7-25: IPC10: INTERRUPT PRIORITY CONTROL REGISTER 10

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
_	—			—	—	—	_
bit 15							bit 8
U-0	R/W-1	R/W-0	R/W-0	U-0	U-0	U-0	U-0
_	OC5IP2	OC5IP1	OC5IP0	—	—	—	—
bit 7				·			bit 0
Legend:							
R = Readable	e bit	W = Writable	bit	U = Unimplen	nented bit, read	l as '0'	
-n = Value at	POR	'1' = Bit is set		'0' = Bit is clea	ared	x = Bit is unkr	iown
bit 15-7	Unimplemen	ted: Read as '	0'				
bit 6-4	OC5IP<2:0>:	Output Compa	are Channel 5 I	Interrupt Priority	y bits		
	111 = Interru	pt is Priority 7 (highest priority	/ interrupt)			
	•						
	•						
	•						
	001 = Interru						
	000 = Interru	pt source is dis	abled				

bit 3-0 Unimplemented: Read as '0'

REGISTER 7-26: IPC11: INTERRUPT PRIORITY CONTROL REGISTER 11

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	
_	—	—	—	—	—	—	—	
bit 15							bit 8	
U-0	R/W-1	R/W-0	R/W-0	U-0	U-0	U-0	U-0	
_	PMPIP2	PMPIP1	PMPIP0	—	—	—		
bit 7							bit 0	
Legend:								
R = Readab	le bit	W = Writable	bit	U = Unimplem	nented bit, read	l as '0'		
-n = Value a	t POR	'1' = Bit is set		'0' = Bit is clea	ared	x = Bit is unknown		
bit 15-7	Unimplemen	ted: Read as '0)'					
bit 6-4	PMPIP<2:0>	: Parallel Maste	r Port Interrupt	t Priority bits				
	111 = Interru	pt is Priority 7 (highest priority	interrupt)				
	•							
	•							
	•							
	001 = Interru	pt is Priority 1						
	000 = Interru	pt source is dis	abled					
bit 3-0	Unimplemen	ted: Read as ')'					

REGISTER 8-1: OSCCON: OSCILLATOR CONTROL REGISTER (CONTINUED)

bit 7	CLKLOCK: Clock Selection Lock Enable bit
	<u>If FSCM is enabled (FCKSM1 = 1):</u>
	1 = Clock and PLL selections are locked
	0 = Clock and PLL selections are not locked and may be modified by setting the OSWEN bit
	<u>If FSCM is disabled (FCKSM1 = 0):</u>
	Clock and PLL selections are never locked and may be modified by setting the OSWEN bit.
bit 6	IOLOCK: I/O Lock Enable bit ⁽²⁾
	1 = I/O lock is active
	0 = I/O lock is not active
bit 5	LOCK: PLL Lock Status bit ⁽³⁾
	1 = PLL module is in lock or PLL module start-up timer is satisfied
	0 = PLL module is out of lock, PLL start-up timer is running or PLL is disabled
bit 4	Unimplemented: Read as '0'
bit 4 bit 3	CF: Clock Fail Detect bit
	•
	CF: Clock Fail Detect bit
	CF: Clock Fail Detect bit 1 = FSCM has detected a clock failure
bit 3	 CF: Clock Fail Detect bit 1 = FSCM has detected a clock failure 0 = No clock failure has been detected
bit 3 bit 2	 CF: Clock Fail Detect bit 1 = FSCM has detected a clock failure 0 = No clock failure has been detected Unimplemented: Read as '0'
bit 3 bit 2	CF: Clock Fail Detect bit 1 = FSCM has detected a clock failure 0 = No clock failure has been detected Unimplemented: Read as '0' SOSCEN: 32 kHz Secondary Oscillator (SOSC) Enable bit
bit 3 bit 2	 CF: Clock Fail Detect bit 1 = FSCM has detected a clock failure 0 = No clock failure has been detected Unimplemented: Read as '0' SOSCEN: 32 kHz Secondary Oscillator (SOSC) Enable bit 1 = Enables Secondary Oscillator
bit 3 bit 2 bit 1	 CF: Clock Fail Detect bit 1 = FSCM has detected a clock failure 0 = No clock failure has been detected Unimplemented: Read as '0' SOSCEN: 32 kHz Secondary Oscillator (SOSC) Enable bit 1 = Enables Secondary Oscillator 0 = Disables Secondary Oscillator
bit 3 bit 2 bit 1	 CF: Clock Fail Detect bit 1 = FSCM has detected a clock failure 0 = No clock failure has been detected Unimplemented: Read as '0' SOSCEN: 32 kHz Secondary Oscillator (SOSC) Enable bit 1 = Enables Secondary Oscillator 0 = Disables Secondary Oscillator OSWEN: Oscillator Switch Enable bit

Note 1: Reset values for these bits are determined by the FNOSCx Configuration bits.

- 2: The state of the IOLOCK bit can only be changed once an unlocking sequence has been executed. In addition, if the IOL1WAY Configuration bit is '1' once the IOLOCK bit is set, it cannot be cleared.
- 3: Also resets to '0' during any valid clock switch or whenever a non-PLL Clock mode is selected.

10.0 I/O PORTS

Note: This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information, refer to the *"PIC24F Family Reference Manual"*, *"I/O* Ports with Peripheral Pin Select (PPS)" (DS39711).

All of the device pins (except VDD, VSS, MCLR and OSCI/CLKI) are shared between the peripherals and the Parallel I/O (PIO) ports. All I/O input ports feature Schmitt Trigger inputs for improved noise immunity.

10.1 Parallel I/O (PIO) Ports

A Parallel I/O port that shares a pin with a peripheral is, in general, subservient to the peripheral. The peripheral's output buffer data and control signals are provided to a pair of multiplexers. The multiplexers select whether the peripheral or the associated port has ownership of the output data and control signals of the I/O pin. The logic also prevents "loop through", in which a port's digital output can drive the input of a peripheral that shares the same pin. Figure 10-1 shows how ports are shared with other peripherals and the associated I/O pin to which they are connected. When a peripheral is enabled and the peripheral is actively driving an associated pin, the use of the pin as a general purpose output pin is disabled. The I/O pin may be read, but the output driver for the parallel port bit will be disabled. If a peripheral is enabled, but the peripheral is not actively driving a pin, that pin may be driven by a port.

All port pins have three registers directly associated with their operation as digital I/O. The Data Direction register (TRISx) determines whether the pin is an input or an output. If the data direction bit is a '1', then the pin is an input. All port pins are defined as inputs after a Reset. Reads from the Output Latch register (LATx), read the latch. Writes to the latch, write the latch. Reads from the port (PORTx), read the port pins, while writes to the port pins, write the latch.

Any bit and its associated data and control registers that are not valid for a particular device will be disabled. That means the corresponding LATx and TRISx registers and the port pin will read as zeros.

When a pin is shared with another peripheral or function that is defined as an input only, it is nevertheless, regarded as a dedicated port because there is no other competing source of outputs.

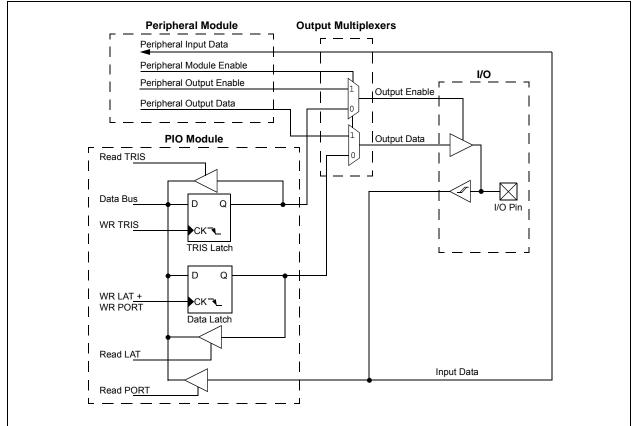


FIGURE 10-1: BLOCK DIAGRAM OF A TYPICAL SHARED PORT STRUCTURE

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
_	_	_	DISSCK ⁽¹⁾	DISSDO ⁽²⁾	MODE16	SMP	CKE ⁽³⁾
bit 15							bit
R/W-0		R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SSEN ⁽⁴⁾) CKP	MSTEN	SPRE2	SPRE1	SPRE0	PPRE1	PPRE0
bit 7							bit
Legend:							
R = Reada	able bit	W = Writable	bit	U = Unimplem	nented bit, read	as '0'	
-n = Value	at POR	'1' = Bit is set		'0' = Bit is clea		x = Bit is unkn	iown
			-				-
bit 15-13	Unimplemen	ted: Read as '	0'				
bit 12	DISSCK: Disa	ables SCKx Pi	n bit (SPI Maste	er modes only)	(1)		
			abled; pin funct	ions as I/O			
		SPI clock is en					
bit 11		ables SDOx Pi					
			y the module; p	in functions as	I/O		
bit 10		n is controlled	•	at hit			
		-	unication Seleo				
		ication is byte-	, ,				
bit 9		ata Input Sam					
	Master mode:						
			t end of data ou				
	-	a is sampled a	t middle of data	output time			
	<u>Slave mode:</u>	cleared when	SPIx is used in	Slave mode			
bit 8		lock Edge Sele					
bit 0		•		n from active c	lock state to Idl	e clock state (s	see bit 6)
					ck state to active		
bit 7	SSEN: Slave	Select Enable	bit (Slave mode	∋) ⁽⁴⁾			
		s used for Slav					
	0 = SSx pin i	s not used by	he module; pin	is controlled by	y port function		
bit 6		olarity Select					
			s a high level; a s a low level; ac				
bit 5		ter Mode Enat	-		lignievei		
DIUD	1 = Master m		ne bit				
	0 = Slave mo						
Note 1:	If DISSCK = 0, So Select (PPS)" for			available RPn	pin. See Sectio	on 10.4 "Perip	heral Pin
2:	If DISSDO = 0, S Select (PPS)" for	DOx must be o	configured to an	available RPn	pin. See Secti	on 10.4 "Perip	oheral Pin
3:	The CKE bit is no SPI modes (FRM	EN = 1).					
4:	If SSEN = 1, SSx (PPS)" for more i		gured to an ava	ilable RPn pin.	See Section 1	0.4 "Peripher	al Pin Selec

R/W-0	U-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0 ⁽³⁾	R/W-0 ⁽³⁾
UARTEN ⁽¹) _	USIDL	IREN ⁽²⁾	RTSMD	_	UEN1	UEN0
bit 15				·		•	bit 8
			D 444 A	D M M	D 444 0	D 444 A	D 444 0
R/C-0, HC		R/W-0, HC	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
WAKE	LPBACK	ABAUD	RXINV	BRGH	PDSEL1	PDSEL0	STSEL
bit 7							bit 0
Legend:		C = Clearable	hit	HC = Hardwa	are Clearable bi	t	
R = Readat	ole hit	W = Writable b			mented bit, read		
-n = Value a		'1' = Bit is set	it.	'0' = Bit is cle			
-n = value a	al POR	I = BILIS SEL		0 = Bit is cle	ared	x = Bit is unkn	IOWN
bit 15		ARTx Enable bit ⁽	1)				
bit io		s enabled; all UA		e controlled by	UARTx as defin	ed by UEN<1.)>
		s disabled; all UA					
bit 14		ted: Read as '0					
bit 13	USIDL: UAR	Tx Stop in Idle M	ode bit				
	1 = Discontir	nues module ope	ration when	device enters le	dle mode		
		es module operation					
bit 12	IREN: IrDA®	Encoder and De	coder Enabl	e bit ⁽²⁾			
		oder and decode					
bit 11		de Selection for I					
2	$1 = \overline{\text{UxRTS}} p$	oin in Simplex mo oin in Flow Contr	ode				
bit 10	•	ted: Read as '0					
bit 9-8	•	JARTx Enable bi					
	10 = UxTX, U 01 = UxTX, U	JxRX and BCLK JxRX, UxCTS ar JxRX and UxRT nd UxRX pins are	d UxRTS pins are er	ns are enabled habled and used	and used d; UxCTS pin is	controlled by F	ORT latches
bit 7	WAKE: Wake	e-up on Start Bit	Detect Durin	g Sleep Mode I	Enable bit		
	hardware	vill continue to sa e on following ris	-	RX pin; interrup	t is generated o	n falling edge, b	it is cleared in
hit C		-up is enabled	Mada Salaat	hit			
bit 6		ARTx Loopback Loopback mode		DIL			
		k mode is disabl					
bit 5		o-Baud Enable b					
	cleared i	baud rate meas n hardware upor	n completion		ter – requires re	ception of a Sy	nc field (55h);
	0 = Baud rat	e measurement	is disabled o	r completed			
	f UARTEN = 1, t Section 10.4 "Pe					vailable RPn p	in. See
	This feature is or	-					
	Bit availability de	-					

REGISTER 17-1: UXMODE: UARTX MODE REGISTER

3: Bit availability depends on pin availability.

R-0 IBF bit 15 R-1 OBE bit 7 Legend:	R/W-0, HS IBOV R/W-0, HS OBUF	U-0 — U-0 —	U-0 — U-0 —	R-0 IB3F R-1 OB3E	R-0 IB2F R-1 OB2E	R-0 IB1F R-1	R-0 IB0F bit 8 R-1	
R-1 OBE bit 7	R/W-0, HS	U-0 —	U-0 —	R-1	R-1	R-1	bit 8	
OBE bit 7	,	U-0 —	U-0	1			R-1	
OBE bit 7	,	<u> </u>	<u> </u>	1			R-1	
bit 7		—	—	OB3E	OB2E		0000	
						OB1E	OB0E bit 0	
l ogond:							DILC	
Legenu.		HS = Hardwar	e Settable bit					
R = Readabl	le bit	W = Writable b	bit	U = Unimplem	ented bit, read	l as '0'		
-n = Value at	POR	'1' = Bit is set		'0' = Bit is clea	ired	x = Bit is unkno	own	
bit 14	0 = Some or a		le Input Buffer	ull r registers are ei	mpty			
bit 14	IBOV: Input B	uffer Overflow	Status bit					
	1 = A write at 0 = No overflo		nput Byte regi	ister occurred (n	nust de cleare	a in software)		
bit 13-12	Unimplement	ted: Read as '0	,					
bit 11-8	 IB3F:IB0F: Input Buffer x Status Full bits 1 = Input Buffer x contains data that has not been read (reading buffer will clear this bit 			vill clear this bit)				
		fer x does not c			J	,		
bit 7	OBE: Output Buffer Empty Status bit							
		ble Output Buffe all of the readal		e empty ffer registers are	e full			
bit 6	OBUF: Output Buffer Underflow Status bit							
	1 = A read oc 0 = No under		empty Output	t Byte register (r	nust be cleare	d in software)		
bit 5-4	Unimplement	t ed: Read as '0	,					
bit 3-0		Output Buffer x						
				to the buffer will not been transn				

REGISTER 18-5: PMSTAT: PARALLEL PORT STATUS REGISTER

24.0 SPECIAL FEATURES

- Note: This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information, refer to the following sections of the *"PIC24F Family Reference Manual"*.
 "Watchdog Timer (WDT)" (DS39697)
 "High-Level Device Integration" (DS39719)
 - "Programming and Diagnostics" (DS39716)

PIC24FJ64GA004 family devices include several features intended to maximize application flexibility and reliability, and minimize cost through elimination of external components. These are:

- Flexible Configuration
- · Watchdog Timer (WDT)
- Code Protection
- · JTAG Boundary Scan Interface
- In-Circuit Serial Programming
- In-Circuit Emulation

24.1 Configuration Bits

The Configuration bits can be programmed (read as '0'), or left unprogrammed (read as '1'), to select various device configurations. These bits are mapped starting at program memory location, F80000h. A complete list of locations is shown in Table 24-1. A detailed explanation of the various bit functions is provided in Register 24-1 through Register 24-4.

Note that address, F80000h, is beyond the user program memory space. In fact, it belongs to the configuration memory space (800000h-FFFFFFh), which can only be accessed using table reads and table writes.

24.1.1 CONSIDERATIONS FOR CONFIGURING PIC24FJ64GA004 FAMILY DEVICES

In PIC24FJ64GA004 family devices, the configuration bytes are implemented as volatile memory. This means that configuration data must be programmed each time the device is powered up. Configuration data is stored in the two words at the top of the on-chip program memory space, known as the Flash Configuration Words. Their specific locations are shown in Table 24-1. These are packed representations of the actual device Configuration bits, whose actual locations are distributed among five locations in configuration space. The configuration data is automatically loaded from the Flash Configuration Words to the proper Configuration registers during device Resets.

Note: Configuration data is reloaded on all types of device Resets.

TABLE 24-1: FLASH CONFIGURATION WORD LOCATIONS FOR PIC24FJ64GA004 FAMILY DEVICES

Device	Configuration Word Addresses		
	1	2	
PIC24FJ16GA	002BFEh	002BFCh	
PIC24FJ32GA	0057FEh	0057FCh	
PIC24FJ48GA	0083FEh	0083FCh	
PIC24FJ64GA	00ABFEh	00ABFCh	

When creating applications for these devices, users should always specifically allocate the location of the Flash Configuration Word for configuration data. This is to make certain that program code is not stored in this address when the code is compiled.

The Configuration bits are reloaded from the Flash Configuration Word on any device Reset.

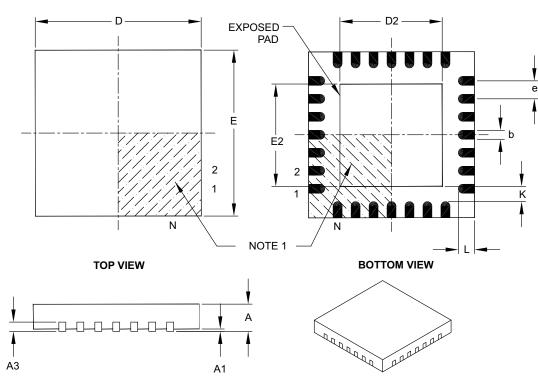
The upper byte of both Flash Configuration Words in program memory should always be '1111 1111'. This makes them appear to be NOP instructions in the remote event that their locations are ever executed by accident. Since Configuration bits are not implemented in the corresponding locations, writing '1's to these locations has no effect on device operation.

TABLE 26-1: SYMBOLS USED IN OPCODE DESCRIPTIONS

Field	Description
#text	Means literal defined by "text"
(text)	Means "content of text"
[text]	Means "the location addressed by text"
{ }	Optional field or operation
<n:m></n:m>	Register bit field
.b	Byte mode selection
.d	Double-Word mode selection
.S	Shadow register select
.W	Word mode selection (default)
bit4	4-bit bit selection field (used in word addressed instructions) $\in \{015\}$
C, DC, N, OV, Z	MCU Status bits: Carry, Digit Carry, Negative, Overflow, Sticky Zero
Expr	Absolute address, label or expression (resolved by the linker)
f	File register address ∈ {0000h1FFFh}
lit1	1-bit unsigned literal ∈ {0,1}
lit4	4-bit unsigned literal ∈ {015}
lit5	5-bit unsigned literal ∈ {031}
lit8	8-bit unsigned literal ∈ {0255}
lit10	10-bit unsigned literal \in {0255} for Byte mode, {0:1023} for Word mode
lit14	14-bit unsigned literal ∈ {016384}
lit16	16-bit unsigned literal ∈ {065535}
lit23	23-bit unsigned literal ∈ {08388608}; LSB must be '0'
None	Field does not require an entry, may be blank
PC	Program Counter
Slit10	10-bit signed literal ∈ {-512511}
Slit16	16-bit signed literal ∈ {-3276832767}
Slit6	6-bit signed literal \in {-1616}
Wb	Base W register \in {W0W15}
Wd	Destination W register \in { Wd, [Wd], [Wd++], [Wd], [++Wd], [Wd] }
Wdo	Destination W register \in { Wnd, [Wnd], [Wnd++], [Wnd], [++Wnd], [Wnd], [Wnd+Wb] }
Wm,Wn	Dividend, Divisor working register pair (direct addressing)
Wn	One of 16 working registers ∈ {W0W15}
Wnd	One of 16 destination working registers ∈ {W0W15}
Wns	One of 16 source working registers ∈ {W0W15}
WREG	W0 (working register used in file register instructions)
Ws	Source W register ∈ { Ws, [Ws], [Ws++], [Ws], [++Ws], [Ws] }
Wso	Source W register ∈ { Wns, [Wns], [Wns++], [Wns], [++Wns], [Wns], [Wns+Wb] }

28-Lead Plastic Quad Flat, No Lead Package (ML) – 6x6 mm Body [QFN] with 0.55 mm Contact Length

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units		MILLIMETERS		
	Dimension Limits	MIN	NOM	MAX	
Number of Pins	N		28		
Pitch	е		0.65 BSC		
Overall Height	A	0.80	0.90	1.00	
Standoff	A1	0.00	0.02	0.05	
Contact Thickness	A3		0.20 REF		
Overall Width	E		6.00 BSC		
Exposed Pad Width	E2	3.65	3.70	4.20	
Overall Length	D		6.00 BSC		
Exposed Pad Length	D2	3.65	3.70	4.20	
Contact Width	b	0.23	0.30	0.35	
Contact Length	L	0.50	0.55	0.70	
Contact-to-Exposed Pad	K	0.20	-	_	

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.

2. Package is saw singulated.

3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-105B

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PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

Product Group Pin Count Tape and Reel Fi		 Examples: a) PIC24FJ32GA002-I/ML: General Purpose PIC24F, 32-Kbyte Program Memory, 28-Pin, Industrial Temp., QFN Package. b) PIC24FJ64GA004-E/PT: General Purpose PIC24F, 64-Kbyte Program Memory, 44-Pin, Extended Temp., TQFP Package.
Architecture	24 = 16-bit modified Harvard without DSP	
Flash Memory Family	FJ = Flash program memory	
Product Group	GA0 = General purpose microcontrollers	
Pin Count	02 = 28-pin 04 = 44-pin	
Temperature Range	$E = -40^{\circ}C \text{ to } +125^{\circ}C \text{ (Extended)}$ I = -40^{\circ}C \text{ to } +85^{\circ}C \text{ (Industrial)}	
Package	SP = SPDIP SO = SOIC SS = SSOP ML = QFN PT = TQFP	
Pattern	Three-digit QTP, SQTP, Code or Special Requirements (blank otherwise) ES = Engineering Sample	