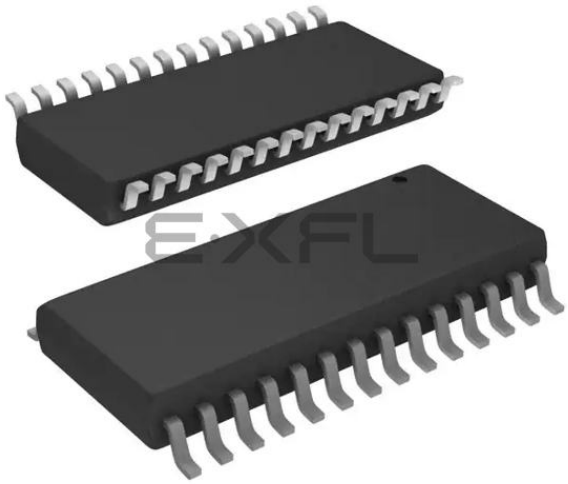

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What is "Embedded - Microcontrollers"?

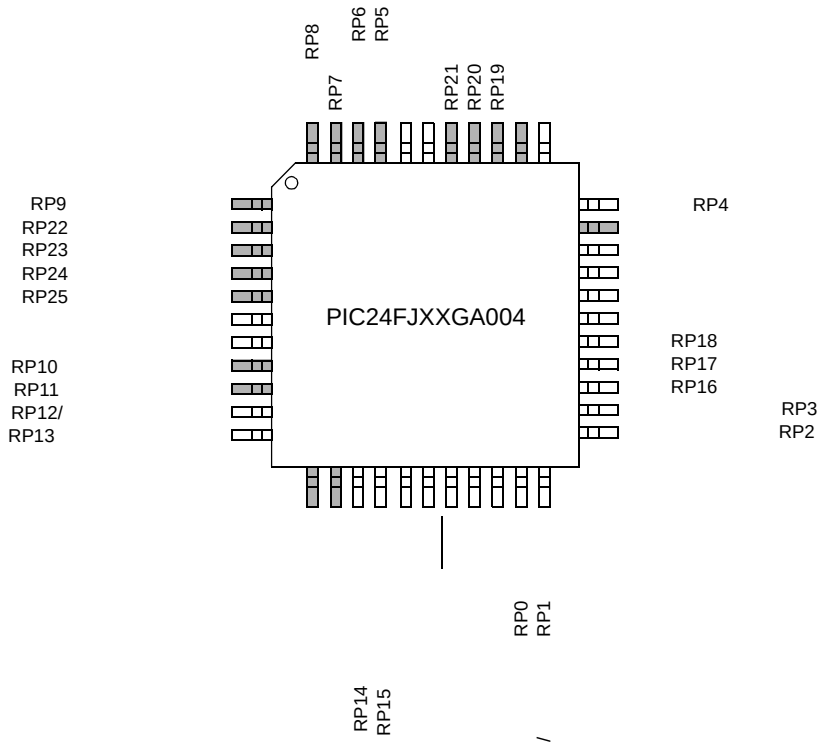
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	PIC
Core Size	16-Bit
Speed	32MHz
Connectivity	I²C, PMP, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LVD, POR, PWM, WDT
Number of I/O	21
Program Memory Size	32KB (11K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 10x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	28-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24fj32ga002t-i-so

Pin Diagrams (Continued)

44-Pin TQFP



Legend: RPn

TABLE 1-2: PIC24FJ64GA004 FAMILY PINOUT DESCRIPTIONS (CONTINUED)

Function	Pin Number			I/O	Input Buffer	Description
	28-Pin SPDIP/ SSOP/SOIC	28-Pin QFN	44-Pin QFN/TQFP			

Legend:

Note 1:

2.2 Power Supply Pins

Value and type of capacitor: P

Placement on the printed circuit board:

Handling high-frequency noise:

P P

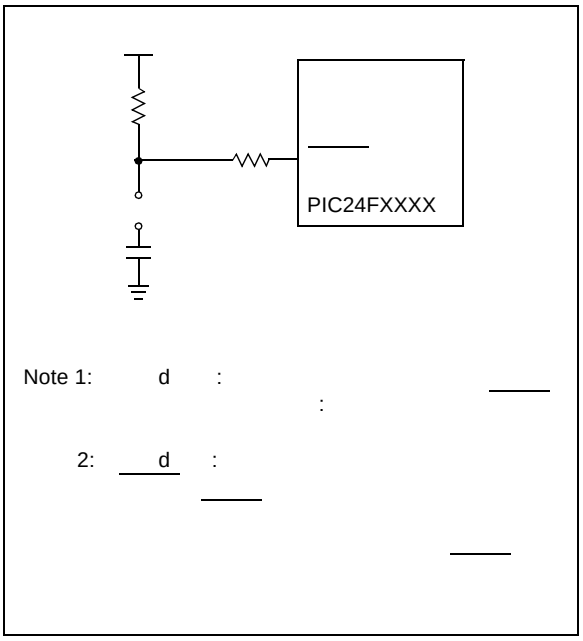
P P

Maximizing performance:

P P

2.3 Master Clear (MCLR) Pin

FIGURE 2-2: EXAMPLE OF MCLR PIN CONNECTIONS



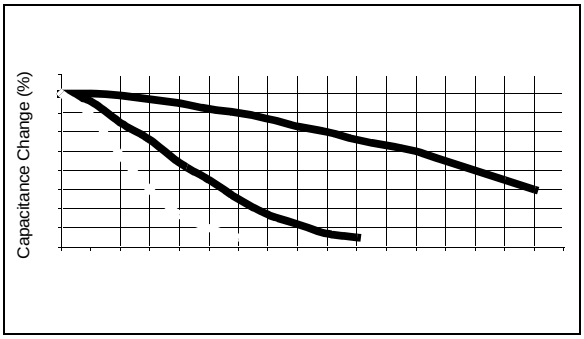
Note 1: d :

:

2: d :

/

FIGURE 2-4: DC BIAS VOLTAGE vs. CAPACITANCE CHARACTERISTICS



P

2.5 ICSP Pins

P

Ω

EXAMPLE 5-2: LOADING THE WRITE BUFFERS

```
; Set up NVMCON for row programming operations
       MOV      #0x4001, W0                    ;
       MOV      W0, NVMCON                     ; Initialize NVMCON
; Set up a pointer to the first program memory location to be written
; program memory selected, and writes enabled
       MOV      #0x0000, W0                    ;
       MOV      W0, TBLPAG                     ; Initialize PM Page Boundary SFR
       MOV      #0x6000, W0                    ; An example program memory address
; Perform the TBLWT instructions to write the latches
; 0th_program_word
       MOV      #LOW_WORD_0, W2                ;
       MOV      #HIGH_BYTE_0, W3               ;
       TBLWTL   W2, [W0]                       ; Write PM low word into program latch
       TBLWTH   W3, [W0++]                     ; Write PM high byte into program latch
; 1st_program_word
       MOV      #LOW_WORD_1, W2                ;
       MOV      #HIGH_BYTE_1, W3               ;
       TBLWTL   W2, [W0]                       ; Write PM low word into program latch
       TBLWTH   W3, [W0++]                     ; Write PM high byte into program latch
; 2nd_program_word
       MOV      #LOW_WORD_2, W2                ;
       MOV      #HIGH_BYTE_2, W3               ;
       TBLWTL   W2, [W0]                       ; Write PM low word into program latch
       TBLWTH   W3, [W0++]                     ; Write PM high byte into program latch



; 63rd_program_word
       MOV      #LOW_WORD_31, W2               ;
       MOV      #HIGH_BYTE_31, W3              ;
       TBLWTL   W2, [W0]                       ; Write PM low word into program latch
       TBLWTH   W3, [W0]                       ; Write PM high byte into program latch
```

EXAMPLE 5-3: INITIATING A PROGRAMMING SEQUENCE

```
       DISI   #5                       ; Block all interrupts with priority <7
                                       ; for next 5 instructions
       MOV    #0x55, W0
       MOV    W0, NVMKEY               ; Write the 55 key
       MOV    #0xAA, W1                ;
       MOV    W1, NVMKEY               ; Write the AA key
       BSET   NVMCON, #WR              ; Start the erase sequence
       NOP                             ; 2 NOPs required after setting WR
       NOP                             ;
       BTSC   NVMCON, #15              ; Wait for the sequence to be completed
       BRA    $-2                      ;
```

6.1 Clock Source Selection at Reset

6.2 Device Reset Times

Section 8.0 “Oscillator Configuration”

TABLE 6-2: OSCILLATOR SELECTION vs. TYPE OF RESET (CLOCK SWITCHING ENABLED)

Reset Type	Clock Source Determinant

TABLE 6-3: RESET DELAY TIMES FOR VARIOUS DEVICE RESETS

Reset Type	Clock Source	SYSRST Delay	System Clock Delay	Notes
(6)				1, 2, 7
				1, 2, 3, 7
				1, 2, 3, 7
				1, 2, 4, 7
				1, 2, 3, 4, 7
				1, 2, 5, 7
				1, 2, 4, 5, 7
				2, 7
				2, 3, 7
				2, 3, 7
				2, 4, 7
				2, 3, 4, 7
				2, 5, 7
				2, 3, 4, 7
				7

Note 1:

2:

3:

4:

5:

6:

7:

REGISTER 7-19: IPC4: INTERRUPT PRIORITY CONTROL REGISTER 4

Legend:

Unimplemented: 0

CNIP<2:0>:

111

001

000

Unimplemented: 0

CMIP<2:0>:

111

001

000

Unimplemented: 0

MI2C1P<2:0>:

111

001

000

Unimplemented: 0

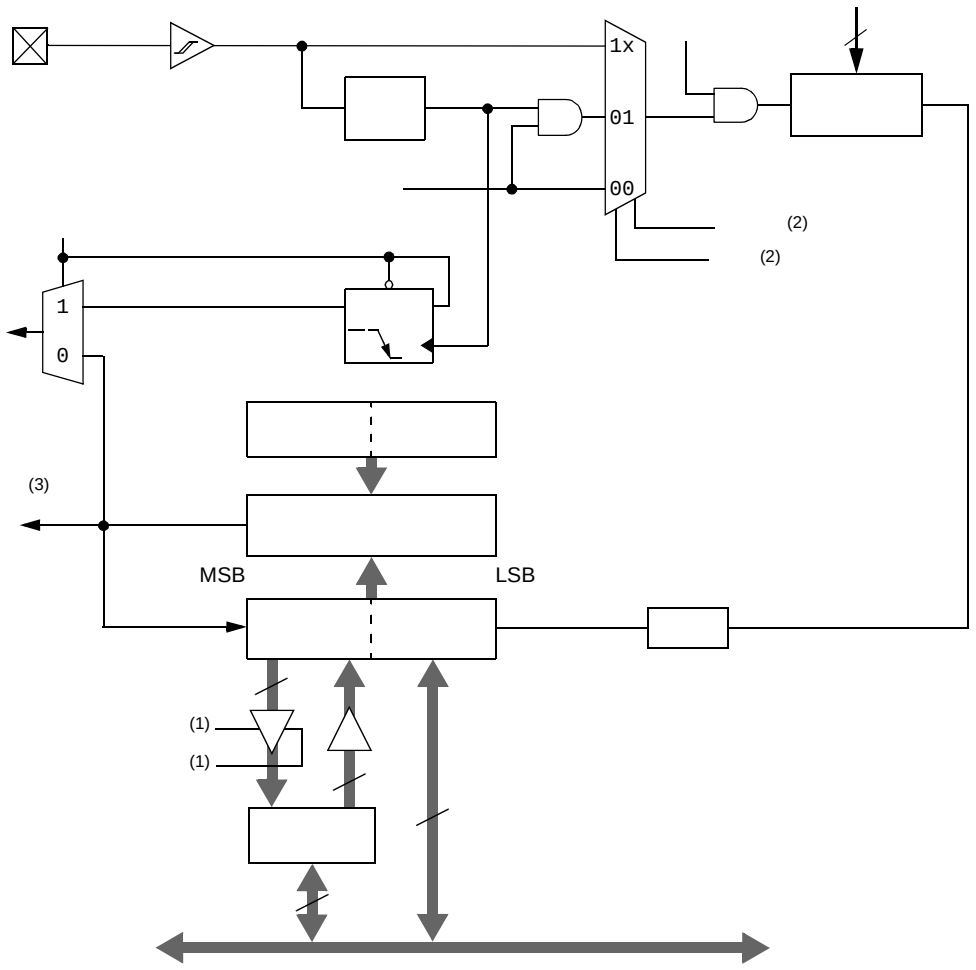
SI2C1P<2:0>:

111

001

000

FIGURE 12-1: TIMER2/3 AND TIMER4/5 (32-BIT) BLOCK DIAGRAM



Note 1:

2:
Section 10.4 “Peripheral Pin Select (PPS)”

3:

REGISTER 12-2: TyCON: TIMER3 AND TIMER5 CONTROL REGISTER

(1)		(1)					

	(1)	(1)	(1)			(1,2)	

Legend:

TON: (1)
1
0
Unimplemented: 0
TSIDL: (1)
1
0
Unimplemented: 0
TGATE: (1)
1
0
TCKPS<1:0>: (1)
11
10
01
00
Unimplemented: 0
TCS: (1,2)
1
0
Unimplemented: 0

Note 1: 1

2: 1 Section 10.4 “Peripheral Pin Select (PPS)”

14.3 Pulse-Width Modulation Mode

Note:

Section 10.4 “Peripheral Pin Select (PPS)”

EQUATION 14-1: CALCULATING THE PWM PERIOD(1)

PWM Period = [(PRy) + 1] TCY (Timer Prescale Value

PWM Frequency = 1/[PWM Period]

Note 1:

Note:

1

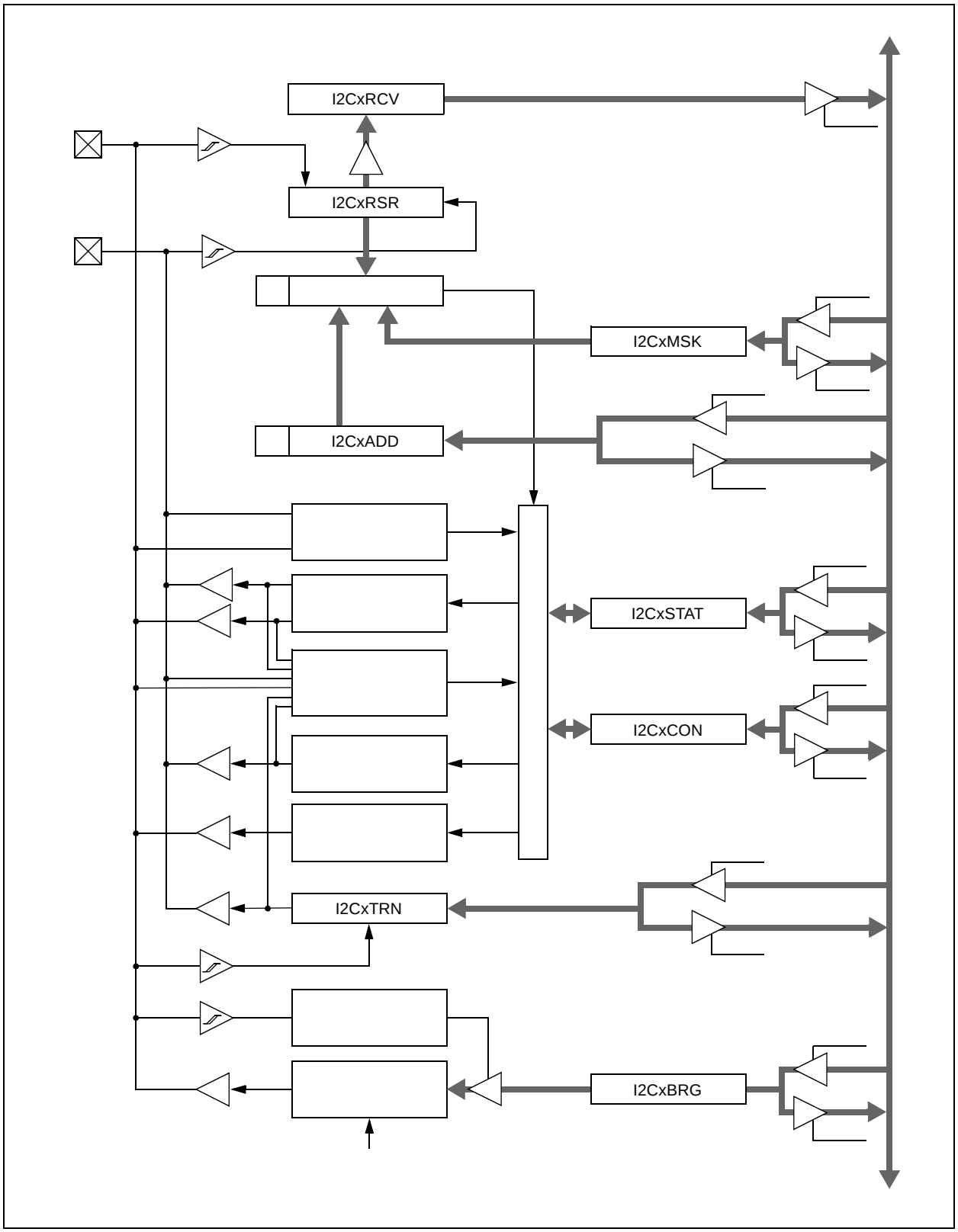
Note:

EQUATION 14-2: CALCULATION FOR MAXIMUM PWM RESOLUTION(1)

$$\text{Maximum PWM Resolution (bits)} = \frac{\log_{10}\left(\frac{F_{CY}}{F_{PWM}\ \text{(Timer Prescale Value)}}\right)}{\log_{10}(2)}\ \text{bits}$$

Note 1:

FIGURE 16-1: I^2C™ BLOCK DIAGRAM



REGISTER 17-2: UxSTA: UARTx STATUS AND CONTROL REGISTER (CONTINUED)

ADDEN: 1

1

0

RIDLE:

1

0

PERR:

1

0

FERR:

1

0

OERR:

1

0 1 o 0

URXDA:

1

0

Note 1: 1

Section 10.4 “Peripheral Pin Select (PPS)”

20.0 PROGRAMMABLE CYCLIC REDUNDANCY CHECK (CRC) GENERATOR

Note:

"PIC24F Family Reference Manual" "Programmable Cyclic Redundancy Check (CRC)"

EQUATION 20-1: CRC POLYNOMIAL

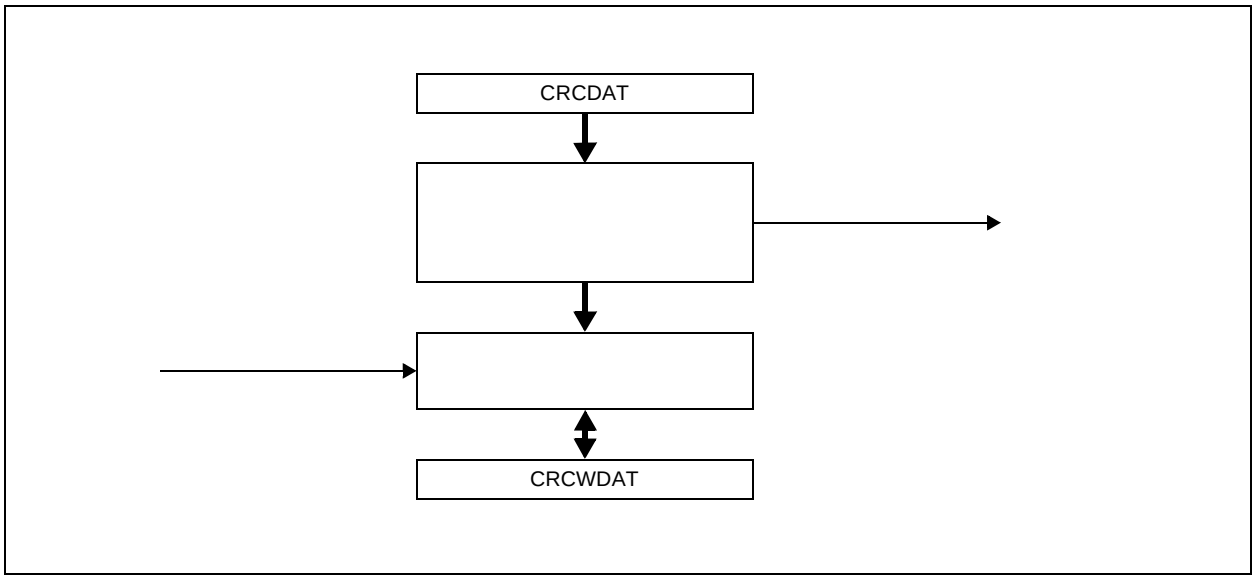
$$x^{16} + x^{12} + x^5 + 1$$

TABLE 20-1: EXAMPLE CRC SETUP

Bit Name	Bit Value
	1111
	000100000010000

1

FIGURE 20-1: CRC BLOCK DIAGRAM



/

REGISTER 21-5: AD1PCFG: A/D PO RT CONFIGURATION REGISTER

							(1)

(1)	(1)						

Legend:	

PCFG15:
1
0
Unimplemented: 0
PCFG<12:0>: (1)
1
0

Note 1:

REGISTER 21-6: AD1CSSL: A/D INPUT SCAN SELECT REGISTER

							(1)

(1)	(1)						

Legend:	

CSSL15:
1 =
0 =
Unimplemented: 0
CSSL<12:0>: (1)
1 =
0 =

Note 1:

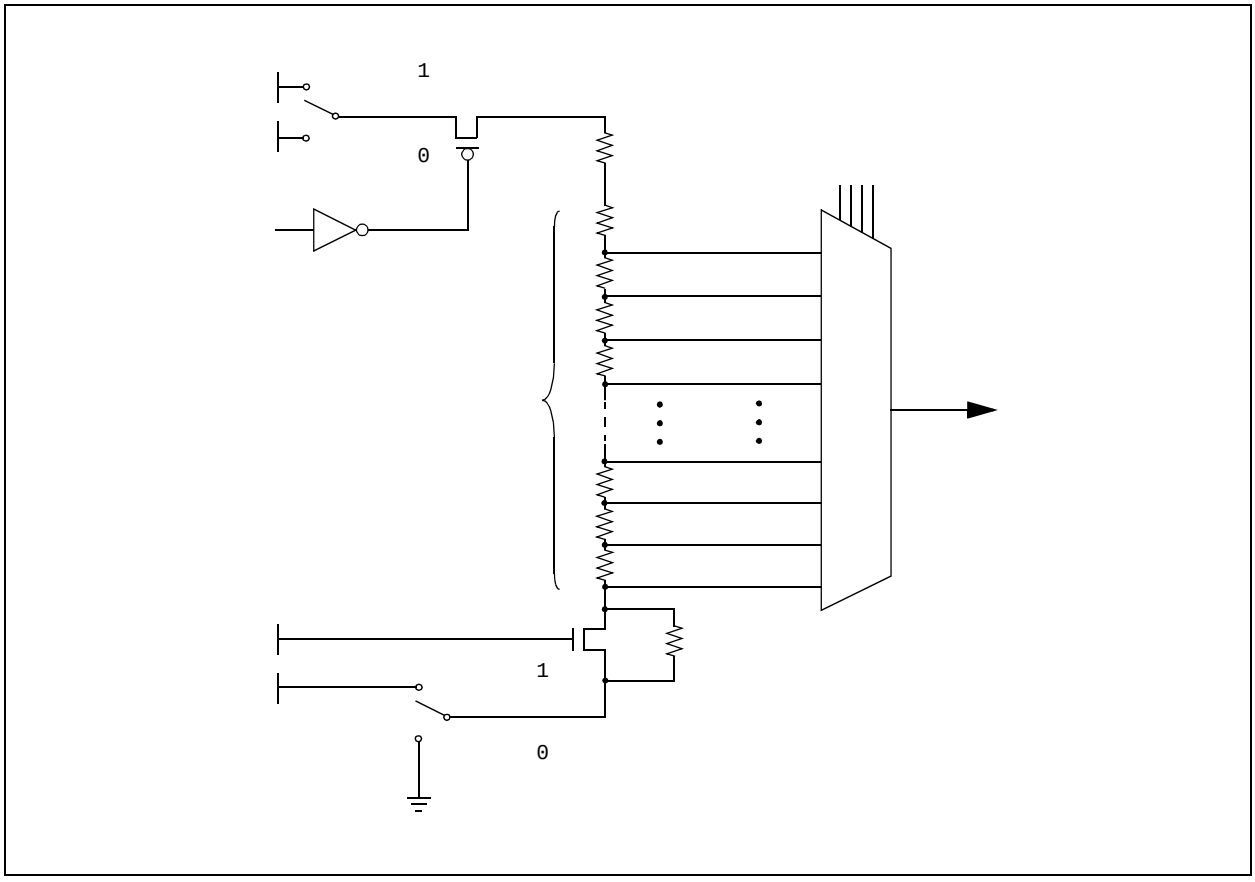
23.0 COMPARATOR VOLTAGE REFERENCE

Note:

"PIC24F Family Reference Manual"
"Comparator Voltage Reference Module"

23.1 Configuring the Comparator Voltage Reference

FIGURE 23-1: COMPARATOR VOLTAGE REFERENCE BLOCK DIAGRAM



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