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Details

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Product Status	Active
Core Processor	PIC
Core Size	16-Bit
Speed	32MHz
Connectivity	I ² C, PMP, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LVD, POR, PWM, WDT
Number of I/O	35
Program Memory Size	32KB (11K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 13x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-TQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24fj32ga004-i-pt

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REGISTER 3-2:	CORCON: CPU	CONTROL REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
							_
bit 15							bit 8
U-0	U-0	U-0	U-0	R/C-0	R/W-0	U-0	U-0
—	—	—	—	IPL3 ⁽¹⁾	PSV	—	—
bit 7				•	•	•	bit 0

Legend:	C = Clearable bit			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'		
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown	

bit 15-4	Unimplemented: Read as '0'
bit 3	IPL3: CPU Interrupt Priority Level Status bit ⁽¹⁾
	1 = CPU Interrupt Priority Level is greater than 70 = CPU Interrupt Priority Level is 7 or less
bit 2	PSV: Program Space Visibility in Data Space Enable bit
	1 = Program space is visible in data space0 = Program space is not visible in data space
bit 1-0	Unimplemented: Read as '0'

Note 1: User interrupts are disabled when IPL3 = 1.

3.3 Arithmetic Logic Unit (ALU)

The PIC24F ALU is 16 bits wide, and is capable of addition, subtraction, bit shifts and logic operations. Unless otherwise mentioned, arithmetic operations are 2's complement in nature. Depending on the operation, the ALU may affect the values of the Carry (C), Zero (Z), Negative (N), Overflow (OV) and Digit Carry (DC) Status bits in the SR register. The C and DC Status bits operate as Borrow and Digit Borrow bits, respectively, for subtraction operations.

The ALU can perform 8-bit or 16-bit operations, depending on the mode of the instruction that is used. Data for the ALU operation can come from the W register array, or data memory, depending on the addressing mode of the instruction. Likewise, output data from the ALU can be written to the W register array or a data memory location.

The PIC24F CPU incorporates hardware support for both multiplication and division. This includes a dedicated hardware multiplier and support hardware for 16-bit divisor division.

3.3.1 MULTIPLIER

The ALU contains a high-speed, 17-bit x 17-bit multiplier. It supports unsigned, signed or mixed sign operation in several multiplication modes:

- 1. 16-bit x 16-bit signed
- 2. 16-bit x 16-bit unsigned
- 3. 16-bit signed x 5-bit (literal) unsigned
- 4. 16-bit unsigned x 16-bit unsigned
- 5. 16-bit unsigned x 5-bit (literal) unsigned
- 6. 16-bit unsigned x 16-bit signed
- 7. 8-bit unsigned x 8-bit unsigned

4.3.3 READING DATA FROM PROGRAM MEMORY USING PROGRAM SPACE VISIBILITY

The upper 32 Kbytes of data space may optionally be mapped into any 16K word page of the program space. This provides transparent access of stored constant data from the data space without the need to use special instructions (i.e., TBLRDL/H).

Program space access through the data space occurs if the Most Significant bit of the data space EA is '1' and Program Space Visibility is enabled by setting the PSV bit in the CPU Control register (CORCON<2>). The location of the program memory space to be mapped into the data space is determined by the Program Space Visibility Page Address register (PSVPAG). This 8-bit register defines any one of 256 possible pages of 16K words in program space. In effect, PSVPAG functions as the upper 8 bits of the program memory address, with the 15 bits of the EA functioning as the lower bits. Note that by incrementing the PC by 2 for each program memory word, the lower 15 bits of data space addresses directly map to the lower 15 bits in the corresponding program space addresses.

Data reads to this area add an additional cycle to the instruction being executed, since two program memory fetches are required.

Although each data space address, 8000h and higher, maps directly into a corresponding program memory address (see Figure 4-7), only the lower 16 bits of the 24-bit program word are used to contain the data. The upper 8 bits of any program space locations used as data should be programmed with '1111 1111' or '0000 0000' to force a NOP. This prevents possible issues should the area of code ever be accidentally executed.

Note:	PSV access is temporarily disabled during
	table reads/writes.

For operations that use PSV and are executed outside a REPEAT loop, the MOV and MOV.D instructions will require one instruction cycle in addition to the specified execution time. All other instructions will require two instruction cycles in addition to the specified execution time.

For operations that use PSV which are executed inside a REPEAT loop, there will be some instances that require two instruction cycles in addition to the specified execution time of the instruction:

- · Execution in the first iteration
- · Execution in the last iteration
- Execution prior to exiting the loop due to an interrupt
- Execution upon re-entering the loop after an interrupt is serviced

Any other iteration of the REPEAT loop will allow the instruction accessing data, using PSV, to execute in a single cycle.

FIGURE 4-7: PROGRAM SPACE VISIBILITY OPERATION



REGISTER 7-1: SR: ALU STATUS REGISTER (IN CPU)

U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0
—	—	—	—	—	—	—	DC ⁽¹⁾
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0
IPL2 ^(2,3)	IPL1 ^(2,3)	IPL0 ^(2,3)	RA ⁽¹⁾	N ⁽¹⁾	OV ⁽¹⁾	Z ⁽¹⁾	C ⁽¹⁾
bit 7							bit 0

Legend:					
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'			
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown		

bit 7-5 IPL<2:0>: CPU Interrupt Priority Level Status bits^(2,3)

- 111 = CPU Interrupt Priority Level is 7 (15); user interrupts are disabled
- 110 = CPU Interrupt Priority Level is 6 (14)
- 101 = CPU Interrupt Priority Level is 5 (13)
- 100 = CPU Interrupt Priority Level is 4 (12)
- 011 = CPU Interrupt Priority Level is 3 (11)
- 010 = CPU Interrupt Priority Level is 2 (10)
- 001 = CPU Interrupt Priority Level is 1 (9)
- 000 = CPU Interrupt Priority Level is 0 (8)
- Note 1: See Register 3-1 for the description of the remaining bit(s) that are not dedicated to interrupt control functions.
 - **2:** The IPLx bits are concatenated with the IPL3 bit (CORCON<3>) to form the CPU interrupt Priority Level. The value in parentheses indicates the Interrupt Priority Level if IPL3 = 1.
 - 3: The IPLx Status bits are read-only when NSTDIS (INTCON1<15>) = 1.

REGISTER 7-2: CORCON: CPU CONTROL REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8
U-0	U-0	U-0	U-0	R/C-0	R/W-0	U-0	U-0
	—	—	—	IPL3 ⁽²⁾	PSV ⁽¹⁾	_	—

Legend:	C = Clearable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit,	, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

IPL3: CPU Interrupt Priority Level Status bit⁽²⁾

1 = CPU Interrupt Priority Level is greater than 7

0 = CPU Interrupt Priority Level is 7 or less

Note 1: See Register 3-2 for the description of the remaining bit(s) that are not dedicated to interrupt control functions.

2: The IPL3 bit is concatenated with the IPL<2:0: bits (SR<7:5>) to form the CPU Interrupt priority Level.

bit 7

bit 3

bit 0

REGISTER 7-7: IFS2: INTERRUPT FLAG STATUS REGISTER 2

U-0	U-0	R/W-0	U-0	U-0	U-0	R/W-0	U-0
—	—	PMPIF	—	—	_	OC5IF	—
bit 15							bit 8
R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	R/W-0	R/W-0
IC5IF	IC4IF	IC3IF	_		_	SPI2IF	SPF2IF
bit 7							bit 0
Legend:							
R = Readable	e bit	W = Writable	bit	U = Unimplen	nented bit, rea	ad as '0'	
-n = Value at	POR	'1' = Bit is set		'0' = Bit is clea	ared	x = Bit is unkn	iown
bit 15-14	Unimplemen	ted: Read as '	כ'				
bit 13	PMPIF: Para	llel Master Port	Interrupt Flag	Status bit			
	1 = Interrupt	request has occ	curred				
		request has not	occurred				
bit 12-10	Unimplemen	ted: Read as '),				
bit 9	OC5IF: Outp	ut Compare Ch	annel 5 Interru	pt Flag Status I	oit		
	1 = Interrupt 0 = Interrupt	request has occ request has not	curred				
bit 8	Unimplemen	ted: Read as ')'				
bit 7	IC5IF: Input (Capture Channe	el 5 Interrupt F	lag Status bit			
	1 = Interrupt	request has occ	curred	lag clatac sit			
	0 = Interrupt	request has not	occurred				
bit 6	IC4IF: Input (Capture Channe	el 4 Interrupt F	lag Status bit			
	1 = Interrupt	request has occ	curred				
	0 = Interrupt	request has not	occurred				
bit 5	IC3IF: Input (Capture Channe	el 3 Interrupt F	lag Status bit			
	1 = Interrupt	request has occ	curred				
h# 4 0		request has not	occurred				
DIT 4-2		ited: Read as					
DIT	SPIZIF: SPIZ	Event Interrup	Flag Status D	IT			
	$\perp = Interrupt$ 0 = Interrupt	request has occ	occurred				
bit 0	SPF2IF: SPI	2 Fault Interrupt	Flag Status bi	it			
	1 = Interrupt	request has occ	curred				
	0 = Interrupt	request has not	occurred				

REGISTER 7-12: IEC2: INTERRUPT ENABLE CONTROL REGISTER 2

U-0	U-0	R/W-0	U-0	U-0	U-0	R/W-0	U-0			
	_	PMPIE		_		OC5IE	_			
bit 15							bit 8			
R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	R/W-0	R/W-0			
IC5IE	IC4IE	IC3IE	—			SPI2IE	SPF2IE			
bit 7							bit 0			
l egend:]			
R = Readable	e bit	W = Writable	bit	U = Unimplem	nented bit rea	ad as '0'				
-n = Value at	POR	'1' = Bit is set		'0' = Bit is clea	ared	x = Bit is unkn	own			
	-									
bit 15-14	Unimplemen	ted: Read as '	כי							
bit 13	PMPIE: Para	llel Master Port	Interrupt Enal	ole bit						
	1 = Interrupt request is enabled									
1 1 10 10	0 = Interrupt request is not enabled									
bit 12-10	Unimplemented: Read as '0'									
bit 9	OC5IE: Output	ut Compare Ch	annel 5 Interru	ipt Enable bit						
	0 = Interrupt i	request is enab	nabled							
bit 8	Unimplemen	ted: Read as '	o'							
bit 7	IC5IE: Input (Capture Channe	el 5 Interrupt E	nable bit						
	1 = Interrupt	request is enab	led							
	0 = Interrupt i	request is not e	nabled							
bit 6	IC4IE: Input (Capture Channe	el 4 Interrupt E	nable bit						
	1 = Interrupt I	request is enab request is not e	ied nabled							
bit 5	IC3IE: Input (Capture Channe	el 3 Interrupt E	nable bit						
	1 = Interrupt	request is enab	led							
	0 = Interrupt	request is not e	nabled							
bit 4-2	Unimplemen	ted: Read as '	כ'							
bit 1	SPI2IE: SPI2 Event Interrupt Enable bit									
	1 = Interrupt	request is enab	led							
hit 0		2 Equit Interrupt	t Enchlo hit							
	1 = Interrupt	request is each								
	0 = Interrupt I	request is not e	nabled							
	·									

				11.0					
0-0				0-0					
	11172	111111	I IIPU	_	UCTIPZ	UCTIPT			
11-0	R/W-1	R/W/-0	R/W-0	11-0	R/M-1	R/W-0	R/W/-0		
	IC1IP2	IC1IP1	IC1IP0		INTOIP2				
bit 7									
Legend:									
R = Readable	e bit	W = Writable I	oit	U = Unimplem	nented bit, read	R/W-0 R/W-0 INT0IP1 INT0IP0 bit 0 ad as '0' x = Bit is unknown			
-n = Value at	POR	'1' = Bit is set		'0' = Bit is clea	ared	x = Bit is unkr	nown		
bit 15	Unimplemen	ted: Read as 'd)'						
bit 14-12	T1IP<2:0>: ⊺	imer1 Interrupt	Priority bits						
	111 = Interru	ot is Priority 7 (I	nighest priority	vinterrupt)					
	•								
	•								
	001 = Interru	pt is Priority 1							
	000 = Interru	pt source is disa	abled						
bit 11	Unimplemen	ted: Read as '0)'						
bit 10-8	OC1IP<2:0>:	Output Compa	re Channel 1 I	Interrupt Priority	/ bits				
	111 = Interrup	pt is Priority 7 (i	nignest priority	(interrupt)					
	•								
	•								
	001 = Interru	pt is Priority 1 of source is dis:	ahled						
bit 7	Unimplemen	ted: Read as '()'						
bit 6-4	IC1IP<2:0>:	nput Capture C	hannel 1 Inter	rupt Priority bits	3				
	111 = Interru	pt is Priority 7 (I	nighest priority	interrupt)	-				
	•		- i - j	. /					
	•								
	- 001 = Interrui	ot is Prioritv 1							
	000 = Interru	ot source is disa	abled						
bit 3	Unimplemen	ted: Read as 'o)'						
bit 2-0	INT0IP<2:0>: External Interrupt 0 Priority bits								
	111 = Interru	pt is Priority 7 (I	nighest priority	interrupt)					
	•								
	•								
	001 = Interru	pt is Priority 1							
	000 = Interru	ot source is disa	abled						

REGISTER 7-15: IPC0: INTERRUPT PRIORITY CONTROL REGISTER 0

REGISTER 7-16: IPC1: INTERRUPT PRIORITY CONTROL REGISTER 1

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0		
_	T2IP2	T2IP1	T2IP0	_	OC2IP2	OC2IP1	OC2IP0		
bit 15							bit 8		
U-0	R/W-1	R/W-0	R/W-0	U-0	U-0	U-0	U-0		
_	IC2IP2	IC2IP1	IC2IP0	—	—	—	—		
bit 7	t 7								
Legend:									
R = Readable	e bit	W = Writable	bit	U = Unimplem	nented bit, read	d as '0'			
-n = Value at	POR	'1' = Bit is set		'0' = Bit is clea	ared	x = Bit is unkr	nown		
bit 15	Unimplemen	nted: Read as '	0'						
bit 14-12	T2IP<2:0>: ⊺	imer2 Interrupt	Priority bits						
	111 = Interru	pt is Priority 7 (highest priority	interrupt)					
	•								
	•								
	001 = Interru	pt is Priority 1							
	000 = Interru	pt source is dis	abled						
bit 11	Unimplemen	nted: Read as '	0'						
bit 10-8	OC2IP<2:0>:	: Output Compa	are Channel 2 I	nterrupt Priority	/ bits				
	111 = Interru	pt is Priority 7 (highest priority	interrupt)					
	•								
	•								
	001 = Interru	pt is Priority 1							
	000 = Interru	pt source is dis	abled						
bit 7	Unimplemen	ted: Read as '	0'						
bit 6-4	IC2IP<2:0>:	Input Capture C	Channel 2 Inter	rupt Priority bits	3				
	111 = Interru	pt is Priority 7 (highest priority	interrupt)					
	•								
	•								
	001 = Interru	pt is Priority 1							
	000 = Interru	ipt source is dis	abled						
bit 3-0	Unimplemen	ted: Read as '	0'						

8.0 OSCILLATOR CONFIGURATION

Note:	This data sheet summarizes the features of							
	this group of PIC24F devices. It is not							
	intended to be a comprehensive reference							
	source. For more information, refer to the							
	"PIC24F Family Reference Manual",							
	"Oscillator" (DS39700).							

The oscillator system for PIC24FJ64GA004 family devices has the following features:

- A total of four external and internal oscillator options as clock sources, providing 11 different clock modes
- On-chip 4x PLL to boost internal operating frequency on select internal and external oscillator sources

- Software-controllable switching between various clock sources
- Software-controllable postscaler for selective clocking of CPU for system power savings
- A Fail-Safe Clock Monitor (FSCM) that detects clock failure and permits safe application recovery or shutdown

A simplified diagram of the oscillator system is shown in Figure 8-1.



FIGURE 8-1: PIC24FJ64GA004 FAMILY CLOCK DIAGRAM

REGISTER 10-3: RPINR3: PERIPHERAL PIN SELECT INPUT REGISTER 3

U-0	U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
_	—	—	T3CKR4	T3CKR3	T3CKR2	T3CKR1	T3CKR0
bit 15							bit 8

U-0	U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	—	T2CKR4	T2CKR3	T2CKR2	T2CKR1	T2CKR0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	1 as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-13 Unimplemented: Read as '0'

bit 12-8 T3CKR<4:0>: Assign Timer3 External Clock (T3CK) to the Corresponding RPn Pin bits

bit 7-5 Unimplemented: Read as '0'

bit 4-0 T2CKR<4:0>: Assign Timer2 External Clock (T2CK) to the Corresponding RPn Pin bits

REGISTER 10-4: RPINR4: PERIPHERAL PIN SELECT INPUT REGISTER 4

U-0	U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	—	T5CKR4	T5CKR3	T5CKR2	T5CKR1	T5CKR0
bit 15							bit 8

U-0	U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	—	T4CKR4	T4CKR3	T4CKR2	T4CKR1	T4CKR0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	d as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-13 Unimplemented: Read as '0'

bit 12-8 T5CKR<4:0>: Assign Timer5 External Clock (T5CK) to the Corresponding RPn Pin bits

bit 7-5 Unimplemented: Read as '0'

bit 4-0 T4CKR<4:0>: Assign Timer4 External Clock (T4CK) to the Corresponding RPn Pin bits

REGISTER 10-9: RPINR18: PERIPHERAL PIN SELECT INPUT REGISTER 18

U-0	U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
	—	—	U1CTSR4	U1CTSR3	U1CTSR2	U1CTSR1	U1CTSR0
bit 15							bit 8

U-0	U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	—	U1RXR4	U1RXR3	U1RXR2	U1RXR1	U1RXR0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	d as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-13	Unimplemented: Read as '0'
bit 12-8	U1CTSR<4:0>: Assign UART1 Clear-to-Send (U1CTS) to the Corresponding RPn Pin bits
bit 7-5	Unimplemented: Read as '0'
bit 4-0	U1RXR<4:0>: Assign UART1 Receive (U1RX) to the Corresponding RPn Pin bits

REGISTER 10-10: RPINR19: PERIPHERAL PIN SELECT INPUT REGISTER 19

U-0	U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	—	U2CTSR4	U2CTSR3	U2CTSR2	U2CTSR1	U2CTSR0
bit 15							bit 8
U-0	U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	—	U2RXR4	U2RXR3	U2RXR2	U2RXR1	U2RXR0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	l as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-13 Unimplemented: Read as '0'

bit 12-8 U2CTSR<4:0>: Assign UART2 Clear-to-Send (U2CTS) to the Corresponding RPn Pin bits

bit 7-5 Unimplemented: Read as '0'

bit 4-0 U2RXR<4:0>: Assign UART2 Receive (U2RX) to the Corresponding RPn Pin bits

FIGURE 14-1: OUTPUT COMPARE x MODULE BLOCK DIAGRAM



4: This peripheral's inputs and outputs must be assigned to an available RPn pin before use. Please see Section 10.4 "Peripheral Pin Select (PPS)" for more information.

NOTES:

17.0 UNIVERSAL ASYNCHRONOUS RECEIVER TRANSMITTER (UART)

Note: This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information, refer to the *"PIC24F Family Reference Manual"*, *"UART"* (DS39708).

The Universal Asynchronous Receiver Transmitter (UART) module is one of the serial I/O modules available in the PIC24F device family. The UART is a full-duplex, asynchronous system that can communicate with peripheral devices, such as personal computers, LIN/J2602, RS-232 and RS-485 interfaces. The module also supports a hardware flow control option with the UxCTS and UxRTS pins, and also includes an IrDA[®] encoder and decoder.

The primary features of the UART module are:

- Full-Duplex, 8 or 9-Bit Data Transmission through the UxTX and UxRX Pins
- Even, Odd or No Parity Options (for 8-bit data)
- One or Two Stop bits
- Hardware Flow Control Option with UxCTS and UxRTS Pins
- Fully Integrated Baud Rate Generator with 16-Bit
 Prescaler

- Baud Rates Ranging from 1 Mbps to 15 bps at 16 MIPS
- 4-Deep, First-In-First-Out (FIFO) Transmit Data Buffer
- · 4-Deep FIFO Receive Data Buffer
- Parity, Framing and Buffer Overrun Error Detection
- Support for 9-bit mode with Address Detect (9th bit = 1)
- · Transmit and Receive Interrupts
- · Loopback mode for Diagnostic Support
- Support for Sync and Break Characters
- Supports Automatic Baud Rate Detection
- IrDA Encoder and Decoder Logic
- 16x Baud Clock Output for IrDA Support

A simplified block diagram of the UART is shown in Figure 17-1. The UART module consists of these key important hardware elements:

- Baud Rate Generator
- Asynchronous Transmitter
- Asynchronous Receiver

Note: In this section, the UART modules are referred to together as UARTx or separately as UART1 and UART2.

FIGURE 17-1: UARTx SIMPLIFIED BLOCK DIAGRAM Baud Rate Generator IrDA® IrDA® Karta Baud Rate Generator IrDA® IrDA®

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19.1.4 RTCVAL REGISTER MAPPINGS

REGISTER 19-4: YEAR: YEAR VALUE REGISTER⁽¹⁾

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
_	_	—	_	—	—	—	—
bit 15							bit 8
R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
YRTEN3	YRTEN2	YRTEN1	YRTEN0	YRONE3	YRONE2	YRONE1	YRONE0
bit 7							bit 0
Legend:							
R = Readable	e bit	W = Writable	bit	U = Unimplemented bit, read as '0'			
-n = Value at	POR	'1' = Bit is set		'0' = Bit is cleared x = Bit is unknow		nown	

bit 15-8 Unimplemented: Read as '0'

- bit 7-4 **YRTEN<3:0>:** Binary Coded Decimal Value of Year's Tens Digit bits Contains a value from 0 to 9.
- bit 3-0 **YRONE<3:0>:** Binary Coded Decimal Value of Year's Ones Digit bits Contains a value from 0 to 9.

Note 1: A write to this register is only allowed when RTCWREN = 1.

REGISTER 19-5: MTHDY: MONTH AND DAY VALUE REGISTER⁽¹⁾

U-0	U-0	U-0	R-x	R-x	R-x	R-x	R-x
—	—	—	MTHTEN0	MTHONE3	MTHONE2	MTHONE1	MTHONE0
bit 15							bit 8

U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
—	—	DAYTEN1	DAYTEN0	DAYONE3	DAYONE2	DAYONE1	DAYONE0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	l as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-13	Unimplemented: Read as '0'
bit 12	MTHTEN0: Binary Coded Decimal Value of Month's Tens Digit bit
	Contains a value of '0' or '1'.
bit 11-8	MTHONE<3:0<: Binary Coded Decimal Value of Month's Ones Digit bits
	Contains a value from 0 to 9.
bit 7-6	Unimplemented: Read as '0'
bit 5-4	DAYTEN<1:0:> Binary Coded Decimal Value of Day's Tens Digit bits
	Contains a value from 0 to 3.
bit 3-0	DAYONE<3:0>: Binary Coded Decimal Value of Day's Ones Digit bits
	Contains a value from 0 to 9.

Note 1: A write to this register is only allowed when RTCWREN = 1.

REGISTER 21-2: AD1CON2: A/D CONTROL REGISTER 2

R/W-0	R/W-0	R/W-0	U-0	U-0	R/W-0	U-0	U-0
VCFG2	VCFG1	VCFG0	—	—	CSCNA	—	—
bit 15							bit 8

R-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
BUFS	—	SMPI3	SMPI2	SMPI1	SMPI0	BUFM	ALTS
bit 7							bit 0

Legend:R = Readable bitW = Writable bitU = Unimplemented bit, read as '0'-n = Value at POR'1' = Bit is set'0' = Bit is clearedx = Bit is unknown

bit 15-13 VCFG<2:0>: Voltage Reference Configuration bits

VCFG<2:0>	VR+	VR-	
000	AVDD*	AVss*	
001	External VREF+ Pin	AVss*	
010	AVDD*	External VREF- Pin	
011	External VREF+ Pin	External VREF- Pin	
lxx	AVDD*	AVss*	

* AVDD and AVSS inputs are tied to VDD and VSS on 28-pin devices.

bit 12-11 Unimplemented: Read as '0'

bit 10	CSCNA: Scan Input Selections for CH0+ S/H Input for MUX A Input Multiplexer Setting bit
	1 = Scans inputs
	0 = Does not scan inputs
bit 9-8	Unimplemented: Read as '0'
bit 7	BUFS: Buffer Fill Status bit (valid only when BUFM = 1)
	 1 = A/D is currently filling Buffer 08-0F, user should access data in 00-07 0 = A/D is currently filling Buffer 00-07, user should access data in 08-0F
bit 6	Unimplemented: Read as '0'
bit 5-2	SMPI<3:0>: Sample/Convert Sequences Per Interrupt Selection bits
	1111 = Interrupts at the completion of conversion for each 16th sample/convert sequence
	1110 = Interrupts at the completion of conversion for each 15th sample/convert sequence
	0001 = Interrupts at the completion of conversion for each sample/convert sequence
bit 1	BUFM: Buffer Mode Select bit
	1 = Buffer configured as two 8-word buffers (ADC1BUEn<15:8> and ADC1BUEn<7:0>)
	 a Buffer configured as one 16-word buffer (ADC1BUFn<15:0>)
bit 0	ALTS: Alternate Input Sample Mode Select bit
	1 = Uses MUX A input multiplexer settings for first sample, then alternates between MUX B and MUX A
	input multiplexer settings for all subsequent samples
	0 = Always uses MUX A input multiplexer settings

REGISTER 24-2: CW2: FLASH CONFIGURATION WORD 2

U-1	U-1	U-1	U-1	U-1	U-1	U-1	U-1	
—	—	—	—	—	—	—	—	
bit 23 bit 16								

R/PO-1	R/PO-1	R/PO-1	R/PO-1	R/PO-1	R/PO-1	R/PO-1	R/PO-1
IESO	WUTSEL1(1)	WUTSEL0 ⁽¹⁾	SOSCSEL1(1)	SOSCSEL0 ⁽¹⁾	FNOSC2	FNOSC1	FNOSC0
bit 15							bit 8

R/PO-1	R/PO-1	R/PO-1	R/PO-1	r	R/PO-1	R/PO-1	R/PO-1
FCKSM1	FCKSM0	OSCIOFCN	IOL1WAY	r	I2C1SEL	POSCMD1	POSCMD0
bit 7 bit 0							

Legend: r = Reserved bit				
R = Readable bit	PO = Program Once bit	bgram Once bit U = Unimplemented bit, read as '0'		
-n = Value when device is unprogrammed		'1' = Bit is set	'0' = Bit is cleared	

bit 23-16	Unimplemented: Read as '1'
bit 15	IESO: Internal External Switchover bit
	 1 = IESO mode (Two-Speed Start-up) is enabled 0 = IESO mode (Two-Speed Start-up) is disabled
bit 14-13	WUTSEL<1:0>: Voltage Regulator Standby Mode Wake-up Time Select bits ⁽¹⁾
	 11 = Default regulator start-up time is used 01 = Fast regulator start-up time is used x0 = Reserved; do not use
bit 12-11	SOSCSEL<1:0>: Secondary Oscillator Power Mode Select bits ⁽¹⁾
	11 = Default (High Drive Strength) mode
	01 = Low-Power (Low Drive Strength) mode
L:1 1 0 0	$x_0 = \text{Reserved}$; do not use
DIT TU-8	FNOSC<2:0>: Initial Oscillator vitte Destancion (FDODIN)
	111 = Fast RC Oscillator with Postscaler (FRCDIV)
	101 = Low-Power RC Oscillator (LPRC)
	100 = Secondary Oscillator (SOSC)
	011 = Primary Oscillator with PLL module (XTPLL, HSPLL, ECPLL)
	010 = Primary Oscillator (XI, HS, EC)
	000 = Fast RC Oscillator (FRC)
bit 7-6	FCKSM<1:0>: Clock Switching and Fail-Safe Clock Monitor Configuration bits
	1x = Clock switching and Fail-Safe Clock Monitor are disabled
	01 = Clock switching is enabled, Fail-Safe Clock Monitor is disabled
	00 = Clock switching is enabled, Fail-Safe Clock Monitor is enabled
bit 5	OSCIOFCN: OSCO Pin Configuration bit
	$\frac{ \text{f POSCMD} < 1:0> = 11 \text{ or } 00:}{1 - 00000000000000000000000000000000000$
	I = OSCO/CLKO/RA3 functions as port I/O (RA3)
	If $POSCMD<1:0> = 1.0 \text{ or } 0.1:$
	OSCIOFCN has no effect on OSCO/CLKO/RA3.

Note 1: These bits are implemented only in devices with a major silicon revision level of B or later (DEVREV register value is 3042h or greater). Refer to **Section 28.0** "**Packaging Information**" in the device data sheet for the location and interpretation of product date codes.

DC CHARACTERISTICS		Standard Operating Conditions:2.0V to 3.6V (unless otherwise stated $-40^{\circ}C \le TA \le +85^{\circ}C$ for Industrial $-40^{\circ}C \le TA \le +125^{\circ}C$ for Extended					
Param No.	Sym	Characteristic	Min	Typ ⁽¹⁾	Мах	Units	Conditions
	VIL	Input Low Voltage ⁽⁴⁾					
DI10		I/O Pins	Vss	—	0.2 VDD	V	
DI11		PMP Pins	Vss	—	0.15 VDD	V	PMPTTL = 1
DI15		MCLR	Vss	_	0.2 VDD	V	
DI16		OSCI (XT mode)	Vss	_	0.2 VDD	V	
DI17		OSCI (HS mode)	Vss	—	0.2 VDD	V	
DI18		I/O Pins with I ² C™ Buffer	Vss	—	0.3 VDD	V	SMBus disabled
DI19		I/O Pins with SMBus Buffer	Vss	_	0.8	V	SMBus enabled
	Vih	Input High Voltage ⁽⁴⁾					
DI20		I/O Pins: with Analog Functions Digital Only	0.8 Vdd 0.8 Vdd	_	Vdd 5.5	V V	
DI21		PMP Pins: with Analog Functions Digital Only	0.25 VDD + 0.8 0.25 VDD + 0.8	_	Vdd 5.5	V V	PMPTTL = 1
DI25		MCLR	0.8 Vdd	—	Vdd	V	
DI26		OSCI (XT mode)	0.7 VDD	—	Vdd	V	
DI27		OSCI (HS mode)	0.7 Vdd	—	Vdd	V	
DI28		I/O Pins with I ² C Buffer: with Analog Functions Digital Only	0.7 Vdd 0.7 Vdd		Vdd 5.5	V V	
DI29		I/O Pins with SMBus Buffer: with Analog Functions Digital Only	2.1	_	VDD	V	2 5V < Vpin < Vpp
DI30	ICNPU	CNxx Pull-up Current	50	250	400	uΑ	$V_{DD} = 3.3V$. VPIN = Vss

TABLE 27-7: DC CHARACTERISTICS: I/O PIN INPUT SPECIFICATIONS

Note 1: Data in "Typ" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

- 2: The leakage current on the MCLR pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.
- 3: Negative current is defined as current sourced by the pin.
- 4: Refer to Table 1-2 for I/O pin buffer types.
- **5:** Parameter is characterized but not tested.
- **6:** Non-5V tolerant pins, VIH source > (VDD + 0.3), 5V tolerant pins VIH source > 5.5V. Characterized but not tested.
- **7:** Digital 5V tolerant pins cannot tolerate any "positive" input injection current from input sources greater than 5.5V.
- 8: Injection currents > | 0 | can affect the performance of all analog peripherals (e.g., A/D, comparators, internal band gap reference, etc.)
- **9:** Any number and/or combination of I/O pins not excluded under IICL or IICH conditions are permitted provided the mathematical "absolute instantaneous" sum of the input injection currents from all pins do not exceed the specified limit. Characterized but not tested.

28-Lead QFN (6X6 mm)



44-Lead QFN (8x8x0.9 mm)



44-Lead TQFP (10x10x1 mm)







Example



Example



28-Lead Plastic Shrink Small Outline (SS) – 5.30 mm Body [SSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging





		MILLIMETERS	3		
Dimensio	MIN	NOM	MAX		
Number of Pins		28			
Pitch	е	0.65 BSC			
Overall Height	А	-	-	2.00	
Molded Package Thickness	A2	1.65	1.75	1.85	
Standoff	A1	0.05	-	-	
Overall Width	Е	7.40	7.80	8.20	
Molded Package Width	E1	5.00	5.30	5.60	
Overall Length	D	9.90	10.20	10.50	
Foot Length	L	0.55	0.75	0.95	
Footprint	L1	1.25 REF			
Lead Thickness	С	0.09	-	0.25	
Foot Angle	ф	0°	4°	8°	
Lead Width	b	0.22	_	0.38	

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.20 mm per side.
 Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-073B

28-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-052C Sheet 1 of 2