E·XFL



Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Active
Core Processor	PIC
Core Size	16-Bit
Speed	32MHz
Connectivity	I ² C, PMP, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LVD, POR, PWM, WDT
Number of I/O	21
Program Memory Size	64KB (22K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 10x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Through Hole
Package / Case	28-DIP (0.300", 7.62mm)
Supplier Device Package	28-SPDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24fj64ga002-e-sp

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Pin Diagrams (Continued)



Table of Contents

1.0	Device Overview	7
2.0	Guidelines for Getting Started with 16-Bit Microcontrollers	17
3.0	CPU	23
4.0	Memory Organization	29
5.0	Flash Program Memory	47
6.0	Resets	53
7.0	Interrupt Controller	59
8.0	Oscillator Configuration	95
9.0	Power-Saving Features	. 103
10.0	I/O Ports	. 105
11.0	Timer1	. 125
12.0	Timer2/3 and Timer4/5	. 127
13.0	Input Capture	. 133
14.0	Output Compare	. 135
15.0	Serial Peripheral Interface (SPI)	. 141
16.0	Inter-Integrated Circuit (I ² C [™])	. 151
17.0	Universal Asynchronous Receiver Transmitter (UART)	. 159
18.0	Parallel Master Port (PMP)	. 167
19.0	Real-Time Clock and Calendar (RTCC)	. 177
20.0	Programmable Cyclic Redundancy Check (CRC) Generator	. 189
21.0	10-Bit High-Speed A/D Converter	. 193
22.0	Comparator Module	203
23.0	Comparator Voltage Reference	207
24.0	Special Features	209
25.0	Development Support	219
26.0	Instruction Set Summary	223
27.0	Electrical Characteristics	. 231
28.0	Packaging Information	251
Appe	ndix A: Revision History	267
Appe	ndix B: Additional Guidance for PIC24FJ64GA004 Family Applications	268
Index		269
The N	/icrochip Web Site	. 273
Custo	mer Change Notification Service	273
Custo	mer Support	. 273
Read	er Response	. 274
Produ	Ict Identification System	275

2.0 GUIDELINES FOR GETTING STARTED WITH 16-BIT MICROCONTROLLERS

2.1 Basic Connection Requirements

Getting started with the PIC24FJ64GA004 family of 16-bit microcontrollers requires attention to a minimal set of device pin connections before proceeding with development.

The following pins must always be connected:

- All VDD and Vss pins (see Section 2.2 "Power Supply Pins")
- All AVDD and AVss pins, regardless of whether or not the analog device features are used (see Section 2.2 "Power Supply Pins")
- MCLR pin (see Section 2.3 "Master Clear (MCLR) Pin")
- ENVREG/DISVREG and VCAP/VDDCORE pins (PIC24F J devices only) (see Section 2.4 "Voltage Regulator Pins (ENVREG/DISVREG and VCAP/VDDCORE)")

These pins must also be connected if they are being used in the end application:

- PGECx/PGEDx pins used for In-Circuit Serial Programming[™] (ICSP[™]) and debugging purposes (see **Section 2.5 "ICSP Pins"**)
- OSCI and OSCO pins when an external oscillator source is used

(see Section 2.6 "External Oscillator Pins")

Additionally, the following pins may be required:

• VREF+/VREF- pins used when external voltage reference for analog modules is implemented

Note: The AVDD and AVss pins must always be connected, regardless of whether any of the analog modules are being used.

The minimum mandatory connections are shown in Figure 2-1.

FIGURE 2-1: RECOMMENDED MINIMUM CONNECTIONS



Key (all values are recommendations):

C1 through C6: 0.1 µF, 20V ceramic

C7: 10 $\mu\text{F},\,6.3\text{V}$ or greater, tantalum or ceramic

R1: 10 kΩ

R2: 100Ω to 470Ω

- Note 1: See Section 2.4 "Voltage Regulator Pins (ENVREG/DISVREG and VCAP/VDDCORE)" for an explanation of the ENVREG/DISVREG pin connections.
 - 2: The example shown is for a PIC24F device with five VDD/VSS and AVDD/AVSS pairs. Other devices may have more or less pairs; adjust the number of decoupling capacitors appropriately.

2.2 Power Supply Pins

2.2.1 DECOUPLING CAPACITORS

The use of decoupling capacitors on every pair of power supply pins, such as VDD, VSS, AVDD and AVSS is required.

Consider the following criteria when using decoupling capacitors:

- Value and type of capacitor: A 0.1 μ F (100 nF), 10-20V capacitor is recommended. The capacitor should be a low-ESR device with a resonance frequency in the range of 200 MHz and higher. Ceramic capacitors are recommended.
- Placement on the printed circuit board: The decoupling capacitors should be placed as close to the pins as possible. It is recommended to place the capacitors on the same side of the board as the device. If space is constricted, the capacitor can be placed on another layer on the PCB using a via; however, ensure that the trace length from the pin to the capacitor is no greater than 0.25 inch (6 mm).
- Handling high-frequency noise: If the board is experiencing high-frequency noise (upward of tens of MHz), add a second ceramic type capacitor in parallel to the above described decoupling capacitor. The value of the second capacitor can be in the range of 0.01 μ F to 0.001 μ F. Place this second capacitor next to each primary decoupling capacitor. In high-speed circuit designs, consider implementing a decade pair of capacitances as close to the power and ground pins as possible (e.g., 0.1 μ F in parallel with 0.001 μ F).
- Maximizing performance: On the board layout from the power supply circuit, run the power and return traces to the decoupling capacitors first, and then to the device pins. This ensures that the decoupling capacitors are first in the power chain. Equally important is to keep the trace length between the capacitor and the power pins to a minimum, thereby reducing PCB trace inductance.

2.2.2 TANK CAPACITORS

On boards with power traces running longer than six inches in length, it is suggested to use a tank capacitor for integrated circuits including microcontrollers to supply a local power source. The value of the tank capacitor should be determined based on the trace resistance that connects the power supply source to the device, and the maximum current drawn by the device in the application. In other words, select the tank capacitor so that it meets the acceptable voltage sag at the device. Typical values range from 4.7 μ F to 47 μ F.

2.3 Master Clear (MCLR) Pin

The MCLR pin provides two specific device functions: device Reset, and device programming and debugging. If programming and debugging are not required in the end application, a direct connection to VDD may be all that is required. The addition of other components, to help increase the application's resistance to spurious Resets from voltage sags, may be beneficial. A typical configuration is shown in Figure 2-1. Other circuit designs may be implemented, depending on the application's requirements.

During programming and debugging, the resistance and capacitance that can be added to the pin must be considered. Device programmers and debuggers drive the $\overline{\text{MCLR}}$ pin. Consequently, specific voltage levels (VIH and VIL) and fast signal transitions must not be adversely affected. Therefore, specific values of R1 and C1 will need to be adjusted based on the application and PCB requirements. For example, it is recommended that the capacitor, C1, be isolated from the $\overline{\text{MCLR}}$ pin during programming and debugging operations by using a jumper (Figure 2-2). The jumper is replaced for normal run-time operations.

Any components associated with the $\overline{\text{MCLR}}$ pin should be placed within 0.25 inch (6 mm) of the pin.

FIGURE 2-2: EXAMPLE OF MCLR PIN CONNECTIONS



TABLE 4-8: OUTPUT COMPARE REGISTER MAP

File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
OC1RS	0180							Output (Compare 1	Secondary	Register							FFFF
OC1R	0182	Output Compare 1 Register									FFFF							
OC1CON	0184		_	OCSIDL	_	_	_	_	_	_	_	_	OCFLT	OCTSEL	OCM2	OCM1	OCM0	0000
OC2RS	0186	Output Compare 2 Secondary Register									FFFF							
OC2R	0188		Output Compare 2 Register								FFFF							
OC2CON	018A	_		OCSIDL			_		—	—		_	OCFLT	OCTSEL	OCM2	OCM1	OCM0	0000
OC3RS	018C	Output Compare 3 Secondary Register								FFFF								
OC3R	018E							Οι	utput Compa	are 3 Regis	ter							FFFF
OC3CON	0190	_		OCSIDL			_		—	—		_	OCFLT	OCTSEL	OCM2	OCM1	OCM0	0000
OC4RS	0192							Output (Compare 4	Secondary	Register							FFFF
OC4R	0194							Οι	utput Compa	are 4 Regis	ter							FFFF
OC4CON	0196	_		OCSIDL			_		—	—		_	OCFLT	OCTSEL	OCM2	OCM1	OCM0	0000
OC5RS	0198		Output Compare 5 Secondary Register								FFFF							
OC5R	019A							Οι	utput Compa	are 5 Regis	ter							FFFF
OC5CON	019C	_	_	OCSIDL	_	_	_	_	_	_	_	_	OCFLT	OCTSEL	OCM2	OCM1	OCM0	0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-9: I²C[™] REGISTER MAP

File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
I2C1RCV	0200	_	-	_	—	—	-	—	I2C1 Receive Register 0								0000	
I2C1TRN	0202	_	_	_	_	_	_	-	_				I2C1 Transı	mit Register	r			00FF
I2C1BRG	0204	—		—	_	_		—				Baud Rate	Generator	Register 1				0000
I2C1CON	0206	I2CEN		12CSIDL	SCLREL	IPMIEN	A10M	DISSLW	SMEN	GCEN	STREN	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN	1000
I2C1STAT	0208	ACKSTAT	TRSTAT	_	_	_	BCL	GCSTAT	ADD10	IWCOL	I2COV	D/A	Р	S	R/W	RBF	TBF	0000
I2C1ADD	020A	_	_	_	_	_	_					I2C1 Addre	ss Register					0000
I2C1MSK	020C	_	_	_	_	_	_	AMSK9	AMSK8	AMSK7	AMSK6	AMSK5	AMSK4	AMSK3	AMSK2	AMSK1	AMSK0	0000
I2C2RCV	0210	_		_	_	_		_	_				I2C2 Recei	ve Register				0000
I2C2TRN	0212	_		_	_	_		_	_				I2C2 Transı	mit Register	r			00FF
I2C2BRG	0214	_		_	_	_		_				Baud Rate	Generator	Register 2				0000
I2C2CON	0216	I2CEN		I2CSIDL	SCLREL	IPMIEN	A10M	DISSLW	SMEN	GCEN	STREN	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN	1000
I2C2STAT	0218	ACKSTAT	TRSTAT	_	_	_	BCL	GCSTAT	ADD10	IWCOL	I2COV	D/A	Р	S	R/W	RBF	TBF	0000
I2C2ADD	021A	—		—	_	_			I2C2 Address Register 00							0000		
I2C2MSK	021C	_	_	_	_	_	_	AMSK9	AMSK8	AMSK7	AMSK6	AMSK5	AMSK4	AMSK3	AMSK2	AMSK1	AMSK0	0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

REGISTER 7-5: IFS0: INTERRUPT FLAG STATUS REGISTER 0 (CONTINUED)

- bit 1 IC1IF: Input Capture Channel 1 Interrupt Flag Status bit
 - 1 = Interrupt request has occurred
 - 0 = Interrupt request has not occurred
- bit 0 INTOIF: External Interrupt 0 Flag Status bit
 - 1 = Interrupt request has occurred
 - 0 = Interrupt request has not occurred

7.4 Interrupt Setup Procedures

7.4.1 INITIALIZATION

To configure an interrupt source:

- 1. Set the NSTDIS Control bit (INTCON1<15>) if nested interrupts are not desired.
- Select the user-assigned priority level for the interrupt source by writing the control bits in the appropriate IPCx register. The priority level will depend on the specific application and type of interrupt source. If multiple priority levels are not desired, the IPCx register control bits for all enabled interrupt sources may be programmed to the same non-zero value.

Note: At a device Reset, the IPCx registers are initialized, such that all user interrupt sources are assigned to Priority Level 4.

- 3. Clear the interrupt flag status bit associated with the peripheral in the associated IFSx register.
- 4. Enable the interrupt source by setting the interrupt enable control bit associated with the source in the appropriate IECx register.

7.4.2 INTERRUPT SERVICE ROUTINE

The method that is used to declare an ISR and initialize the IVT with the correct vector address will depend on the programming language (i.e., 'C' or assembler) and the language development toolsuite that is used to develop the application. In general, the user must clear the interrupt flag in the appropriate IFSx register for the source of the interrupt that the ISR handles. Otherwise, the ISR will be re-entered immediately after exiting the routine. If the ISR is coded in assembly language, it must be terminated using a RETFIE instruction to unstack the saved PC value, SRL value and old CPU priority level.

7.4.3 TRAP SERVICE ROUTINE

A Trap Service Routine (TSR) is coded like an ISR, except that the appropriate trap status flag in the INTCON1 register must be cleared to avoid re-entry into the TSR.

7.4.4 INTERRUPT DISABLE

All user interrupts can be disabled using the following procedure:

- 1. Push the current SR value onto the software stack using the PUSH instruction.
- 2. Force the CPU to Priority Level 7 by inclusive ORing the value, OEh, with SRL.

To enable user interrupts, the POP instruction may be used to restore the previous SR value.

Note that only user interrupts with a priority level of 7 or less can be disabled. Trap sources (Levels 8-15) cannot be disabled.

The DISI instruction provides a convenient way to disable interrupts of Priority Levels 1-6 for a fixed period of time. Level 7 interrupt sources are not disabled by the DISI instruction.

PIC24FJ64GA004 FAMILY

TABLE 10-2: SELECTABLE INPUT SOURCES (MAPS INPUT TO FUNCTION)⁽¹⁾

Input Name	Function Name	Register	Configuration Bits
External Interrupt 1	INT1	RPINR0	INTR1<4:0>
External Interrupt 2	INT2	RPINR1	INTR2R<4:0>
Timer2 External Clock	T2CK	RPINR3	T2CKR<4:0>
Timer3 External Clock	T3CK	RPINR3	T3CKR<4:0>
Timer4 External Clock	T4CK	RPINR4	T4CKR<4:0>
Timer5 External Clock	T5CK	RPINR4	T5CKR<4:0>
Input Capture 1	IC1	RPINR7	IC1R<4:0>
Input Capture 2	IC2	RPINR7	IC2R<4:0>
Input Capture 3	IC3	RPINR8	IC3R<4:0>
Input Capture 4	IC4	RPINR8	IC4R<4:0>
Input Capture 5	IC5	RPINR9	IC5R<4:0>
Output Compare Fault A	OCFA	RPINR11	OCFAR<4:0>
Output Compare Fault B	OCFB	RPINR11	OCFBR<4:0>
UART1 Receive	U1RX	RPINR18	U1RXR<4:0>
UART1 Clear-to-Send	U1CTS	RPINR18	U1CTSR<4:0>
UART2 Receive	U2RX	RPINR19	U2RXR<4:0>
UART2 Clear-to-Send	U2CTS	RPINR19	U2CTSR<4:0>
SPI1 Data Input	SDI1	RPINR20	SDI1R<4:0>
SPI1 Clock Input	SCK1IN	RPINR20	SCK1R<4:0>
SPI1 Slave Select Input	SS1IN	RPINR21	SS1R<4:0>
SPI2 Data Input	SDI2	RPINR22	SDI2R<4:0>
SPI2 Clock Input	SCK2IN	RPINR22	SCK2R<4:0>
SPI2 Slave Select Input	SS2IN	RPINR23	SS2R<4:0>

Note 1: Unless otherwise noted, all inputs use the Schmitt Trigger input buffers.

PIC24FJ64GA004 FAMILY

REGISTER 10-23: RPOR8: PERIPHERAL PIN SELECT OUTPUT REGISTER 8

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	RP17R4 ⁽¹⁾	RP17R3 ⁽¹⁾	RP17R2 ⁽¹⁾	RP17R1 ⁽¹⁾	RP17R0 ⁽¹⁾
bit 15							bit 8

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	RP16R4 ⁽¹⁾	RP16R3 ⁽¹⁾	RP16R2 ⁽¹⁾	RP16R1 ⁽¹⁾	RP16R0 ⁽¹⁾
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	1 as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-13	Unimplemented: Read	as	'0'
	ormpicific a. Read	uu	0

bit 12-8	RP17R<4:0>: Peripheral Output Function is Assigned to RP17 Output Pin bits ⁽¹⁾ (see Table 10-3 for peripheral function numbers)
bit 7-5	Unimplemented: Read as '0'
bit 4-0	RP16R<4:0>: Peripheral Output Function is Assigned to RP16 Output Pin bits ⁽¹⁾

(see Table 10-3 for peripheral function numbers)

REGISTER 10-24: RPOR9: PERIPHERAL PIN SELECT OUTPUT REGISTER 9

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	RP19R4 ⁽¹⁾	RP19R3 ⁽¹⁾	RP19R2 ⁽¹⁾	RP19R1 ⁽¹⁾	RP19R0 ⁽¹⁾
bit 15							bit 8

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	RP18R4 ⁽¹⁾	RP18R3 ⁽¹⁾	RP18R2 ⁽¹⁾	RP18R1 ⁽¹⁾	RP18R0 ⁽¹⁾
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-13 Unimplemented: Read as '0'

- bit 12-8 **RP19R<4:0>:** Peripheral Output Function is Assigned to RP19 Output Pin bits⁽¹⁾ (see Table 10-3 for peripheral function numbers)
- bit 7-5 Unimplemented: Read as '0'
- bit 4-0 **RP18R<4:0>:** Peripheral Output Function is Assigned to RP18 Output Pin bits⁽¹⁾ (see Table 10-3 for peripheral function numbers)
- Note 1: These bits are only available on the 44-pin devices; otherwise, they read as '0'.

Note 1: These bits are only available on the 44-pin devices; otherwise, they read as '0'.

13.1 Input Capture Registers

REGISTER 13-1: ICxCON: INPUT CAPTURE x CONTROL REGISTER

U-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0
	—	ICSIDL	—	—	—	—	—
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R-0, HC	R-0, HC	R/W-0	R/W-0	R/W-0
ICTMR	ICI1	ICI0	ICOV	ICBNE	ICM2 ⁽¹⁾	ICM1 ⁽¹⁾	ICM0 ⁽¹⁾
bit 7							bit 0

Legend:	HC = Hardware Clearable bit			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'		
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown	

bit 15-14	Unimplemented: Read as '0'
bit 13	ICSIDL: Input Capture x Stop in Idle Control bit
	 1 = Input capture module will halt in CPU Idle mode 0 = Input capture module will continue to operate in CPU Idle mode
bit 12-8	Unimplemented: Read as '0'
bit 7	ICTMR: Input Capture x Timer Select bit
	 1 = TMR2 contents are captured on capture event 0 = TMR3 contents are captured on capture event
bit 6-5	ICI<1:0>: Select Number of Captures per Interrupt bits
	 11 = Interrupt on every fourth capture event 10 = Interrupt on every third capture event 01 = Interrupt on every second capture event 00 = Interrupt on every capture event
bit 4	ICOV: Input Capture x Overflow Status Flag bit (read-only)
	 1 = Input capture overflow occurred 0 = No input capture overflow occurred
bit 3	ICBNE: Input Capture x Buffer Empty Status bit (read-only)
	 1 = Input capture buffer is not empty, at least one more capture value can be read 0 = Input capture buffer is empty
bit 2-0	ICM<2:0>: Input Capture x Mode Select bits ⁽¹⁾
	 111 = Input capture functions as interrupt pin only when device is in Sleep or Idle mode (rising edge detect only, all other control bits are not applicable) 110 = Unused (module is disabled) 101 = Capture mode, every 16th rising edge 100 = Capture mode, every 4th rising edge 011 = Capture mode, every rising edge 010 = Capture mode, every falling edge 010 = Capture mode, every falling edge 001 = Capture mode, every edge (rising and falling) – ICI<1:0> bits do not control interrupt generation for this mode 000 = Input capture module is turned off
Note 1:	RPINRx (ICxRx) must be configured to an available RPn pin. For more information, see Section 10.4 "Peripheral Pin Select (PPS)".

PIC24FJ64GA004 FAMILY

FIGURE 14-1: OUTPUT COMPARE x MODULE BLOCK DIAGRAM



4: This peripheral's inputs and outputs must be assigned to an available RPn pin before use. Please see Section 10.4 "Peripheral Pin Select (PPS)" for more information.

R/W-0	U-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0 ⁽³⁾	R/W-0 ⁽³⁾
UARTEN ⁽	1)	USIDL	IREN ⁽²⁾	RTSMD	_	UEN1	UEN0
bit 15							bit 8
R/C-0, HC	C R/W-0	R/W-0, HC	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
WAKE	LPBACK	ABAUD	RXINV	BRGH	PDSEL1	PDSEL0	STSEL
bit 7							bit 0
· · ·							
Legend:		C = Clearable	bit	HC = Hardwa	re Clearable bi	t . (c)	
R = Reada	ble bit	W = Writable I	Dit		nented bit, read		
-n = Value	at POR	'1' = Bit is set		0° = Bit is clea	ared	x = Bit is unkn	own
bit 15		DTy Enable bit	(1)				
DIL 15	1 = 11 ARTy	R IX Enabled: all LL	ΔRTx nins are	controlled by I	IARTy as defin	ed by LIEN<1.0)>
	0 = UARTx is minimal	s disabled; all U	ARTx pins are	controlled by F	PORT latches;	UARTx power c	onsumption is
bit 14	Unimplemen	ted: Read as 'o	,				
bit 13	USIDL: UAR	Tx Stop in Idle N	lode bit				
	1 = Discontin	ues module op	eration when o	device enters lo	lle mode		
	0 = Continue	s module opera	ition in Idle mo	ode			
bit 12	IREN: IrDA® I	Encoder and De	ecoder Enable	bit'~			
	1 = IrDA encoder0 = IrDA encoder	oder and decod	er are enable er are disable	d d			
bit 11	RTSMD: Mod	le Selection for	UxRTS Pin bi	t			
	$1 = \frac{UxRTS}{UxRTS} p$ 0 = UxRTS p	in in Simplex m in in Flow Cont	ode rol mode				
bit 10	Unimplemen	ted: Read as 'o	,				
bit 9-8	UEN<1:0>: U	ARTx Enable b	its ⁽³⁾				
	11 = UxTX, L	JxRX and BCLK	x p <u>ins are</u> ena	abled and used	; UxCTS pin is	controlled by P	ORT latches
	10 = UxTX, L	JxRX, UxCTS a	nd UxRTS pin	s are enabled a	and used	controlled by P	
	00 = UxTX ar	d UxRX pins are	enabled and u	used; UxCTS an	d UxRTS/BCL	CX pins are contr	olled by PORT
	latches	·					
bit 7	WAKE: Wake	e-up on Start Bit	Detect During	g Sleep Mode E	nable bit		
	1 = UARTx w	/ill continue to sa	ample the UxR	X pin; interrupt	is generated o	n falling edge, b	it is cleared in
	0 = No wake	-up is enabled	sing edge				
bit 6	LPBACK: UA	RTx Loopback	Mode Select I	bit			
	1 = Enables	Loopback mode	;				
	0 = Loopbac	k mode is disab	led				
bit 5	ABAUD: Auto	o-Baud Enable I	oit				
	1 = Enables	baud rate meas	urement on th	ne next characte	er – requires re	eception of a Sy	nc field (55h);
	0 = Baud rate	e measurement	is disabled or	completed			
					Course of the second		
NOTE 1:	IT UARIEN = 1, th Section 10.4 "Pe	ne peripheral in eripheral Pin Se	puts and outpo elect (PPS)" f	uts must be cor or more information	nigured to an a ation.	ivaliable RPh pi	in. See
2:	This feature is on	ly available for	the 16x BRG r	mode (BRGH =	0).		
	B., .,						

REGISTER 17-1: UXMODE: UARTX MODE REGISTER

3: Bit availability depends on pin availability.

REGISTER 17-2: UxSTA: UARTx STATUS AND CONTROL REGISTER (CONTINUED)

bit 5	ADDEN: Address Character Detect bit (bit 8 of received data = 1)
	 1 = Address Detect mode is enabled; if 9-bit mode is not selected, this does not take effect 0 = Address Detect mode is disabled
bit 4	RIDLE: Receiver Idle bit (read-only)
	1 = Receiver is Idle0 = Receiver is active
bit 3	PERR: Parity Error Status bit (read-only)
	 1 = Parity error has been detected for the current character (character at the top of the receive FIFO) 0 = Parity error has not been detected
bit 2	FERR: Framing Error Status bit (read-only)
	 1 = Framing error has been detected for the current character (character at the top of the receive FIFO) 0 = Framing error has not been detected
bit 1	OERR: Receive Buffer Overrun Error Status bit (clear/read-only)
	1 = Receive buffer has overflowed
	 0 = Receive buffer has not overflowed (clearing a previously set OERR bit (1 → 0 transition) will reset the receiver buffer and the RSR to the empty state)
bit 0	URXDA: UARTx Receive Buffer Data Available bit (read-only)
	 1 = Receive buffer has data; at least one more character can be read 0 = Receive buffer is empty
Note 1:	If UARTEN = 1, the peripheral inputs and outputs must be configured to an available RPn pin. See Section 10.4 "Peripheral Pin Select (PPS)" for more information.

PIC24FJ64GA004 FAMILY

REGISTER 18-3: PMADDR: PARALLEL PORT ADDRESS REGISTER

U-0	R/W-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
—	CS1	—	—	—	ADDR10 ⁽¹⁾	ADDR9 ⁽¹⁾	ADDR8 ⁽¹⁾
bit 15							bit 8

| R/W-0 |
|----------------------|----------------------|----------------------|----------------------|----------------------|----------------------|----------------------|----------------------|
| ADDR7 ⁽¹⁾ | ADDR6 ⁽¹⁾ | ADDR5 ⁽¹⁾ | ADDR4 ⁽¹⁾ | ADDR3 ⁽¹⁾ | ADDR2 ⁽¹⁾ | ADDR1 ⁽¹⁾ | ADDR0 ⁽¹⁾ |
| bit 7 | | | | | | | bit 0 |

Legend:				
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'		
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown	

- bit 14 CS1: Chip Select 1 bit
 - 1 = Chip Select 1 is active
 - 0 = Chip Select 1 is inactive
- bit 13-11 Unimplemented: Read as '0'
- bit 10-0 ADDR<10:0>: Parallel Port Destination Address bits⁽¹⁾
- **Note 1:** PMA<10:2> bits are not available on 28-pin devices.

REGISTER 18-4: PMAEN: PARALLEL PORT ENABLE REGISTER

U-0	R/W-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
—	PTEN14	—	—	—	PTEN10 ⁽¹⁾	PTEN9 ⁽¹⁾	PTEN8 ⁽¹⁾
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PTEN7 ⁽¹⁾	PTEN6 ⁽¹⁾	PTEN5 ⁽¹⁾	PTEN4 ⁽¹⁾	PTEN3 ⁽¹⁾	PTEN2 ⁽¹⁾	PTEN1	PTEN0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	l as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15	Unimplemented: Read as '0'
bit 14	PTEN14: PMCS1 Strobe Enable bit
	1 = PMCS1 pin functions as chip select0 = PMCS1 pin functions as port I/O
bit 13-11	Unimplemented: Read as '0'
bit 10-2	PTEN<10:2>: PMP Address Port Enable bits ⁽¹⁾
	1 = PMA<10:2> function as PMP address lines0 = PMA<10:2> function as port I/O
bit 1-0	PTEN<1:0>: PMALH/PMALL Strobe Enable bits
	 1 = PMA1 and PMA0 function as either PMA<1:0> or PMALH and PMALL 0 = PMA1 and PMA0 pads functions as port I/O

Note 1: PMA<10:2> bits are not available on 28-pin devices.

REGISTER 19-9: ALWDHR: ALARM WEEKDAY AND HOURS VALUE REGISTEI	REGISTER 19-9:	ALWDHR: ALARM WEEKDAY AND HOURS VALUE REGISTER ⁽¹⁾
---	----------------	---

U-0	U-0	U-0	U-0	U-0	R/W-x	R/W-x	R/W-x
	—	—	_		WDAY2	WDAY1	WDAY0
bit 15							bit 8
U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
_	—	HRTEN1	HRTEN0	HRONE3	HRONE2	HRONE1	HRONE0
bit 7					•	•	bit 0
Legend:							
R = Readable bit W = Writable bit		U = Unimplemented bit, read as '0'					
-n = Value at POR '1' = Bit is set		'0' = Bit is cleared x = Bit is unknown			iown		
bit 15-11	bit 15-11 Unimplemented: Read as '0'						
bit 10-8 WDAY<2:0>: Binary Coded Decimal Value of Weekday Digit bits							
	Contains a value from 0 to 6.						
bit 7-6	bit 7-6 Unimplemented: Read as '0'						
bit 5-4	HRTEN<1:0>	Binary Coded	Decimal Value	e of Hour's Ten	s Digit bits		
	Contains a value from 0 to 2.						

bit 3-0 **HRONE<3:0>:** Binary Coded Decimal Value of Hour's Ones Digit bits Contains a value from 0 to 9.

REGISTER 19-10: ALMINSEC: ALARM MINUTES AND SECONDS VALUE REGISTER

U-0	R/W-x						
—	MINTEN2	MINTEN1	MINTEN0	MINONE3	MINONE2	MINONE1	MINONE0
bit 15							bit 8

U-0	R/W-x						
—	SECTEN2	SECTEN1	SECTEN0	SECONE3	SECONE2	SECONE1	SECONE0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	d as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15	Unimplemented: Read as '0'
bit 14-12	MINTEN<2:0>: Binary Coded Decimal Value of Minute's Tens Digit bits
	Contains a value from 0 to 5.
bit 11-8	MINONE<3:0>: Binary Coded Decimal Value of Minute's Ones Digit bits
	Contains a value from 0 to 9.
bit 7	Unimplemented: Read as '0'
bit 6-4	SECTEN<2:0>: Binary Coded Decimal Value of Second's Tens Digit bits
	Contains a value from 0 to 5.
bit 3-0	SECONE<3:0>: Binary Coded Decimal Value of Second's Ones Digit bits
	Contains a value from 0 to 9.

© 2010-2013 Microchip Technology Inc.

Note 1: A write to this register is only allowed when RTCWREN = 1.

21.0 10-BIT HIGH-SPEED A/D CONVERTER

Note:	This data sheet summarizes the features of
	this group of PIC24F devices. It is not
	intended to be a comprehensive reference
	source. For more information, refer to the
	"PIC24F Family Reference Manual",
	"10-Bit A/D Converter" (DS39705).

The 10-bit A/D Converter has the following key features:

- · Successive Approximation (SAR) conversion
- Conversion speeds of up to 500 ksps
- Up to 13 analog input pins
- External voltage reference input pins
- · Automatic Channel Scan mode
- · Selectable conversion trigger source
- 16-word conversion result buffer
- · Selectable Buffer Fill modes
- · Four result alignment options
- Operation during CPU Sleep and Idle modes

Depending on the particular device pinout, the 10-bit A/D Converter can have up to three analog input pins, designated AN0 through AN12. In addition, there are two analog input pins for external voltage reference connections. These voltage reference inputs may be shared with other analog input pins. The actual number of analog input pins and the external voltage reference input configuration will depend on the specific device.

A block diagram of the A/D Converter is shown in Figure 21-1.

To perform an A/D conversion:

- 1. Configure the A/D module:
 - a) Select the port pins as analog inputs (AD1PCFG<15:0>).
 - b) Select the voltage reference source to match the expected range on the analog inputs (AD1CON2<15:13>).
 - c) Select the analog conversion clock to match the desired data rate with the processor clock (AD1CON3<7:0>).
 - d) Select the appropriate sample/conversion sequence (AD1CON1<7:5> and AD1CON3<12:8>).
 - e) Select how conversion results are presented in the buffer (AD1CON1<9:8>).
 - f) Select the interrupt rate (AD1CON2<5:2>).
 - g) Turn on the A/D module (AD1CON1<15>).
- 2. Configure the A/D interrupt (if required):
 - a) Clear the AD1IF bit.
 - b) Select the A/D interrupt priority.

NOTES:

44-Lead Plastic Quad Flat, No Lead Package (ML) - 8x8 mm Body [QFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-103C Sheet 1 of 2

APPENDIX B: ADDITIONAL GUIDANCE FOR PIC24FJ64GA004 FAMILY APPLICATIONS

B.1 Additional Methods for Power Reduction

Devices in the PIC24FJ64GA004 family include a number of core features to significantly reduce the application's power requirements. For truly power-sensitive applications, it is possible to further reduce the application's power demands by taking advantage of the device's regulator architecture. These methods help decrease power in two ways: by disabling the internal voltage regulator to eliminate its power consumption, and by reducing the voltage on VDDCORE to lower the device's dynamic current requirements. Using these methods, it is possible to reduce Sleep currents (IPD) from 3.5 µA to 250 nA (typical values, refer to Parameters DC60d and DC60g in Table 27-6). For dynamic power consumption, the reduction in VDDCORE from 2.5V provided by the regulator, to 2.0V, can provide a power reduction of about 30%.

When using a regulated power source or a battery with a constant output voltage, it is possible to decrease power consumption by disabling the regulator. In this case (Figure B-1), a simple diode can be used to reduce the voltage from 3V or greater to the 2V-2.5V required for VDDCORE. This method is only advised on power supplies, such as Lithium Coin cells, which maintain a constant voltage over the life of the battery.

FIGURE B-1: POWER REDUCTION EXAMPLE FOR CONSTANT VOLTAGE SUPPLIES



A similar method can be used for non-regulated sources (Figure B-2). In this case, it can be beneficial to use a low quiescent current, external voltage regulator. Devices, such as the MCP1700, consume only 1 μ A to regulate to 2V or 2.5V, which is lower than the current required to power the internal voltage regulator.

FIGURE B-2: POWER REDUCTION EXAMPLE FOR NON-REGULATED SUPPLIES



NOTES: