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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM® Cortex®-A9
Number of Cores/Bus Width	2 Core, 32-Bit
Speed	1.0GHz
Co-Processors/DSP	Multimedia; NEON™ SIMD
RAM Controllers	LPDDR2, DDR3L, DDR3
Graphics Acceleration	Yes
Display & Interface Controllers	HDMI, Keypad, LCD, LVDS, MIPI/DSI, Parallel
Ethernet	10/100/1000Mbps (1)
SATA	SATA 3Gbps (1)
USB	USB 2.0 + PHY (3), USB 2.0 OTG + PHY (1)
Voltage - I/O	1.8V, 2.5V, 2.8V, 3.3V
Operating Temperature	-40°C ~ 125°C (TJ)
Security Features	ARM TZ, A-HAB, CAAM, CSU, SJC, SNVS
Package / Case	624-FBGA, FCBGA
Supplier Device Package	624-FCBGA (21x21)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcimx6dp4avt1aa

1.1 Ordering Information

Table 1 shows examples of orderable part numbers covered by this data sheet. This table does not include all possible orderable part numbers. The latest part numbers are available on freescale.com/imx6series. If your desired part number is not listed in the table, or you have questions about available parts, see freescale.com/imx6series or contact your Freescale representative.

Table 1. Example Orderable Part Numbers

Part Number	Quad/Dual	CPU Options	Speed[1]	Temperature Grade	Package
MCIMX6DP4AVT8AA	i.MX 6DualPlus	no VPU	852 MHz	Automotive	21 mm x 21 mm, 0.8 mm pitch, FCPBGA (lidded)
MCIMX6DP6AVT8AA	i.MX 6DualPlus	Full Featured Product	852 MHz	Automotive	21 mm x 21 mm, 0.8 mm pitch, FCPBGA (lidded)
MCIMX6DP4AVT1AA	i.MX 6DualPlus	no VPU	1 GHz	Automotive	21 mm x 21 mm, 0.8 mm pitch, FCPBGA (lidded)
MCIMX6DP6AVT1AA	i.MX 6DualPlus	Full Featured Product	1 GHz	Automotive	21 mm x 21 mm, 0.8 mm pitch, FCPBGA (lidded)
MCIMX6QP4AVT8AA	i.MX 6QuadPlus	no VPU	852 MHz	Automotive	21 mm x 21 mm, 0.8 mm pitch, FCPBGA (lidded)
MCIMX6QP6AVT8AA	i.MX 6QuadPlus	Full Featured Product	852 MHz	Automotive	21 mm x 21 mm, 0.8 mm pitch, FCPBGA (lidded)
MCIMX6QP4AVT1AA	i.MX 6QuadPlus	no VPU	1 GHz	Automotive	21 mm x 21 mm, 0.8 mm pitch, FCPBGA (lidded)
MCIMX6QP6AVT1AA	i.MX 6QuadPlus	Full Featured Product	1 GHz	Automotive	21 mm x 21 mm, 0.8 mm pitch, FCPBGA (lidded)

[1] If a 24 MHz input clock is used (required for USB), the maximum speed is limited to 996 MHz.

Figure 1 describes the part number nomenclature to identify the characteristics of the specific part number you have (for example, cores, frequency, temperature grade, fuse options, silicon revision). Figure 1 applies to the i.MX 6DualPlus/6QuadPlus.

The two characteristics that identify which data sheet a specific part applies to are the part number series field and the temperature grade (junction) field:

- The i.MX 6DualPlus/6QuadPlus Automotive Applications Processors data sheet (IMX6DQPAEC) covers parts listed for the “Plus” series and with “A” indicating automotive temperature.
- The i.MX 6DualPlus/6QuadPlus Applications Processors for Consumer Products data sheet (IMX6DQPCEC) covers parts listed with “D (Commercial temp)” or “E (Extended Commercial temp)”
- The i.MX 6DualPlus/6QuadPlus Applications Processors for Industrial Products data sheet (IMX6DQPIEC) covers parts listed with “C (Industrial temp)”

Ensure that you have the right data sheet for your specific part by checking the fields: Part # Series (DP/QP), temperature grade (junction) (A), and Frequency (8).

Table 2. i.MX 6DualPlus/6QuadPlus Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
EPIT-1 EPIT-2	Enhanced Periodic Interrupt Timer	Timer Peripherals	Each EPIT is a 32-bit “set and forget” timer that starts counting after the EPIT is enabled by software. It is capable of providing precise interrupts at regular intervals with minimal processor intervention. It has a 12-bit prescaler for division of input clock frequency to get the required time setting for the interrupts to occur, and counter value can be programmed on the fly.
ESAI	Enhanced Serial Audio Interface	Connectivity Peripherals	The Enhanced Serial Audio Interface (ESAI) provides a full-duplex serial port for serial communication with a variety of serial devices, including industry-standard codecs, SPDIF transceivers, and other processors. The ESAI consists of independent transmitter and receiver sections, each section with its own clock generator. All serial transfers are synchronized to a clock. Additional synchronization signals are used to delineate the word frames. The normal mode of operation is used to transfer data at a periodic rate, one word per period. The network mode is also intended for periodic transfers; however, it supports up to 32 words (time slots) per period. This mode can be used to build time division multiplexed (TDM) networks. In contrast, the on-demand mode is intended for non-periodic transfers of data and to transfer data serially at high speed when the data becomes available. The ESAI has 12 pins for data and clocking connection to external devices.
FlexCAN-1 FlexCAN-2	Flexible Controller Area Network	Connectivity Peripherals	The CAN protocol was primarily, but not only, designed to be used as a vehicle serial data bus, meeting the specific requirements of this field: real-time processing, reliable operation in the Electromagnetic interference (EMI) environment of a vehicle, cost-effectiveness and required bandwidth. The FlexCAN module is a full implementation of the CAN protocol specification, Version 2.0 B, which supports both standard and extended message frames.
GPIO-1 GPIO-2 GPIO-3 GPIO-4 GPIO-5 GPIO-6 GPIO-7	General Purpose I/O Modules	System Control Peripherals	Used for general purpose input/output to external devices. Each GPIO module supports 32 bits of I/O.
GPMI	General Purpose Media Interface	Connectivity Peripherals	The GPMI module supports up to 8x NAND devices. 40-bit ECC error correction for NAND Flash controller (GPMI2). The GPMI supports separate DMA channels per NAND device.
GPT	General Purpose Timer	Timer Peripherals	Each GPT is a 32-bit “free-running” or “set and forget” mode timer with programmable prescaler and compare and capture register. A timer counter value can be captured using an external event and can be configured to trigger a capture event on either the leading or trailing edges of an input pulse. When the timer is configured to operate in “set and forget” mode, it is capable of providing precise interrupts at regular intervals with minimal processor intervention. The counter has output compare logic to provide the status and interrupt at comparison. This timer can be configured to run either on an external clock or on an internal clock.

4 Refer to JEDEC DDR3 SDRAM Standards for Data Setup (tDS), Hold (tDH) and Slew Rate Derating tables.

Figure 26 shows the DDR3/DDR3L read timing diagram. The timing parameters for this diagram appear in Table 44.

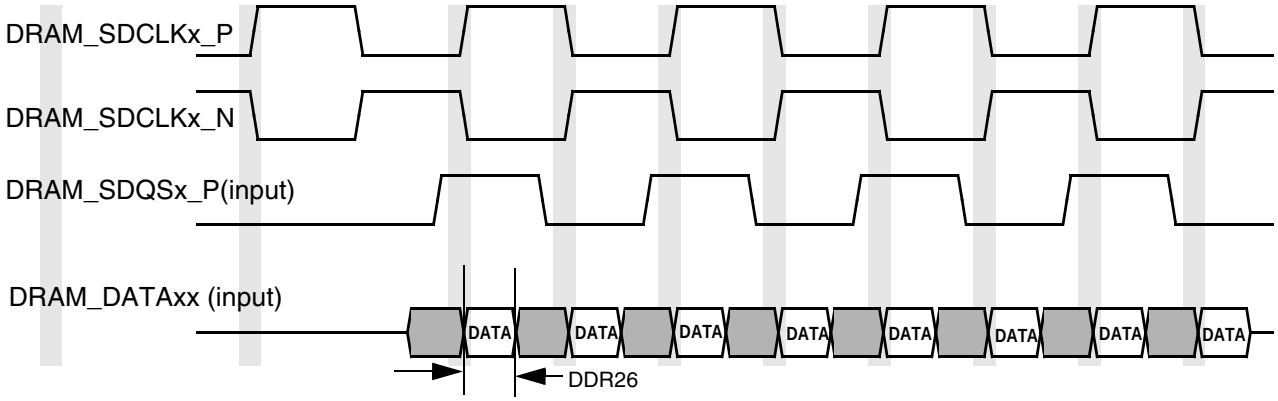


Figure 26. DDR3/DDR3L Read Cycle

Table 44. DDR3/DDR3L Read Cycle

ID	Parameter[1,2,3]	Symbol	CK = 532 MHz		Unit
			Min	Max	
DDR26	Minimum required DRAM_DATAxx valid window width.	—	450	—	ps

1 To receive the reported setup and hold values, the read calibration must be performed to locate the DRAM_SDQSx_P in the middle of DRAM_DATAxx window.

2 All measurements are in reference to Vref level.

3 Measurements were completed using balanced load and a 25 Ω resistor from outputs to DRAM_VREF.

4.9.4.2 LPDDR2 Parameters

Figure 27 shows the LPDDR2 basic timing diagram. The timing parameters for this diagram appear in Table 45.

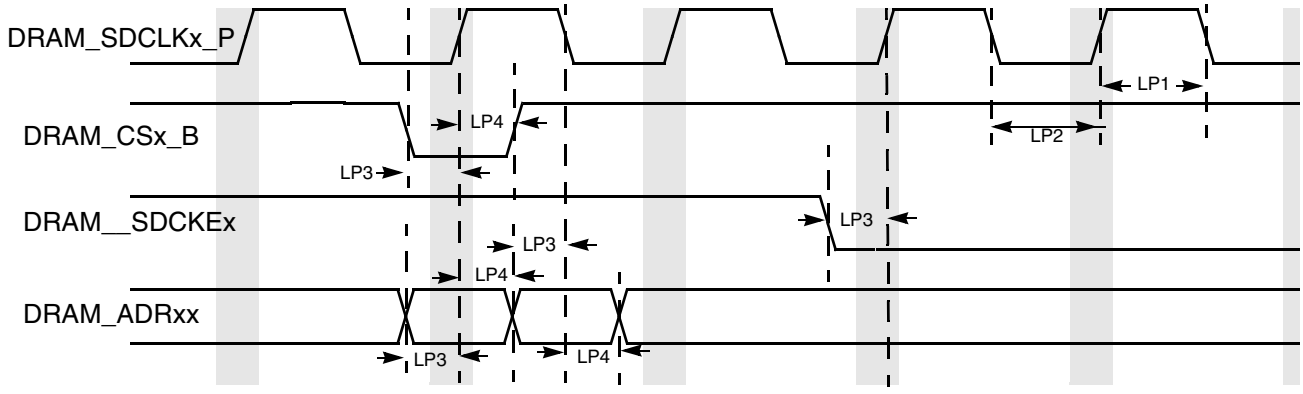


Figure 27. LPDDR2 Command and Address Timing Diagram

Table 46. LPDDR2 Write Cycle (continued)

ID	Parameter[1,2,3]	Symbol	CK = 400 MHz		Unit
			Min	Max	
LP22	DRAM_SDQSx_P high level width	t_{DQSH}	0.4	—	tCK
LP23	DRAM_SDQSx_P low level width	t_{DQSL}	0.4	—	tCK

1 To receive the reported setup and hold values, the write calibration must be performed to locate the DRAM_SDQSx_P in the middle of DRAM_DATAxx window.

2 All measurements are in reference to Vref level.

3 Measurements were completed using balanced load and a 25 Ω resistor from outputs to DRAM_VREF.

Figure 29 shows the LPDDR2 read timing diagram. The timing parameters for this diagram appear in Table 47.

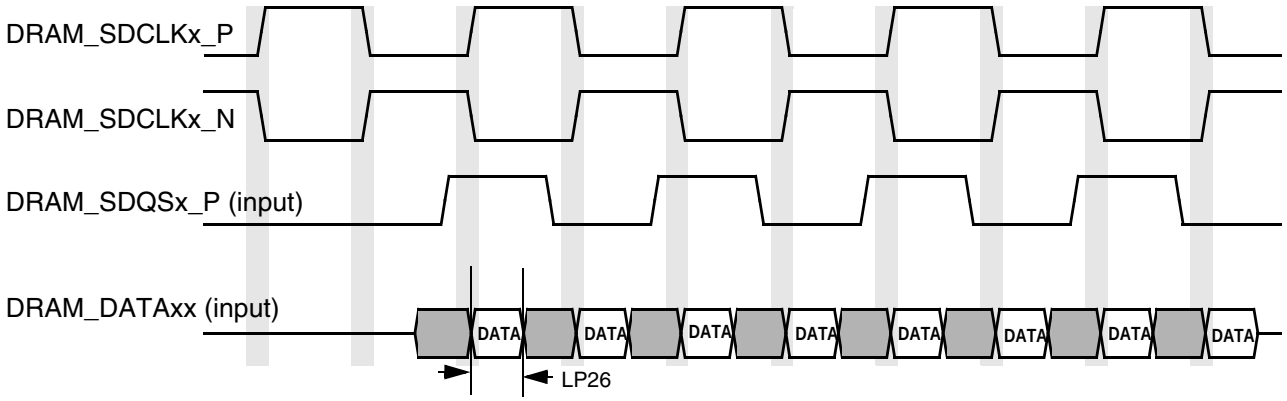


Figure 29. LPDDR2 Read Cycle

Table 47. LPDDR2 Read Cycle

ID	Parameter[1,2,3]	Symbol	CK = 400 MHz		Unit
			Min	Max	
LP26	Minimum required DRAM_DATAxx valid window width for LPDDR2	—	330	—	ps

1 To receive the reported setup and hold values, read calibration must be performed to locate the DRAM_SDQSx_P in the middle of DRAM_DATAxx window.

2 All measurements are in reference to Vref level.

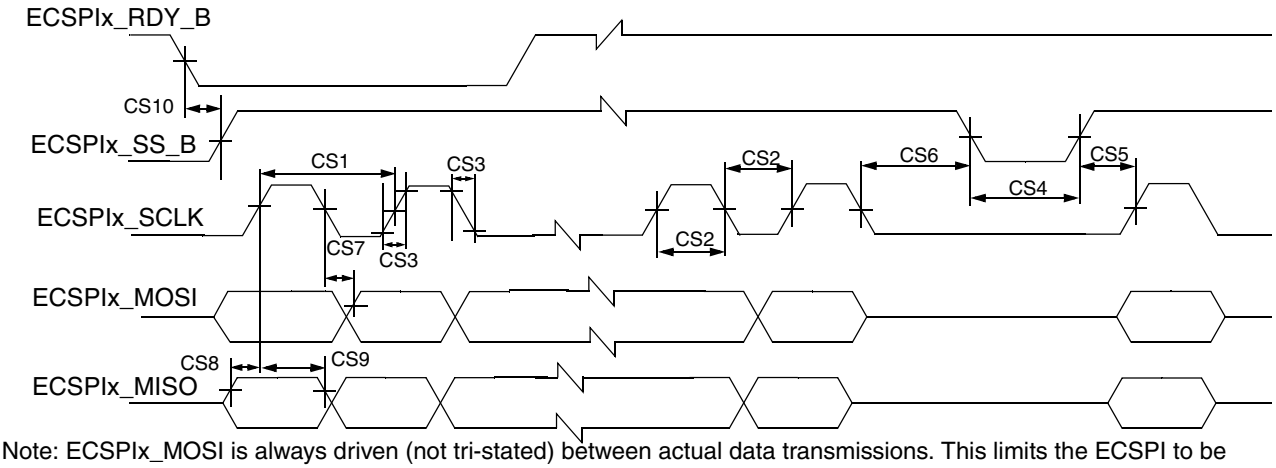
3 Measurements were completed using balanced load and a 25 Ω resistor from outputs to DRAM_VREF.

4.10 General-Purpose Media Interface (GPMI) Timing

The i.MX 6DualPlus/6QuadPlus GPMI controller is a flexible interface NAND Flash controller with 8-bit data width, up to 200 MB/s I/O speed and individual chip select. It supports Asynchronous timing mode, Source Synchronous timing mode, and Samsung Toggle timing mode separately described in the following subsections.

4.11.2.1 ECSPI Master Mode Timing

Figure 41 depicts the timing of ECSPI in master mode and Table 51 lists the ECSPI master mode timing characteristics.



Note: ECSPIx_MOSI is always driven (not tri-stated) between actual data transmissions. This limits the ECSPI to be connected between a single master and a single slave.

Figure 41. ECSPI Master Mode Timing Diagram

Table 51. ECSPI Master Mode Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
CS1	ECSPIx_SCLK Cycle Time–Read • Slow group[1] • Fast group[2] ECSPIx_SCLK Cycle Time–Write	t_{clk}	 55 40 15	—	ns
CS2	ECSPIx_SCLK High or Low Time–Read • Slow group[1] • Fast group[2] ECSPIx_SCLK High or Low Time–Write	t_{SW}	 26 20 7	—	ns
CS3	ECSPIx_SCLK Rise or Fall[3]	$t_{RISE/FALL}$	—	—	ns
CS4	ECSPIx_SSx pulse width	t_{CSLH}	Half ECSPIx_SCLK period	—	ns
CS5	ECSPIx_SSx Lead Time (CS setup time)	t_{SCS}	Half ECSPIx_SCLK period - 4	—	ns
CS6	ECSPIx_SSx Lag Time (CS hold time)	t_{HCS}	Half ECSPIx_SCLK period - 2	—	ns
CS7	ECSPIx_MOSI Propagation Delay (C_{LOAD} = 20 pF)	t_{PDmosi}	-1	1	ns
CS8	ECSPIx_MISO Setup Time • Slow group[1] • Fast group[2]	t_{Smiso}	 21.5 16	—	ns
CS9	ECSPIx_MISO Hold Time	t_{Hmiso}	0	—	ns
CS10	ECSPIx_RDY to ECSPIx_SSx Time[4]	t_{SDRY}	5	—	ns

1 ECSPI slow includes:

ECSPI1/DISP0_DAT22, ECSPI1/KEY_COL1, ECSPI1/CSI0_DAT6, ECSPI2/EIM_OE, ECSPI2/ ECSPI2/CSI0_DAT10, ECSPI3/DISP0_DAT2

2 ECSPI fast includes:

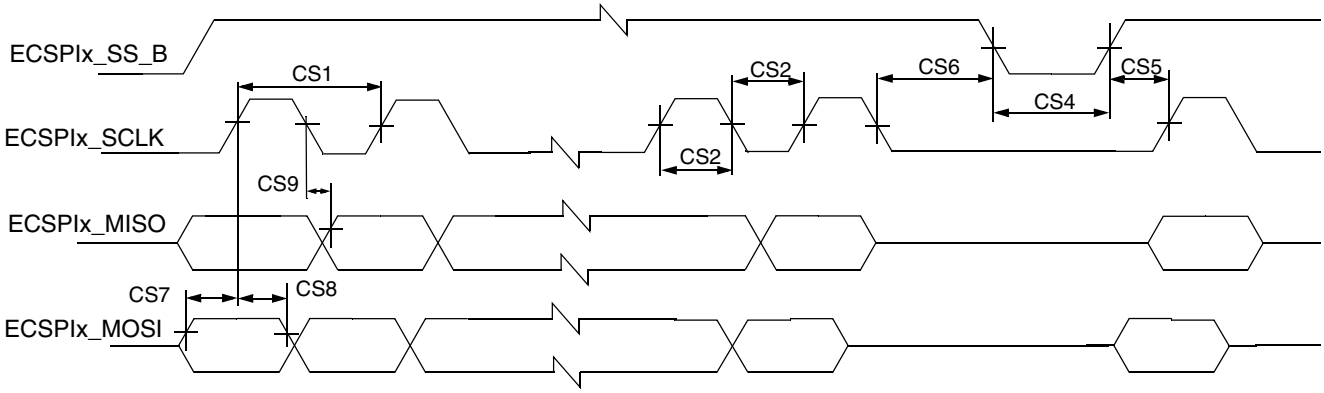
ECSPI1/EIM_D17, ECSPI4/EIM_D22, ECSPI5/SD2_DAT0, ECSPI5/SD1_DAT0

3 See specific I/O AC parameters Section 4.7, “I/O AC Parameters.”

4 ECSPI_RDY is sampled internally by ipg_clk and is asynchronous to all other CSPI signals.

4.11.2.2 ECSPI Slave Mode Timing

Figure 42 depicts the timing of ECSPI in slave mode and Table 52 lists the ECSPI slave mode timing characteristics.



Note: ECSPIx_MISO is always driven (not tri-stated) between actual data transmissions. This limits the ECSPI to be connected between a single master and a single slave.

Figure 42. ECSPI Slave Mode Timing Diagram

Table 52. ECSPI Slave Mode Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
CS1	ECSPIx_SCLK Cycle Time–Read • Slow group[1] • Fast group[2] ECSPIx_SCLK Cycle Time–Write	t_{clk}	 55 40 15	—	ns
CS2	ECSPIx_SCLK High or Low Time–Read • Slow group[1] • Fast group[2] ECSPIx_SCLK High or Low Time–Write	t_{SW}	 26 20 7	—	ns
CS4	ECSPIx_SSx pulse width	t_{CSLH}	Half ECSPIx_SCLK period	—	ns
CS5	ECSPIx_SSx Lead Time (CS setup time)	t_{SCS}	5	—	ns
CS6	ECSPIx_SSx Lag Time (CS hold time)	t_{HCS}	5	—	ns
CS7	ECSPIx_MOSI Setup Time	t_{Smosi}	4	—	ns
CS8	ECSPIx_MOSI Hold Time	t_{Hmosi}	4	—	ns
CS9	ECSPIx_MISO Propagation Delay (C_{LOAD} = 20 pF) • Slow group[1] • Fast group[2]	t_{PDmiso}	4	 25 17	ns

[1] ECSPI slow includes:
ECSPI1/DISP0_DAT22, ECSPI1/KEY_COL1, ECSPI1/CSI0_DAT6, ECSPI2/EIM_OE, ECSPI2/DISP0_DAT17, ECSPI2/CSI0_DAT10, ECSPI3/DISP0_DAT2

[2] ECSPI fast includes:
ECSPI1/EIM_D17, ECSPI4/EIM_D22, ECSPI5/SD2_DAT0, ECSPI5/SD1_DAT0

Table 53. Enhanced Serial Audio Interface (ESAI) Timing (continued)

ID	Parameter[1,2]	Symbol	Expression[2]	Min	Max	Condition[3]	Unit
81	ESAI_TX_CLK rising edge to ESAI_TX_FS out (wr) low[5]	— —	— —	— —	22.0 12.0	x ck i ck	ns
82	ESAI_TX_CLK rising edge to ESAI_TX_FS out (wl) high	— —	— —	— —	19.0 9.0	x ck i ck	ns
83	ESAI_TX_CLK rising edge to ESAI_TX_FS out (wl) low	— —	— —	— —	20.0 10.0	x ck i ck	ns
84	ESAI_TX_CLK rising edge to data out enable from high impedance	— —	— —	— —	22.0 17.0	x ck i ck	ns
86	ESAI_TX_CLK rising edge to data out valid	— —	— —	— —	19.0 13.0	x ck i ck	ns
87	ESAI_TX_CLK rising edge to data out high impedance [67]	— —	— —	— —	21.0 16.0	x ck i ck	ns
89	ESAI_TX_FS input (bl, wr) setup time before ESAI_TX_CLK falling edge[5]	— —	— —	2.0 18.0	— —	x ck i ck	ns
90	ESAI_TX_FS input (wl) setup time before ESAI_TX_CLK falling edge	— —	— —	2.0 18.0	— —	x ck i ck	ns
91	ESAI_TX_FS input hold time after ESAI_TX_CLK falling edge	— —	— —	4.0 5.0	— —	x ck i ck	ns
95	ESAI_RX_HF_CLK/ESAI_TX_HF_CLK clock cycle	—	$2 \times T_C$	15	—	—	ns
96	ESAI_TX_HF_CLK input rising edge to ESAI_TX_CLK output	—	—	—	18.0	—	ns
97	ESAI_RX_HF_CLK input rising edge to ESAI_RX_CLK output	—	—	—	18.0	—	ns

1 i ck = internal clock
x ck = external clock
i ck a = internal clock, asynchronous mode
(asynchronous implies that ESAI_TX_CLK and ESAI_RX_CLK are two different clocks)
i ck s = internal clock, synchronous mode
(synchronous implies that ESAI_TX_CLK and ESAI_RX_CLK are the same clock)

2 bl = bit length
wl = word length
wr = word length relative

3 ESAI_TX_CLK(ESAI_TX_CLK pin) = transmit clock
ESAI_RX_CLK(ESAI_RX_CLK pin) = receive clock
ESAI_TX_FS(ESAI_TX_FS pin) = transmit frame sync
ESAI_RX_FS(ESAI_RX_FS pin) = receive frame sync
ESAI_TX_HF_CLK(ESAI_TX_HF_CLK pin) = transmit high frequency clock
ESAI_RX_HF_CLK(ESAI_RX_HF_CLK pin) = receive high frequency clock

4 For the internal clock, the external clock cycle is defined by Icyc and the ESAI control register.

5 The word-relative frame sync signal waveform relative to the clock operates in the same manner as the bit-length frame sync signal waveform, but it spreads from one serial clock before the first bit clock (like the bit length frame sync signal), until the second-to-last bit clock of the first word in the frame.

6 Periodically sampled and not 100% tested.

2 The MSB bits are duplicated on LSB bits implementing color extension.

3 The two MSB bits are duplicated on LSB bits implementing color extension.

4 YCbCr, 8 bits—Supported within the BT.656 protocol (sync embedded within the data stream).

5 RGB, 16 bits—Supported in two ways: (1) As a “generic data” input—with no on-the-fly processing; (2) With on-the-fly processing, but only under some restrictions on the control protocol.

6 YCbCr, 16 bits—Supported as a “generic-data” input—with no on-the-fly processing.

7 YCbCr, 16 bits—Supported as a sub-case of the YCbCr, 20 bits, under the same conditions (BT.1120 protocol).

8 YCbCr, 20 bits—Supported only within the BT.1120 protocol (syncs embedded within the data stream).

4.11.10.2 Sensor Interface Timings

There are three camera timing modes supported by the IPU.

4.11.10.2.1 BT.656 and BT.1120 Video Mode

Smart camera sensors, which include imaging processing, usually support video mode transfer. They use an embedded timing syntax to replace the IPU2_CSIx_VSYNC and IPU2_CSIx_HSYNC signals. The timing syntax is defined by the BT.656/BT.1120 standards.

This operation mode follows the recommendations of ITU BT.656/ ITU BT.1120 specifications. The only control signal used is IPU2_CSIx_PIX_CLK. Start-of-frame and active-line signals are embedded in the data stream. An active line starts with a SAV code and ends with a EAV code. In some cases, digital blanking is inserted in between EAV and SAV code. The CSI decodes and filters out the timing-coding from the data stream, thus recovering IPU2_CSIx_VSYNC and IPU2_CSIx_HSYNC signals for internal use. On BT.656 one component per cycle is received over the IPU2_CSIx_DATA_EN bus. On BT.1120 two components per cycle are received over the IPU2_CSIx_DATA_EN bus.

4.11.10.2.2 Gated Clock Mode

The IPU2_CSIx_VSYNC, IPU2_CSIx_HSYNC, and IPU2_CSIx_PIX_CLK signals are used in this mode. See Figure 65.

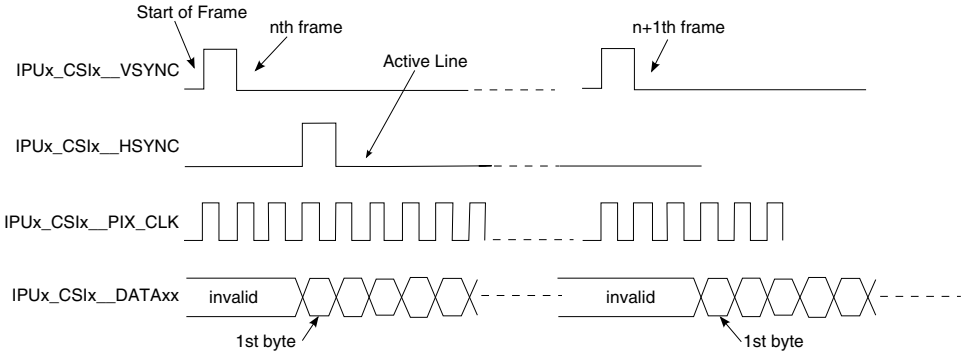


Figure 65. Gated Clock Mode Timing Diagram

A frame starts with a rising edge on IPU2_CSIx_VSYNC (all the timings correspond to straight polarity of the corresponding signals). Then IPU2_CSIx_HSYNC goes to high and hold for the entire line. Pixel clock is valid as long as IPU2_CSIx_HSYNC is high. Data is latched at the rising edge of the valid pixel clocks. IPU2_CSIx_HSYNC goes to low at the end of line. Pixel clocks then become invalid and the CSI

There are special physical outputs to provide synchronous controls:

- The ipp_disp_clk is a dedicated base synchronous signal that is used to generate a base display (component, pixel) clock for a display.
- The ipp_pin_1– ipp_pin_7 are general purpose synchronous pins, that can be used to provide HSYNC, VSYNC, DRDY or any else independent signal to a display.

The IPU has a system of internal binding counters for internal events (such as, HSYNC/VSYNC) calculation. The internal event (local start point) is synchronized with internal DI_CLK. A suitable control starts from the local start point with predefined UP and DOWN values to calculate control's changing points with half DI_CLK resolution. A full description of the counter system can be found in the IPU chapter of the i.MX 6DualPlus/6QuadPlus reference manual (IMX6DQPRM).

4.11.10.5.2 Asynchronous Controls

The asynchronous control is a data-oriented signal that changes its value with an output data according to additional internal flags coming with the data.

There are special physical outputs to provide asynchronous controls, as follows:

- The ipp_d0_cs and ipp_d1_cs pins are dedicated to provide chip select signals to two displays.
- The ipp_pin_11– ipp_pin_17 are general purpose asynchronous pins, that can be used to provide WR. RD, RS or any other data-oriented signal to display.

NOTE

The IPU has independent signal generators for asynchronous signals toggling. When a DI decides to put a new asynchronous data on the bus, a new internal start (local start point) is generated. The signal generators calculate predefined UP and DOWN values to change pins states with half DI_CLK resolution.

4.11.10.6 Synchronous Interfaces to Standard Active Matrix TFT LCD Panels

4.11.10.6.1 IPU Display Operating Signals

The IPU uses four control signals and data to operate a standard synchronous interface:

- IPP_DISP_CLK—Clock to display
- HSYNC—Horizontal synchronization
- VSYNC—Vertical synchronization
- DRDY—Active data

All synchronous display controls are generated on the base of an internally generated "local start point". The synchronous display controls can be placed on time axis with DI's offset, up and down parameters. The display access can be whole number of DI clock (Tdiclk) only. The IPP_DATA can not be moved relative to the local start point. The data bus of the synchronous interface is output direction only.

4.11.13.3 Receiver Real-Time Data Flow

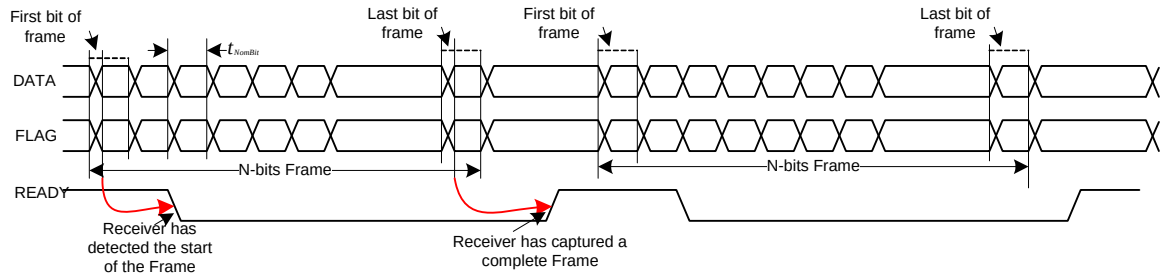


Figure 81. Receiver Real-Time Data Flow READY Signal Timing

4.11.13.4 Synchronized Data Flow Transmission with Wake

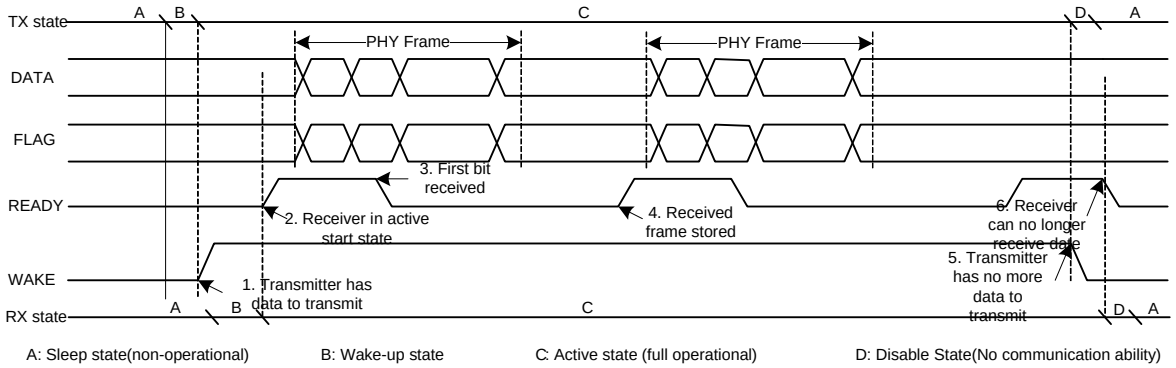


Figure 82. Synchronized Data Flow Transmission with WAKE

4.11.13.5 Stream Transmission Mode Frame Transfer

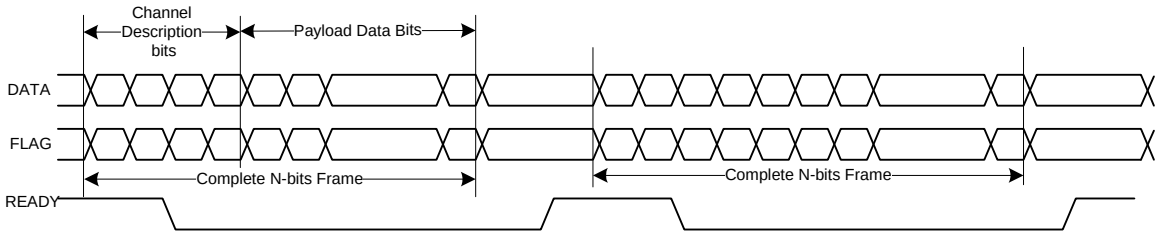


Figure 83. Stream Transmission Mode Frame Transfer (Synchronized Data Flow)

Table 79. MLB 6-Pin Interface Timing Parameters

Parameter	Symbol	Min	Max	Unit	Comment
Cycle-to-cycle system jitter	t_{jitter}	—	600	ps	—
Transmitter MLB_SIG_P/_N (MLB_DATA_P/_N) output valid from transition of MLB_CLK_P/_N (low-to-high)[1]	t_{delay}	0.6	1.3	ns	—
Disable turnaround time from transition of MLB_CLK_P/_N (low-to-high)	t_{phz}	0.6	3.5	ns	—
Enable turnaround time from transition of MLB_CLK_P/_N (low-to-high)	t_{plz}	0.6	5.6	ns	—
MLB_SIG_P/_N (MLB_DATA_P/_N) valid to transition of MLB_CLK_P/_N (low-to-high)	t_{su}	0.05	—	ns	—
MLB_SIG_P/_N (MLB_DATA_P/_N) hold from transition of MLB_CLK_P/_N (low-to-high)[2]	t_{hd}	0.6	—	ns	—

1 t_{delay}, t_{phz}, t_{plz}, t_{su}, and t_{hd} may also be referenced from a low-to-high transition of the recovered clock for 2:1 and 4:1 recovered-to-external clock ratios.

2 The transmitting device must ensure valid data on MLB_SIG_P/_N (MLB_DATA_P/_N) for at least $t_{hd(min)}$ following the rising edge of MLBCP/N; receivers must latch MLB_SIG_P/_N (MLB_DATA_P/_N) data within $t_{hd(min)}$ of the rising edge of MLB_CLK_P/_N.

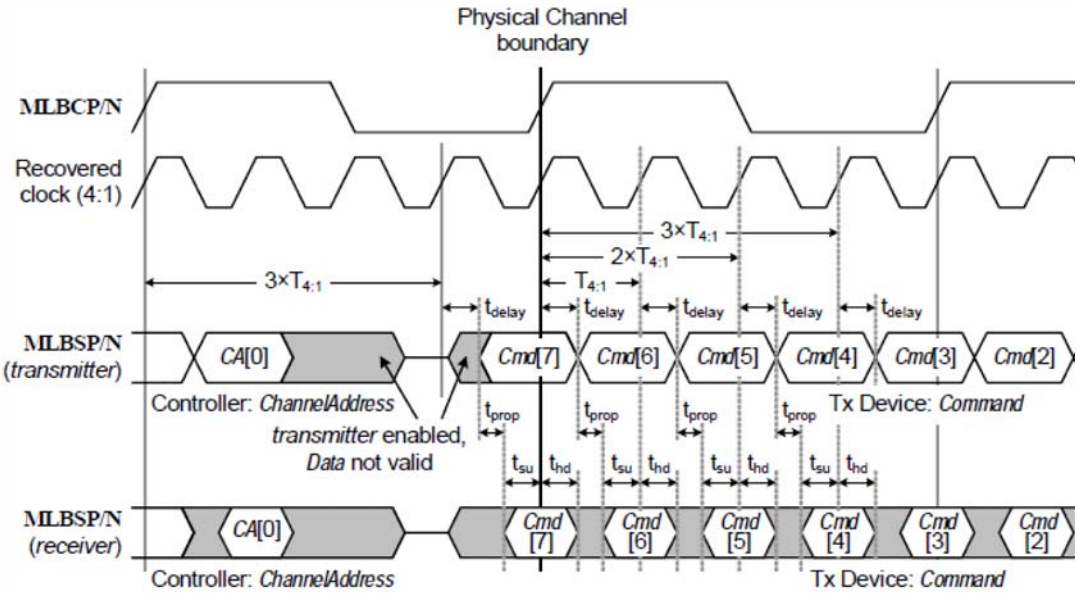


Figure 88. MLB 6-Pin Delay, Setup, and Hold Times

4.11.15 PCIe PHY Parameters

The PCIe interface complies with PCIe specification Gen2 x1 lane and supports the PCI Express 1.1/2.0 standard.

4.11.20.2 SSI Receiver Timing with Internal Clock

Figure 97 depicts the SSI receiver internal clock timing and Table 87 lists the timing parameters for the receiver timing with the internal clock.

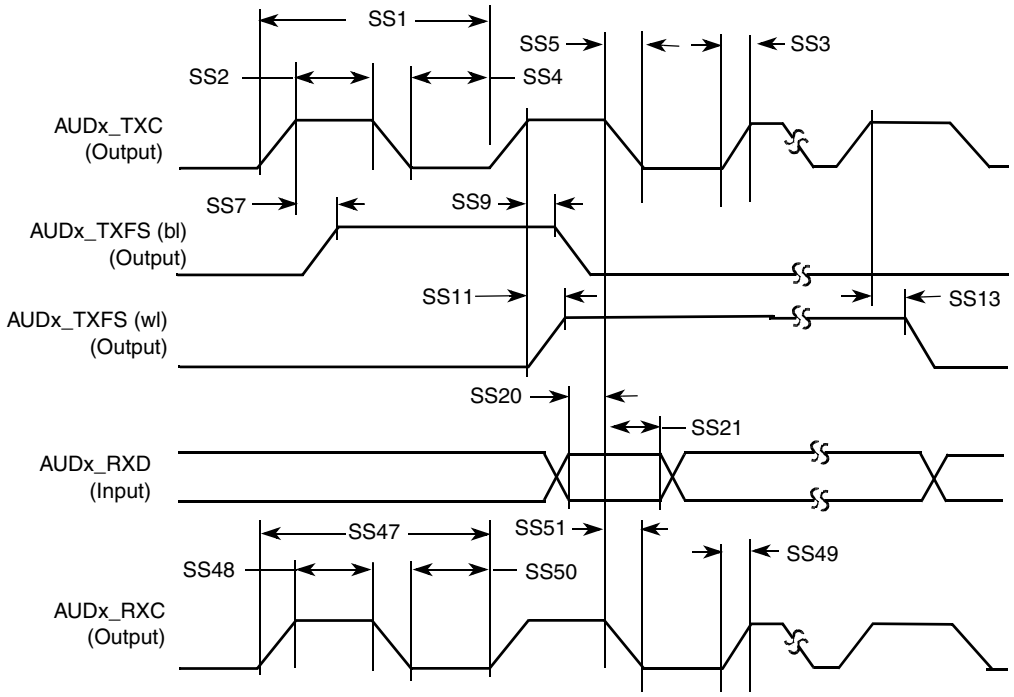


Figure 97. SSI Receiver Internal Clock Timing Diagram

Table 87. SSI Receiver Timing with Internal Clock

ID	Parameter	Min	Max	Unit
Internal Clock Operation				
SS1	AUDx_TXC/AUDx_RXC clock period	81.4	—	ns
SS2	AUDx_TXC/AUDx_RXC clock high period	36.0	—	ns
SS3	AUDx_TXC/AUDx_RXC clock rise time	—	6.0	ns
SS4	AUDx_TXC/AUDx_RXC clock low period	36.0	—	ns
SS5	AUDx_TXC/AUDx_RXC clock fall time	—	6.0	ns
SS7	AUDx_RXC high to AUDx_TXFS (bl) high	—	15.0	ns
SS9	AUDx_RXC high to AUDx_TXFS (bl) low	—	15.0	ns
SS11	AUDx_RXC high to AUDx_TXFS (wl) high	—	15.0	ns
SS13	AUDx_RXC high to AUDx_TXFS (wl) low	—	15.0	ns
SS20	AUDx_RXD setup time before AUDx_RXC low	10.0	—	ns
SS21	AUDx_RXD hold time after AUDx_RXC low	0.0	—	ns

Table 87. SSI Receiver Timing with Internal Clock (continued)

ID	Parameter	Min	Max	Unit
Oversampling Clock Operation				
SS47	Oversampling clock period	15.04	—	ns
SS48	Oversampling clock high period	6.0	—	ns
SS49	Oversampling clock rise time	—	3.0	ns
SS50	Oversampling clock low period	6.0	—	ns
SS51	Oversampling clock fall time	—	3.0	ns

NOTE

- All the timings for the SSI are given for a non-inverted serial clock polarity (TSCKP/RSCKP = 0) and a non-inverted frame sync (TFSI/RFSI = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal AUDx_TXC/AUDx_RXC and/or the frame sync AUDx_TXFS/AUDx_RXFS shown in the tables and in the figures.
- All timings are on Audiomux Pads when SSI is being used for data transfer.
- AUDx_TXC and AUDx_RXC refer to the Transmit and Receive sections of the SSI.
- The terms, WL and BL, refer to Word Length (WL) and Bit Length(BL).
- For internal Frame Sync operation using external clock, the frame sync timing is same as that of transmit data (for example, during AC97 mode of operation).

Table 89. SSI Receiver Timing with External Clock

ID	Parameter	Min	Max	Unit
External Clock Operation				
SS22	AUDx_TXC/AUDx_RXC clock period	81.4	—	ns
SS23	AUDx_TXC/AUDx_RXC clock high period	36	—	ns
SS24	AUDx_TXC/AUDx_RXC clock rise time	—	6.0	ns
SS25	AUDx_TXC/AUDx_RXC clock low period	36	—	ns
SS26	AUDx_TXC/AUDx_RXC clock fall time	—	6.0	ns
SS28	AUDx_RXC high to AUDx_TXFS (bl) high	–10	15.0	ns
SS30	AUDx_RXC high to AUDx_TXFS (bl) low	10	—	ns
SS32	AUDx_RXC high to AUDx_TXFS (wl) high	–10	15.0	ns
SS34	AUDx_RXC high to AUDx_TXFS (wl) low	10	—	ns
SS35	AUDx_TXC/AUDx_RXC External AUDx_TXFS rise time	—	6.0	ns
SS36	AUDx_TXC/AUDx_RXC External AUDx_TXFS fall time	—	6.0	ns
SS40	AUDx_RXD setup time before AUDx_RXC low	10	—	ns
SS41	AUDx_RXD hold time after AUDx_RXC low	2	—	ns

NOTE

- All the timings for the SSI are given for a non-inverted serial clock polarity (TSCKP/RSCKP = 0) and a non-inverted frame sync (TFSI/RFSI = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal AUDx_TXC/AUDx_RXC and/or the frame sync AUDx_TXFS/AUDx_RXFS shown in the tables and in the figures.
- All timings are on Audiomux Pads when SSI is being used for data transfer.
- AUDx_TXC and AUDx_RXC refer to the Transmit and Receive sections of the SSI.
- The terms, WL and BL, refer to Word Length (WL) and Bit Length(BL).
- For internal Frame Sync operation using external clock, the frame sync timing is same as that of transmit data (for example, during AC97 mode of operation).

4.11.23 USB PHY Parameters

This section describes the USB-OTG PHY and the USB Host port PHY parameters.

The USB PHY meets the electrical compliance requirements defined in the Universal Serial Bus Revision 2.0 OTG, USB Host with the amendments below (On-The-Go and Embedded Host Supplement to the USB Revision 2.0 Specification is not applicable to Host port).

- USB ENGINEERING CHANGE NOTICE
  - Title: 5V Short Circuit Withstand Requirement Change
  - Applies to: Universal Serial Bus Specification, Revision 2.0
- Errata for USB Revision 2.0 April 27, 2000 as of 12/7/2000
- USB ENGINEERING CHANGE NOTICE
  - Title: Pull-up/Pull-down resistors
  - Applies to: Universal Serial Bus Specification, Revision 2.0
- USB ENGINEERING CHANGE NOTICE
  - Title: Suspend Current Limit Changes
  - Applies to: Universal Serial Bus Specification, Revision 2.0
- USB ENGINEERING CHANGE NOTICE
  - Title: USB 2.0 Phase Locked SOFs
  - Applies to: Universal Serial Bus Specification, Revision 2.0
- On-The-Go and Embedded Host Supplement to the USB Revision 2.0 Specification
  - Revision 2.0 plus errata and ecn June 4, 2010
- Battery Charging Specification (available from USB-IF)
  - Revision 1.2, December 7, 2010
  - Portable device only

Table 97. Fuses and Associated Pins Used for Boot (continued)

Pin	Direction at Reset	eFuse Name
EIM_A19	Input	BOOT_CFG3[3]
EIM_A20	Input	BOOT_CFG3[4]
EIM_A21	Input	BOOT_CFG3[5]
EIM_A22	Input	BOOT_CFG3[6]
EIM_A23	Input	BOOT_CFG3[7]
EIM_A24	Input	BOOT_CFG4[0]
EIM_WAIT	Input	BOOT_CFG4[1]
EIM_LBA	Input	BOOT_CFG4[2]
EIM_EB0	Input	BOOT_CFG4[3]
EIM_EB1	Input	BOOT_CFG4[4]
EIM_RW	Input	BOOT_CFG4[5]
EIM_EB2	Input	BOOT_CFG4[6]
EIM_EB3	Input	BOOT_CFG4[7]

[1] Pin value overrides fuse settings for BT_FUSE_SEL = '0'. Signal Configuration as Fuse Override Input at Power Up. These are special I/O lines that control the boot up configuration during product development. In production, the boot configuration can be controlled by fuses.

5.2 Boot Devices Interfaces Allocation

Table 98 lists the interfaces that can be used by the boot process in accordance with the specific boot mode configuration. The table also describes the interface's specific modes and IOMUXC allocation, which are configured during boot when appropriate.

Table 98. Interfaces Allocation During Boot

Interface	IP Instance	Allocated Pads During Boot	Comment
SPI	ECSPI-1	EIM_D17, EIM_D18, EIM_D16, EIM_EB2, EIM_D19, EIM_D24, EIM_D25	—
SPI	ECSPI-2	CSI0_DAT10, CSI0_DAT9, CSI0_DAT8, CSI0_DAT11, EIM_LBA, EIM_D24, EIM_D25	—
SPI	ECSPI-3	DISP0_DAT2, DISP0_DAT1, DISP0_DAT0, DISP0_DAT3, DISP0_DAT4, DISP0_DAT5, DISP0_DAT6	—
SPI	ECSPI-4	EIM_D22, EIM_D28, EIM_D21, EIM_D20, EIM_A25, EIM_D24, EIM_D25	—
SPI	ECSPI-5	SD1_DAT0, SD1_CMD, SD1_CLK, SD1_DAT1, SD1_DAT2, SD1_DAT3, SD2_DAT3	—
EIM	EIM	EIM_DA[15:0], EIM_D[31:16], CSI0_DAT[19:4], CSI0_DATA_EN, CSI0_VSYNC	Used for NOR, OneNAND boot Only CS0 is supported

NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM A.
4. DATUM A, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.
6. 21.2MM MAXIMUM PACKAGE ASSEMBLY (LID + LAMINATE) X AND Y.

	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: 624 I/O FC PBGA, 21 X 21 X 2 PKG, 0.8 MM PITCH, STAMPED LID	DOCUMENT NO: 98ASA00330D	REV: D
	STANDARD: NON–JEDEC	
	08 OCT 2013	

Figure 107. 21 x 21 mm Lidded Package Top, Bottom, and Side Views (Sheet 2 of 2)

Table 100. 21 x 21 mm Functional Contact Assignments (continued)

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition[1]			
				Default Mode (Reset Mode)	Default Function (Signal Name)	Input/Output	Value[2]
EIM_A19	G25	NVCC_EIM1	GPIO	ALT0	EIM_ADDR19	Output	0
EIM_A20	H22	NVCC_EIM1	GPIO	ALT0	EIM_ADDR20	Output	0
EIM_A21	H23	NVCC_EIM1	GPIO	ALT0	EIM_ADDR21	Output	0
EIM_A22	F24	NVCC_EIM1	GPIO	ALT0	EIM_ADDR22	Output	0
EIM_A23	J21	NVCC_EIM1	GPIO	ALT0	EIM_ADDR23	Output	0
EIM_A24	F25	NVCC_EIM1	GPIO	ALT0	EIM_ADDR24	Output	0
EIM_A25	H19	NVCC_EIM0	GPIO	ALT0	EIM_ADDR25	Output	0
EIM_BCLK	N22	NVCC_EIM2	GPIO	ALT0	EIM_BCLK	Output	0
EIM_CS0	H24	NVCC_EIM1	GPIO	ALT0	EIM_CS0_B	Output	1
EIM_CS1	J23	NVCC_EIM1	GPIO	ALT0	EIM_CS1_B	Output	1
EIM_D16	C25	NVCC_EIM0	GPIO	ALT5	GPIO3_IO16	Input	PU (100K)
EIM_D17	F21	NVCC_EIM0	GPIO	ALT5	GPIO3_IO17	Input	PU (100K)
EIM_D18	D24	NVCC_EIM0	GPIO	ALT5	GPIO3_IO18	Input	PU (100K)
EIM_D19	G21	NVCC_EIM0	GPIO	ALT5	GPIO3_IO19	Input	PU (100K)
EIM_D20	G20	NVCC_EIM0	GPIO	ALT5	GPIO3_IO20	Input	PU (100K)
EIM_D21	H20	NVCC_EIM0	GPIO	ALT5	GPIO3_IO21	Input	PU (100K)
EIM_D22	E23	NVCC_EIM0	GPIO	ALT5	GPIO3_IO22	Input	PD (100K)
EIM_D23	D25	NVCC_EIM0	GPIO	ALT5	GPIO3_IO23	Input	PU (100K)
EIM_D24	F22	NVCC_EIM0	GPIO	ALT5	GPIO3_IO24	Input	PU (100K)
EIM_D25	G22	NVCC_EIM0	GPIO	ALT5	GPIO3_IO25	Input	PU (100K)
EIM_D26	E24	NVCC_EIM0	GPIO	ALT5	GPIO3_IO26	Input	PU (100K)
EIM_D27	E25	NVCC_EIM0	GPIO	ALT5	GPIO3_IO27	Input	PU (100K)
EIM_D28	G23	NVCC_EIM0	GPIO	ALT5	GPIO3_IO28	Input	PU (100K)
EIM_D29	J19	NVCC_EIM0	GPIO	ALT5	GPIO3_IO29	Input	PU (100K)
EIM_D30	J20	NVCC_EIM0	GPIO	ALT5	GPIO3_IO30	Input	PU (100K)
EIM_D31	H21	NVCC_EIM0	GPIO	ALT5	GPIO3_IO31	Input	PD (100K)
EIM_DA0	L20	NVCC_EIM2	GPIO	ALT0	EIM_AD00	Input	PU (100K)
EIM_DA1	J25	NVCC_EIM2	GPIO	ALT0	EIM_AD01	Input	PU (100K)
EIM_DA2	L21	NVCC_EIM2	GPIO	ALT0	EIM_AD02	Input	PU (100K)
EIM_DA3	K24	NVCC_EIM2	GPIO	ALT0	EIM_AD03	Input	PU (100K)
EIM_DA4	L22	NVCC_EIM2	GPIO	ALT0	EIM_AD04	Input	PU (100K)
EIM_DA5	L23	NVCC_EIM2	GPIO	ALT0	EIM_AD05	Input	PU (100K)
EIM_DA6	K25	NVCC_EIM2	GPIO	ALT0	EIM_AD06	Input	PU (100K)
EIM_DA7	L25	NVCC_EIM2	GPIO	ALT0	EIM_AD07	Input	PU (100K)
EIM_DA8	L24	NVCC_EIM2	GPIO	ALT0	EIM_AD08	Input	PU (100K)
EIM_DA9	M21	NVCC_EIM2	GPIO	ALT0	EIM_AD09	Input	PU (100K)

Table 100. 21 x 21 mm Functional Contact Assignments (continued)

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition[1]			
				Default Mode (Reset Mode)	Default Function (Signal Name)	Input/Output	Value[2]
SD3_CLK	D14	NVCC_SD3	GPIO	ALT5	GPIO7_IO03	Input	PU (100K)
SD3_CMD	B13	NVCC_SD3	GPIO	ALT5	GPIO7_IO02	Input	PU (100K)
SD3_DAT0	E14	NVCC_SD3	GPIO	ALT5	GPIO7_IO04	Input	PU (100K)
SD3_DAT1	F14	NVCC_SD3	GPIO	ALT5	GPIO7_IO05	Input	PU (100K)
SD3_DAT2	A15	NVCC_SD3	GPIO	ALT5	GPIO7_IO06	Input	PU (100K)
SD3_DAT3	B15	NVCC_SD3	GPIO	ALT5	GPIO7_IO07	Input	PU (100K)
SD3_DAT4	D13	NVCC_SD3	GPIO	ALT5	GPIO7_IO01	Input	PU (100K)
SD3_DAT5	C13	NVCC_SD3	GPIO	ALT5	GPIO7_IO00	Input	PU (100K)
SD3_DAT6	E13	NVCC_SD3	GPIO	ALT5	GPIO6_IO18	Input	PU (100K)
SD3_DAT7	F13	NVCC_SD3	GPIO	ALT5	GPIO6_IO17	Input	PU (100K)
SD3_RST	D15	NVCC_SD3	GPIO	ALT5	GPIO7_IO08	Input	PU (100K)
SD4_CLK	E16	NVCC_NANDF	GPIO	ALT5	GPIO7_IO10	Input	PU (100K)
SD4_CMD	B17	NVCC_NANDF	GPIO	ALT5	GPIO7_IO09	Input	PU (100K)
SD4_DAT0	D18	NVCC_NANDF	GPIO	ALT5	GPIO2_IO08	Input	PU (100K)
SD4_DAT1	B19	NVCC_NANDF	GPIO	ALT5	GPIO2_IO09	Input	PU (100K)
SD4_DAT2	F17	NVCC_NANDF	GPIO	ALT5	GPIO2_IO10	Input	PU (100K)
SD4_DAT3	A20	NVCC_NANDF	GPIO	ALT5	GPIO2_IO11	Input	PU (100K)
SD4_DAT4	E18	NVCC_NANDF	GPIO	ALT5	GPIO2_IO12	Input	PU (100K)
SD4_DAT5	C19	NVCC_NANDF	GPIO	ALT5	GPIO2_IO13	Input	PU (100K)
SD4_DAT6	B20	NVCC_NANDF	GPIO	ALT5	GPIO2_IO14	Input	PU (100K)
SD4_DAT7	D19	NVCC_NANDF	GPIO	ALT5	GPIO2_IO15	Input	PU (100K)
TAMPER	E11	VDD_SNVS_IN	GPIO	ALT0	SNVS_TAMPER	Input	PD (100K)
TEST_MODE	E12	VDD_SNVS_IN	—	—	TCU_TEST_MODE	Input	PD (100K)
USB_H1_DN	F10	VDD_USB_CAP	—	—	USB_H1_DN	—	—
USB_H1_DP	E10	VDD_USB_CAP	—	—	USB_H1_DP	—	—
USB_OTG_CHD_B	B8	VDD_USB_CAP	—	—	USB_OTG_CHD_B	—	—
USB_OTG_DN	B6	VDD_USB_CAP	—	—	USB_OTG_DN	—	—
USB_OTG_DP	A6	VDD_USB_CAP	—	—	USB_OTG_DP	—	—
XTALI	A7	NVCC_PLL	—	—	XTALI	—	—
XTALO	B7	NVCC_PLL	—	—	XTALO	—	—

1 The state immediately after reset and before ROM firmware or software has executed.

2 Variance of the pull-up and pull-down strengths are shown in the tables as follows:

- Table 22, "GPIO I/O DC Parameters," on page 39.
- Table 23, "LPDDR2 I/O DC Electrical Parameters," on page 40.
- Table 24, "DDR3/DDR3L I/O DC Electrical Parameters," on page 41.

Table 102. 21 x 21 mm, 0.8 mm Pitch Ball Map (continued)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25
AC	DRAM_D4	DRAM_VREF	DRAM_DQM0	DRAM_D2	DRAM_D13	DRAM_DQM1	DRAM_D15	DRAM_D22	DRAM_D28	DRAM_SDQS3	DRAM_D31	DRAM_A11	DRAM_A6	DRAM_A0	DRAM_SDBA0	DRAM_SDODT0	DRAM_A13	DRAM_D34	DRAM_D39	DRAM_DQM5	DRAM_D47	DRAM_D48	DRAM_D53	DRAM_D51	DRAM_D55
AD	DRAM_D5	DRAM_D0	DRAM_SDQS0_B	GND	DRAM_D8	DRAM_SDQS1	GND	DRAM_SDQS2	DRAM_D29	GND	DRAM_D30	DRAM_A12	GND	DRAM_SDCLK_1	DRAM_SDCLK_0	GND	DRAM_CS1	DRAM_SDQS4	GND	DRAM_SDQS5	DRAM_D43	GND	DRAM_SDQS6	DRAM_DQM6	DRAM_D54
AE	GND	DRAM_D1	DRAM_SDQS0	DRAM_D7	DRAM_D9	DRAM_SDQS1_B	DRAM_D11	DRAM_SDQS2_B	DRAM_D24	DRAM_DQM3	DRAM_D26	DRAM_A9	DRAM_A5	DRAM_SDCLK_1_B	DRAM_SDCLK_0_B	DRAM_CAS	ZQPAD	DRAM_SDQS4_B	DRAM_D35	DRAM_SDQS5_B	DRAM_D46	DRAM_D49	DRAM_SDQS6_B	DRAM_D50	GND