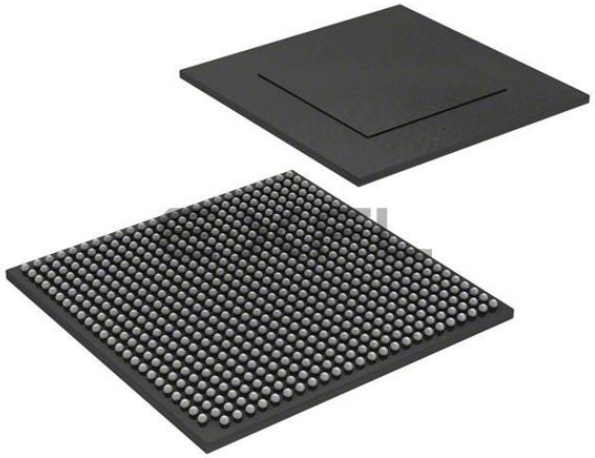


Welcome to E-XFL.COM

Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM® Cortex®-A9
Number of Cores/Bus Width	2 Core, 32-Bit
Speed	1.0GHz
Co-Processors/DSP	Multimedia; NEON™ SIMD
RAM Controllers	LPDDR2, DDR3L, DDR3
Graphics Acceleration	Yes
Display & Interface Controllers	HDMI, Keypad, LCD, LVDS, MIPI/DSI, Parallel
Ethernet	10/100/1000Mbps (1)
SATA	SATA 3Gbps (1)
USB	USB 2.0 + PHY (3), USB 2.0 OTG + PHY (1)
Voltage - I/O	1.8V, 2.5V, 2.8V, 3.3V
Operating Temperature	-20°C ~ 105°C (TJ)
Security Features	ARM TZ, A-HAB, CAAM, CSU, SJC, SNVS
Package / Case	624-LFBGA, FCBGA
Supplier Device Package	624-FCPBGA (21x21)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcimx6dp5eym1aa

Table 2. i.MX 6DualPlus/6QuadPlus Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
PRE1 PRE2 PRE3 PRE4	Prefetch/Resolve Engine	Multimedia Peripherals	The PRE includes the Resolve engine, Prefetch engine, and Store engine 3 blocks.The PRE key features are: **The Resolve engine supports:** • GPU 32bpp 4x4 standard tile, 4x4 split tile, 4x4 super tile, 4x4 super split tile format. • GPU 16bpp 8x4 standard tile, 8x4 split tile, 8x4 super tile, 8x4 super split format. • 32/16x4 block mode and scan mode. **The prefetch engine supports:** • Transfer of non-interleaved YUV422(NI422), non-interleaved YUV420(NI420), partial interleaved YUV422(PI422), and partial interleaved YUV420(PI420), inputs to interleaved YUV422. • Vertical flip function both in block mode and scan mode. In block mode, vertical flip function should complete with TPR module enable. • 8bpp, 16bpp, 32bpp and 64bpp data format as generic data. • Transfer of non-interleaved YUV444(NI444), input to interleaved YUV444 output. **The store Engine supports:** 4/8/16 lines handshake modes with PRG.
PRG1 PRG2	Prefetch/Resolve Gasket	Multimedia Peripherals	The PRG is a digital core function which works as a gasket interface between the fabric and the IPU system. The primary function is to re-map the ARADDR from a frame-based address to a band-based address depending on the different ARIDs. The PRG also implements the handshake logic with the Prefetch Resolve Engine (PRE).
PMU	Power-Management Functions	Data Path	Integrated power management unit. Used to provide power to various SoC domains.
PWM-1 PWM-2 PWM-3 PWM-4	Pulse Width Modulation	Connectivity Peripherals	The pulse-width modulator (PWM) has a 16-bit counter and is optimized to generate sound from stored sample audio images and it can also generate tones. It uses 16-bit resolution and a 4x16 data FIFO to generate sound.
RAM 16 KB	Secure/non-secure RAM	Secured Internal Memory	Secure/non-secure Internal RAM, interfaced through the CAAM.
RAM 512 KB	Internal RAM	Internal Memory	Internal RAM, which is accessed through OCRAM memory controllers.
ROM 96 KB	Boot ROM	Internal Memory	Supports secure and regular Boot Modes. Includes read protection on 4K region for content protection
SATA	Serial ATA	Connectivity Peripherals	The SATA controller and PHY is a complete mixed-signal IP solution designed to implement SATA II, 3.0 Gbps HDD connectivity.

[10] All digital I/O supplies (NVCC_xxxx) must be powered under normal conditions whether the associated I/O pins are in use or not, and associated I/O pins need to have a pull-up or pull-down resistor applied to limit any floating gate current.

[11] This supply also powers the pre-drivers of the DDR I/O pins; therefore, it must always be provided, even when LVDS is not used.

4.1.4 External Clock Sources

Each i.MX 6DualPlus/6QuadPlus processor has two external input system clocks: a low frequency (RTC_XTALI) and a high frequency (XTALI).

The RTC_XTALI is used for low-frequency functions. It supplies the clock for wake-up circuit, power-down real time clock operation, and slow system and watchdog counters. The clock input can be connected to either an external oscillator or a crystal using the internal oscillator amplifier. Additionally, there is an internal ring oscillator, that can be used instead of RTC_XTALI when accuracy is not important.

The system clock input XTALI is used to generate the main system clock. It supplies the PLLs and other peripherals. The system clock input can be connected to either an external oscillator or a crystal using the internal oscillator amplifier.

NOTE

The internal RTC oscillator does not provide an accurate frequency and is affected by process, voltage and temperature variations. Freescale strongly recommends using an external crystal as the RTC_XTALI reference. If the internal oscillator is used instead, careful consideration should be given to the timing implications on all of the SoC modules dependent on this clock.

Table 7 shows the interface frequency requirements.

Table 7. External Input Clock Frequency

Parameter Description	Symbol	Min	Typ	Max	Unit
RTC_XTALI Oscillator[1,2]	f_{ckil}	—	32.768[3]/32.0	—	kHz
XTALI Oscillator[4,2]	f_{xtal}	—	24	—	MHz

[1] External oscillator or a crystal with internal oscillator amplifier.

[2] The required frequency stability of this clock source is application dependent. For recommendations, see the Hardware Development Guide for i.MX 6Dual, 6Quad, 6Solo, 6DualLite Families of Applications Processors (IMX6DQ6SDLHDG).

[3] Recommended nominal frequency 32.768 kHz.

[4] External oscillator or a fundamental frequency crystal with internal oscillator amplifier.

The typical values shown in Table 7 are required for use with Freescale BSPs to ensure precise time keeping and USB operation. For RTC_XTALI operation, two clock sources are available:

- On-chip 40 kHz ring oscillator: This clock source has the following characteristics:
  - Approximately 25 µA more Idd than crystal oscillator
  - Approximately ±50% tolerance
  - No external component required
  - Starts up quicker than 32 kHz crystal oscillator
- External crystal oscillator with on-chip support circuit

4.2 Power Supplies Requirements and Restrictions

The system design must comply with power-up sequence, power-down sequence, and steady state guidelines as described in this section to ensure the reliable operation of the device. Any deviation from these sequences may result in the following situations:

- Excessive current during power-up phase
- Prevention of the device from booting
- Irreversible damage to the processor

4.2.1 Power-Up Sequence

For power-up sequence, the restrictions are as follows:

- VDD_SNVS_IN supply must be turned ON before any other power supply. It may be connected (shorted) with VDD_HIGH_IN supply.
- If a coin cell is used to power VDD_SNVS_IN, then ensure that it is connected before any other supply is switched on.
- If the external SRC_POR_B signal is used to control the processor POR, then SRC_POR_B must be immediately asserted at power-up and remain asserted until the VDD_ARM_CAP, VDD_SOC_CAP, and VDD_PU_CAP supplies are stable. VDD_ARM_IN and VDD_SOC_IN may be applied in either order with no restrictions. In the absence of an external reset feeding the SRC_POR_B input, the internal POR module takes control. See the i.MX 6DualPlus/6QuadPlus reference manual (IMX6DQPRM) for further details and to ensure that all necessary requirements are being met.
- If the external SRC_POR_B signal is not used (always held high or left unconnected), the processor defaults to the internal POR function (where the PMU controls generation of the POR based on the power supplies). If the internal POR function is used, the following power supply requirements must be met:
  - VDD_ARM_IN and VDD_SOC_IN may be supplied from the same source, or
  - VDD_SOC_IN can be supplied before VDD_ARM_IN with a maximum delay of 1 ms.

NOTE

Ensure that there is no back voltage (leakage) from any supply on the board towards the 3.3 V supply (for example, from the external components that use both the 1.8 V and 3.3 V supplies).

NOTE

USB_OTG_VBUS and USB_H1_VBUS are not part of the power supply sequence and can be powered at any time.

4.2.2 Power-Down Sequence

No special restrictions for i.MX 6DualPlus/6QuadPlus SoC.

4.2.3 Power Supplies Usage

- All I/O pins should not be externally driven while the I/O power supply for the pin (NVCC_xxx) is OFF. This can cause internal latch-up and malfunctions due to reverse current flows. For information about I/O power supply of each pin, see “Power Group” column of Table 100, "21 x 21 mm Functional Contact Assignments," on page 149.
- When the SATA interface is not used, the SATA_VP and SATA_VPH supplies should be grounded. The input and output supplies for rest of the ports (SATA_REXT, SATA_PHY_RX_N, SATA_PHY_RX_P, and SATA_PHY_TX_N) can be left floating. It is recommended not to turn OFF the SATA_VPH supply while the SATA_VP supply is ON, as it may lead to excessive power consumption. If boundary scan test is used, SATA_VP and SATA_VPH must remain powered.
- When the PCIE interface is not used, the PCIE_VP, PCIE_VPH, and PCIE_VPTX supplies should be grounded. The input and output supplies for rest of the ports (PCIE_REXT, PCIE_RX_N, PCIE_RX_P, PCIE_TX_N, and PCIE_TX_P) can be left floating. It is recommended not to turn the PCIE_VPH supply OFF while the PCIE_VP supply is ON, as it may lead to excessive power consumption. If boundary scan test is used, PCIE_VP, PCIE_VPH, and PCIE_VPTX must remain powered.

4.3 Integrated LDO Voltage Regulator Parameters

Various internal supplies can be powered ON from internal LDO voltage regulators. All the supply pins named *_CAP must be connected to external capacitors. The onboard LDOs are intended for internal use only and should not be used to power any external circuitry. See the i.MX 6DualPlus/6QuadPlus reference manual (IMX6DQPRM) for details on the power tree scheme recommended operation.

NOTE

The *_CAP signals should not be powered externally. These signals are intended for internal LDO or LDO bypass operation only.

4.3.1 Digital Regulators (LDO_ARM, LDO_PU, LDO_SOC)

There are three digital LDO regulators (“Digital”, because of the logic loads that they drive, not because of their construction). The advantages of the regulators are to reduce the input supply variation because of their input supply ripple rejection and their on die trimming. This translates into more voltage for the die producing higher operating frequencies. These regulators have three basic modes.

- Bypass. The regulation FET is switched fully on passing the external voltage, DCDC_LOW, to the load unaltered. The analog part of the regulator is powered down in this state, removing any loss other than the IR drop through the power grid and FET.
- Power Gate. The regulation FET is switched fully off limiting the current draw from the supply. The analog part of the regulator is powered down here limiting the power consumption.
- Analog regulation mode. The regulation FET is controlled such that the output voltage of the regulator equals the programmed target voltage. The target voltage is fully programmable in 25 mV steps.

4.5 On-Chip Oscillators

4.5.1 OSC24M

This block implements an amplifier that when combined with a suitable quartz crystal and external load capacitors implements an oscillator. The oscillator is powered from NVCC_PLL_OUT.

The system crystal oscillator consists of a Pierce-type structure running off the digital supply. A straight forward biased-inverter implementation is used.

4.5.2 OSC32K

This block implements an amplifier that when combined with a suitable quartz crystal and external load capacitors implements a low power oscillator. It also implements a power mux such that it can be powered from either a ~3 V backup battery (VDD_SNVS_IN) or VDD_HIGH_IN such as the oscillator consumes power from VDD_HIGH_IN when that supply is available and transitions to the back up battery when VDD_HIGH_IN is lost.

In addition, if the clock monitor determines that the OSC32K is not present, then the source of the 32 kHz clock will automatically switch to the internal ring oscillator.

CAUTION

The internal RTC oscillator does not provide an accurate frequency and is affected by process, voltage, and temperature variations. Freescale strongly recommends using an external crystal as the RTC_XTALI reference. If the internal oscillator is used instead, careful consideration must be given to the timing implications on all of the SoC modules dependent on this clock.

The OSC32k runs from VDD_SNVS_CAP, which comes from the VDD_HIGH_IN/VDD_SNVS_IN power mux. The target battery is a ~3 V coin cell. Proper choice of coin cell type is necessary for chosen VDD_HIGH_IN range. Appropriate series resistor (Rs) must be used when connecting the coin cell. Rs depends on the charge current limit that depends on the chosen coin cell. For example, for Panasonic ML621:

- Average Discharge Voltage is 2.5 V
- Maximum Charge Current is 0.6 mA

For a charge voltage of 3.2 V, Rs = (3.2-2.5)/0.6 m = 1.17 k

NOTE

Always refer to the chosen coin cell manufacturer's data sheet for the latest information.

4.8.2 DDR I/O Output Buffer Impedance

The LPDDR2 interface fully complies with JESD209-2B LPDDR2 JEDEC standard release June, 2009. The DDR3 interface fully complies with JESD79-3D DDR3 JEDEC standard release April, 2008.

Table 35 shows DDR I/O output buffer impedance of i.MX 6DualPlus/6QuadPlus processors.

Table 35. DDR I/O Output Buffer Impedance

Parameter	Symbol	Test Conditions	Typical		Unit
			NVCC_DRAM=1.5 V (DDR3) DDR_SEL=11	NVCC_DRAM=1.2 V (LPDDR2) DDR_SEL=10	
Output Driver Impedance	Rdrv	Drive Strength (DSE) =			Ω
		000	Hi-Z	Hi-Z	
		001	240	240	
		010	120	120	
		011	80	80	
		100	60	60	
		101	48	48	
		110	40	40	
		111	34	34	

Note:

1. Output driver impedance is controlled across PVTs using ZQ calibration procedure.
2. Calibration is done against 240 W external reference resistor.
3. Output driver impedance deviation (calibration accuracy) is ±5% (max/min impedance) across PVTs.

4.8.3 LVDS I/O Output Buffer Impedance

The LVDS interface complies with TIA/EIA 644-A standard. See, TIA/EIA STANDARD 644-A, “Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits” for details.

4.8.4 MLB 6-Pin I/O Differential Output Impedance

Table 36 shows MLB 6-pin I/O differential output impedance of i.MX 6DualPlus/6QuadPlus processors.

Table 36. MLB 6-Pin I/O Differential Output Impedance

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Differential Output Impedance	Z_O	—	1.6	—	—	kΩ

4.9.3.2 General EIM Timing-Synchronous Mode

Figure 12, Figure 13, and Table 40 specify the timings related to the EIM module. All EIM output control signals may be asserted and deasserted by an internal clock synchronized to the EIM_BCLK rising edge according to corresponding assertion/negation control fields.

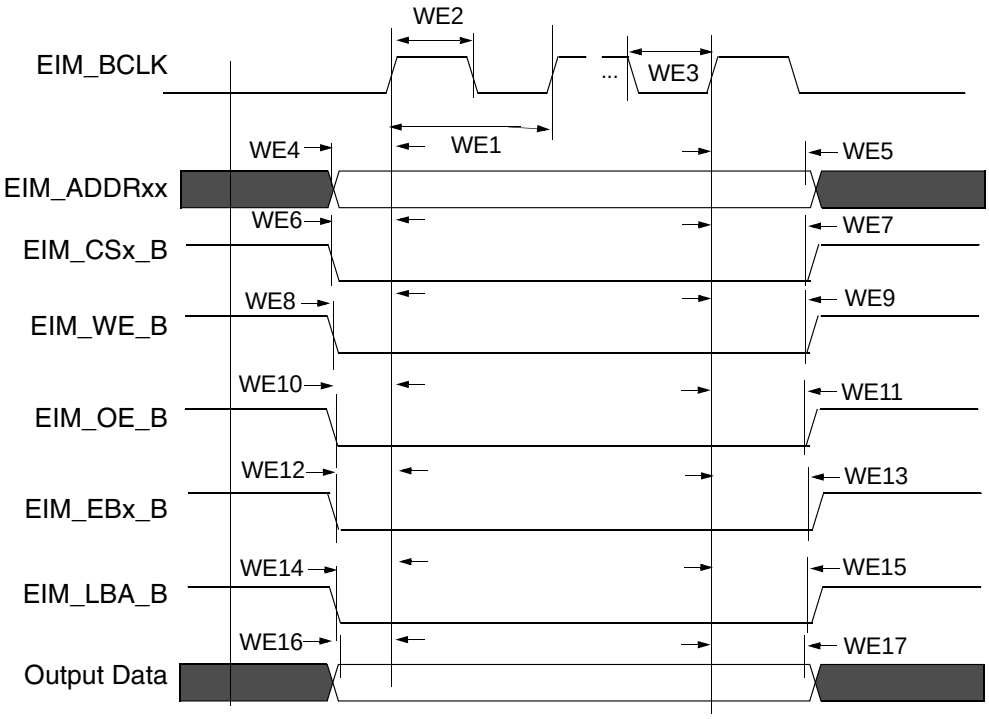


Figure 12. EIM Output Timing Diagram

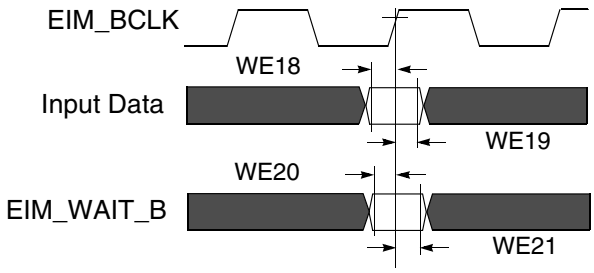


Figure 13. EIM Input Timing Diagram

4.9.3.3 Examples of EIM Synchronous Accesses

Table 40. EIM Bus Timing Parameters

ID	Parameter	Min[1]	Max[1]	Unit
WE1	EIM_BCLK cycle time[2]	t × (k+1)	—	ns
WE2	EIM_BCLK high level width	0.4 × t × (k+1)	—	ns
WE3	EIM_BCLK low level width	0.4 × t × (k+1)	—	ns

Table 45. LPDDR2 Command and Address Timing Parameters

ID	Parameter[1,2]	Symbol	CK = 400 MHz		Unit
			Min	Max	
LP1	DRAM_SDCLKx_P clock high-level width	t_{CH}	0.45	0.55	t_{CK}
LP2	DRAM_SDCLKx_P clock low-level width	t_{CL}	0.45	0.55	t_{CK}
LP3	DRAM_CSx_B, DRAM_ADDRxx setup time	t_{IS}	390	—	ps
LP4	DRAM_CSx_B, DRAM_ADDRxx hold time	t_{IH}	390	—	ps
LP3	DRAM_ADDRxx setup time	t_{IS}	390	—	ps
LP4	DRAM_ADDRxx hold time	t_{IH}	390	—	ps

1 All measurements are in reference to Vref level.

2 Measurements were completed using balanced load and a 25 Ω resistor from outputs to DRAM_VREF.

Figure 28 shows the LPDDR2 write timing diagram. The timing parameters for this diagram appear in Table 46.

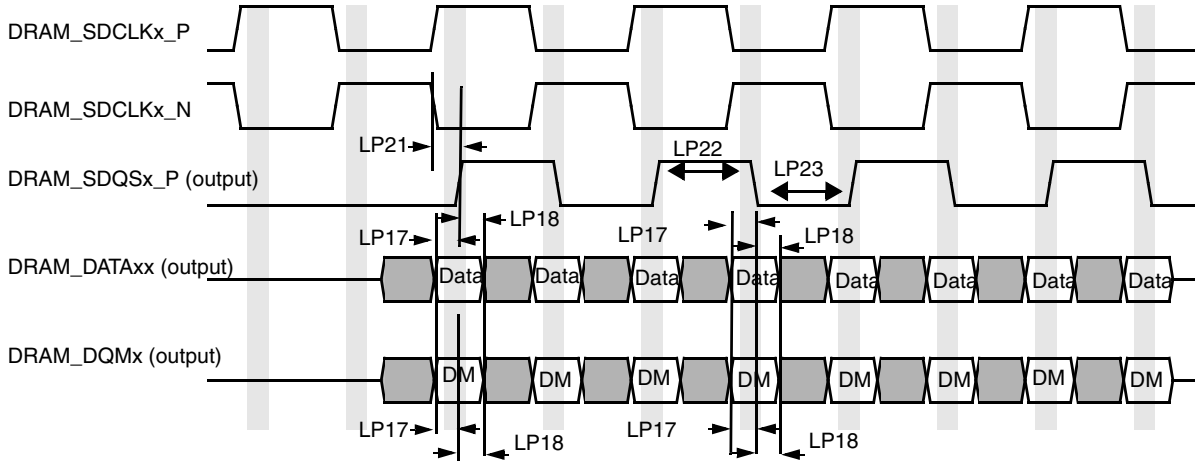


Figure 28. LPDDR2 Write Cycle

Table 46. LPDDR2 Write Cycle

ID	Parameter[1,2,3]	Symbol	CK = 400 MHz		Unit
			Min	Max	
LP17	DRAM_DATAxx and DRAM_DQMx setup time to DRAM_SDQSx_P (differential strobe)	t_{DS}	370	—	ps
LP18	DRAM_DATAxx and DRAM_DQMx hold time to DRAM_SDQSx_P (differential strobe)	t_{DH}	370	—	ps
LP21	DRAM_SDQSx_P latching rising transitions to associated clock edges	t_{DQSS}	0.75	1.25	tCK

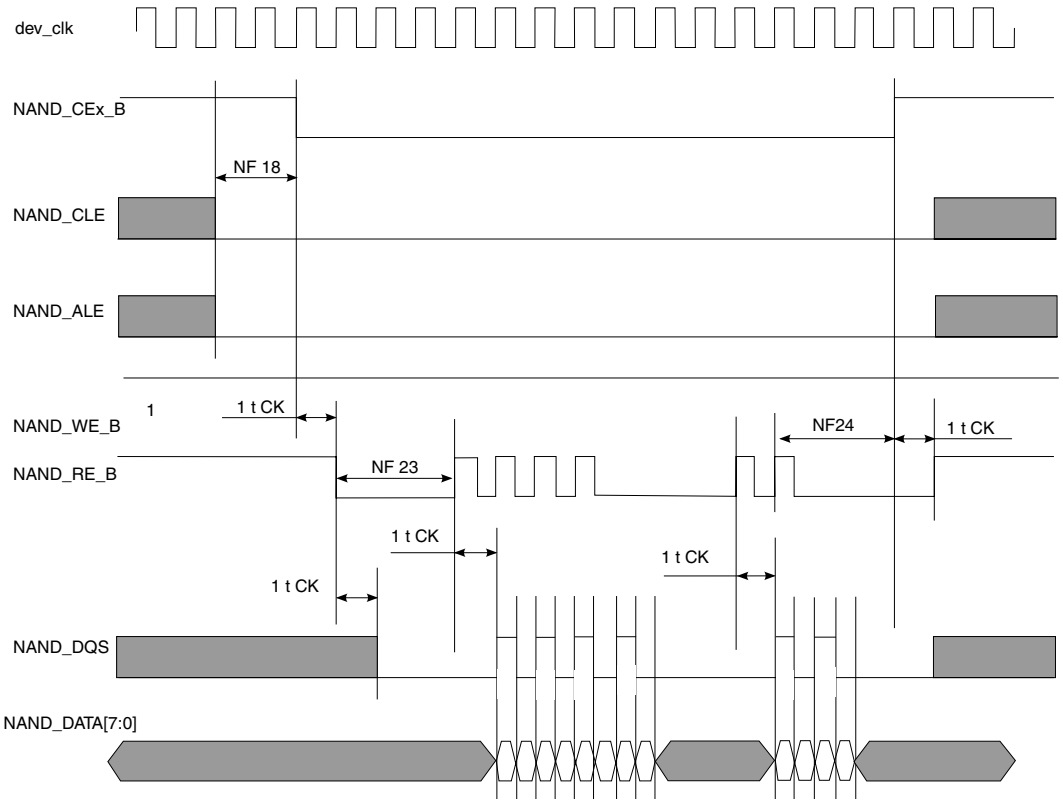


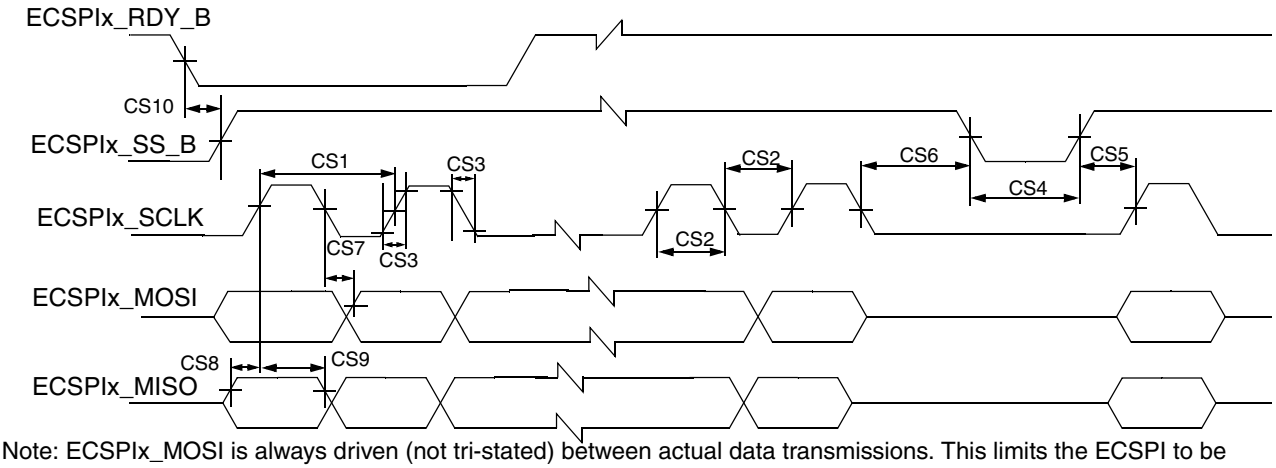
Figure 40. Samsung Toggle Mode Data Read Timing

Table 50. Samsung Toggle Mode Timing Parameters[1]

ID	Parameter	Symbol	Timing T = GPMI Clock Cycle		Unit
			Min	Max	
NF1	NAND_CLE setup time	tCLS	(AS + DS) × T - 0.12 [see 2,3]		—
NF2	NAND_CLE hold time	tCLH	DH × T - 0.72 [see 2]		—
NF3	NAND_CEx_B setup time	tCS	(AS + DS) × T - 0.58 [see 3,2]		—
NF4	NAND_CEx_B hold time	tCH	DH × T - 1 [see 2]		—
NF5	NAND_WE_B pulse width	tWP	DS × T [see 2]		—
NF6	NAND_ALE setup time	tALS	(AS + DS) × T - 0.49 [see 3,2]		—
NF7	NAND_ALE hold time	tALH	DH × T - 0.42 [see 2]		—
NF8	Command/address NAND_DATAxx setup time	tCAS	DS × T - 0.26 [see 2]		—
NF9	Command/address NAND_DATAxx hold time	tCAH	DH × T - 1.37 [see 2]		—
NF18	NAND_CEx_B access time	tCE	CE_DELAY × T [see 4,2]	—	ns
NF22	clock period	tCK	—	—	ns
NF23	preamble delay	tPRE	PRE_DELAY × T [see 5,2]	—	ns
NF24	postamble delay	tPOST	POST_DELAY × T +0.43 [see 2]	—	ns

4.11.2.1 ECSPI Master Mode Timing

Figure 41 depicts the timing of ECSPI in master mode and Table 51 lists the ECSPI master mode timing characteristics.



Note: ECSPIx_MOSI is always driven (not tri-stated) between actual data transmissions. This limits the ECSPI to be connected between a single master and a single slave.

Figure 41. ECSPI Master Mode Timing Diagram

Table 51. ECSPI Master Mode Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
CS1	ECSPIx_SCLK Cycle Time–Read • Slow group[1] • Fast group[2] ECSPIx_SCLK Cycle Time–Write	t_{clk}	 55 40 15	—	ns
CS2	ECSPIx_SCLK High or Low Time–Read • Slow group[1] • Fast group[2] ECSPIx_SCLK High or Low Time–Write	t_{SW}	 26 20 7	—	ns
CS3	ECSPIx_SCLK Rise or Fall[3]	$t_{RISE/FALL}$	—	—	ns
CS4	ECSPIx_SSx pulse width	t_{CSLH}	Half ECSPIx_SCLK period	—	ns
CS5	ECSPIx_SSx Lead Time (CS setup time)	t_{SCS}	Half ECSPIx_SCLK period - 4	—	ns
CS6	ECSPIx_SSx Lag Time (CS hold time)	t_{HCS}	Half ECSPIx_SCLK period - 2	—	ns
CS7	ECSPIx_MOSI Propagation Delay (C_{LOAD} = 20 pF)	t_{PDmosi}	-1	1	ns
CS8	ECSPIx_MISO Setup Time • Slow group[1] • Fast group[2]	t_{Smiso}	 21.5 16	—	ns
CS9	ECSPIx_MISO Hold Time	t_{Hmiso}	0	—	ns
CS10	ECSPIx_RDY to ECSPIx_SSx Time[4]	t_{SDRY}	5	—	ns

1 ECSPI slow includes:

ECSPI1/DISP0_DAT22, ECSPI1/KEY_COL1, ECSPI1/CSI0_DAT6, ECSPI2/EIM_OE, ECSPI2/ ECSPI2/CSI0_DAT10, ECSPI3/DISP0_DAT2

2 ECSPI fast includes:

ECSPI1/EIM_D17, ECSPI4/EIM_D22, ECSPI5/SD2_DAT0, ECSPI5/SD1_DAT0

3 See specific I/O AC parameters Section 4.7, “I/O AC Parameters.”

4 ECSPI_RDY is sampled internally by ipg_clk and is asynchronous to all other CSPI signals.

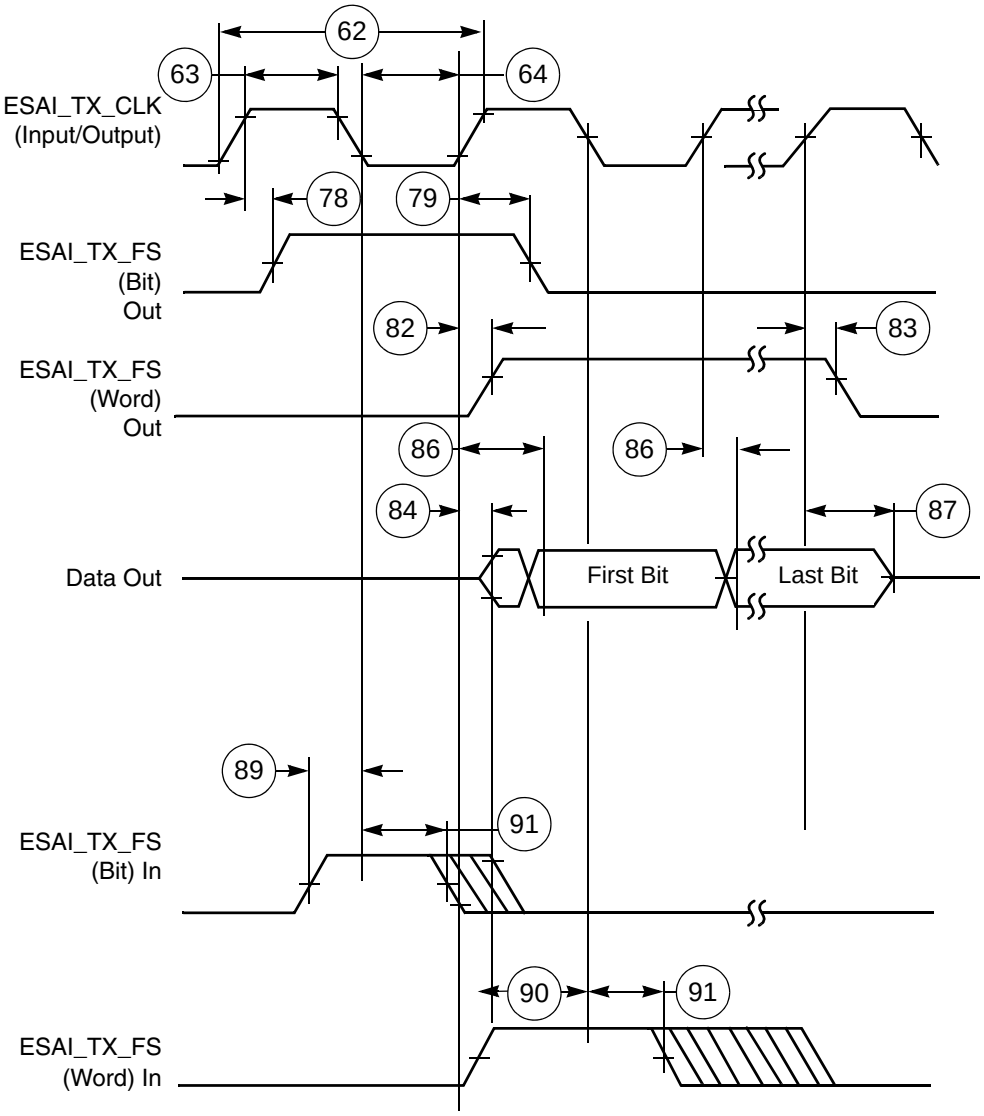


Figure 43. ESAI Transmitter Timing

4.11.5.1.2 MII Transmit Signal Timing (ENET_TX_DATA3,2,1,0, ENET_TX_EN, ENET_TX_ER, and ENET_TX_CLK)

The transmitter functions correctly up to an ENET_TX_CLK maximum frequency of 25 MHz + 1%. There is no minimum frequency requirement. Additionally, the processor clock frequency must exceed twice the ENET_TX_CLK frequency.

Figure 49 shows MII transmit signal timings. Table 58 describes the timing parameters (M5–M8) shown in the figure.

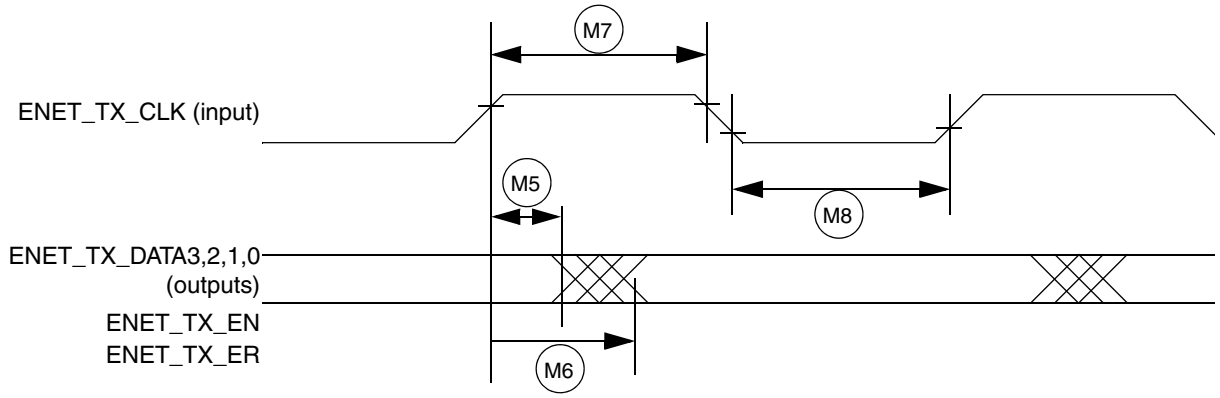


Figure 49. MII Transmit Signal Timing Diagram

Table 58. MII Transmit Signal Timing

ID	Characteristic[1]	Min	Max	Unit
M5	ENET_TX_CLK to ENET_TX_DATA3,2,1,0, ENET_TX_EN, ENET_TX_ER invalid	5	—	ns
M6	ENET_TX_CLK to ENET_TX_DATA3,2,1,0, ENET_TX_EN, ENET_TX_ER valid	—	20	ns
M7	ENET_TX_CLK pulse width high	35%	65%	ENET_TX_CLK period
M8	ENET_TX_CLK pulse width low	35%	65%	ENET_TX_CLK period

[1] ENET_TX_EN, ENET_TX_CLK, and ENET0_TXD0 have the same timing in 10-Mbps 7-wire interface mode.

4.11.5.1.3 MII Asynchronous Inputs Signal Timing (ENET_CRS and ENET_COL)

Figure 50 shows MII asynchronous input timings. Table 59 describes the timing parameter (M9) shown in the figure.

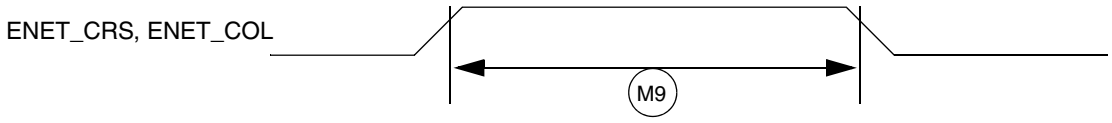


Figure 50. MII Async Inputs Timing Diagram

4.11.5.3 RGMII Signal Switching Specifications

The following timing specifications meet the requirements for RGMII interfaces for a range of transceiver devices.

Table 62. RGMII Signal Switching Specifications[1]

Symbol	Description	Min	Max	Unit
T_{cyc}[2]	Clock cycle duration	7.2	8.8	ns
T_{skewT}[3]	Data to clock output skew at transmitter	-100	900	ps
T_{skewR}[3]	Data to clock input skew at receiver	1	2.6	ns
Duty_G[4]	Duty cycle for Gigabit	45	55	%
Duty_T[4]	Duty cycle for 10/100T	40	60	%
Tr/Tf	Rise/fall time (20–80%)	—	0.75	ns

1 The timings assume the following configuration:
DDR_SEL = (11)b
DSE (drive-strength) = (111)b

2 For 10 Mbps and 100 Mbps, T_{cyc} will scale to 400 ns ±40 ns and 40 ns ±4 ns respectively.

3 For all versions of RGMII prior to 2.0; This implies that PC board design will require clocks to be routed such that an additional delay of greater than 1.2 ns and less than 1.7 ns will be added to the associated clock signal. For 10/100, the max value is unspecified.

4 Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domain as long as minimum duty cycle is not violated and stretching occurs for no more than three Tcyc of the lowest speed transitioned between.

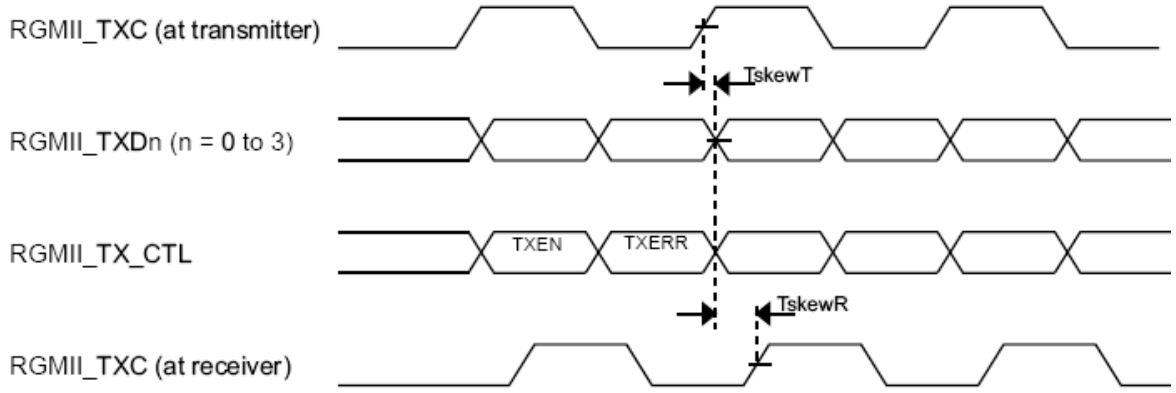


Figure 53. RGMII Transmit Signal Timing Diagram Original

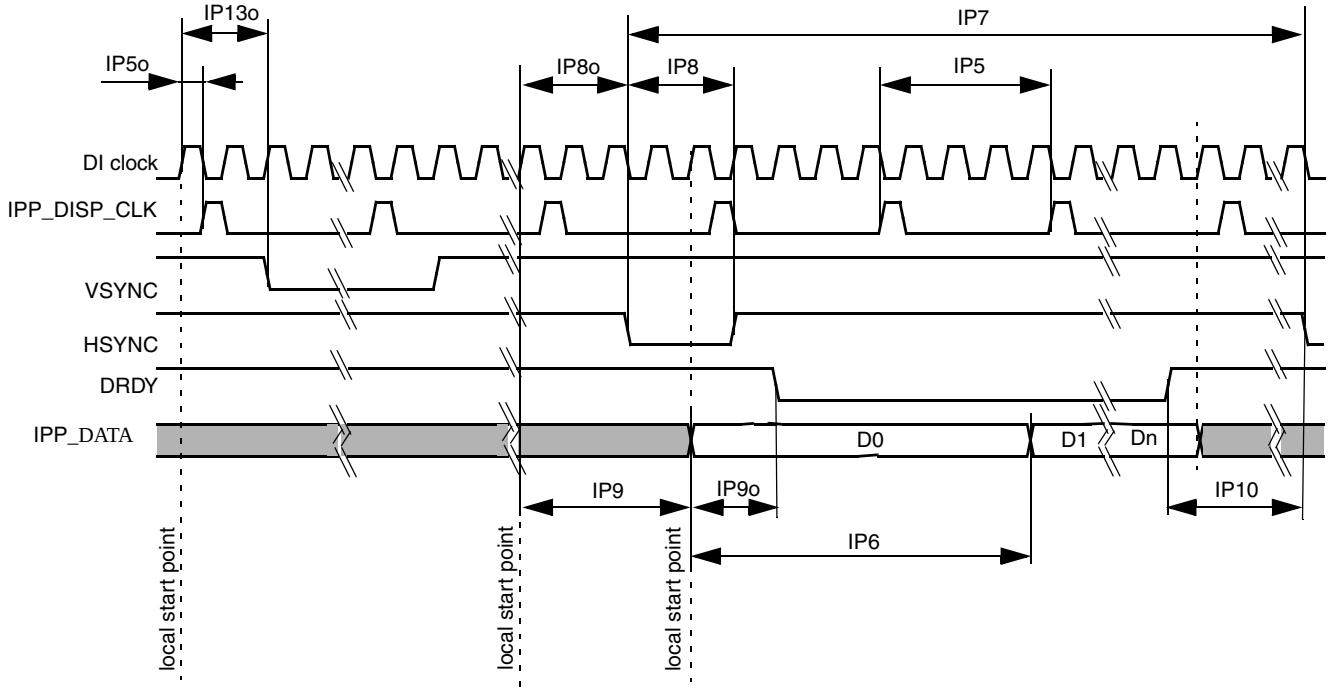


Figure 69. TFT Panels Timing Diagram—Horizontal Sync Pulse

Figure 70 depicts the vertical timing (timing of one frame). All parameters shown in the figure are programmable.

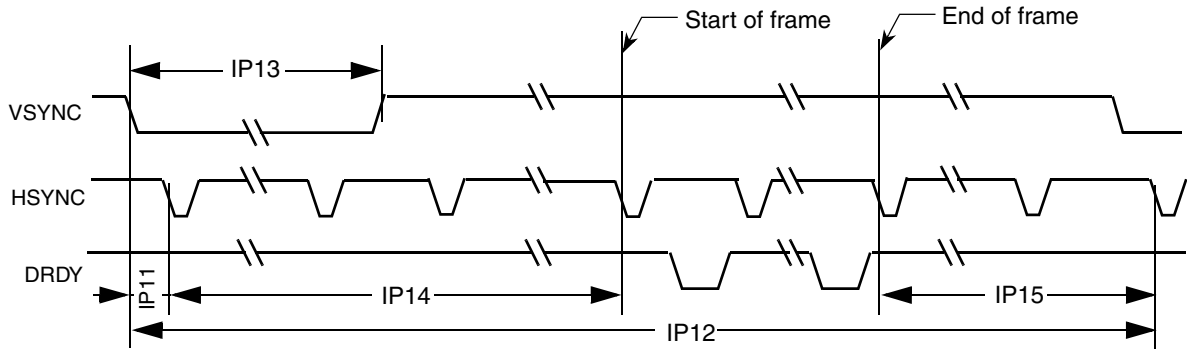


Figure 70. TFT Panels Timing Diagram—Vertical Sync Pulse

Table 72. Electrical and Timing Information (continued)

Symbol	Parameters	Test Conditions	Min	Typ	Max	Unit
HS Line Drivers DC Specifications						
$\|V_{OD}\|$	HS Transmit Differential output voltage magnitude	80 Ω<= RL< = 125 Ω	140	200	270	mV
$\Delta\|V_{OD}\|$	Change in Differential output voltage magnitude between logic states	80 Ω<= RL< = 125 Ω	—	—	10	mV
V_{CMTX}	Steady-state common-mode output voltage.	80 Ω<= RL< = 125 Ω	150	200	250	mV
$\Delta V_{CMTX}(1,0)$	Changes in steady-state common-mode output voltage between logic states	80 Ω<= RL< = 125 Ω	—	—	5	mV
V_{OHHS}	HS output high voltage	80 Ω<= RL< = 125 Ω	—	—	360	mV
Z_{OS}	Single-ended output impedance.	—	40	50	62.5	Ω
ΔZ_{OS}	Single-ended output impedance mismatch.	—	—	—	10	%
LP Line Drivers DC Specifications						
V_{OL}	Output low-level SE voltage	—	-50		50	mV
V_{OH}	Output high-level SE voltage	—	1.1	1.2	1.3	V
Z_{OLP}	Single-ended output impedance.	—	110	—	—	Ω
$\Delta Z_{OLP(01-10)}$	Single-ended output impedance mismatch driving opposite level	—	—	—	20	%
$\Delta Z_{OLP(0-11)}$	Single-ended output impedance mismatch driving same level	—	—	—	5	%
HS Line Receiver DC Specifications						
V_{IDTH}	Differential input high voltage threshold	—	—	—	70	mV
V_{IDTL}	Differential input low voltage threshold	—	-70	—	—	mV
V_{IHHS}	Single ended input high voltage	—	—	—	460	mV
V_{ILHS}	Single ended input low voltage	—	-40	—	—	mV
V_{CMRXDC}	Input common mode voltage	—	70	—	330	mV
Z_{ID}	Differential input impedance	—	80	—	125	Ω

Table 73. Electrical and Timing Information (continued)

Symbol	Parameters	Test Conditions	Min	Typ	Max	Unit
L_S	Equivalent wire bond series inductance	—	—	—	1.5	nH
R_S	Equivalent wire bond series resistance	—	—	—	0.15	Ω
R_L	Load Resistance	—	80	100	125	Ω

4.11.12.6 High-Speed Clock Timing

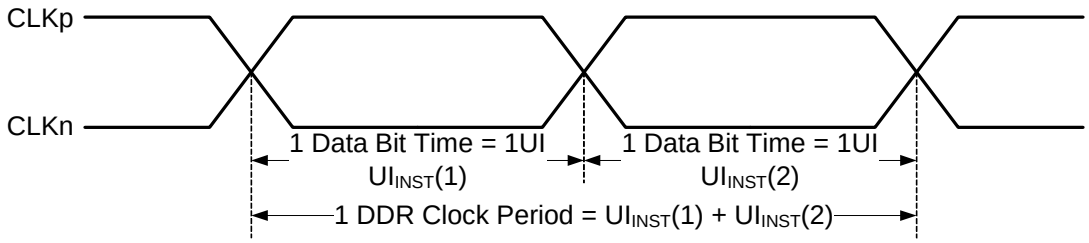


Figure 75. DDR Clock Definition

4.11.12.7 Forward High-Speed Data Transmission Timing

The timing relationship of the DDR Clock differential signal to the Data differential signal is shown in Figure 76:

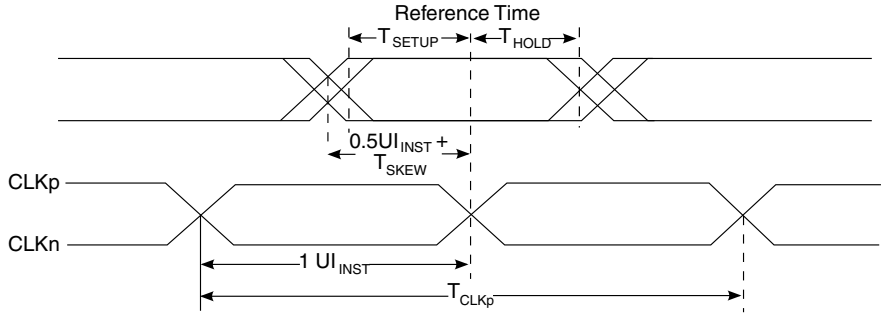


Figure 76. Data to Clock Timing Definitions

4.11.12.8 Reverse High-Speed Data Transmission Timing

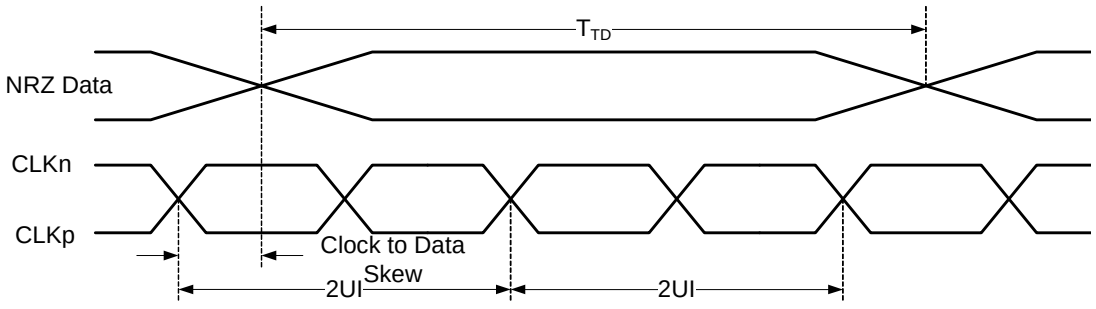


Figure 77. Reverse High-Speed Data Transmission Timing at Slave Side

Table 87. SSI Receiver Timing with Internal Clock (continued)

ID	Parameter	Min	Max	Unit
Oversampling Clock Operation				
SS47	Oversampling clock period	15.04	—	ns
SS48	Oversampling clock high period	6.0	—	ns
SS49	Oversampling clock rise time	—	3.0	ns
SS50	Oversampling clock low period	6.0	—	ns
SS51	Oversampling clock fall time	—	3.0	ns

NOTE

- All the timings for the SSI are given for a non-inverted serial clock polarity (TSCKP/RSCKP = 0) and a non-inverted frame sync (TFSI/RFSI = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal AUDx_TXC/AUDx_RXC and/or the frame sync AUDx_TXFS/AUDx_RXFS shown in the tables and in the figures.
- All timings are on Audiomux Pads when SSI is being used for data transfer.
- AUDx_TXC and AUDx_RXC refer to the Transmit and Receive sections of the SSI.
- The terms, WL and BL, refer to Word Length (WL) and Bit Length(BL).
- For internal Frame Sync operation using external clock, the frame sync timing is same as that of transmit data (for example, during AC97 mode of operation).

Table 100. 21 x 21 mm Functional Contact Assignments (continued)

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition[1]			
				Default Mode (Reset Mode)	Default Function (Signal Name)	Input/Output	Value[2]
EIM_A19	G25	NVCC_EIM1	GPIO	ALT0	EIM_ADDR19	Output	0
EIM_A20	H22	NVCC_EIM1	GPIO	ALT0	EIM_ADDR20	Output	0
EIM_A21	H23	NVCC_EIM1	GPIO	ALT0	EIM_ADDR21	Output	0
EIM_A22	F24	NVCC_EIM1	GPIO	ALT0	EIM_ADDR22	Output	0
EIM_A23	J21	NVCC_EIM1	GPIO	ALT0	EIM_ADDR23	Output	0
EIM_A24	F25	NVCC_EIM1	GPIO	ALT0	EIM_ADDR24	Output	0
EIM_A25	H19	NVCC_EIM0	GPIO	ALT0	EIM_ADDR25	Output	0
EIM_BCLK	N22	NVCC_EIM2	GPIO	ALT0	EIM_BCLK	Output	0
EIM_CS0	H24	NVCC_EIM1	GPIO	ALT0	EIM_CS0_B	Output	1
EIM_CS1	J23	NVCC_EIM1	GPIO	ALT0	EIM_CS1_B	Output	1
EIM_D16	C25	NVCC_EIM0	GPIO	ALT5	GPIO3_IO16	Input	PU (100K)
EIM_D17	F21	NVCC_EIM0	GPIO	ALT5	GPIO3_IO17	Input	PU (100K)
EIM_D18	D24	NVCC_EIM0	GPIO	ALT5	GPIO3_IO18	Input	PU (100K)
EIM_D19	G21	NVCC_EIM0	GPIO	ALT5	GPIO3_IO19	Input	PU (100K)
EIM_D20	G20	NVCC_EIM0	GPIO	ALT5	GPIO3_IO20	Input	PU (100K)
EIM_D21	H20	NVCC_EIM0	GPIO	ALT5	GPIO3_IO21	Input	PU (100K)
EIM_D22	E23	NVCC_EIM0	GPIO	ALT5	GPIO3_IO22	Input	PD (100K)
EIM_D23	D25	NVCC_EIM0	GPIO	ALT5	GPIO3_IO23	Input	PU (100K)
EIM_D24	F22	NVCC_EIM0	GPIO	ALT5	GPIO3_IO24	Input	PU (100K)
EIM_D25	G22	NVCC_EIM0	GPIO	ALT5	GPIO3_IO25	Input	PU (100K)
EIM_D26	E24	NVCC_EIM0	GPIO	ALT5	GPIO3_IO26	Input	PU (100K)
EIM_D27	E25	NVCC_EIM0	GPIO	ALT5	GPIO3_IO27	Input	PU (100K)
EIM_D28	G23	NVCC_EIM0	GPIO	ALT5	GPIO3_IO28	Input	PU (100K)
EIM_D29	J19	NVCC_EIM0	GPIO	ALT5	GPIO3_IO29	Input	PU (100K)
EIM_D30	J20	NVCC_EIM0	GPIO	ALT5	GPIO3_IO30	Input	PU (100K)
EIM_D31	H21	NVCC_EIM0	GPIO	ALT5	GPIO3_IO31	Input	PD (100K)
EIM_DA0	L20	NVCC_EIM2	GPIO	ALT0	EIM_AD00	Input	PU (100K)
EIM_DA1	J25	NVCC_EIM2	GPIO	ALT0	EIM_AD01	Input	PU (100K)
EIM_DA2	L21	NVCC_EIM2	GPIO	ALT0	EIM_AD02	Input	PU (100K)
EIM_DA3	K24	NVCC_EIM2	GPIO	ALT0	EIM_AD03	Input	PU (100K)
EIM_DA4	L22	NVCC_EIM2	GPIO	ALT0	EIM_AD04	Input	PU (100K)
EIM_DA5	L23	NVCC_EIM2	GPIO	ALT0	EIM_AD05	Input	PU (100K)
EIM_DA6	K25	NVCC_EIM2	GPIO	ALT0	EIM_AD06	Input	PU (100K)
EIM_DA7	L25	NVCC_EIM2	GPIO	ALT0	EIM_AD07	Input	PU (100K)
EIM_DA8	L24	NVCC_EIM2	GPIO	ALT0	EIM_AD08	Input	PU (100K)
EIM_DA9	M21	NVCC_EIM2	GPIO	ALT0	EIM_AD09	Input	PU (100K)

Table 100. 21 x 21 mm Functional Contact Assignments (continued)

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition[1]			
				Default Mode (Reset Mode)	Default Function (Signal Name)	Input/Output	Value[2]
LVDS0_TX3_P	W1	NVCC_LVDS_2P5	LVDS	ALT0	LVDS0_TX3_P	Input	Keeper
LVDS1_CLK_N	Y3	NVCC_LVDS_2P5	LVDS	—	LVDS1_CLK_N	—	—
LVDS1_CLK_P	Y4	NVCC_LVDS_2P5	LVDS	ALT0	LVDS1_CLK_P	Input	Keeper
LVDS1_TX0_N	Y1	NVCC_LVDS_2P5	LVDS	—	LVDS1_TX0_N	—	—
LVDS1_TX0_P	Y2	NVCC_LVDS_2P5	LVDS	ALT0	LVDS1_TX0_P	Input	Keeper
LVDS1_TX1_N	AA2	NVCC_LVDS_2P5	LVDS	—	LVDS1_TX1_N	—	—
LVDS1_TX1_P	AA1	NVCC_LVDS_2P5	LVDS	ALT0	LVDS1_TX1_P	Input	Keeper
LVDS1_TX2_N	AB1	NVCC_LVDS_2P5	LVDS	—	LVDS1_TX2_N	—	—
LVDS1_TX2_P	AB2	NVCC_LVDS_2P5	LVDS	ALT0	LVDS1_TX2_P	Input	Keeper
LVDS1_TX3_N	AA3	NVCC_LVDS_2P5	LVDS	—	LVDS1_TX3_N	—	—
LVDS1_TX3_P	AA4	NVCC_LVDS_2P5	LVDS	ALT0	LVDS1_TX3_P	Input	Keeper
MLB_CN	A11	VDD_HIGH_CAP	LVDS	—	MLB_CLK_N	—	—
MLB_CP	B11	VDD_HIGH_CAP	LVDS	—	MLB_CLK_P	—	—
MLB_DN	B10	VDD_HIGH_CAP	LVDS	—	MLB_DATA_N	—	—
MLB_DP	A10	VDD_HIGH_CAP	LVDS	—	MLB_DATA_P	—	—
MLB_SN	A9	VDD_HIGH_CAP	LVDS	—	MLB_SIG_N	—	—
MLB_SP	B9	VDD_HIGH_CAP	LVDS	—	MLB_SIG_P	—	—
NANDF_ALE	A16	NVCC_NANDF	GPIO	ALT5	GPIO6_IO08	Input	PU (100K)
NANDF_CLE	C15	NVCC_NANDF	GPIO	ALT5	GPIO6_IO07	Input	PU (100K)
NANDF_CS0	F15	NVCC_NANDF	GPIO	ALT5	GPIO6_IO11	Input	PU (100K)
NANDF_CS1	C16	NVCC_NANDF	GPIO	ALT5	GPIO6_IO14	Input	PU (100K)
NANDF_CS2	A17	NVCC_NANDF	GPIO	ALT5	GPIO6_IO15	Input	PU (100K)
NANDF_CS3	D16	NVCC_NANDF	GPIO	ALT5	GPIO6_IO16	Input	PU (100K)
NANDF_D0	A18	NVCC_NANDF	GPIO	ALT5	GPIO2_IO00	Input	PU (100K)
NANDF_D1	C17	NVCC_NANDF	GPIO	ALT5	GPIO2_IO01	Input	PU (100K)
NANDF_D2	F16	NVCC_NANDF	GPIO	ALT5	GPIO2_IO02	Input	PU (100K)
NANDF_D3	D17	NVCC_NANDF	GPIO	ALT5	GPIO2_IO03	Input	PU (100K)
NANDF_D4	A19	NVCC_NANDF	GPIO	ALT5	GPIO2_IO04	Input	PU (100K)
NANDF_D5	B18	NVCC_NANDF	GPIO	ALT5	GPIO2_IO05	Input	PU (100K)
NANDF_D6	E17	NVCC_NANDF	GPIO	ALT5	GPIO2_IO06	Input	PU (100K)
NANDF_D7	C18	NVCC_NANDF	GPIO	ALT5	GPIO2_IO07	Input	PU (100K)
NANDF_RB0	B16	NVCC_NANDF	GPIO	ALT5	GPIO6_IO10	Input	PU (100K)
NANDF_WP_B	E15	NVCC_NANDF	GPIO	ALT5	GPIO6_IO09	Input	PU (100K)
ONOFF	D12	VDD_SNVS_IN	GPIO	—	SRC_ONOFF	Input	PU (100K)
PCIE_RXM	B1	PCIE_VPH	—	—	PCIE_RX_N	—	—
PCIE_RXP	B2	PCIE_VPH	—	—	PCIE_RX_P	—	—

[3] ENET_REF_CLK is used as a clock source for MII and RGMII modes only. RMII mode uses either GPIO_16 or RGMII_TX_CTL as a clock source. For more information on these clocks, see your specific device reference manual and the *Hardware Development Guide for i.MX 6Quad, 6Dual, 6DualLite, 6Solo Families of Applications Processors* (IMX6DQ6SDLHDG).

For most of the signals, the state during reset is same as the state after reset, given in Out of Reset Condition column of Table 100. However, there are few signals for which the state during reset is different from the state after reset. These signals along with their state during reset are given in Table 101.

Table 101. Signals with Differing Before Reset and After Reset States

Ball Name	Before Reset State	
	Input/Output	Value
EIM_A16	Input	PD (100K)
EIM_A17	Input	PD (100K)
EIM_A18	Input	PD (100K)
EIM_A19	Input	PD (100K)
EIM_A20	Input	PD (100K)
EIM_A21	Input	PD (100K)
EIM_A22	Input	PD (100K)
EIM_A23	Input	PD (100K)
EIM_A24	Input	PD (100K)
EIM_A25	Input	PD (100K)
EIM_DA0	Input	PD (100K)
EIM_DA1	Input	PD (100K)
EIM_DA2	Input	PD (100K)
EIM_DA3	Input	PD (100K)
EIM_DA4	Input	PD (100K)
EIM_DA5	Input	PD (100K)
EIM_DA6	Input	PD (100K)
EIM_DA7	Input	PD (100K)
EIM_DA8	Input	PD (100K)
EIM_DA9	Input	PD (100K)
EIM_DA10	Input	PD (100K)
EIM_DA11	Input	PD (100K)
EIM_DA12	Input	PD (100K)
EIM_DA13	Input	PD (100K)
EIM_DA14	Input	PD (100K)
EIM_DA15	Input	PD (100K)