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Understanding Embedded - Microprocessors

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Applications of **Embedded - Microprocessors**

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Active
Core Processor	ARM® Cortex®-A9
Number of Cores/Bus Width	4 Core, 32-Bit
Speed	852MHz
Co-Processors/DSP	Multimedia; NEON™ SIMD
RAM Controllers	LPDDR2, DDR3L, DDR3
Graphics Acceleration	Yes
Display & Interface Controllers	HDMI, Keypad, LCD, LVDS, MIPI/DSI, Parallel
Ethernet	10/100/1000Mbps (1)
SATA	SATA 3Gbps (1)
USB	USB 2.0 + PHY (3), USB 2.0 OTG + PHY (1)
Voltage - I/O	1.8V, 2.5V, 2.8V, 3.3V
Operating Temperature	-40°C ~ 125°C (TJ)
Security Features	ARM TZ, A-HAB, CAAM, CSU, SJC, SNVS
Package / Case	624-FBGA, FCBGA
Supplier Device Package	624-FCBGA (21x21)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcimx6qp6avt8aa

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Introduction

The i.MX 6DualPlus/6QuadPlus processors are specifically useful for applications such as the following:

- Reconfigurable instrument cluster high performance infotainment
- Graphics rendering for Human Machine Interfaces (HMI)
- Video processing and display

The i.MX 6DualPlus/6QuadPlus processors offers numerous advanced features, such as:

- Multilevel memory system—The multilevel memory system of each processor is based on the L1 instruction and data caches, L2 cache, and internal and external memory. The processors support many types of external memory devices, including DDR3, DDR3L, LPDDR2, NOR Flash, PSRAM, cellular RAM, NAND Flash (MLC and SLC), OneNANDTM, and managed NAND, including eMMC up to rev 4.4/4.41.
- Smart speed technology—The processors have power management throughout the device that enables the rich suite of multimedia features and peripherals to consume minimum power in both active and various low power modes. Smart speed technology enables the designer to deliver a feature-rich product, requiring levels of power far lower than industry expectations.
- Dynamic voltage and frequency scaling—The processors improve the power efficiency of devices by scaling the voltage and frequency to optimize performance.
- Multimedia powerhouse—The multimedia performance of each processor is enhanced by a multilevel cache system, Neon[®] MPE (Media Processor Engine) co-processor, a multi-standard hardware video codec, 2 autonomous and independent image processing units (IPU), and a programmable smart DMA (SDMA) controller.
- Powerful graphics acceleration—Each processor provides three independent, integrated graphics processing units: an OpenGL[®] ES 3.0 3D graphics accelerator with four shaders (up to 198 MTri/s and OpenCL support), 2D graphics accelerator, and dedicated OpenVGTM 1.1 accelerator.
- Interface flexibility—Each processor supports connections to a variety of interfaces: LCD controller for up to four displays (including parallel display, HDMI1.4, MIPI display, and LVDS display), dual CMOS sensor interface (parallel or through MIPI), high-speed USB on-the-go with PHY, high-speed USB host with PHY, multiple expansion card ports (high-speed MMC/SDIO host and other), 10/100/1000 Mbps Gigabit Ethernet controller, and a variety of other popular interfaces (such as UART, I²C, and I²S serial audio, SATA-II, and PCIe-II).
- Automotive environment support—Each processor includes interfaces, such as two CAN ports, an MLB150/50 port, an ESAI audio interface, and an asynchronous sample rate converter for multichannel/multisource audio.
- Advanced security—The processors deliver hardware-enabled security features that enable secure e-commerce, digital rights management (DRM), information encryption, secure boot, and secure software downloads. The security features are discussed in detail in the i.MX 6Dual/6Quad security reference manual (IMX6DQ6SDLSRM).
- Integrated power management—The processors integrate linear regulators and internally generate voltage levels for different domains. This significantly simplifies system power management structure.

Mode	Test Conditions	Supply	Typical ¹	Unit
STOP_ON ARM LDO set to 0.9 V SoC and PU LDOs set to 1.225 V HIGH LDO set to 2.5 V 	VDD_ARM_IN (1.4 V)	7.5	mA	
	 SoC and PU LDOs set to 1.225 V HIGH LDO set to 2.5 V 	VDD_SOC_IN (1.4 V)	22	mA
	PLLs disabled DDB is in self refresh	VDD_HIGH_IN (3.0 V)	3.7	mA
		Total	52	mW
STOP_OFF	STOP_OFF • ARM LDO set to 0.9 V		7.5	mA
	 Soc LDO set to 1.225 V PU LDO is power gated 	VDD_SOC_IN (1.4 V)	13.5	mA
	HIGH LDO set to 2.5 V PLLs disabled	VDD_HIGH_IN (3.0 V)	3.7	mA
	DDR is in self refresh	Total	41	mW
STANDBY	ARM and PU LDOs are power gated	VDD_ARM_IN (0.9 V)	0.1	mA
	 Soc LDO is in bypass HIGH LDO is set to 2.5 V 	VDD_SOC_IN (1.05 V)	13	mA
	PLLs are disabled	VDD_HIGH_IN (3.0 V)	3.7	mA
	Well Bias ON Crystal oscillator is enabled	Total	22	mW
Deep Sleep Mode	ARM and PU LDOs are power gated	VDD_ARM_IN (0.9 V)	0.1	mA
(DSM)	Soc LDO is in bypass HIGH LDO is set to 2.5 V	VDD_SOC_IN (1.05 V)	2	mA
	PLLs are disabled Low voltage	VDD_HIGH_IN (3.0 V)	0.5	mA
	 Well Bias ON Crystal oscillator and bandgap are disabled 	Total	3.4	mW
SNVS Only	VDD_SNVS_IN powered	VDD_SNVS_IN (2.8V)	41	μA
	All other supplies off SRTC running	Total	115	μW

Table 9. Stop Mode Current and Power Consumption (continued)

¹ The typical values shown here are for information only and are not guaranteed. These values are average values measured on a worst-case wafer at 25°C.

4.8.1 GPIO Output Buffer Impedance

Table 33 shows the GPIO output buffer impedance (OVDD 1.8 V).

Table 33. GPIO Output Buffer Average Impedance (OVDD 1.8 V)

Parameter	Symbol	Drive Strength (ipp_dse)	Typ Value	Unit
		001	260	
		010	130	
		011	90	
	Rdrv	100	60	Ω
Impedance		101	50	
		110	40	
		111	33	

Table 34 shows the GPIO output buffer impedance (OVDD 3.3 V).

Table 34. GPIO Output Buffer Average Impedance (OVDD 3.3 V)

Parameter	Symbol	Drive Strength (ipp_dse)	Typ Value	Unit
		001	150	
		010	75	
	Rdrv	011	50	
		100	37	Ω
Impedance		101	30	
		110	25	
		111	20	

4.9.3.2 General EIM Timing-Synchronous Mode

Figure 12, Figure 13, and Table 40 specify the timings related to the EIM module. All EIM output control signals may be asserted and deasserted by an internal clock synchronized to the EIM_BCLK rising edge according to corresponding assertion/negation control fields.



Figure 12. EIM Output Timing Diagram



Figure 13. EIM Input Timing Diagram

4.9.3.3 Examples of EIM Synchronous Accesses

Table 40. EIM Bus Timing Parameters

ID	Parameter	Min ¹	Max ¹	Unit
WE1	EIM_BCLK cycle time ²	t × (k+1)	—	ns
WE2	EIM_BCLK high level width	$0.4 \times t \times (k+1)$	—	ns
WE3	EIM_BCLK low level width	$0.4 \times t \times (k+1)$	_	ns

4.9.3.4 General EIM Timing-Asynchronous Mode

Figure 18 through Figure 22 and Table 41 provide timing parameters relative to the chip select (CS) state for asynchronous and DTACK EIM accesses with corresponding EIM bit fields and the timing parameters mentioned above.

Asynchronous read and write access length in cycles may vary from what is shown in Figure 18 through Figure 21 as RWSC, OEN & CSN is configured differently. See the i.MX 6DualPlus/6QuadPlus reference manual (IMX6DQPRM) for the EIM programming model.



Figure 18. Asynchronous Memory Read Access (RWSC = 5)

4.10.1 Asynchronous Mode AC Timing (ONFI 1.0 Compatible)

Asynchronous mode AC timings are provided as multiplications of the clock cycle and fixed delay. The Maximum I/O speed of GPMI in Asynchronous mode is about 50 MB/s. Figure 30 through Figure 33 depict the relative timing between GPMI signals at the module level for different operations under Asynchronous mode. Table 48 describes the timing parameters (NF1–NF17) that are shown in the figures.



Figure 30. Command Latch Cycle Timing Diagram



Figure 31. Address Latch Cycle Timing Diagram







Figure 38. NAND_DQS/NAND_DQ Read Valid Window

ID	D Parameter		Timin T = GPMI Clo	g ck Cycle	Unit		
			Min	Мах			
NF18	NAND_CEx_B access time	tCE	CE_DELAY × T -	0.79 [see ²]	ns		
NF19	NAND_CEx_B hold time	tCH	0.5 × tCK - 0.6	63 [see ²]	ns		
NF20	Command/address NAND_DATAxx setup time	tCAS	$0.5 imes tCK \cdot$	0.05	ns		
NF21	Command/address NAND_DATAxx hold time	tCAH	0.5 × tCK - 1.23		0.5 × tCK - 1.23		ns
NF22	clock period	tCK	_		ns		
NF23	preamble delay	tPRE	PRE_DELAY × T - 0.29 [see ²]		ns		
NF24	postamble delay	tPOST	POST_DELAY × T - 0.78 [see ²]		ns		
NF25	NAND_CLE and NAND_ALE setup time	tCALS	$0.5 imes tCK \cdot$	0.86	ns		
NF26	NAND_CLE and NAND_ALE hold time	tCALH	$0.5 imes tCK \cdot$	0.37	ns		
NF27	NAND_CLK to first NAND_DQS latching transition	tDQSS	T - 0.41 [s	ee ²]	ns		
NF28	Data write setup	tDS	0.25 × tCK - 0.35		_		
NF29	Data write hold	tDH	0.25 × tCK - 0.85		_		
NF30	NAND_DQS/NAND_DQ read setup skew	tDQSQ	— 2.06		—		
NF31	NAND_DQS/NAND_DQ read hold skew	tQHS	—	1.95			

Table 49. Source Synchronous Mode Timing Parameters¹

¹ The GPMI source synchronous mode output timing can be controlled by the module's internal registers GPMI_TIMING2_CE_DELAY, GPMI_TIMING_PREAMBLE_DELAY, GPMI_TIMING2_POST_DELAY. This AC timing depends on these registers settings. In the table, CE_DELAY/PRE_DELAY/POST_DELAY represents each of these settings.

² T = tCK (GPMI clock period) -0.075ns (half of maximum p-p jitter).

Figure 38 shows the timing diagram of NAND_DQS/NAND_DATAxx read valid window. For Source Synchronous mode, the typical value of tDQSQ is 0.85 ns (max) and 1 ns (max) for tQHS at 200MB/s. GPMI will sample NAND_DATA[7:0] at both rising and falling edge of a delayed NAND_DQS signal, which can be provided by an internal DPLL. The delay value can be controlled by GPMI register GPMI_READ_DDR_DLL_CTRL.SLV_DLY_TARGET (see the GPMI chapter of the i.MX 6DualPlus/6QuadPlus reference manual (IMX6DQPRM)). Generally, the typical delay value of this register is equal to 0x7 which means 1/4 clock cycle delay expected. However, if the board delay is large enough and cannot be ignored, the delay value should be made larger to compensate the board delay.

Electrical Characteristics

ID	Parameter ^{1,2}	Symbol	Expression ²	Min	Мах	Condition ³	Unit
81	ESAI_TX_CLK rising edge to ESAI_TX_FS out (wr) low ⁵	_			22.0 12.0	x ck i ck	ns
82	ESAI_TX_CLK rising edge to ESAI_TX_FS out (wI) high	_			19.0 9.0	x ck i ck	ns
83	ESAI_TX_CLK rising edge to ESAI_TX_FS out (wl) low	_			20.0 10.0	x ck i ck	ns
84	ESAI_TX_CLK rising edge to data out enable from high impedance	_			22.0 17.0	x ck i ck	ns
86	ESAI_TX_CLK rising edge to data out valid	_	_		19.0 13.0	x ck i ck	ns
87	ESAI_TX_CLK rising edge to data out high impedance ⁶⁷	_			21.0 16.0	x ck i ck	ns
89	ESAI_TX_FS input (bl, wr) setup time before ESAI_TX_CLK falling edge ⁵	_		2.0 18.0		x ck i ck	ns
90	ESAI_TX_FS input (wI) setup time before ESAI_TX_CLK falling edge	—		2.0 18.0		x ck i ck	ns
91	ESAI_TX_FS input hold time after ESAI_TX_CLK falling edge	_		4.0 5.0		x ck i ck	ns
95	ESAI_RX_HF_CLK/ESAI_TX_HF_CLK clock cycle	—	2 x T _C	15	_	—	ns
96	ESAI_TX_HF_CLK input rising edge to ESAI_TX_CLK output	—	_		18.0	_	ns
97	ESAI_RX_HF_CLK input rising edge to ESAI_RX_CLK output		_		18.0	_	ns

Table 53. Enhanced Serial Audio Interface (ESAI) Timing (continued)

¹ i ck = internal clock

x ck = external clock

i ck a = internal clock, asynchronous mode

(asynchronous implies that ESAI_TX_CLK and ESAI_RX_CLK are two different clocks)

i ck s = internal clock, synchronous mode

(synchronous implies that ESAI_TX_CLK and ESAI_RX_CLK are the same clock)

² bl = bit length

- wl = word length
- wr = word length relative
- ³ ESAI_TX_CLK(ESAI_TX_CLK pin) = transmit clock

ESAI_RX_CLK(ESAI_RX_CLK pin) = receive clock

ESAI_TX_FS(ESAI_TX_FS pin) = transmit frame sync

ESAI_RX_FS(ESAI_RX_FS pin) = receive frame sync

ESAI_TX_HF_CLK(ESAI_TX_HF_CLK pin) = transmit high frequency clock

ESAI_RX_HF_CLK(ESAI_RX_HF_CLK pin) = receive high frequency clock

⁴ For the internal clock, the external clock cycle is defined by lcyc and the ESAI control register.

- ⁵ The word-relative frame sync signal waveform relative to the clock operates in the same manner as the bit-length frame sync signal waveform, but it spreads from one serial clock before the first bit clock (like the bit length frame sync signal), until the second-to-last bit clock of the first word in the frame.
- ⁶ Periodically sampled and not 100% tested.



Figure 59. TMDS Clock Signal Definitions



Figure 60. Eye Diagram Mask Definition for HDMI Driver Signal Specification at TP1



Figure 61. Intra-Pair Skew Definition

Electrical Characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit			
t _F	Differential output signal fall time	20-80% RL = 50 Ω See Figure 63.	75	—	0.4 UI	ps			
—	Differential signal overshoot	Referred to 2x V _{SWING}	—	—	15	%			
—	Differential signal undershoot	oot Referred to 2x V _{SWING}		—	25	%			
Data and Control Interface Specifications									
t _{Power-up} 2	HDMI 3D Tx PHY power-up time	From power-down to HSI_TX_READY assertion	_	—	3.35	ms			

Table 64. Switching Characteristics (continued)

¹ Relative to ideal recovery clock, as specified in the HDMI specification, version 1.4a, section 4.2.3.

² For information about latencies and associated timings, see Section 4.11.7.1, "Latencies and Timing Information."

4.11.9 I²C Module Timing Parameters

This section describes the timing parameters of the I²C module. Figure 64 depicts the timing of I²C module, and Table 65 lists the I²C module timing characteristics.



Figure 64. I²C Bus Timing

Table 65. I²C Module Timing Parameters

	Baramatar	Standa	ard Mode	Fast Mo	Unit	
	Farameter	Min	Мах	Min	Max	Unit
IC1	I2Cx_SCL cycle time	10	—	2.5	—	μs
IC2	Hold time (repeated) START condition	4.0	—	0.6	_	μs
IC3	Set-up time for STOP condition	4.0	—	0.6	—	μs
IC4	Data hold time	01	3.45 ²	0 ¹	0.9 ²	μs
IC5	HIGH Period of I2Cx_SCL Clock	4.0	—	0.6	—	μs
IC6	LOW Period of the I2Cx_SCL Clock	4.7	—	1.3	—	μs
IC7	Set-up time for a repeated START condition	4.7	—	0.6	—	μs
IC8	Data set-up time	250	—	100 ³	_	ns

4.11.10.3 Electrical Characteristics

Figure 67 depicts the sensor interface timing. IPU2_CSIx_PIX_CLK signal described here is not generated by the IPU. Table 67 lists the sensor interface timing characteristics.



Figure 67. Sensor Interface Timing Diagram

Table 67. Sensor Interface Timing Characteristics

ID	Parameter	Symbol	Min	Мах	Unit
IP1	Sensor output (pixel) clock frequency	Fpck	0.01	180	MHz
IP2	Data and control setup time	Tsu	2	_	ns
IP3	Data and control holdup time	Thd	1	_	ns
—	Vsync to Hsync	Tv-h	1/Fpck	_	ns
—	Vsync and Hsync pulse width	Tpulse	1/Fpck	_	ns
_	Vsync to first data	Tv-d	1/Fpck		ns

4.11.10.4 IPU Display Interface Signal Mapping

The IPU supports a number of display output video formats. Table 68 defines the mapping of the Display Interface Pins used during various supported video interface formats.

i.MX 6DualPlus/6QuadPlus								
	RGB,	R	GB/TV	Signal A	Allocation	(Examp	le)	Comment ^{1,2}
Port Name (x = 0, 1)	Signal Name (General)	16-bit RGB	18-bit RGB	24 Bit RGB	8-bit YCrCb ³	16-bit YCrCb	20-bit YCrCb	
IPUx_DISPx_DAT00	DAT[0]	B[0]	B[0]	B[0]	Y/C[0]	C[0]	C[0]	—
IPUx_DISPx_DAT01	DAT[1]	B[1]	B[1]	B[1]	Y/C[1]	C[1]	C[1]	—
IPUx_DISPx_DAT02	DAT[2]	B[2]	B[2]	B[2]	Y/C[2]	C[2]	C[2]	_
IPUx_DISPx_DAT03	DAT[3]	B[3]	B[3]	B[3]	Y/C[3]	C[3]	C[3]	_
IPUx_DISPx_DAT04	DAT[4]	B[4]	B[4]	B[4]	Y/C[4]	C[4]	C[4]	_

Table 68. Video Signal Cross-Reference

i.MX 6DualPlus/6QuadPlus Automotive Applications Processors, Rev. 1, 03/2016

Freescale Semiconductor Inc.

Electrical Characteristics



Figure 69. TFT Panels Timing Diagram—Horizontal Sync Pulse

Figure 70 depicts the vertical timing (timing of one frame). All parameters shown in the figure are programmable.



Figure 70. TFT Panels Timing Diagram—Vertical Sync Pulse

Electrical Characteristics

Parameter	Symbol	Test Conditions	Min	Max	Unit
Common-mode output voltage: (V _{O+} - V _{O-}) / 2	V _{OCM}	_	1.0	1.5	V
Difference in common-mode output between (high/low) steady-states: I V _{OCM, high} - V _{OCM, low} I	ΔV _{OCM}	_	-50	50	mV
Variations on common-mode output during a logic state transitions	V _{CMV}	See Note ²		150	mVpp
Short circuit current	ll _{OS} l	See Note ³	—	43	mA
Differential output impedance	Z _O	_	1.6		kΩ
	Receiv	er Characteristics			
Differential clock input: • logic low steady-state • logic high steady-state • hysteresis	V _{ILC} V _{IHC} V _{HSC}	See Note ⁴	50 -25	-50 25	mV mV mV
Differential signal/data input: • logic low steady-state • logic high steady-state	V _{ILS} V _{IHS}	_	 50	-50 —	mV mV
Signal-ended input voltage (steady-state): • MLB_SIG_P, MLB_DATA_P • MLB_SIG_N, MLB_DATA_N	V _{IN+} V _{IN-}	_	0.5 0.5	2.0 2.0	V V

Table 76. MediaLB 6-Pin Interface Electrical DC Specifications (continued)

¹ The signal-ended output voltage of a driver is defined as V_{O+} on MLB_CLK_P, MLB_SIG_P, and MLB_DATA_P. The signal-ended output voltage of a driver is defined as V_{O-} on MLB_CLK_N, MLB_SIG_N, and MLB_DATA_N.

² Variations in the common-mode voltage can occur between logic states (for example, during state transitions) as a result of differences in the transition rate of V_{O+} and V_{O-}.

 $^3\,$ Short circuit current is applicable when V_{O_{+}} and V_{O_{-}} are shorted together and/or shorted to ground.

 $^4\,$ The logic state of the receiver is undefined when -50 mV < V_{ID} < 50 mV.

4.11.20 SSI Timing Parameters

This section describes the timing parameters of the SSI module. The connectivity of the serial synchronous interfaces are summarized in Table 85.

Port	Signal Nomenclature	Type and Access
AUDMUX port 1	SSI 1	Internal
AUDMUX port 2	SSI 2	Internal
AUDMUX port 3	AUD3	External – AUD3 I/O
AUDMUX port 4	AUD4	External – EIM or CSPI1 I/O through IOMUXC
AUDMUX port 5	AUD5	External – EIM or SD1 I/O through IOMUXC
AUDMUX port 6	AUD6	External – EIM or DISP2 through IOMUXC
AUDMUX port 7	SSI 3	Internal

Table 85. AUDMUX Port Allocation

NOTE

The terms WL and BL used in the timing diagrams and tables refer to Word Length (WL) and Bit Length (BL).

4.11.20.1 SSI Transmitter Timing with Internal Clock

Figure 96 depicts the SSI transmitter internal clock timing and Table 86 lists the timing parameters for the SSI transmitter internal clock.



Figure 96. SSI Transmitter Internal Clock Timing Diagram

ID	Parameter	Min	Мах	Unit
	External Clock Operation	on		
SS22	AUDx_TXC/AUDx_RXC clock period	81.4	_	ns
SS23	AUDx_TXC/AUDx_RXC clock high period	36	_	ns
SS24	AUDx_TXC/AUDx_RXC clock rise time	_	6.0	ns
SS25	AUDx_TXC/AUDx_RXC clock low period	36	_	ns
SS26	AUDx_TXC/AUDx_RXC clock fall time	_	6.0	ns
SS28	AUDx_RXC high to AUDx_TXFS (bl) high	-10	15.0	ns
SS30	AUDx_RXC high to AUDx_TXFS (bl) low	10	_	ns
SS32	AUDx_RXC high to AUDx_TXFS (wl) high	-10	15.0	ns
SS34	AUDx_RXC high to AUDx_TXFS (wl) low	10	_	ns
SS35	AUDx_TXC/AUDx_RXC External AUDx_TXFS rise time	_	6.0	ns
SS36	AUDx_TXC/AUDx_RXC External AUDx_TXFS fall time	_	6.0	ns
SS40	AUDx_RXD setup time before AUDx_RXC low	10		ns
SS41	AUDx_RXD hold time after AUDx_RXC low	2		ns

Table 89. SSI Receiver Timing with External Clock

NOTE

- All the timings for the SSI are given for a non-inverted serial clock polarity (TSCKP/RSCKP = 0) and a non-inverted frame sync (TFSI/RFSI = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal AUDx_TXC/AUDx_RXC and/or the frame sync AUDx_TXFS/AUDx_RXFS shown in the tables and in the figures.
- All timings are on Audiomux Pads when SSI is being used for data transfer.
- AUDx_TXC and AUDx_RXC refer to the Transmit and Receive sections of the SSI.
- The terms, WL and BL, refer to Word Length (WL) and Bit Length (BL).
- For internal Frame Sync operation using external clock, the frame sync timing is same as that of transmit data (for example, during AC97 mode of operation).

6.2.1.1 21 x 21 mm Lidded Package

Figure 106 and Figure 107 show the top, bottom, and side views of the 21×21 mm lidded package.



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TITLE: 624 1/0 FC F	BGA.	DOCUME	NT NO: 98ASA00330D	REV: D	
21 X 21 X 2	PKG,	STANDARD: NON-JEDEC			
0.8 MM PITCH, STA	AMPED LID		C	08 OCT 2013	

Figure 106. 21 x 21 mm Lidded Package Top, Bottom, and Side Views (Sheet 1 of 2)

Supply Rail Name	Ball(s) Position(s)	Remark
VDDHIGH_CAP	H10, J10	Secondary supply for the 2.5 V domain (internal regulator output—requires capacitor if internal regulator is used)
VDDHIGH_IN	H9, J9	Primary supply for the 2.5 V regulator
VDDPU_CAP	H17, J17, K17, L17, M17, N17, P17	Secondary supply for the VPU and GPU (internal regulator output— requires capacitor if internal regulator is used)
VDDSOC_CAP	R10, T10, T13, T14, U10, U13, U14	Secondary supply for the SoC and PU (internal regulator output—requires capacitor if internal regulator is used)
VDDSOC_IN	H16, J16, K16, L16, M16, N16, P16, R16, T16, U16	Primary supply for the SoC and PU regulators
VDDUSB_CAP	F9	Secondary supply for the 3 V domain (internal regulator output—requires capacitor if internal regulator is used)
ZQPAD	AE17	—

Table 99. 21 x 21 mm Supplies Contact Assignment (continued)

Table 100 displays an alpha-sorted list of the signal assignments including power rails. The table also includes out of reset pad state.

fable 100. 21 x 21 mm Function	nal Contact Assignments
--------------------------------	-------------------------

				Out of Reset Condition ¹				
Ball Name	Ball	Power Group	Ball Type	Default Mode (Reset Mode)	Default Function (Signal Name)	Input/Output	Value ²	
BOOT_MODE0	C12	VDD_SNVS_IN	GPIO	ALT0	SRC_BOOT_MODE0	Input	PD (100K)	
BOOT_MODE1	F12	VDD_SNVS_IN	GPIO	ALT0	SRC_BOOT_MODE1	Input	PD (100K)	
CLK1_N	C7	VDD_HIGH_CAP	—	_	CLK1_N	—	—	
CLK1_P	D7	VDD_HIGH_CAP	—	—	CLK1_P	—	—	
CLK2_N	C5	VDD_HIGH_CAP	—	—	CLK2_N	—	—	
CLK2_P	D5	VDD_HIGH_CAP	—	—	CLK2_P	—	—	
CSI_CLK0M	F4	NVCC_MIPI	—	_	CSI_CLK_N	—	—	
CSI_CLK0P	F3	NVCC_MIPI	—	_	CSI_CLK_P	—	—	
CSI_D0M	E4	NVCC_MIPI	—	_	CSI_DATA0_N	—	—	
CSI_D0P	E3	NVCC_MIPI	—	_	CSI_DATA0_P	—	—	
CSI_D1M	D1	NVCC_MIPI	—	_	CSI_DATA1_N	—	—	
CSI_D1P	D2	NVCC_MIPI	—	—	CSI_DATA1_P	—	—	
CSI_D2M	E1	NVCC_MIPI	—	—	CSI_DATA2_N	—	—	
CSI_D2P	E2	NVCC_MIPI	—	—	CSI_DATA2_P		—	
CSI_D3M	F2	NVCC_MIPI	_	—	CSI_DATA3_N		—	

				Out of Reset Condition ¹			
Ball Name	Ball	Power Group	Ball Type	Default Mode (Reset Mode)	Default Function (Signal Name)	Input/Output	Value ²
DRAM_D11	AE7	NVCC_DRAM	DDR	ALT0	DRAM_DATA11	Input	PU (100K)
DRAM_D12	AB5	NVCC_DRAM	DDR	ALT0	DRAM_DATA12	Input	PU (100K)
DRAM_D13	AC5	NVCC_DRAM	DDR	ALT0	DRAM_DATA13	Input	PU (100K)
DRAM_D14	AB6	NVCC_DRAM	DDR	ALT0	DRAM_DATA14	Input	PU (100K)
DRAM_D15	AC7	NVCC_DRAM	DDR	ALT0	DRAM_DATA15	Input	PU (100K)
DRAM_D16	AB7	NVCC_DRAM	DDR	ALT0	DRAM_DATA16	Input	PU (100K)
DRAM_D17	AA8	NVCC_DRAM	DDR	ALT0	DRAM_DATA17	Input	PU (100K)
DRAM_D18	AB9	NVCC_DRAM	DDR	ALT0	DRAM_DATA18	Input	PU (100K)
DRAM_D19	Y9	NVCC_DRAM	DDR	ALT0	DRAM_DATA19	Input	PU (100K)
DRAM_D2	AC4	NVCC_DRAM	DDR	ALT0	DRAM_DATA02	Input	PU (100K)
DRAM_D20	Y7	NVCC_DRAM	DDR	ALT0	DRAM_DATA20	Input	PU (100K)
DRAM_D21	Y8	NVCC_DRAM	DDR	ALT0	DRAM_DATA21	Input	PU (100K)
DRAM_D22	AC8	NVCC_DRAM	DDR	ALT0	DRAM_DATA22	Input	PU (100K)
DRAM_D23	AA9	NVCC_DRAM	DDR	ALT0	DRAM_DATA23	Input	PU (100K)
DRAM_D24	AE9	NVCC_DRAM	DDR	ALT0	DRAM_DATA24	Input	PU (100K)
DRAM_D25	Y10	NVCC_DRAM	DDR	ALT0	DRAM_DATA25	Input	PU (100K)
DRAM_D26	AE11	NVCC_DRAM	DDR	ALT0	DRAM_DATA26	Input	PU (100K)
DRAM_D27	AB11	NVCC_DRAM	DDR	ALT0	DRAM_DATA27	Input	PU (100K)
DRAM_D28	AC9	NVCC_DRAM	DDR	ALT0	DRAM_DATA28	Input	PU (100K)
DRAM_D29	AD9	NVCC_DRAM	DDR	ALT0	DRAM_DATA29	Input	PU (100K)
DRAM_D3	AA5	NVCC_DRAM	DDR	ALT0	DRAM_DATA03	Input	PU (100K)
DRAM_D30	AD11	NVCC_DRAM	DDR	ALT0	DRAM_DATA30	Input	PU (100K)
DRAM_D31	AC11	NVCC_DRAM	DDR	ALT0	DRAM_DATA31	Input	PU (100K)
DRAM_D32	AA17	NVCC_DRAM	DDR	ALT0	DRAM_DATA32	Input	PU (100K)
DRAM_D33	AA18	NVCC_DRAM	DDR	ALT0	DRAM_DATA33	Input	PU (100K)
DRAM_D34	AC18	NVCC_DRAM	DDR	ALT0	DRAM_DATA34	Input	PU (100K)
DRAM_D35	AE19	NVCC_DRAM	DDR	ALT0	DRAM_DATA35	Input	PU (100K)
DRAM_D36	Y17	NVCC_DRAM	DDR	ALT0	DRAM_DATA36	Input	PU (100K)
DRAM_D37	Y18	NVCC_DRAM	DDR	ALT0	DRAM_DATA37	Input	PU (100K)
DRAM_D38	AB19	NVCC_DRAM	DDR	ALT0	DRAM_DATA38	Input	PU (100K)
DRAM_D39	AC19	NVCC_DRAM	DDR	ALT0	DRAM_DATA39	Input	PU (100K)
DRAM_D4	AC1	NVCC_DRAM	DDR	ALT0	DRAM_DATA04	Input	PU (100K)
DRAM_D40	Y19	NVCC_DRAM	DDR	ALT0	DRAM_DATA40	Input	PU (100K)
DRAM_D41	AB20	NVCC_DRAM	DDR	ALT0	DRAM_DATA41	Input	PU (100K)
DRAM_D42	AB21	NVCC_DRAM	DDR	ALT0	DRAM_DATA42	Input	PU (100K)
DRAM_D43	AD21	NVCC_DRAM	DDR	ALT0	DRAM_DATA43	Input	PU (100K)

Table 100. 21 x 21 mm Functional Contact Assignments (continued)

				Out of Reset Condition ¹			
Ball Name	Ball	Power Group	Ball Type	Default Mode (Reset Mode)	Default Function (Signal Name)	Input/Output	Value ²
EIM_DA10	M22	NVCC_EIM2	GPIO	ALT0	EIM_AD10	Input	PU (100K)
EIM_DA11	M20	NVCC_EIM2	GPIO	ALT0	EIM_AD11	Input	PU (100K)
EIM_DA12	M24	NVCC_EIM2	GPIO	ALT0	EIM_AD12	Input	PU (100K)
EIM_DA13	M23	NVCC_EIM2	GPIO	ALT0	EIM_AD13	Input	PU (100K)
EIM_DA14	N23	NVCC_EIM2	GPIO	ALT0	EIM_AD14	Input	PU (100K)
EIM_DA15	N24	NVCC_EIM2	GPIO	ALT0	EIM_AD15	Input	PU (100K)
EIM_EB0	K21	NVCC_EIM2	GPIO	ALT0	EIM_EB0_B	Output	1
EIM_EB1	K23	NVCC_EIM2	GPIO	ALT0	EIM_EB1_B	Output	1
EIM_EB2	E22	NVCC_EIM0	GPIO	ALT5	GPIO2_IO30	Input	PU (100K)
EIM_EB3	F23	NVCC_EIM0	GPIO	ALT5	GPIO2_IO31	Input	PU (100K)
EIM_LBA	K22	NVCC_EIM1	GPIO	ALT0	EIM_LBA_B	Output	1
EIM_OE	J24	NVCC_EIM1	GPIO	ALT0	EIM_OE	Output	1
EIM_RW	K20	NVCC_EIM1	GPIO	ALT0	EIM_RW	Output	1
EIM_WAIT	M25	NVCC_EIM2	GPIO	ALT0	EIM_WAIT	Input	PU (100K)
ENET_CRS_DV	U21	NVCC_ENET	GPIO	ALT5	GPIO1_IO25	Input	PU (100K)
ENET_MDC	V20	NVCC_ENET	GPIO	ALT5	GPIO1_IO31	Input	PU (100K)
ENET_MDIO	V23	NVCC_ENET	GPIO	ALT5	GPIO1_IO22	Input	PU (100K)
ENET_REF_CLK ³	V22	NVCC_ENET	GPIO	ALT5	GPIO1_IO23	Input	PU (100K)
ENET_RX_ER	W23	NVCC_ENET	GPIO	ALT5	GPIO1_IO24	Input	PU (100K)
ENET_RXD0	W21	NVCC_ENET	GPIO	ALT5	GPI01_I027	Input	PU (100K)
ENET_RXD1	W22	NVCC_ENET	GPIO	ALT5	GPIO1_IO26	Input	PU (100K)
ENET_TX_EN	V21	NVCC_ENET	GPIO	ALT5	GPIO1_IO28	Input	PU (100K)
ENET_TXD0	U20	NVCC_ENET	GPIO	ALT5	GPIO1_IO30	Input	PU (100K)
ENET_TXD1	W20	NVCC_ENET	GPIO	ALT5	GPIO1_IO29	Input	PU (100K)
GPIO_0	T5	NVCC_GPIO	GPIO	ALT5	GPIO1_IO00	Input	PD (100K)
GPIO_1	T4	NVCC_GPIO	GPIO	ALT5	GPIO1_IO01	Input	PU (100K)
GPIO_16	R2	NVCC_GPIO	GPIO	ALT5	GPI07_I011	Input	PU (100K)
GPIO_17	R1	NVCC_GPIO	GPIO	ALT5	GPI07_I012	Input	PU (100K)
GPIO_18	P6	NVCC_GPIO	GPIO	ALT5	GPIO7_IO13	Input	PU (100K)
GPIO_19	P5	NVCC_GPIO	GPIO	ALT5	GPIO4_IO05	Input	PU (100K)
GPIO_2	T1	NVCC_GPIO	GPIO	ALT5	GPIO1_IO02	Input	PU (100K)
GPIO_3	R7	NVCC_GPIO	GPIO	ALT5	GPIO1_IO03	Input	PU (100K)
GPIO_4	R6	NVCC_GPIO	GPIO	ALT5	GPIO1_IO04	Input	PU (100K)
GPIO_5	R4	NVCC_GPIO	GPIO	ALT5	GPIO1_IO05	Input	PU (100K)
GPIO_6	Т3	NVCC_GPIO	GPIO	ALT5	GPIO1_IO06	Input	PU (100K)
GPIO_7	R3	NVCC_GPIO	GPIO	ALT5	GPIO1_IO07	Input	PU (100K)

Table 100. 21 x 21 mm Functional Contact Assignments (continued)

					Out of Reset Cor	ndition ¹	
Ball Name	Ball	Power Group	Ball Type	Default Mode (Reset Mode)	Default Function (Signal Name)	Input/Output	Value ²
LVDS0_TX3_P	W1	NVCC_LVDS_2P5	LVDS	ALT0	LVDS0_TX3_P	Input	Keeper
LVDS1_CLK_N	Y3	NVCC_LVDS_2P5	LVDS	_	LVDS1_CLK_N	—	_
LVDS1_CLK_P	Y4	NVCC_LVDS_2P5	LVDS	ALT0	LVDS1_CLK_P	Input	Keeper
LVDS1_TX0_N	Y1	NVCC_LVDS_2P5	LVDS	—	LVDS1_TX0_N	—	—
LVDS1_TX0_P	Y2	NVCC_LVDS_2P5	LVDS	ALT0	LVDS1_TX0_P	Input	Keeper
LVDS1_TX1_N	AA2	NVCC_LVDS_2P5	LVDS	_	LVDS1_TX1_N	—	_
LVDS1_TX1_P	AA1	NVCC_LVDS_2P5	LVDS	ALT0	LVDS1_TX1_P	Input	Keeper
LVDS1_TX2_N	AB1	NVCC_LVDS_2P5	LVDS	—	LVDS1_TX2_N	—	—
LVDS1_TX2_P	AB2	NVCC_LVDS_2P5	LVDS	ALT0	LVDS1_TX2_P	Input	Keeper
LVDS1_TX3_N	AA3	NVCC_LVDS_2P5	LVDS	—	LVDS1_TX3_N	—	—
LVDS1_TX3_P	AA4	NVCC_LVDS_2P5	LVDS	ALT0	LVDS1_TX3_P	Input	Keeper
MLB_CN	A11	VDD_HIGH_CAP	LVDS	—	MLB_CLK_N	—	—
MLB_CP	B11	VDD_HIGH_CAP	LVDS	—	MLB_CLK_P	—	—
MLB_DN	B10	VDD_HIGH_CAP	LVDS	—	MLB_DATA_N	—	—
MLB_DP	A10	VDD_HIGH_CAP	LVDS	—	MLB_DATA_P	—	—
MLB_SN	A9	VDD_HIGH_CAP	LVDS	—	MLB_SIG_N	—	—
MLB_SP	B9	VDD_HIGH_CAP	LVDS	—	MLB_SIG_P	_	
NANDF_ALE	A16	NVCC_NANDF	GPIO	ALT5	GPIO6_IO08	Input	PU (100K)
NANDF_CLE	C15	NVCC_NANDF	GPIO	ALT5	GPIO6_I007	Input	PU (100K)
NANDF_CS0	F15	NVCC_NANDF	GPIO	ALT5	GPIO6_IO11	Input	PU (100K)
NANDF_CS1	C16	NVCC_NANDF	GPIO	ALT5	GPIO6_IO14	Input	PU (100K)
NANDF_CS2	A17	NVCC_NANDF	GPIO	ALT5	GPIO6_IO15	Input	PU (100K)
NANDF_CS3	D16	NVCC_NANDF	GPIO	ALT5	GPIO6_IO16	Input	PU (100K)
NANDF_D0	A18	NVCC_NANDF	GPIO	ALT5	GPIO2_IO00	Input	PU (100K)
NANDF_D1	C17	NVCC_NANDF	GPIO	ALT5	GPIO2_IO01	Input	PU (100K)
NANDF_D2	F16	NVCC_NANDF	GPIO	ALT5	GPIO2_IO02	Input	PU (100K)
NANDF_D3	D17	NVCC_NANDF	GPIO	ALT5	GPIO2_IO03	Input	PU (100K)
NANDF_D4	A19	NVCC_NANDF	GPIO	ALT5	GPIO2_IO04	Input	PU (100K)
NANDF_D5	B18	NVCC_NANDF	GPIO	ALT5	GPIO2_IO05	Input	PU (100K)
NANDF_D6	E17	NVCC_NANDF	GPIO	ALT5	GPIO2_IO06	Input	PU (100K)
NANDF_D7	C18	NVCC_NANDF	GPIO	ALT5	GPIO2_I007	Input	PU (100K)
NANDF_RB0	B16	NVCC_NANDF	GPIO	ALT5	GPIO6_IO10	Input	PU (100K)
NANDF_WP_B	E15	NVCC_NANDF	GPIO	ALT5	GPIO6_IO09	Input	PU (100K)
ONOFF	D12	VDD_SNVS_IN	GPIO	—	SRC_ONOFF	Input	PU (100K)
PCIE_RXM	B1	PCIE_VPH	—	—	PCIE_RX_N	_	—
PCIE_RXP	B2	PCIE_VPH	—	—	PCIE_RX_P	—	

Table 100. 21 x 21 mm Functional Contact Assignments (continued)