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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	Coldfire V2
Core Size	32-Bit Single-Core
Speed	166.67MHz
Connectivity	EBI/EMI, I²C, SPI, UART/USART
Peripherals	DMA, WDT
Number of I/O	30
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.4V ~ 3.6V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mcf5207cag166

1 MCF5207/8 Device Configurations

The following table compares the two devices described in this document:

Table 1. MCF5207 & MCF5208 Configurations

Module	MCF5207	MCF5208
Version 2 ColdFire Core with EMAC (Enhanced Multiply-Accumulate Unit)	•	•
Core (System) Clock	up to 166.67 MHz	
Peripheral and External Bus Clock (Core clock ÷ 2)	up to 83.33 MHz	
Performance (Dhrystone/2.1 MIPS)	up to 159	
Instruction/Data Cache	8 Kbytes	
Static RAM (SRAM)	16 Kbytes	
SDR/DDR SDRAM Controller	•	•
Fast Ethernet Controller (FEC)	—	•
Low-Power Management Module	•	•
UARTs	3	3
I^2C	•	•
QSPI	•	•
32-bit DMA Timers	4	4
Watchdog Timer (WDT)	•	•
Periodic Interrupt Timers (PIT)	4	4
Edge Port Module (EPORT)	•	•
Interrupt Controllers (INTC)	1	1
16-channel Direct Memory Access (DMA)	•	•
FlexBus External Interface	•	•
General Purpose I/O Module (GPIO)	•	•
JTAG - IEEE® 1149.1 Test Access Port	•	•
Package	144 LQFP 144 MAPBGA	160 QFP 196 MAPBGA

2 Ordering Information

Table 2. Orderable Part Numbers

Freescale Part Number	Description	Speed	Temperature
MCF5207CAG166	MCF5207 RISC Microprocessor, 144 LQFP	166.67 MHz	–40° to +85° C
MCF5207CVM166	MCF5207 RISC Microprocessor, 144 MAPBGA	166.67 MHz	–40° to +85° C
MCF5208CAB166	MCF5208 RISC Microprocessor, 160 QFP	166.67 MHz	–40° to +85° C
MCF5208CVM166	MCF5208 RISC Microprocessor, 196 MAPBGA	166.67 MHz	–40° to +85° C

3 Signal Descriptions

The following table lists all the MCF5208 pins grouped by function. The Dir column is the direction for the primary function of the pin only. Refer to Section 4, "Mechanicals and Pinouts" for package diagrams. For a more detailed discussion of the MCF5208 signals, consult the *MCF5208 Reference Manual* (MCF5208RM).

NOTE

In this table and throughout this document, a single signal within a group is designated without square brackets (i.e., A23), while designations for multiple signals within a group use brackets (i.e., A[23:21]) and is meant to include all signals within the two bracketed numbers when these numbers are separated by a colon.

NOTE

The primary functionality of a pin is not necessarily its default functionality. Pins that are muxed with GPIO default to their GPIO functionality.

Table 3. MCF5207/8 Signal Information and Muxing

Signal Name	GPIO	Alternate 1	Alternate 2	Dir.[1]	Voltage Domain	MCF5207 144 LQFP	MCF5207 144 MAPBGA	MCF5208 160 QFP	MCF5208 196 MAPBGA
Reset									
$\overline{\text{RESET}}$[2]	—	—	—	I	EVDD	82	J10	90	J14
$\overline{\text{RSTOUT}}$	—	—	—	O	EVDD	74	M12	82	N14
Clock									
EXTAL	—	—	—	I	EVDD	78	K12	86	L14
XTAL	—	—	—	O	EVDD	80	J12	88	K14
FB_CLK	—	—	—	O	SDVDD	34	L1	40	N1
Mode Selection									
$\overline{\text{RCON}}$[2]	—	—	—	I	EVDD	144	C4	160	C3
DRAMSEL	—	—	—	I	EVDD	79	H10	87	K11
FlexBus									
A[23:22]	—	$\overline{\text{FB\_CS}}$[5:4]	—	O	SDVDD	118, 117	B9, A10	126, 125	B11, A11
A[21:16]	—	—	—	O	SDVDD	116–114, 112, 108, 107	C9, A11, B10, A12, C11, B11	124, 123, 122, 120, 116, 115	B12, A12, A13, B13, B14, C13
A[15:14]	—	SD_BA[1:0][3]	—	O	SDVDD	106, 105	B12, C12	114, 113	C14, D12
A[13:11]	—	SD_A[13:11][3]	—	O	SDVDD	104–102	D11, E10, D12	112, 111, 110	D13, D14, E11
A10	—	—	—	O	SDVDD	101	C10	109	E12

Table 3. MCF5207/8 Signal Information and Muxing (continued)

Signal Name	GPIO	Alternate 1	Alternate 2	Dir.[1]	Voltage Domain	MCF5207 144 LQFP	MCF5207 144 MAPBGA	MCF5208 160 QFP	MCF5208 196 MAPBGA
A[9:0]	—	SD_A[9:0][3]	—	O	SDVDD	100–91	E11, D9, E12, F10, F11, E9, F12, G10, G12, F9	108–99	E13, E14, F11–F14, G11–G14
D[31:16]	—	SD_D[31:16][4]	—	I/O	SDVDD	21–28, 40–47	F1, F2, G1, G2, G4, G3, H1, H2, K3, L2, L3, K2, M3, J4, M4, K4	27–34, 46–53	J4–J1, K4–K1, M3, N3, M4, N4, P4, L5, M5, N5
D[15:0]	—	FB_D[31:16][4]	—	I/O	SDVDD	8–15, 51–58	B2, B1, C2, C1, D2, D1, E2, E1, L5, K5, L6, J6, M6, J7, L7, K7	16–23, 57–64	F3–F1, G4–G1, H1, N6, P6, L7, M7, N7, P7, N8, P8
$\overline{\text{BE/BWE}}$[3:0]	PBE[3:0]	$\overline{\text{SD\_DQM}}$[3:0][3]	—	O	SDVDD	20, 48, 18, 50	F4, L4, E3, J5	26, 54, 24, 56	H2, P5, H4, M6
$\overline{\text{OE}}$	PBUSCTL3	—	—	O	SDVDD	60	J8	66	M8
$\overline{\text{TA}}$[2]	PBUSCTL2	—	—	I	SDVDD	90	G11	98	H14
R/$\overline{\text{W}}$	PBUSCTL1	—	—	O	SDVDD	59	K6	65	L8
$\overline{\text{TS}}$	PBUSCTL0	$\overline{\text{DACK0}}$	—	O	SDVDD	4	B3	12	E3
Chip Selects									
$\overline{\text{FB\_CS}}$[3:2]	PCS[3:2]	—	—	O	SDVDD	119, 120	D7, A9	—	C11, A10
$\overline{\text{FB\_CS1}}$	PCS1	$\overline{\text{SD\_CS1}}$	—	O	SDVDD	121	C8	127	B10
$\overline{\text{FB\_CS0}}$	—	—	—	O	SDVDD	122	B8	128	C10
SDRAM Controller									
SD_A10	—	—	—	O	SDVDD	37	M1	43	N2
SD_CKE	—	—	—	O	SDVDD	6	C3	14	E1
SD_CLK	—	—	—	O	SDVDD	31	J1	37	L1
$\overline{\text{SD\_CLK}}$	—	—	—	O	SDVDD	32	K1	38	M1
$\overline{\text{SD\_CS0}}$	—	—	—	O	SDVDD	7	A1	15	F4
SD_DQS[3:2]	—	—	—	O	SDVDD	19, 49	F3, M5	25, 55	H3, L6
$\overline{\text{SD\_SCAS}}$	—	—	—	O	SDVDD	38	M2	44	P2
$\overline{\text{SD\_SRAS}}$	—	—	—	O	SDVDD	39	J2	45	P3
SD_SDR_DQS	—	—	—	O	SDVDD	29	H3	35	L3
$\overline{\text{SD\_WE}}$	—	—	—	O	SDVDD	5	D3	13	E2

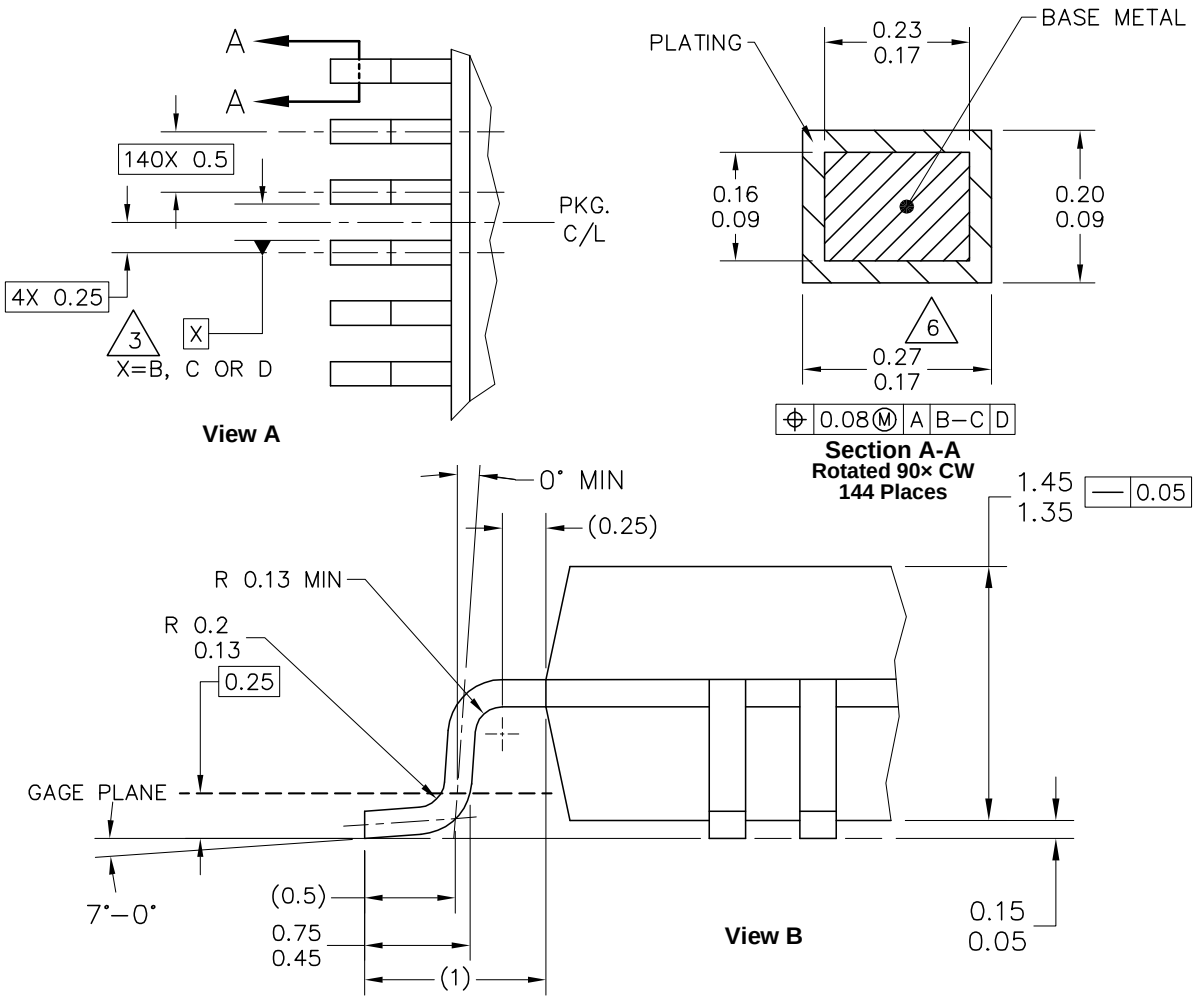
Table 3. MCF5207/8 Signal Information and Muxing (continued)

Signal Name	GPIO	Alternate 1	Alternate 2	Dir.[1]	Voltage Domain	MCF5207 144 LQFP	MCF5207 144 MAPBGA	MCF5208 160 QFP	MCF5208 196 MAPBGA
QSPI									
QSPI_CS2	PQSPI3	$\overline{\text{DACK0}}$	$\overline{\text{U2RTS}}$	O	EVDD	126	A8	132	D10
QSPI_CLK	PQSPI0	I2C_SCL[2]	—	O	EVDD	127	C7	133	A9
QSPI_DOUT	PQSPI1	I2C_SDA[2]	—	O	EVDD	128	A7	134	B9
QSPI_DIN	PQSPI2	$\overline{\text{DREQ0}}$[2]	$\overline{\text{U2CTS}}$	I	EVDD	129	B7	135	C9
Note: The QSPI_CS1 and QSPI_CS0 signals are available on the $\overline{\text{U1CTS}}$, $\overline{\text{U1RTS}}$, $\overline{\text{U0CTS}}$, or $\overline{\text{U0RTS}}$ pins for the 196 and 160-pin packages.									
UARTs									
$\overline{\text{U1CTS}}$	PUARTL7	DT1IN	QSPI_CS1	I	EVDD	—	—	136	D9
$\overline{\text{U1RTS}}$	PUARTL6	DT1OUT	QSPI_CS1	O	EVDD	—	—	137	C8
U1TXD	PUARTL5	—	—	O	EVDD	131	A6	139	A8
U1RXD	PUARTL4	—	—	I	EVDD	130	D6	138	B8
$\overline{\text{U0CTS}}$	PUARTL3	DT0IN	QSPI_CS0	I	EVDD	—	—	76	N12
$\overline{\text{U0RTS}}$	PUARTL2	DT0OUT	QSPI_CS0	O	EVDD	—	—	77	P12
U0TXD	PUARTL1	—	—	O	EVDD	71	L10	79	P13
U0RXD	PUARTL0	—	—	I	EVDD	70	M10	78	N13
Note: The UART2 signals are multiplexed on the DMA Timers, QSPI, FEC, and I2C pins. For the MCF5207 devices, the UART0 and UART1 control signals are multiplexed internally on the FEC signals.									
DMA Timers									
DT3IN	PTIMER3	DT3OUT	$\overline{\text{U2CTS}}$	I	EVDD	135	B5	143	B7
DT2IN	PTIMER2	DT2OUT	$\overline{\text{U2RTS}}$	I	EVDD	136	C5	144	A7
DT1IN	PTIMER1	DT1OUT	U2RXD	I	EVDD	137	A4	145	A6
DT0IN	PTIMER0	DT0OUT	U2TXD	I	EVDD	138	A3	146	B6
BDM/JTAG[6]									
JTAG_EN[7]	—	—	—	I	EVDD	83	J11	91	J13
DSCLK	—	$\overline{\text{TRST}}$[2]	—	I	EVDD	76	K11	84	L12
PSTCLK	—	TCLK[2]	—	O	EVDD	64	M7	70	P9
$\overline{\text{BKPT}}$	—	TMS[2]	—	I	EVDD	75	L12	83	M14
DSI	—	TDI[2]	—	I	EVDD	77	H9	85	K12
DSO	—	TDO	—	O	EVDD	69	M9	75	M12
DDATA[3:0]	—	—	—	O	EVDD	—	K9, L9, M11, M8	—	P11, N11, M11, P10
PST[3:0]	—	—	—	O	EVDD	—	L11, L8, K10, K8	—	N10, M10, L10, L9

Table 3. MCF5207/8 Signal Information and Muxing (continued)

Signal Name	GPIO	Alternate 1	Alternate 2	Dir.[1]	Voltage Domain	MCF5207 144 LQFP	MCF5207 144 MAPBGA	MCF5208 160 QFP	MCF5208 196 MAPBGA
ALLPST	—	—	—	O	EVDD	67	—	73	—
Test									
TEST[7]	—	—	—	I	EVDD	109	—	—	C12
PLL_TEST	—	—	—	I	EVDD	—	—	—	M13
Power Supplies									
EVDD	—	—	—	—	—	1, 33, 63, 66, 72, 81, 87, 125	E5–E6, F5, G8–G9, H7–H8	2, 9, 69, 72, 80, 89, 95, 131	E5–E7, F5, F6, G5, H10, J9, J10, K8–K10, K13, M9
IVDD	—	—	—	—	—	30, 68, 84, 113, 143	D4, D8, H4, H11, J9	36, 74, 92, 121, 159	J12, D4, D11, H11, L4, L11,
PLL_VDD	—	—	—	—	—	86	H12	94	H13
SD_VDD	—	—	—	—	—	3, 17, 35, 61, 89, 110, 123	E7–E8, F8, G5, H5–H6, J3	11, 39, 41, 67, 97, 118, 129	E8–E10, F9, F10, G10, H5, J5, J6, K5–K7, L2
VSS	—	—	—	—	—	2, 16, 36, 62, 65, 73, 88, 111, 124	D10, F6–F7, G6–G7	1, 10, 42, 68, 71, 81, 96, 117, 119, 130	A1, A14, F7–F8, G6–G9, H6–H9, J7–J8, L13, M2, N9, P1, P14
PLL_VSS	—	—	—	—	—	85	—	93	H12

NOTES:
1 Refers to pin's primary function.
2 Pull-up enabled internally on this signal for this mode.
3 The SDRAM functions of these signals are not programmable by the user. They are dynamically switched by the processor when accessing SDRAM memory space and are included here for completeness.
4 Primary functionality selected by asserting the DRAMSEL signal (SDR mode). Alternate functionality selected by negating the DRAMSEL signal (DDR mode). The GPIO module is not responsible for assigning these pins.
5 GPIO functionality is determined by the edge port module. The GPIO module is only responsible for assigning the alternate functions.
6 If JTAG_EN is asserted, these pins default to Alternate 1 (JTAG) functionality. The GPIO module is not responsible for assigning these pins.
7 Pull-down enabled internally on this signal for this mode.



NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.

2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.

3. DATUMS B, C AND D TO BE DETERMINED AT DATUM PLANE H.

4. THE TOP PACKAGE BODY SIZE MAY BE SMALLER THAN THE BOTTOM PACKAGE SIZE BY A MAXIMUM OF 0.1 mm.

5. THIS DIMENSIONS DO NOT INCLUDE MOLD PROTRUSIONS. THE MAXIMUM ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. THIS DIMENSIONS ARE MAXIMUM BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.

6. THIS DIMENSION DOES NOT INCLUDE DAM BAR PROTRUSION. PROTRUSIONS SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.35. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD SHALL BE 0.07 MM.

7. THIS DIMENSIONS ARE DETERMINED AT THE SEATING PLANE, DATUM A.

Figure 3. MCF5207CAB166 Package Dimensions (Sheet 2 of 2)

4.5 Pinout—160 QFP

Figure 6 shows a pinout of the MCF5208CAB166 device.

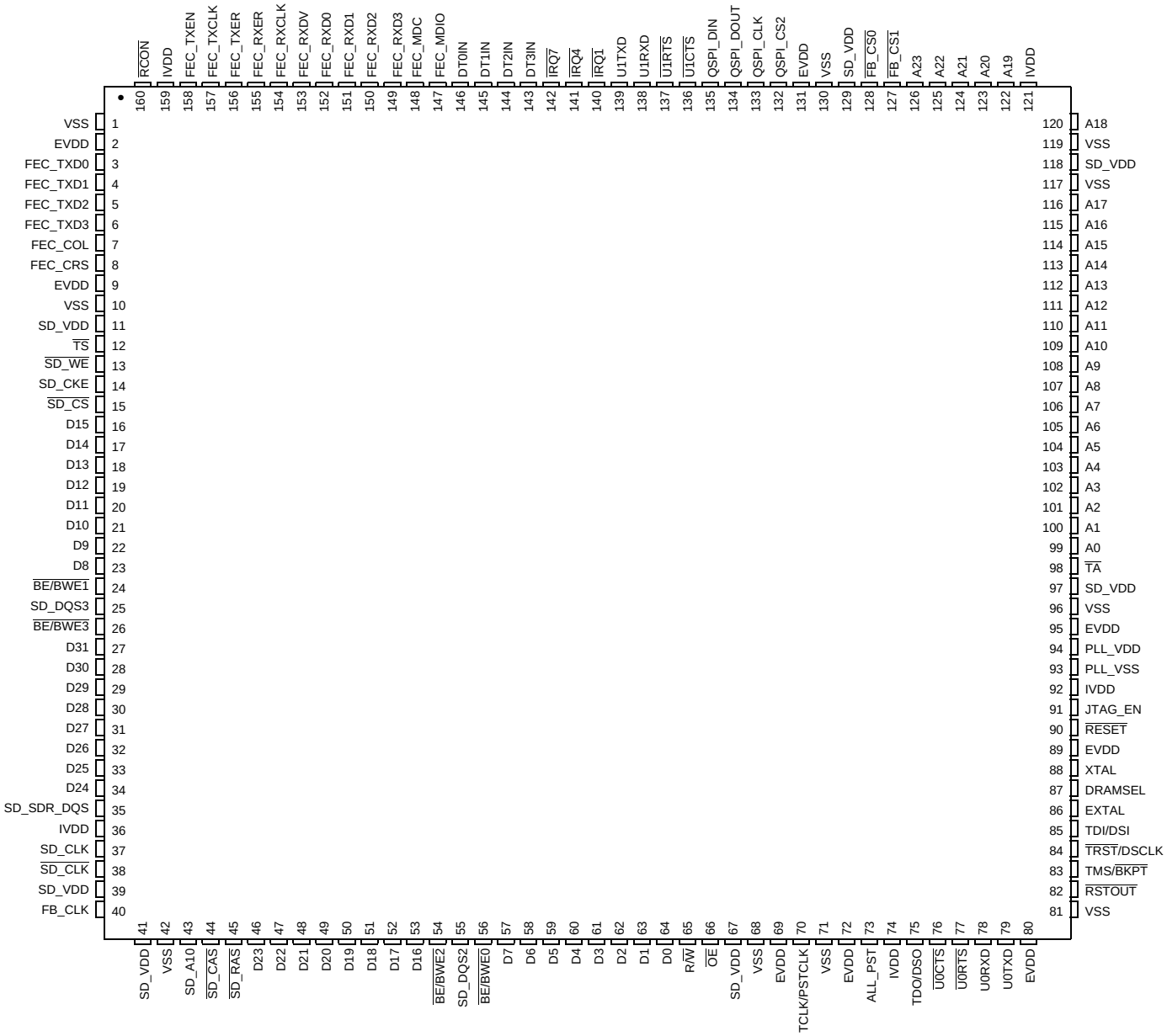


Figure 6. MCF5208CAB166 Pinout Top View (160 QFP)

4.6 Package Dimensions—160 QFP

The package dimensions of the MCF5208CAB166 device are shown in the figures below.

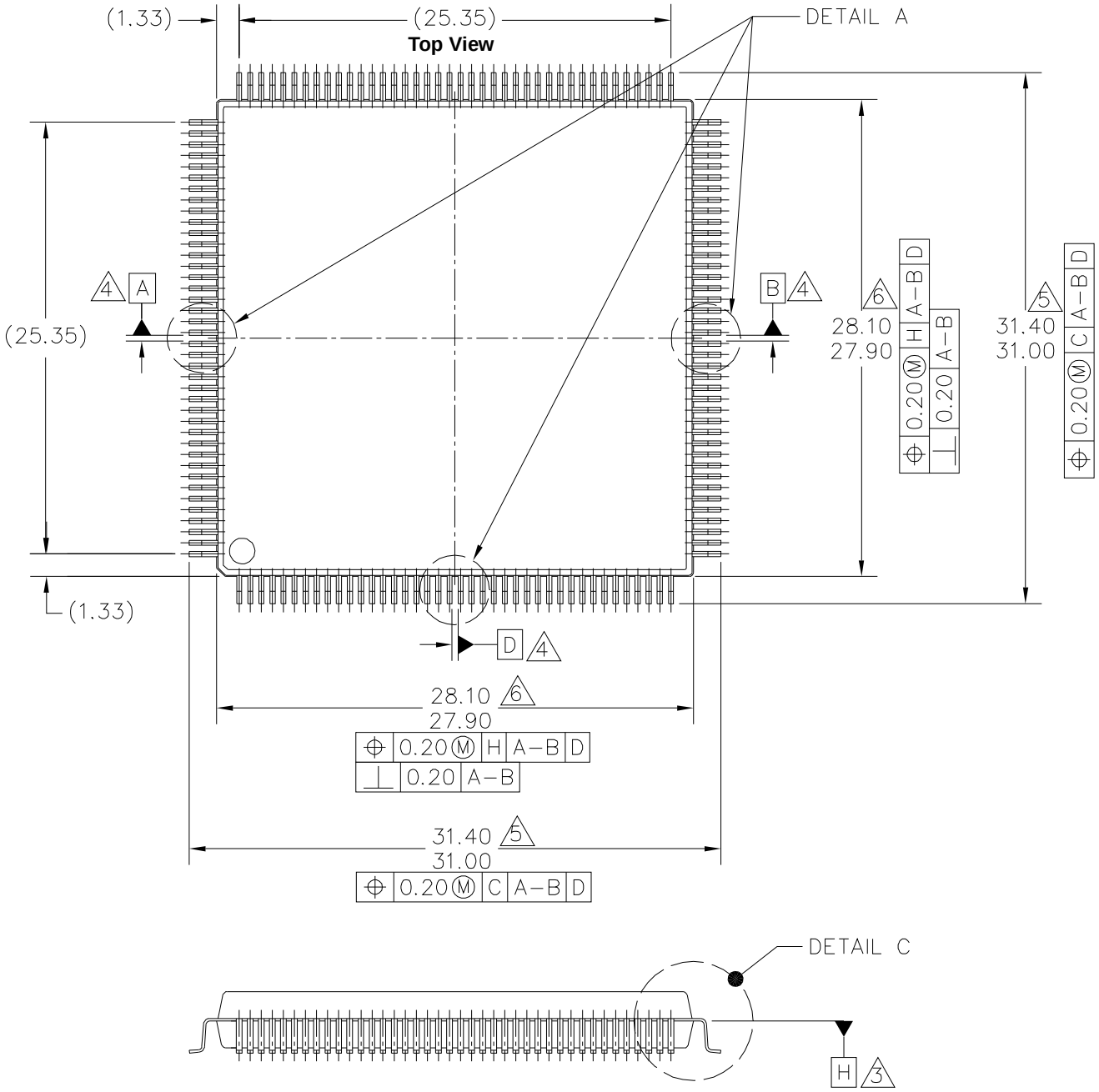


Figure 7. MCF5208CAB166 Package Dimensions (Sheet 1 of 2)

4.7 Pinout—196 MAPBGA

Figure 9 shows a pinout of the MCF5208CVM166 device.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	
A	VSS	FEC_ TXEN	FEC_ TXER	FEC_ RXDV	FEC_ RXD3	DT1IN	DT2IN	U1TXD	QSPI_ CLK	FB_CS2	A22	A20	A19	VSS	A
B	FEC_ TXD0	FEC_ TXD1	FEC_ TXCLK	FEC_ RXCLK	FEC_ RXD2	DT0IN	DT3IN	U1RXD	QSPI_ DOUT	FB_CS1	A23	A21	A18	A17	B
C	FEC_ TXD3	FEC_ TXD2	RCON	FEC_ RXER	FEC_ RXD1	FEC_ MDIO	IRQ7	U1RTS	QSPI_ DIN	FB_CS0	FB_CS3	TEST	A16	A15	C
D	I2C_SDA	FEC_ CRS	FEC_ COL	IVDD	FEC_ RXD0	FEC_ MDC	IRQ4	IRQ1	U1CTS	QSPI_ CS2	IVDD	A14	A13	A12	D
E	SD_CKE	SD_WE	TS	I2C_SCL	EVDD	EVDD	EVDD	SD_VDD	SD_VDD	SD_VDD	A11	A10	A9	A8	E
F	D13	D14	D15	SD_CS	EVDD	EVDD	VSS	VSS	SD_VDD	SD_VDD	A7	A6	A5	A4	F
G	D9	D10	D11	D12	EVDD	VSS	VSS	VSS	VSS	SD_VDD	A3	A2	A1	A0	G
H	D8	BE/ BWE3	SD_ DQS3	BE/ BWE1	SD_VDD	VSS	VSS	VSS	VSS	EVDD	IVDD	PLL_ VSS	PLL_ VDD	TA	H
J	D28	D29	D30	D31	SD_VDD	SD_VDD	VSS	VSS	EVDD	EVDD	NC	IVDD	JTAG_ EN	RESET	J
K	D24	D25	D26	D27	SD_VDD	SD_VDD	SD_VDD	EVDD	EVDD	EVDD	DRAM SEL	TDI/ DSI	EVDD	XTAL	K
L	SD_CLK	SD_VDD	SD_SDR _DQS	IVDD	D18	SD_ DQS2	D5	R/W	PST0	PST1	IVDD	TRST/ DSCLK	VSS	EXTAL	L
M	SD_CLK	VSS	D23	D21	D17	BE/ BWE0	D4	OE	EVDD	PST2	DDATA1	TDO/ DSO	PLL_ TEST	TMS/ BKPT	M
N	FB_CLK	SD_A10	D22	D20	D16	D7	D3	D1	VSS	PST3	DDATA2	U0CTS	U0RXD	RSTOUT	N
P	VSS	SD_CAS	SD_RAS	D19	BE/ BWE2	D6	D2	D0	TCLK/ PSTCLK	DDATA0	DDATA3	U0RTS	U0TXD	VSS	P
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

Figure 9. MCF5208CVM166 Pinout Top View (196 MAPBGA)

Table 4. Absolute Maximum Ratings[1, 2] (continued)

Operating Temperature Range (Packaged)	T_A (T_L - T_H)	– 40 to 85	°C
Storage Temperature Range	T_{stg}	– 55 to 150	°C

NOTES:
1. Functional operating conditions are given in Section 5.4, "DC Electrical Specifications". Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Continued operation at these levels may affect device reliability or cause permanent damage to the device.
2. This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (V_{SS} or EV_{DD}).
3. Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.
4. All functional non-supply pins are internally clamped to V_{SS} and EV_{DD}.
5. Power supply must maintain regulation within operating EV_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{in} > EV_{DD}$) is greater than I_{DD}, the injection current may flow out of EV_{DD} and could result in external power supply going out of regulation. Ensure external EV_{DD} load shunts current greater than maximum injection current. This is the greatest risk when the MCU is not consuming power (ex; no clock). Power supply must maintain regulation within operating EV_{DD} range during instantaneous and operating maximum current conditions.

5.2 Thermal Characteristics

Table 5 lists thermal resistance values

Table 5. Thermal Characteristics

Characteristic		Symbol	196MBGA	144MBGA	160QFP	144LQFP	Unit
Junction to ambient, natural convection	Four layer board (2s2p)	θ_{JMA}	47[1,2]	47[1,2]	49[1,2]	65[1,2]	°C/W
Junction to ambient (@200 ft/min)	Four layer board (2s2p)	θ_{JMA}	43[1,2]	43[1,2]	44[1,2]	58[1,2]	°C/W
Junction to board		θ_{JB}	36[3]	36[3]	40[3]	50[3]	°C/W
Junction to case		θ_{JC}	22[4]	22[4]	39[4]	19[4]	°C/W
Junction to top of package		Ψ_{jt}	6[1,5]	6[1,5]	12[1,6]	5[1,7]	°C/W
Maximum operating junction temperature		T_j	105	105	105	105	°C

NOTES:
1. θ_{JMA} and Ψ_{jt} parameters are simulated in conformance with EIA/JESD Standard 51-2 for natural convection. Freescale recommends the use of θ_{JmA} and power dissipation specifications in the system design to prevent device junction temperatures from exceeding the rated specification. System designers should be aware that device junction temperatures can be significantly influenced by board layout and surrounding devices. Conformance to the device junction temperature specification can be verified by physical measurement in the customer's system using the Ψ_{jt} parameter, the device power dissipation, and the method described in EIA/JESD Standard 51-2.
2. Per JEDEC JESD51-6 with the board horizontal.

5 See the description of the low-power control register (LCPR) in the *MCF5208 Reference Manual* for more information on stop modes 0–3.

The figure below illustrates the power consumption in a graphical format.

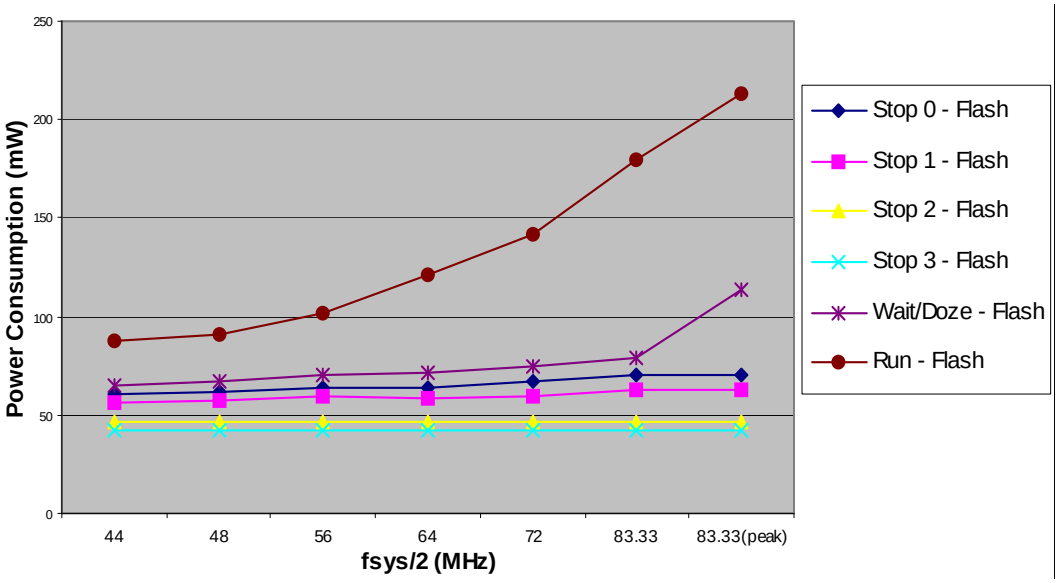


Figure 12. Current Consumption in Low-Power Modes

Table 9. Typical Active Current Consumption Specifications[1]

$f_{sys/2}$ Frequency	Voltage (V)	Typical[2] Active (mA)		Peak[3] Active (mA)
		SRAM	Flash	
1 MHz	3.3	2.04	2.12	2.28
	2.5	15.24	15.32	15.24
	1.5	1.30	1.41	1.49
2 MHz	3.3	2.23	2.40	3.57
	2.5	15.26	15.42	15.26
	1.5	1.71	1.92	2.09
4 MHz	3.3	2.60	2.95	3.58
	2.5	15.30	15.61	15.30
	1.5	2.49	2.95	3.29
44 MHz	3.3	7.61	17.67	25.34
	2.5	16.13	19.49	16.95
	1.5	24.04	28.72	39.02
48 MHz	3.3	8.16	26.21	34.45
	2.5	16.28	20.06	17.17
	1.5	26.05	31.13	42.30

Table 9. Typical Active Current Consumption Specifications[1] (continued)

$f_{sys/2}$ Frequency	Voltage (V)	Typical[2] Active (mA)		Peak[3] Active (mA)
		SRAM	Flash	
56 MHz	3.3	10.09	30.71	38.97
	2.5	16.43	20.71	17.65
	1.5	30.07	35.90	47.90
64 MHz	3.3	15.72	31.37	42.10
	2.5	16.56	21.08	17.95
	1.5	32.19	38.72	53.50
72 MHz	3.3	20.97	31.40	48.80
	2.5	16.87	21.70	18.20
	1.5	35.90	43.20	59.50
83.33 MHz	3.3	31.37	25.83	48.60
	2.5	17.21	22.80	18.83
	1.5	41.10	49.40	67.50

NOTES:
1. All values are measured with a 3.30V EV_{DD}, 2.50V SDV_{DD}, and 1.5V IV_{DD} power supplies. Tests performed at room temperature with pins configured for high drive strength.
2. CPU polling a status register. All peripheral clocks except UART0, FlexBus, INTC, reset controller, PLL, and edge port disabled.
3. Peak current measured while running a while(1) loop with all modules active.

5.6 Oscillator and PLL Electrical Characteristics

Table 10. PLL Electrical Characteristics

Num	Characteristic	Symbol	Min. Value	Max. Value	Unit
1	PLL Reference Frequency Range Crystal reference External reference	 $f_{ref\_crystal}$ f_{ref_ext}	 12 12	 25[1] 40[1]	 MHz MHz
2	Core frequency CLKOUT Frequency[2]	f_{sys} $f_{sys/2}$	488×10^{-6} 244×10^{-6}	166.66 83.33	MHz MHz
3	Crystal Start-up Time[3, 4]	t_{cst}	—	10	ms
4	EXTAL Input High Voltage Crystal Mode[5] All other modes (External, Limp)	 V_{IHEXT} V_{IHEXT}	 V_{XTAL} + 0.4 $E_{VDD}/2$ + 0.4	 — —	 V V
5	EXTAL Input Low Voltage Crystal Mode[5] All other modes (External, Limp)	 V_{ILEXT} V_{ILEXT}	 — —	 V_{XTAL} - 0.4 $E_{VDD}/2$ - 0.4	 V V
7	PLL Lock Time [3, 6]	t_{lpll}	—	50000	CLKIN
8	Duty Cycle of reference [3]	t_{dc}	40	60	%

All other timing relationships can be derived from these values. Timings listed in Table 11 are shown in Figure 14 and Figure 15.

* The timings are also valid for inputs sampled on the negative clock edge.

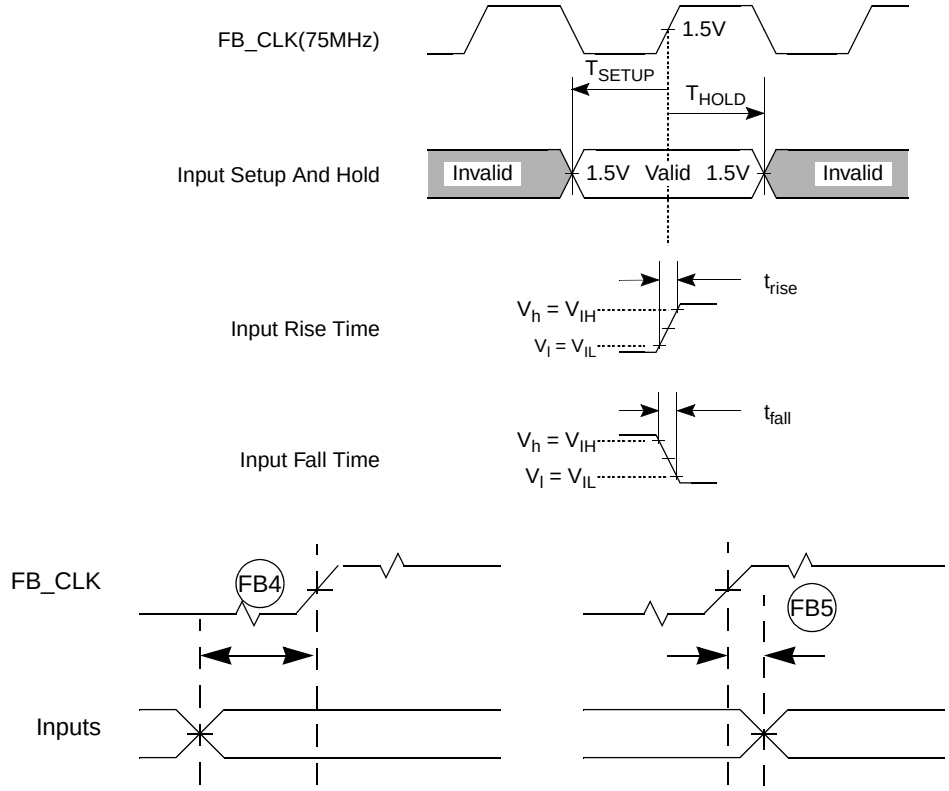


Figure 13. General Input Timing Requirements

5.7.1 FlexBus

FlexBus is a multi-function external bus interface provided to interface to slave-only devices up to a maximum bus frequency of 83.33 MHz. It can be directly connected to asynchronous or synchronous devices such as external boot ROMs, flash memories, gate-array logic, or other simple target (slave) devices with little or no additional circuitry. For asynchronous devices, a simple chip-select based interface can be used. The FlexBus interface has six general purpose chip-selects ($\overline{\text{FB\_CS}}$[5:0]) that can be configured to be distributed between the FlexBus or SDRAM memory interfaces. Chip-select $\overline{\text{FB\_CS}}$[0] can be dedicated to boot ROM access and can be programmed to be byte (8 bits), word (16 bits), or longword (32 bits) wide. Control signal timing is compatible with common ROM/flash memories.

5.8.2 DDR SDRAM AC Timing Characteristics

When using the SDRAM controller in DDR mode, the following timing numbers must be followed to properly latch or drive data onto the memory bus. All timing numbers are relative to the four DQS byte lanes. The following timing numbers are subject to change at anytime, and are only provided to aid in early board design. Please contact your local Freescale representative if questions develop.

Table 13. DDR Timing Specifications

Num	Characteristic	Symbol	Min	Max	Unit	Notes
—	Frequency of Operation	—	60	83.33	Mhz	1
DD1	Clock Period (SD_CLK)	t_{DDCK}	12	16.67	ns	2
DD2	Pulse Width High	t_{DDCKH}	0.45	0.55	SD_CLK	3
DD3	Pulse Width Low	t_{DDCKL}	0.45	0.55	SD_CLK	3
DD4	Address, SD_CKE, $\overline{\text{SD\_CAS}}$, $\overline{\text{SD\_RAS}}$, $\overline{\text{SD\_WE}}$, $\overline{\text{SD\_CS}}$[1:0] - Output Valid	$t_{SDCHACV}$	—	0.5 × SD_CLK + 1.0	ns	4
DD5	Address, SD_CKE, $\overline{\text{SD\_CAS}}$, $\overline{\text{SD\_RAS}}$, $\overline{\text{SD\_WE}}$, $\overline{\text{SD\_CS}}$[1:0] - Output Hold	$t_{SDCHACI}$	2.0	—	ns	—
DD6	Write Command to first DQS Latching Transition	t_{CMDVDQ}		1.25	SD_CLK	—
DD7	Data and Data Mask Output Setup (DQ-->DQS) Relative to DQS (DDR Write Mode)	t_{DQDMV}	1.5	—	ns	5 6
DD8	Data and Data Mask Output Hold (DQS-->DQ) Relative to DQS (DDR Write Mode)	t_{DQDMI}	1.0	—	ns	7
DD9	Input Data Skew Relative to DQS (Input Setup)	t_{DVDQ}	—	1	ns	8
DD10	Input Data Hold Relative to DQS.	t_{DIDQ}	0.25 × SD_CLK + 0.5ns	—	ns	9
DD11	DQS falling edge from SDCLK rising (output hold time)	$t_{DQLSDCH}$	0.5	—	ns	—
DD12	DQS input read preamble width (t_{RPRE})	t_{DQRPRE}	0.9	1.1	SD_CLK	—
DD13	DQS input read postamble width (t_{RPST})	t_{DQRPST}	0.4	0.6	SD_CLK	—
DD14	DQS output write preamble width (t_{WPRE})	t_{DQWPRE}	0.25	—	SD_CLK	—
DD15	DQS output write postamble width (t_{WPST})	t_{DQWPST}	0.4	0.6	SD_CLK	—

NOTES:
1. The frequency of operation is 2x or 4x the FB_CLK frequency of operation. FlexBus and SDRAM clock operate at the same frequency as the internal bus clock.
2. SD_CLK is one SDRAM clock in (ns).
3. Pulse width high plus pulse width low cannot exceed min and max clock period.
4. Command output valid should be 1/2 the memory bus clock (SD_CLK) plus some minor adjustments for process, temperature, and voltage variations.
5. This specification relates to the required input setup time of today's DDR memories. The device's output setup should be larger than the input setup of the DDR memories. If it is not larger, the input setup on the memory is in violation. MEM_DATA[31:24] is relative to MEM_DQS[3], MEM_DATA[23:16] is relative to MEM_DQS[2], MEM_DATA[15:8] is relative to MEM_DQS[1], and MEM_[7:0] is relative MEM_DQS[0].
6. The first data beat is valid before the first rising edge of DQS and after the DQS write preamble. The remaining data beats are valid for each subsequent DQS edge.

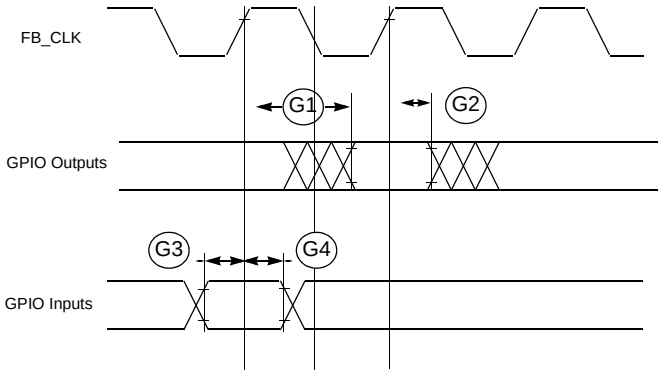


Figure 20. GPIO Timing

5.10 Reset and Configuration Override Timing

Table 15. Reset and Configuration Override Timing

Num	Characteristic	Symbol	Min	Max	Unit
R1	$\overline{\text{RESET}}$ Input valid to FB_CLK High	t_{RVCH}	9	—	ns
R2	FB_CLK High to $\overline{\text{RESET}}$ Input invalid	t_{CHRI}	1.5	—	ns
R3	$\overline{\text{RESET}}$ Input valid Time [1]	t_{RIVT}	5	—	t_{CYC}
R4	FB_CLK High to $\overline{\text{RSTOUT}}$ Valid	t_{CHROV}	—	10	ns
R5	$\overline{\text{RSTOUT}}$ valid to Config. Overrides valid	t_{ROVCV}	0	—	ns
R6	Configuration Override Setup Time to $\overline{\text{RSTOUT}}$ invalid	t_{COS}	20	—	t_{CYC}
R7	Configuration Override Hold Time after $\overline{\text{RSTOUT}}$ invalid	t_{COH}	0	—	ns
R8	$\overline{\text{RSTOUT}}$ invalid to Configuration Override High Impedance	t_{ROICZ}	—	1	t_{CYC}

NOTES:
1 During low power STOP, the synchronizers for the $\overline{\text{RESET}}$ input are bypassed and $\overline{\text{RESET}}$ is asserted asynchronously to the system. Thus, $\overline{\text{RESET}}$ must be held a minimum of 100 ns.

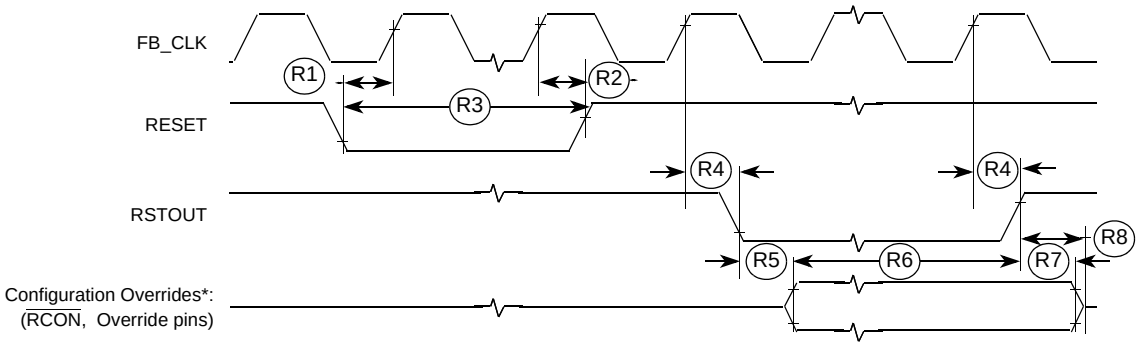


Figure 21. $\overline{\text{RESET}}$ and Configuration Override Timing

5.12.2 MII Transmit Signal Timing (FEC_TXD[3:0], FEC_TXEN, FEC_TXER, FEC_TXCLK)

Table 19 lists MII transmit channel timings.

The transmitter functions correctly up to a FEC_TXCLK maximum frequency of 25 MHz +1%. In addition, the processor clock frequency must exceed twice the FEC_TXCLK frequency.

Table 19. MII Transmit Signal Timing

Num	Characteristic	Min	Max	Unit
M5	FEC_TXCLK to FEC_TXD[3:0], FEC_TXEN, FEC_TXER invalid	5	—	ns
M6	FEC_TXCLK to FEC_TXD[3:0], FEC_TXEN, FEC_TXER valid	—	25	ns
M7	FEC_TXCLK pulse width high	35%	65%	FEC_TXCLK period
M8	FEC_TXCLK pulse width low	35%	65%	FEC_TXCLK period

Figure 24 shows MII transmit signal timings listed in Table 19.

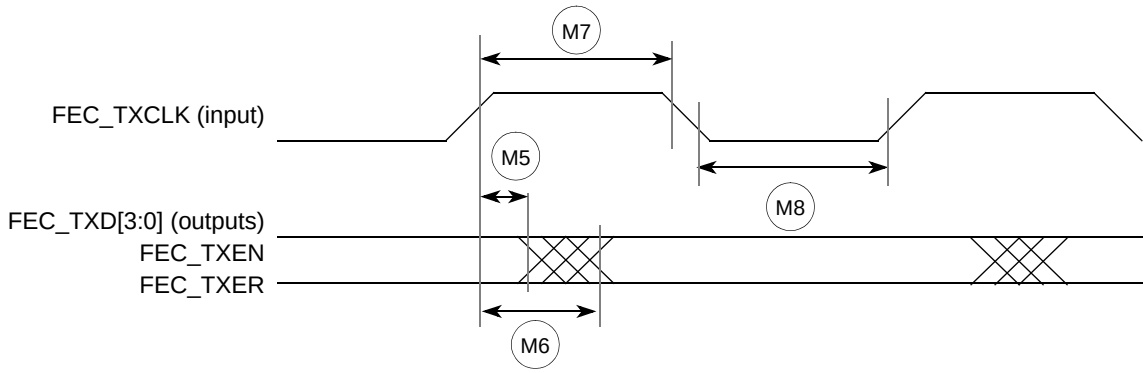


Figure 24. MII Transmit Signal Timing Diagram

5.12.3 MII Async Inputs Signal Timing (FEC_CRS and FEC_COL)

Table 20 lists MII asynchronous inputs signal timing.

Table 20. MII Async Inputs Signal Timing

Num	Characteristic	Min	Max	Unit
M9	FEC_CRS, FEC_COL minimum pulse width	1.5	—	FEC_TXCLK period

Figure 25 shows MII asynchronous input timings listed in Table 20.

Figure 25. MII Async Inputs Timing Diagram

5.13 32-Bit Timer Module AC Timing Specifications

Table 22 lists timer module AC timings.

Table 22. Timer Module AC Timing Specifications

Name	Characteristic	Min	Max	Unit
T1	DT0IN / DT1IN / DT2IN / DT3IN cycle time	3	—	t_{CYC}
T2	DT0IN / DT1IN / DT2IN / DT3IN pulse width	1	—	t_{CYC}

5.14 QSPI Electrical Specifications

Table 23 lists QSPI timings.

Table 23. QSPI Modules AC Timing Specifications

Name	Characteristic	Min	Max	Unit
QS1	QSPI_CS[3:0] to QSPI_CLK	1	510	tcyc
QS2	QSPI_CLK high to QSPI_DOUT valid.	—	10	ns
QS3	QSPI_CLK high to QSPI_DOUT invalid. (Output hold)	1.5	—	ns
QS4	QSPI_DIN to QSPI_CLK (Input setup)	9	—	ns
QS5	QSPI_DIN to QSPI_CLK (Input hold)	9	—	ns

The values in Table 23 correspond to Figure 27.

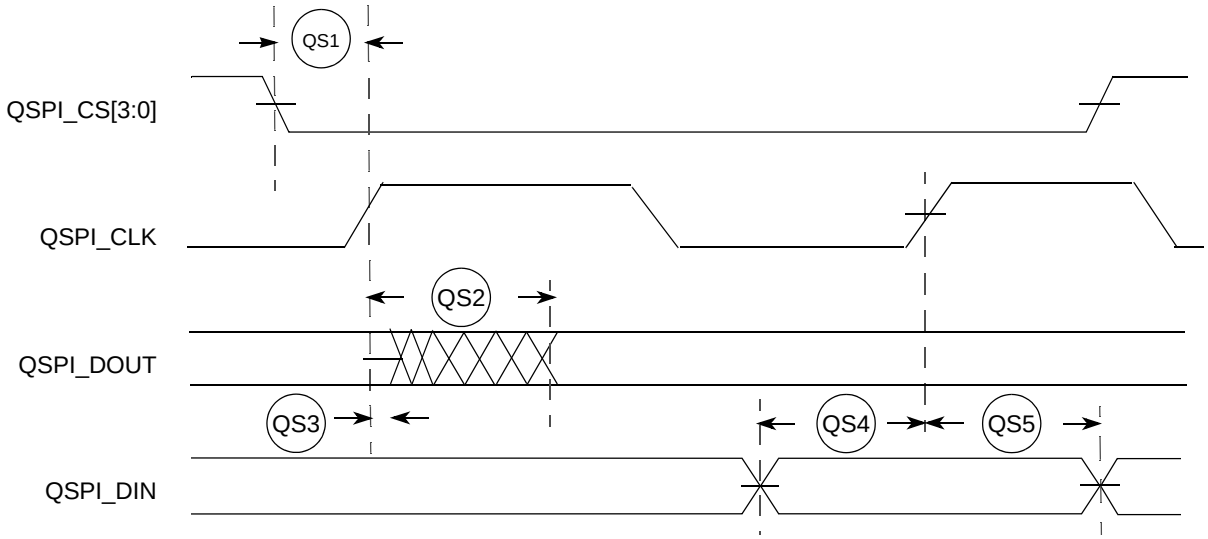


Figure 27. QSPI Timing

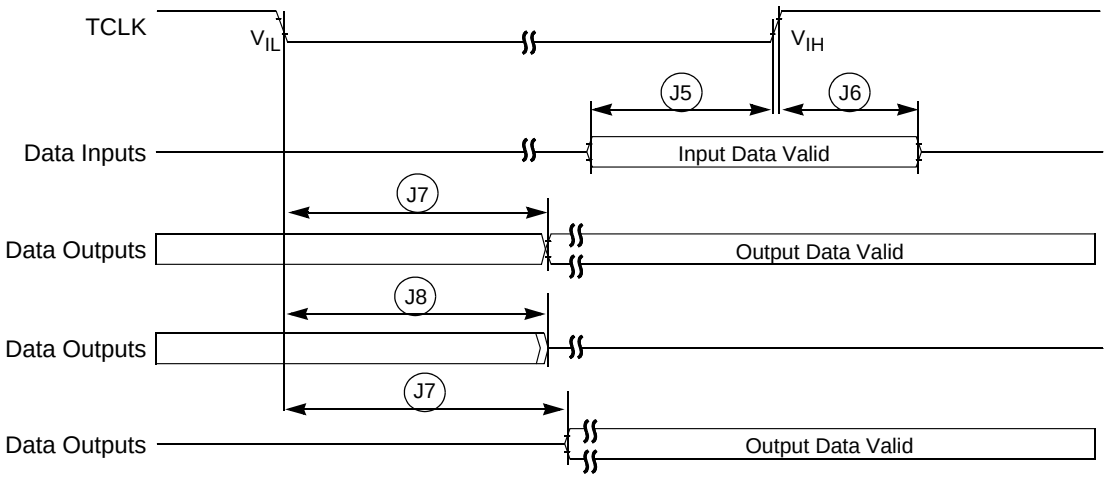


Figure 29. Boundary Scan (JTAG) Timing

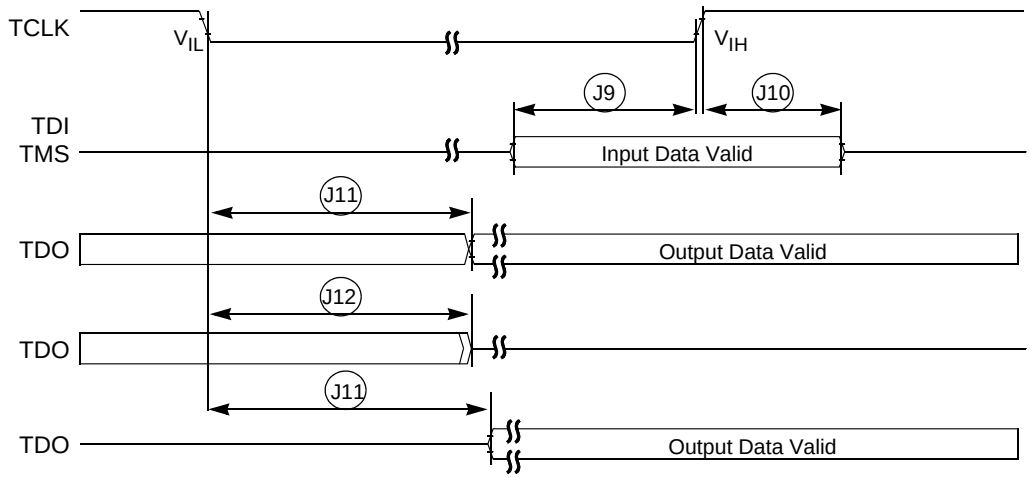


Figure 30. Test Access Port Timing

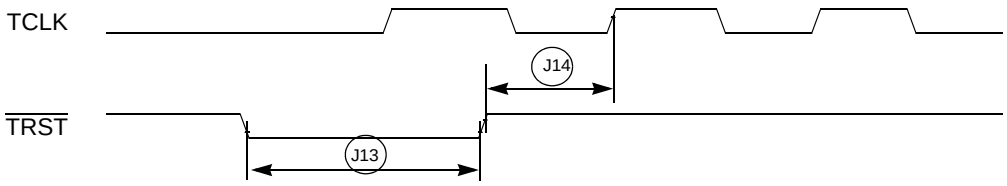


Figure 31. $\overline{\text{TRST}}$ Timing

5.16 Debug AC Timing Specifications

Table 25 lists specifications for the debug AC timing parameters shown in Figure 32.

Table 25. Debug AC Timing Specification

Num	Characteristic	Min	Max	Unit
D0	PSTCLK cycle time	1	1	t_{SYS}
D1	PSTCLK rising to PSTDDATA valid	—	3.0	ns
D2	PSTCLK rising to PSTDDATA invalid	1.5	—	ns
D3	DSI-to-DSCLK setup	1	—	PSTCLK
D4[1]	DSCLK-to-DSO hold	4	—	PSTCLK
D5	DSCLK cycle time	5	—	PSTCLK
D6	BKPT assertion time	1	—	PSTCLK

NOTES:
1 DSCLK and DSI are synchronized internally. D4 is measured from the synchronized DSCLK input relative to the rising edge of PSTCLK.

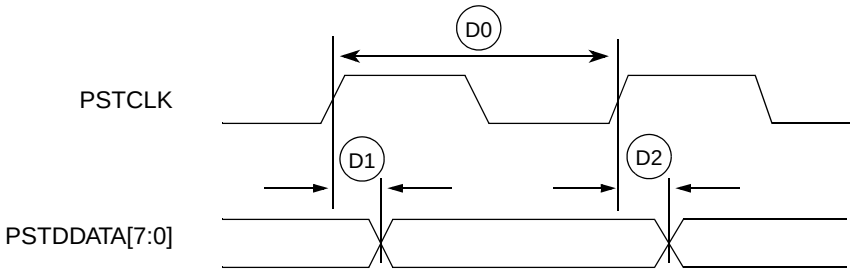


Figure 32. Real-Time Trace AC Timing

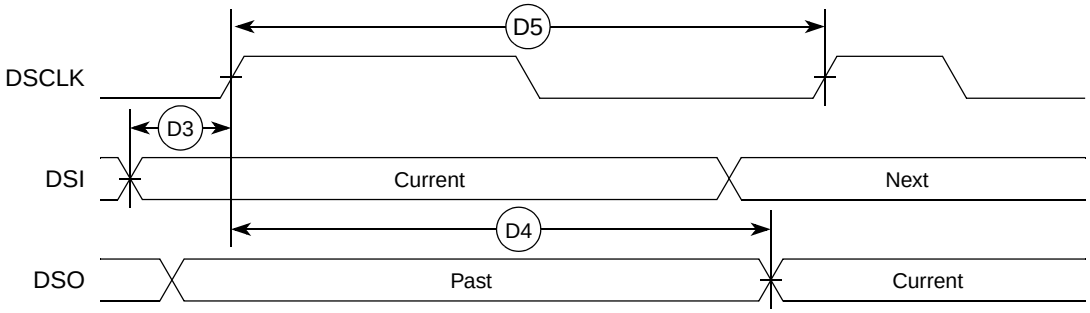


Figure 33. BDM Serial Port AC Timing