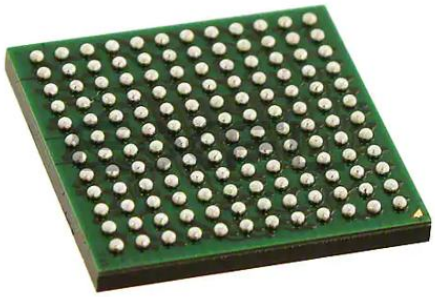


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	Coldfire V2
Core Size	32-Bit Single-Core
Speed	166.67MHz
Connectivity	EBI/EMI, I²C, SPI, UART/USART
Peripherals	DMA, WDT
Number of I/O	30
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.4V ~ 3.6V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LBGA
Supplier Device Package	144-MAPBGA (13x13)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcf5207cvm166

1 MCF5207/8 Device Configurations

The following table compares the two devices described in this document:

Table 1. MCF5207 & MCF5208 Configurations

Module	MCF5207	MCF5208
Version 2 ColdFire Core with EMAC (Enhanced Multiply-Accumulate Unit)	•	•
Core (System) Clock	up to 166.67 MHz	
Peripheral and External Bus Clock (Core clock ÷ 2)	up to 83.33 MHz	
Performance (Dhrystone/2.1 MIPS)	up to 159	
Instruction/Data Cache	8 Kbytes	
Static RAM (SRAM)	16 Kbytes	
SDR/DDR SDRAM Controller	•	•
Fast Ethernet Controller (FEC)	—	•
Low-Power Management Module	•	•
UARTs	3	3
I^2C	•	•
QSPI	•	•
32-bit DMA Timers	4	4
Watchdog Timer (WDT)	•	•
Periodic Interrupt Timers (PIT)	4	4
Edge Port Module (EPORT)	•	•
Interrupt Controllers (INTC)	1	1
16-channel Direct Memory Access (DMA)	•	•
FlexBus External Interface	•	•
General Purpose I/O Module (GPIO)	•	•
JTAG - IEEE® 1149.1 Test Access Port	•	•
Package	144 LQFP 144 MAPBGA	160 QFP 196 MAPBGA

2 Ordering Information

Table 2. Orderable Part Numbers

Freescale Part Number	Description	Speed	Temperature
MCF5207CAG166	MCF5207 RISC Microprocessor, 144 LQFP	166.67 MHz	–40° to +85° C
MCF5207CVM166	MCF5207 RISC Microprocessor, 144 MAPBGA	166.67 MHz	–40° to +85° C
MCF5208CAB166	MCF5208 RISC Microprocessor, 160 QFP	166.67 MHz	–40° to +85° C
MCF5208CVM166	MCF5208 RISC Microprocessor, 196 MAPBGA	166.67 MHz	–40° to +85° C

Table 3. MCF5207/8 Signal Information and Muxing (continued)

Signal Name	GPIO	Alternate 1	Alternate 2	Dir.[1]	Voltage Domain	MCF5207 144 LQFP	MCF5207 144 MAPBGA	MCF5208 160 QFP	MCF5208 196 MAPBGA
External Interrupts Port[5]									
$\overline{\text{IRQ7}}$[2]	PIRQ7[2]	—	—	I	EVDD	134	A5	142	C7
$\overline{\text{IRQ4}}$[2]	PIRQ4[2]	$\overline{\text{DREQ0}}$[2]	—	I	EVDD	133	C6	141	D7
$\overline{\text{IRQ1}}$[2]	PIRQ1[2]	—	—	I	EVDD	132	B6	140	D8
FEC									
FEC_MDC	PFECI2C3	I2C_SCL[2]	U2TXD	O	EVDD	—	—	148	D6
FEC_MDIO	PFECI2C2	I2C_SDA[2]	U2RXD	I/O	EVDD	—	—	147	C6
FEC_TXCLK	PFECH7	—	—	I	EVDD	—	—	157	B3
—	PFECH6	—	$\overline{\text{U1RTS}}$	O	EVDD	142	A2	—	—
FEC_TXEN	PFECH6	—	$\overline{\text{U1RTS}}$	O	EVDD	—	—	158	A2
FEC_TXD0	PFECH5	—	—	O	EVDD	—	—	3	B1
FEC_COL	PFECH4	—	—	I	EVDD	—	—	7	D3
FEC_RXCLK	PFECH3	—	—	I	EVDD	—	—	154	B4
FEC_RXDV	PFECH2	—	—	I	EVDD	—	—	153	A4
FEC_RXD0	PFECH1	—	—	I	EVDD	—	—	152	D5
FEC_CRS	PFECH0	—	—	I	EVDD	—	—	8	D2
FEC_TXD[3:1]	PFECL[7:5]	—	—	O	EVDD	—	—	6–4	C1, C2, B2
—	PFECL4	—	$\overline{\text{U0RTS}}$	O	EVDD	141	D5	—	—
FEC_TXER	PFECL4	—	$\overline{\text{U0RTS}}$	O	EVDD	—	—	156	A3
FEC_RXD[3:2]	PFECL[3:2]	—	—	I	EVDD	—	—	149–150	A5, B5
—	PFECL1	—	$\overline{\text{U1CTS}}$	I	EVDD	139	B4	—	—
FEC_RXD1	PFECL1	—	$\overline{\text{U1CTS}}$	I	EVDD	—	—	151	C5
—	PFECL0	—	$\overline{\text{U0CTS}}$	I	EVDD	140	E4	—	—
FEC_RXER	PFECL0	—	$\overline{\text{U0CTS}}$	I	EVDD	—	—	155	C4
Note: The MCF5207 does not contain an FEC module. However, the UART0 and UART1 control signals (as well as their GPIO signals) are available by setting the appropriate FEC GPIO port registers.									
I²C									
I2C_SDA[2]	PFECI2C0[2]	U2RXD[2]	—	I/O	EVDD	—	—	—	D1
I2C_SCL[2]	PFECI2C1[2]	U2TXD[2]	—	I/O	EVDD	—	—	—	E4
DMA									
$\overline{\text{DACK0}}$ and $\overline{\text{DREQ0}}$ do not have a dedicated bond pads. Please refer to the following pins for muxing: $\overline{\text{TS}}$ and QSPI_CS2 for $\overline{\text{DACK0}}$, $\overline{\text{IRQ4}}$ and QSPI_DIN for $\overline{\text{DREQ0}}$.									

4 Mechanicals and Pinouts

Drawings in this section show the pinout and the packaging and mechanical characteristics of the MCF5207 and MCF5208 devices.

NOTE

The mechanical drawings are the latest revisions at the time of publication of this document. The most up-to-date mechanical drawings can be found at the product summary page located at http://www.freescale.com/coldfire.

4.1 Pinout—144 LQFP

Figure 1 shows a pinout of the MCF5207CAG166 device.

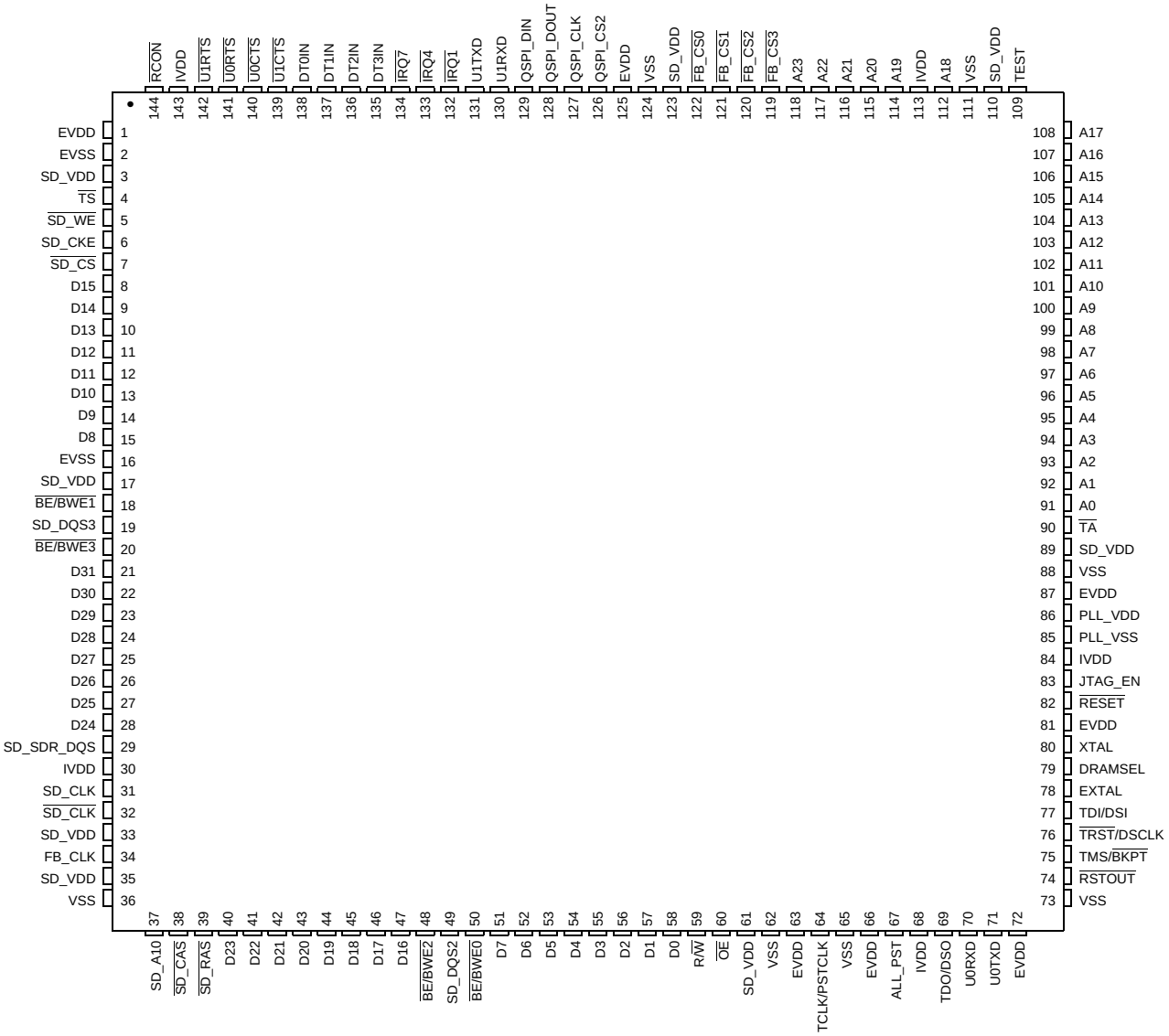
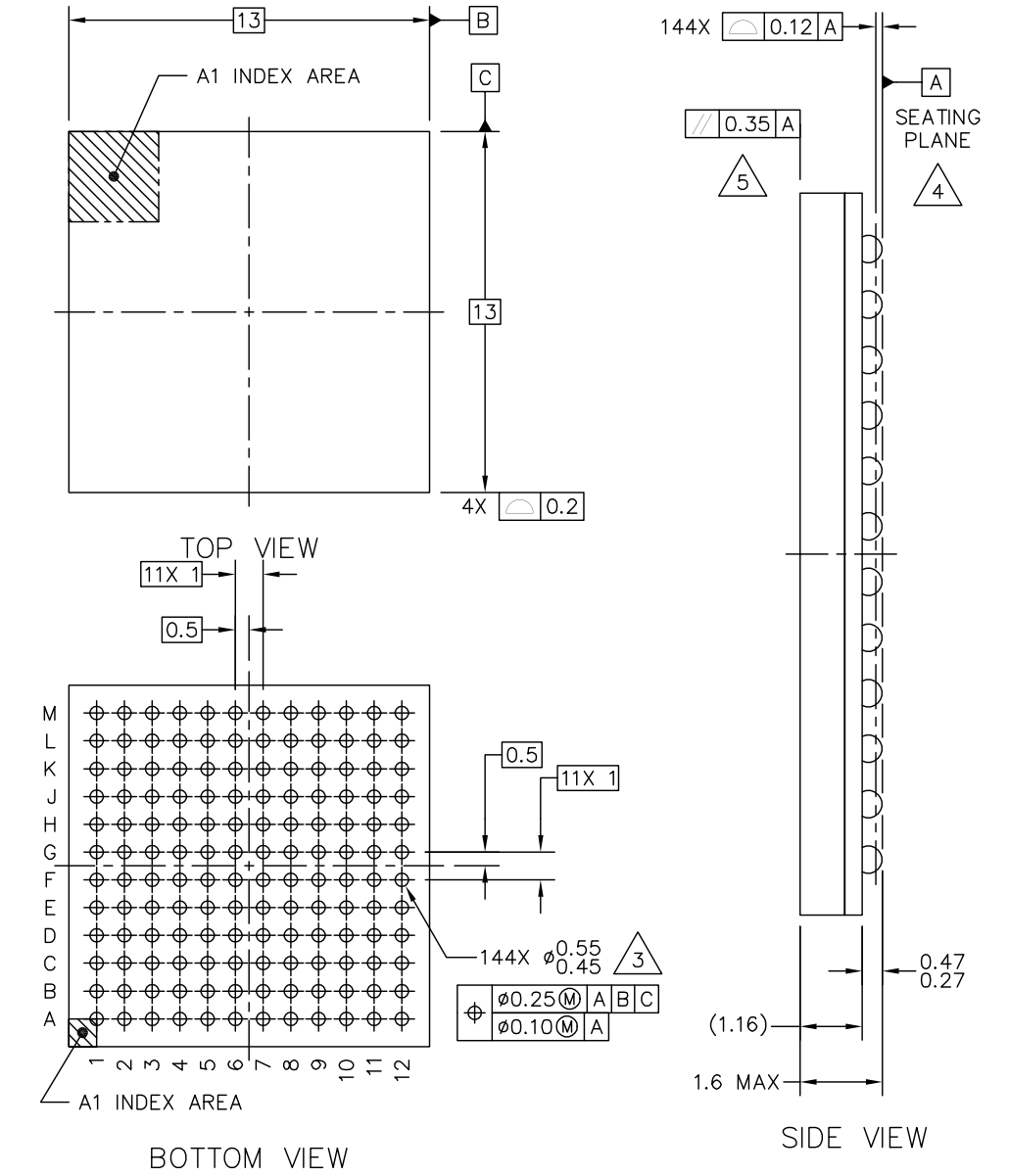


Figure 1. MCF5207CAG166 Pinout Top View (144 LQFP)

4.4 Package Dimensions—144 MAPBGA

Figure 5 shows the MCF5207CAB166 package dimensions.



NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM A.
4. DATUM A, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

Figure 5. MCF5207CAB166 Package Dimensions (144 MAPBGA)

4.5 Pinout—160 QFP

Figure 6 shows a pinout of the MCF5208CAB166 device.

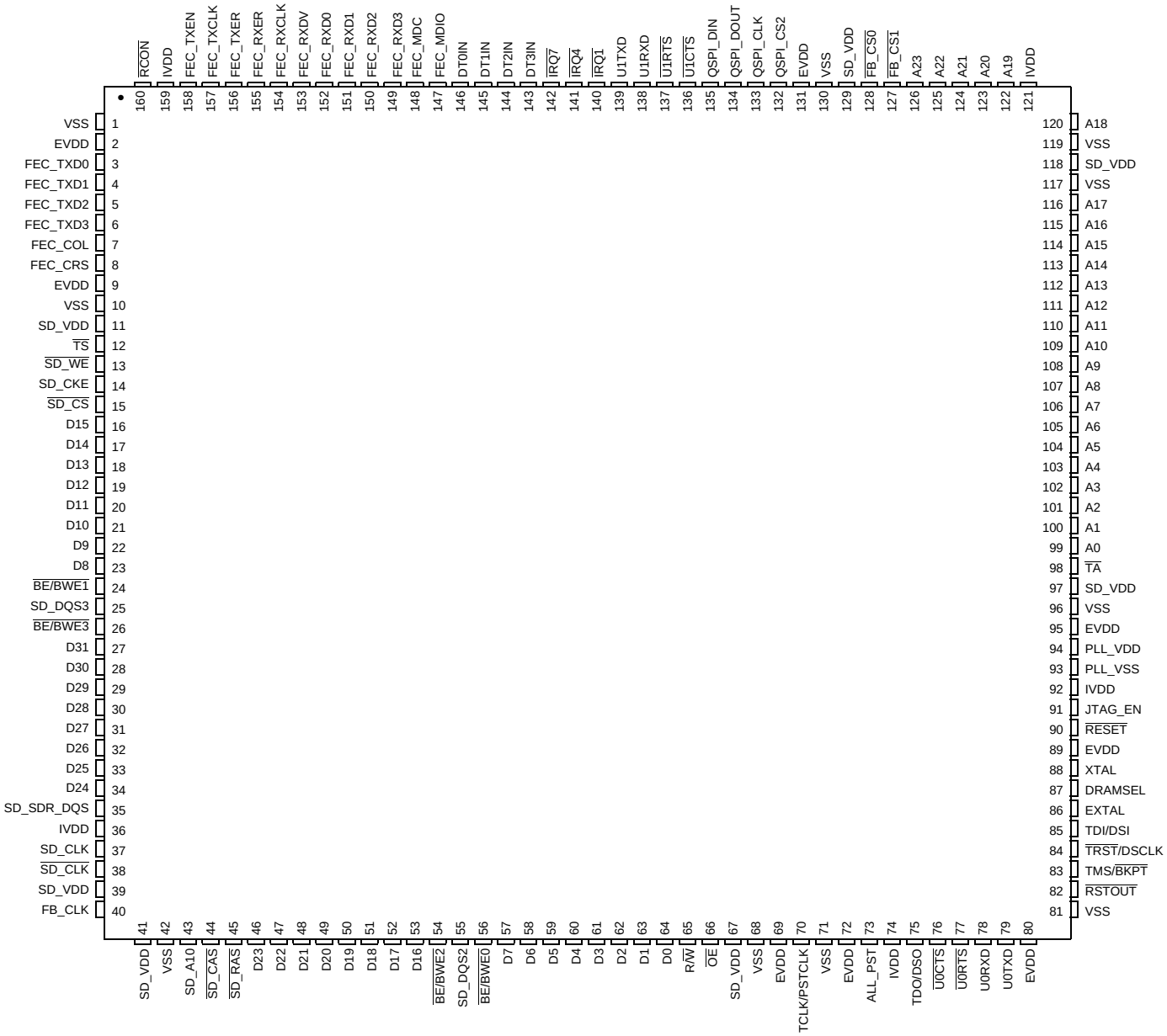


Figure 6. MCF5208CAB166 Pinout Top View (160 QFP)

Table 4. Absolute Maximum Ratings[1, 2] (continued)

Operating Temperature Range (Packaged)	T_A (T_L - T_H)	– 40 to 85	°C
Storage Temperature Range	T_{stg}	– 55 to 150	°C

NOTES:
1. Functional operating conditions are given in Section 5.4, "DC Electrical Specifications". Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Continued operation at these levels may affect device reliability or cause permanent damage to the device.
2. This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (V_{SS} or EV_{DD}).
3. Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.
4. All functional non-supply pins are internally clamped to V_{SS} and EV_{DD}.
5. Power supply must maintain regulation within operating EV_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{in} > EV_{DD}$) is greater than I_{DD}, the injection current may flow out of EV_{DD} and could result in external power supply going out of regulation. Ensure external EV_{DD} load shunts current greater than maximum injection current. This is the greatest risk when the MCU is not consuming power (ex; no clock). Power supply must maintain regulation within operating EV_{DD} range during instantaneous and operating maximum current conditions.

5.2 Thermal Characteristics

Table 5 lists thermal resistance values

Table 5. Thermal Characteristics

Characteristic		Symbol	196MBGA	144MBGA	160QFP	144LQFP	Unit
Junction to ambient, natural convection	Four layer board (2s2p)	θ_{JMA}	47[1,2]	47[1,2]	49[1,2]	65[1,2]	°C/W
Junction to ambient (@200 ft/min)	Four layer board (2s2p)	θ_{JMA}	43[1,2]	43[1,2]	44[1,2]	58[1,2]	°C/W
Junction to board		θ_{JB}	36[3]	36[3]	40[3]	50[3]	°C/W
Junction to case		θ_{JC}	22[4]	22[4]	39[4]	19[4]	°C/W
Junction to top of package		Ψ_{jt}	6[1,5]	6[1,5]	12[1,6]	5[1,7]	°C/W
Maximum operating junction temperature		T_j	105	105	105	105	°C

NOTES:
1. θ_{JMA} and Ψ_{jt} parameters are simulated in conformance with EIA/JESD Standard 51-2 for natural convection. Freescale recommends the use of θ_{JmA} and power dissipation specifications in the system design to prevent device junction temperatures from exceeding the rated specification. System designers should be aware that device junction temperatures can be significantly influenced by board layout and surrounding devices. Conformance to the device junction temperature specification can be verified by physical measurement in the customer's system using the Ψ_{jt} parameter, the device power dissipation, and the method described in EIA/JESD Standard 51-2.
2. Per JEDEC JESD51-6 with the board horizontal.

[2] A device is defined as a failure if, after exposure to ESD pulses, the device no longer meets the device specification requirements. Complete DC parametric and functional testing is performed per applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

5.4 DC Electrical Specifications

Table 7. DC Electrical Specifications

Characteristic	Symbol	Min	Max	Unit
Core Supply Voltage	IV_{DD}	1.4	1.6	V
PLL Supply Voltage	$PLLV_{DD}$	1.4	1.6	V
CMOS Pad Supply Voltage	EV_{DD}	3.0	3.6	V
SDRAM and FlexBus Supply Voltage Mobile DDR/Bus Pad Supply Voltage (nominal 1.8V) DDR/Bus Pad Supply Voltage (nominal 2.5V) SDR/Bus Pad Supply Voltage (nominal 3.3V)	SDV_{DD}	 1.70 2.25 3.0	 1.95 2.75 3.6	V
CMOS Input High Voltage	EV_{IH}	2	EV_{DD} + 0.3	V
CMOS Input Low Voltage	EV_{IL}	V_{SS} - 0.3	0.8	V
CMOS Output High Voltage I_{OH} = –5.0 mA	EV_{OH}	EV_{DD} - 0.4	—	V
CMOS Output Low Voltage I_{OL} = 5.0 mA	EV_{OL}	—	0.4	V
SDRAM and FlexBus Input High Voltage Mobile DDR/Bus Input High Voltage (nominal 1.8V) DDR/Bus Pad Supply Voltage (nominal 2.5V) SDR/Bus Pad Supply Voltage (nominal 3.3V)	SDV_{IH}	 1.35 1.7 2	 SDV_{DD} + 0.3 SDV_{DD} + 0.3 SDV_{DD} + 0.3	V
SDRAM and FlexBus Input Low Voltage Mobile DDR/Bus Input High Voltage (nominal 1.8V) DDR/Bus Pad Supply Voltage (nominal 2.5V) SDR/Bus Pad Supply Voltage (nominal 3.3V)	SDV_{IL}	 V_{SS} - 0.3 V_{SS} - 0.3 V_{SS} - 0.3	 0.45 0.8 0.8	V
SDRAM and FlexBus Output High Voltage Mobile DDR/Bus Input High Voltage (nominal 1.8V) DDR/Bus Pad Supply Voltage (nominal 2.5V) SDR/Bus Pad Supply Voltage (nominal 3.3V) I_{OH} = –5.0 mA for all modes	SDV_{OH}	 SDV_{DD} - 0.35 2.1 2.4	 — — —	V
SDRAM and FlexBus Output Low Voltage Mobile DDR/Bus Input High Voltage (nominal 1.8V) DDR/Bus Pad Supply Voltage (nominal 2.5V) SDR/Bus Pad Supply Voltage (nominal 3.3V) I_{OL} = 5.0 mA for all modes	SDV_{OL}	 — — —	 0.3 0.3 0.5	V
Input Leakage Current V_{in} = IV_{DD} or V_{SS}, Input-only pins	I_{in}	–1.0	1.0	µA

Table 7. DC Electrical Specifications (continued)

Characteristic	Symbol	Min	Max	Unit
Weak Internal Pull Up Device Current, tested at V_{IL} Max.[1]	I_{APU}	-10	- 130	µA
Input Capacitance [2] All input-only pins All input/output (three-state) pins	C_{in}	 — —	 7 7	pF

NOTES:
1 Refer to the signals section for pins having weak internal pull-up devices.
2 This parameter is characterized before qualification rather than 100% tested.

5.4.1 PLL Power Filtering

To further enhance noise isolation, an external filter is strongly recommended for PLL analog V_{DD} pins. The filter shown in Figure 11 should be connected between the board V_{DD} and the $PLLV_{DD}$ pins. The resistor and capacitors should be placed as close to the dedicated $PLLV_{DD}$ pin as possible.

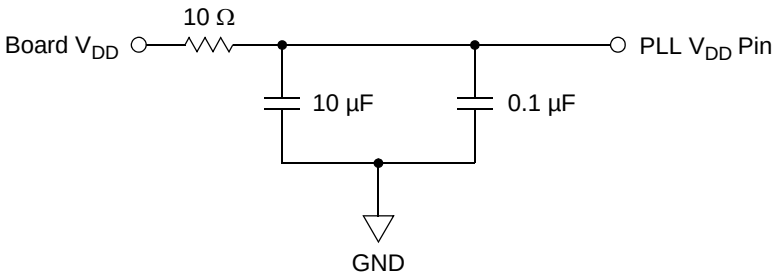


Figure 11. System PLL V_{DD} Power Filter

5.4.2 Supply Voltage Sequencing and Separation Cautions

The relationship between SDV_{DD} and EV_{DD} is non-critical during power-up and power-down sequences. SDV_{DD} (2.5V or 3.3V) and EV_{DD} are specified relative to IV_{DD}.

5.4.2.1 Power Up Sequence

If EV_{DD}/SDV_{DD} are powered up with IV_{DD} at 0 V, the sense circuits in the I/O pads cause all pad output drivers connected to the EV_{DD}/SDV_{DD} to be in a high impedance state. There is no limit on how long after EV_{DD}/SDV_{DD} powers up before IV_{DD} must power up. IV_{DD} should not lead the EV_{DD}, SDV_{DD}, or $PLLV_{DD}$ by more than 0.4 V during power ramp-up or there will be high current in the internal ESD protection diodes. The rise times on the power supplies should be slower than 500 us to avoid turning on the internal ESD protection clamp diodes.

5.4.2.2 Power Down Sequence

If $IV_{DD}/PLLV_{DD}$ are powered down first, sense circuits in the I/O pads cause all output drivers to be in a high impedance state. There is no limit on how long after IV_{DD} and $PLLV_{DD}$ power down before EV_{DD} or SDV_{DD} must power down. IV_{DD} should not lag EV_{DD}, SDV_{DD}, or $PLLV_{DD}$ going low by more than

5 See the description of the low-power control register (LCPR) in the *MCF5208 Reference Manual* for more information on stop modes 0–3.

The figure below illustrates the power consumption in a graphical format.

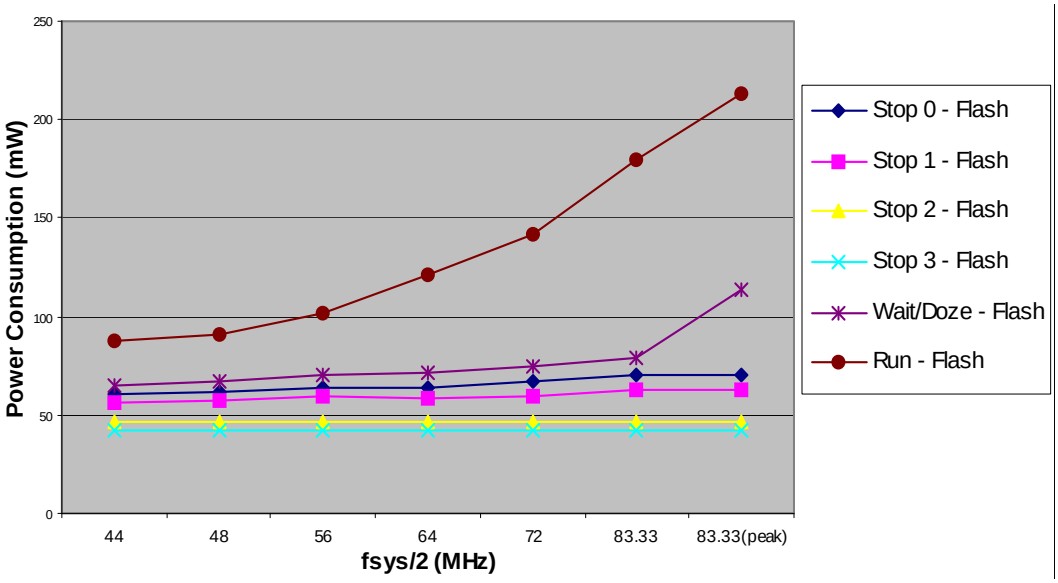


Figure 12. Current Consumption in Low-Power Modes

Table 9. Typical Active Current Consumption Specifications[1]

$f_{sys/2}$ Frequency	Voltage (V)	Typical[2] Active (mA)		Peak[3] Active (mA)
		SRAM	Flash	
1 MHz	3.3	2.04	2.12	2.28
	2.5	15.24	15.32	15.24
	1.5	1.30	1.41	1.49
2 MHz	3.3	2.23	2.40	3.57
	2.5	15.26	15.42	15.26
	1.5	1.71	1.92	2.09
4 MHz	3.3	2.60	2.95	3.58
	2.5	15.30	15.61	15.30
	1.5	2.49	2.95	3.29
44 MHz	3.3	7.61	17.67	25.34
	2.5	16.13	19.49	16.95
	1.5	24.04	28.72	39.02
48 MHz	3.3	8.16	26.21	34.45
	2.5	16.28	20.06	17.17
	1.5	26.05	31.13	42.30

All other timing relationships can be derived from these values. Timings listed in Table 11 are shown in Figure 14 and Figure 15.

* The timings are also valid for inputs sampled on the negative clock edge.

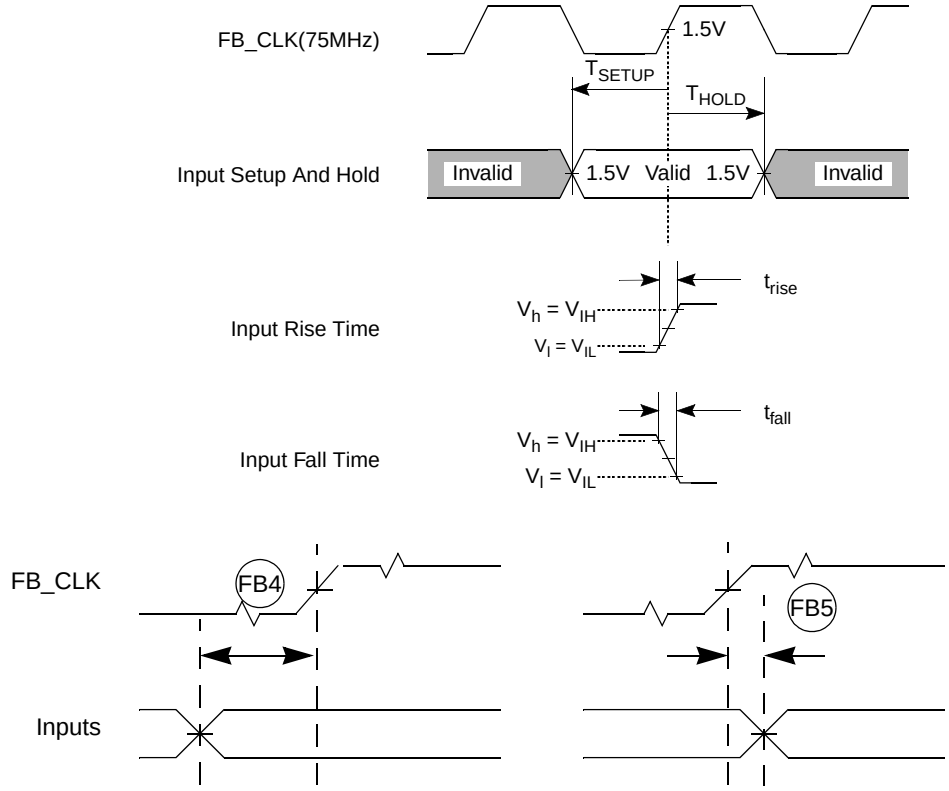


Figure 13. General Input Timing Requirements

5.7.1 FlexBus

FlexBus is a multi-function external bus interface provided to interface to slave-only devices up to a maximum bus frequency of 83.33 MHz. It can be directly connected to asynchronous or synchronous devices such as external boot ROMs, flash memories, gate-array logic, or other simple target (slave) devices with little or no additional circuitry. For asynchronous devices, a simple chip-select based interface can be used. The FlexBus interface has six general purpose chip-selects ($\overline{\text{FB\_CS}}$[5:0]) that can be configured to be distributed between the FlexBus or SDRAM memory interfaces. Chip-select $\overline{\text{FB\_CS}}$[0] can be dedicated to boot ROM access and can be programmed to be byte (8 bits), word (16 bits), or longword (32 bits) wide. Control signal timing is compatible with common ROM/flash memories.

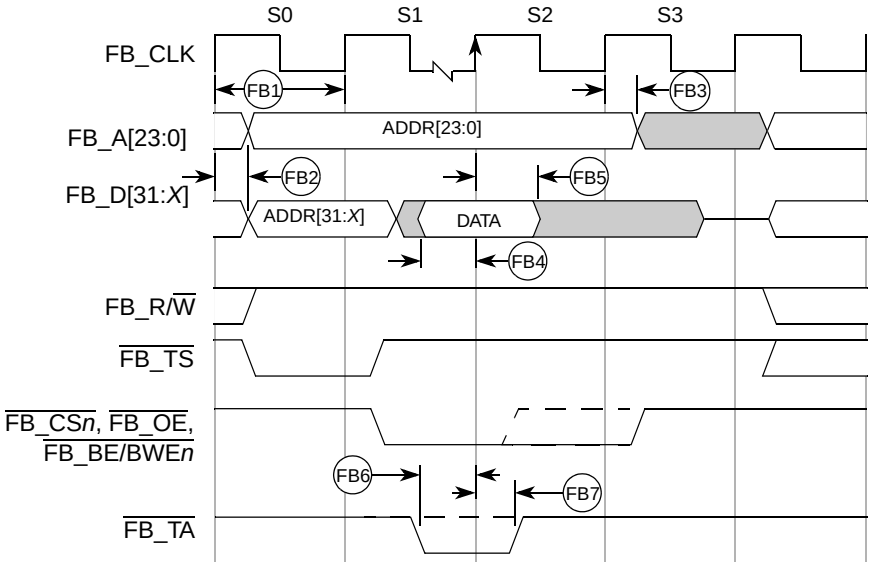


Figure 14. FlexBus Read Timing

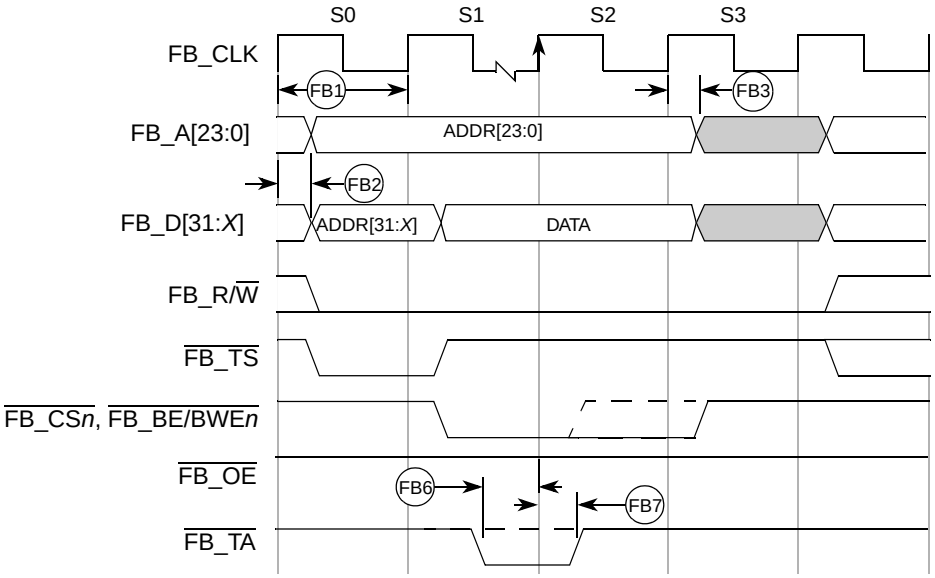


Figure 15. Flexbus Write Timing

5.8 SDRAM Bus

The SDRAM controller supports accesses to main SDRAM memory from any internal master. It supports standard SDRAM or double data rate (DDR) SDRAM, but it does not support both at the same time. The SDRAM controller uses SSTL2 and SSTL3 I/O drivers. Both SSTL drive modes are programmable for Class I or Class II drive strength.

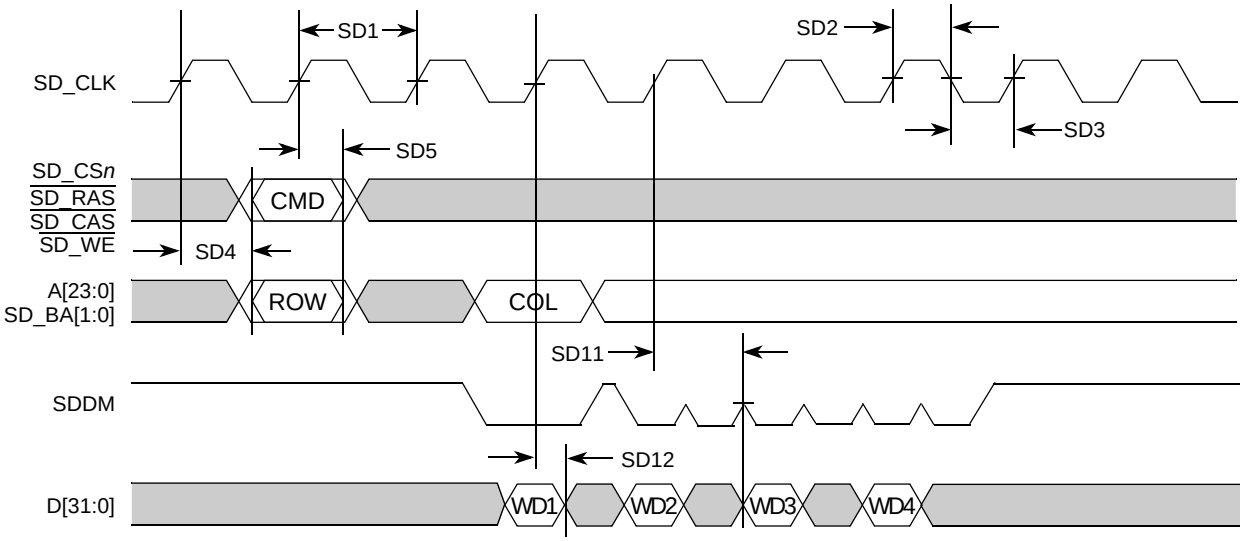


Figure 16. SDR Write Timing

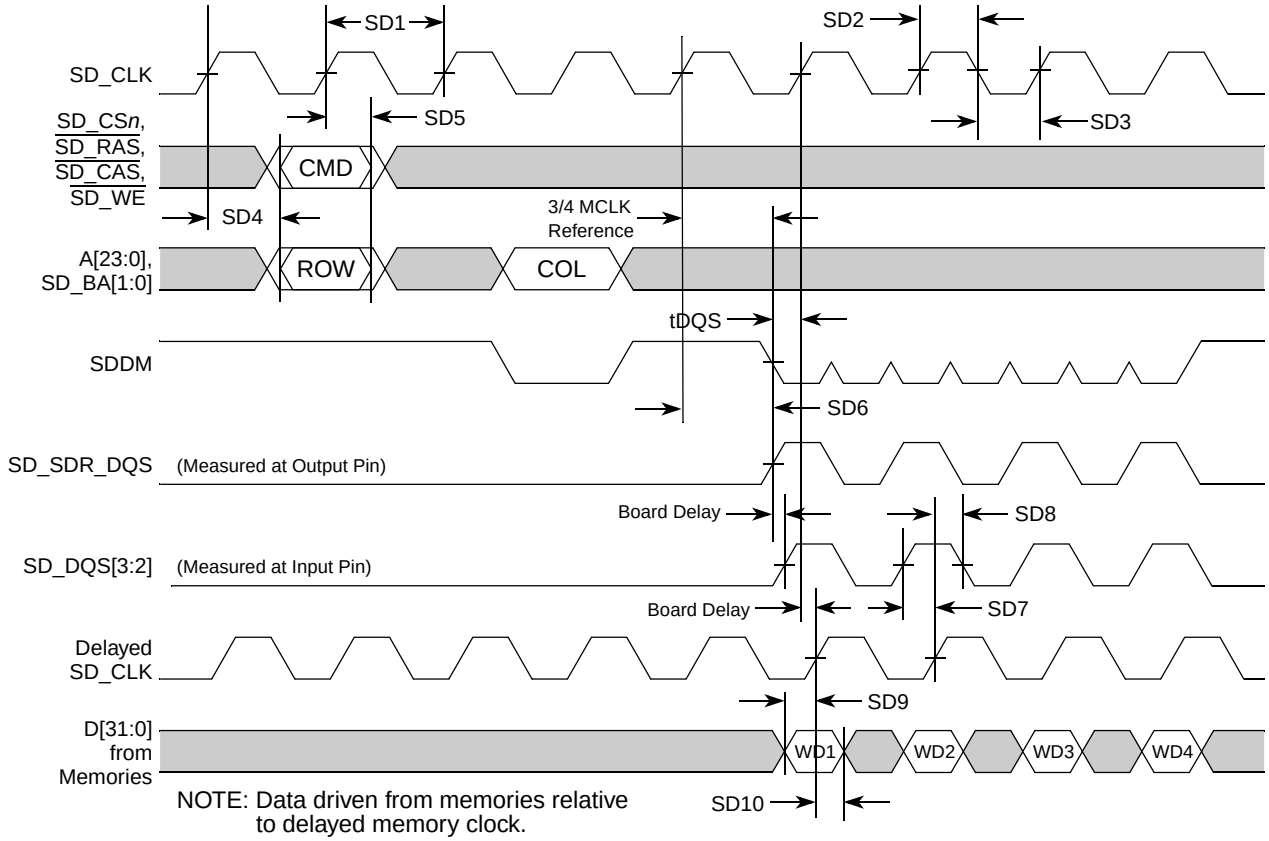


Figure 17. SDR Read Timing

5.8.2 DDR SDRAM AC Timing Characteristics

When using the SDRAM controller in DDR mode, the following timing numbers must be followed to properly latch or drive data onto the memory bus. All timing numbers are relative to the four DQS byte lanes. The following timing numbers are subject to change at anytime, and are only provided to aid in early board design. Please contact your local Freescale representative if questions develop.

Table 13. DDR Timing Specifications

Num	Characteristic	Symbol	Min	Max	Unit	Notes
—	Frequency of Operation	—	60	83.33	Mhz	1
DD1	Clock Period (SD_CLK)	t_{DDCK}	12	16.67	ns	2
DD2	Pulse Width High	t_{DDCKH}	0.45	0.55	SD_CLK	3
DD3	Pulse Width Low	t_{DDCKL}	0.45	0.55	SD_CLK	3
DD4	Address, SD_CKE, $\overline{\text{SD\_CAS}}$, $\overline{\text{SD\_RAS}}$, $\overline{\text{SD\_WE}}$, $\overline{\text{SD\_CS}}$[1:0] - Output Valid	$t_{SDCHACV}$	—	0.5 × SD_CLK + 1.0	ns	4
DD5	Address, SD_CKE, $\overline{\text{SD\_CAS}}$, $\overline{\text{SD\_RAS}}$, $\overline{\text{SD\_WE}}$, $\overline{\text{SD\_CS}}$[1:0] - Output Hold	$t_{SDCHACI}$	2.0	—	ns	—
DD6	Write Command to first DQS Latching Transition	t_{CMDVDQ}		1.25	SD_CLK	—
DD7	Data and Data Mask Output Setup (DQ-->DQS) Relative to DQS (DDR Write Mode)	t_{DQDMV}	1.5	—	ns	5 6
DD8	Data and Data Mask Output Hold (DQS-->DQ) Relative to DQS (DDR Write Mode)	t_{DQDMI}	1.0	—	ns	7
DD9	Input Data Skew Relative to DQS (Input Setup)	t_{DVDQ}	—	1	ns	8
DD10	Input Data Hold Relative to DQS.	t_{DIDQ}	0.25 × SD_CLK + 0.5ns	—	ns	9
DD11	DQS falling edge from SDCLK rising (output hold time)	$t_{DQLSDCH}$	0.5	—	ns	—
DD12	DQS input read preamble width (t_{RPRE})	t_{DQRPRE}	0.9	1.1	SD_CLK	—
DD13	DQS input read postamble width (t_{RPST})	t_{DQRPST}	0.4	0.6	SD_CLK	—
DD14	DQS output write preamble width (t_{WPRE})	t_{DQWPRE}	0.25	—	SD_CLK	—
DD15	DQS output write postamble width (t_{WPST})	t_{DQWPST}	0.4	0.6	SD_CLK	—

NOTES:
1. The frequency of operation is 2x or 4x the FB_CLK frequency of operation. FlexBus and SDRAM clock operate at the same frequency as the internal bus clock.
2. SD_CLK is one SDRAM clock in (ns).
3. Pulse width high plus pulse width low cannot exceed min and max clock period.
4. Command output valid should be 1/2 the memory bus clock (SD_CLK) plus some minor adjustments for process, temperature, and voltage variations.
5. This specification relates to the required input setup time of today's DDR memories. The device's output setup should be larger than the input setup of the DDR memories. If it is not larger, the input setup on the memory is in violation. MEM_DATA[31:24] is relative to MEM_DQS[3], MEM_DATA[23:16] is relative to MEM_DQS[2], MEM_DATA[15:8] is relative to MEM_DQS[1], and MEM_[7:0] is relative MEM_DQS[0].
6. The first data beat is valid before the first rising edge of DQS and after the DQS write preamble. The remaining data beats are valid for each subsequent DQS edge.

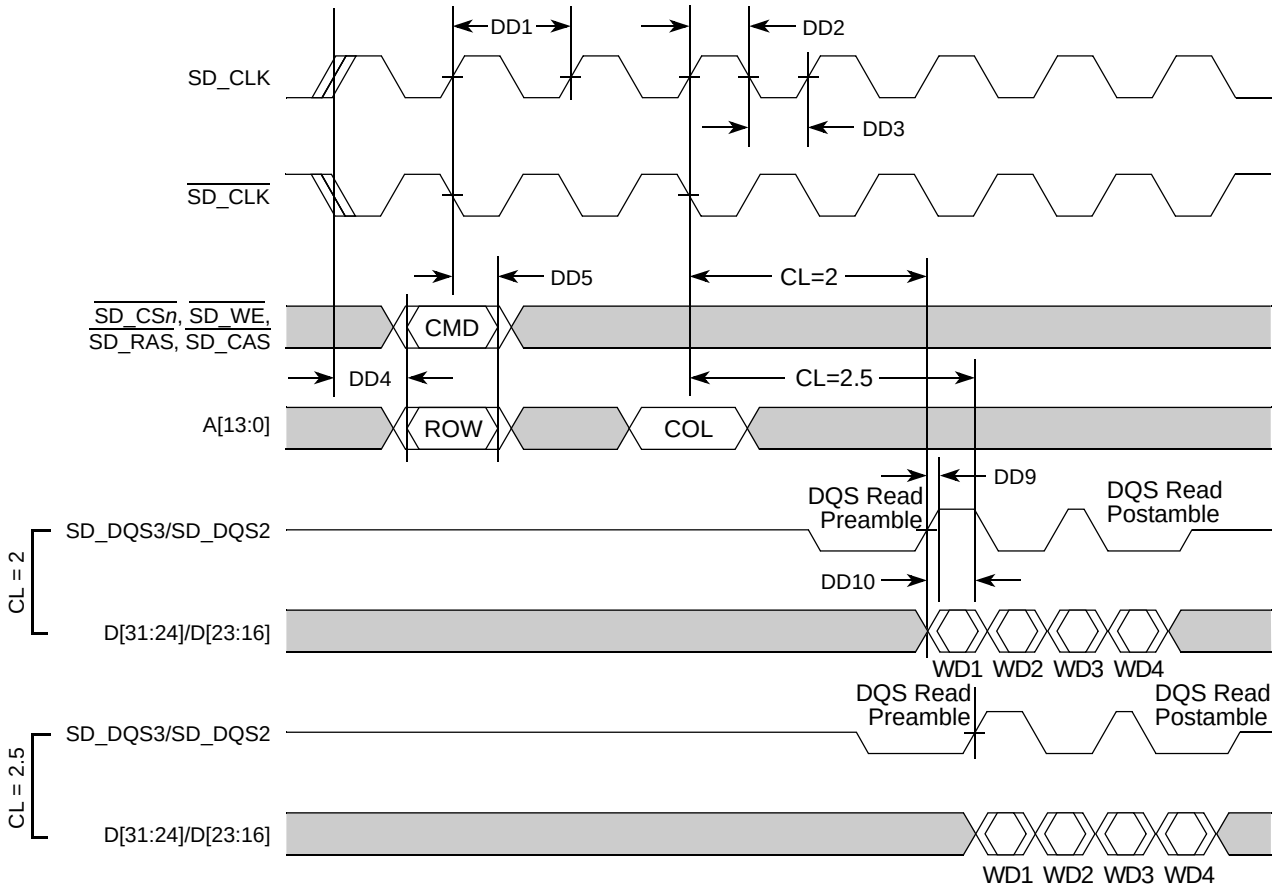


Figure 19. DDR Read Timing

5.9 General Purpose I/O Timing

Table 14. GPIO Timing[1]

Num	Characteristic	Symbol	Min	Max	Unit
G1	FB_CLK High to GPIO Output Valid	t_{CHPOV}	—	8	ns
G2	FB_CLK High to GPIO Output Invalid	t_{CHPOI}	1.5	—	ns
G3	GPIO Input Valid to FB_CLK High	t_{PVCH}	8	—	ns
G4	FB_CLK High to GPIO Input Invalid	t_{CHPI}	1.5	—	ns

NOTES:
1 GPIO spec cover: $\overline{IRQn}$, UART and Timer pins.

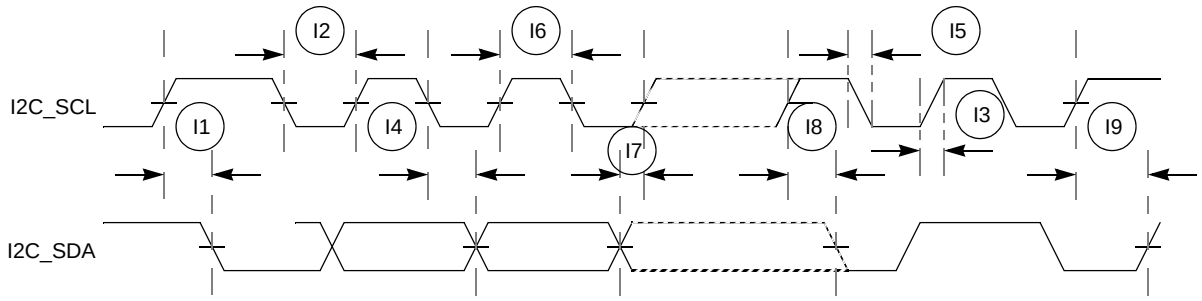


Figure 22. I²C Input/Output Timings

5.12 Fast Ethernet AC Timing Specifications

MII signals use TTL signal levels compatible with devices operating at 5.0 V or 3.3 V.

5.12.1 MII Receive Signal Timing (FEC_RXD[3:0], FEC_RXDV, FEC_RXER, and FEC_RXCLK)

The receiver functions correctly up to a FEC_RXCLK maximum frequency of 25 MHz +1%. There is no minimum frequency requirement. In addition, the processor clock frequency must exceed twice the FEC_RXCLK frequency.

Table 18 lists MII receive channel timings.

Table 18. MII Receive Signal Timing

Num	Characteristic	Min	Max	Unit
M1	FEC_RXD[3:0], FEC_RXDV, FEC_RXER to FEC_RXCLK setup	5	—	ns
M2	FEC_RXCLK to FEC_RXD[3:0], FEC_RXDV, FEC_RXER hold	5	—	ns
M3	FEC_RXCLK pulse width high	35%	65%	FEC_RXCLK period
M4	FEC_RXCLK pulse width low	35%	65%	FEC_RXCLK period

Figure 23 shows MII receive signal timings listed in Table 18.

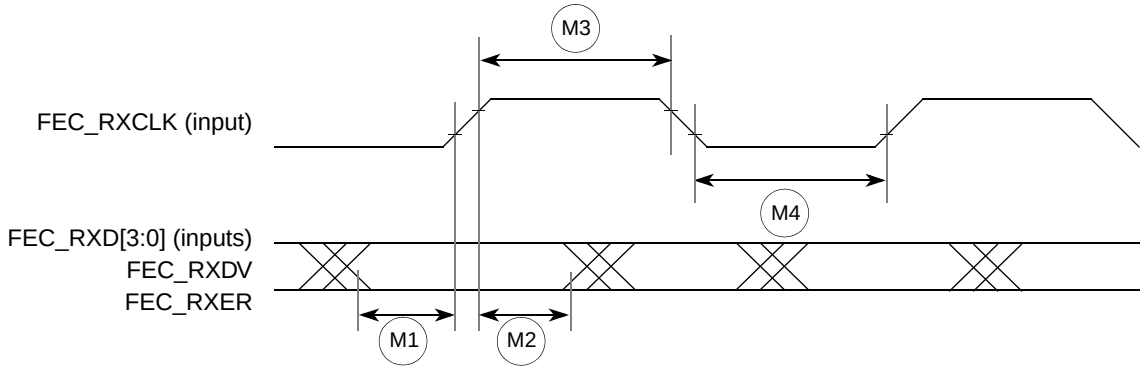


Figure 23. MII Receive Signal Timing Diagram

5.12.4 MII Serial Management Channel Timing (FEC_MDIO and FEC_MDC)

Table 21 lists MII serial management channel timings. The FEC functions correctly with a maximum MDC frequency of 2.5 MHz.

Table 21. MII Serial Management Channel Timing

Num	Characteristic	Min	Max	Unit
M10	FEC_MDC falling edge to FEC_MDIO output invalid (minimum propagation delay)	0	—	ns
M11	FEC_MDC falling edge to FEC_MDIO output valid (max prop delay)	—	25	ns
M12	FEC_MDIO (input) to FEC_MDC rising edge setup	10	—	ns
M13	FEC_MDIO (input) to FEC_MDC rising edge hold	0	—	ns
M14	FEC_MDC pulse width high	40%	60%	FEC_MDC period
M15	FEC_MDC pulse width low	40%	60%	FEC_MDC period

Figure 26 shows MII serial management channel timings listed in Table 21.

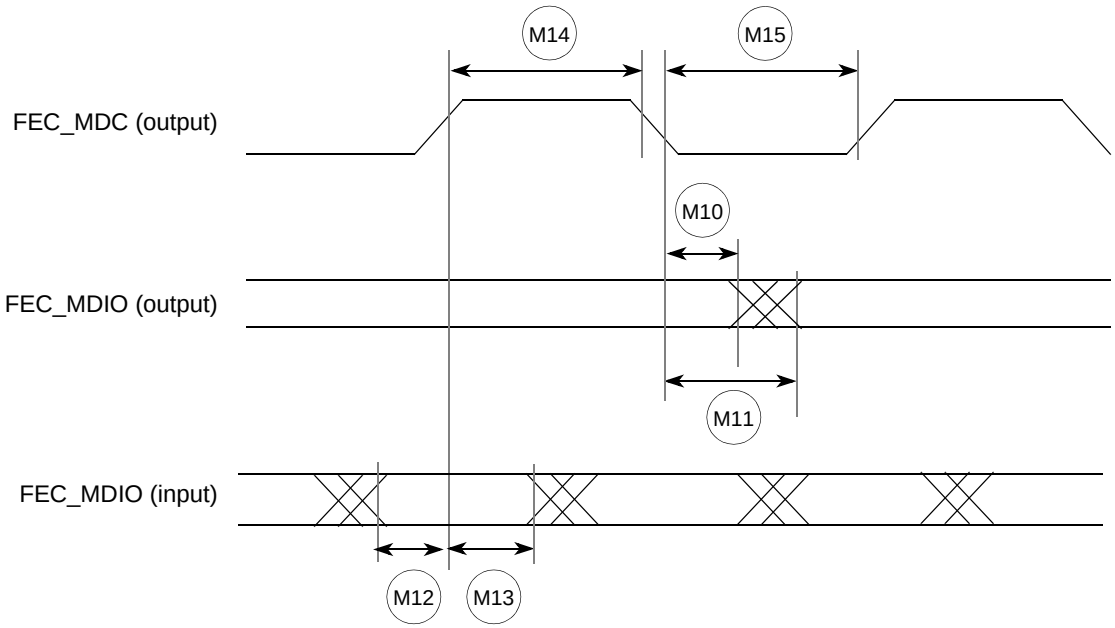


Figure 26. MII Serial Management Channel Timing Diagram

5.13 32-Bit Timer Module AC Timing Specifications

Table 22 lists timer module AC timings.

Table 22. Timer Module AC Timing Specifications

Name	Characteristic	Min	Max	Unit
T1	DT0IN / DT1IN / DT2IN / DT3IN cycle time	3	—	t_{CYC}
T2	DT0IN / DT1IN / DT2IN / DT3IN pulse width	1	—	t_{CYC}

5.14 QSPI Electrical Specifications

Table 23 lists QSPI timings.

Table 23. QSPI Modules AC Timing Specifications

Name	Characteristic	Min	Max	Unit
QS1	QSPI_CS[3:0] to QSPI_CLK	1	510	tcyc
QS2	QSPI_CLK high to QSPI_DOUT valid.	—	10	ns
QS3	QSPI_CLK high to QSPI_DOUT invalid. (Output hold)	1.5	—	ns
QS4	QSPI_DIN to QSPI_CLK (Input setup)	9	—	ns
QS5	QSPI_DIN to QSPI_CLK (Input hold)	9	—	ns

The values in Table 23 correspond to Figure 27.

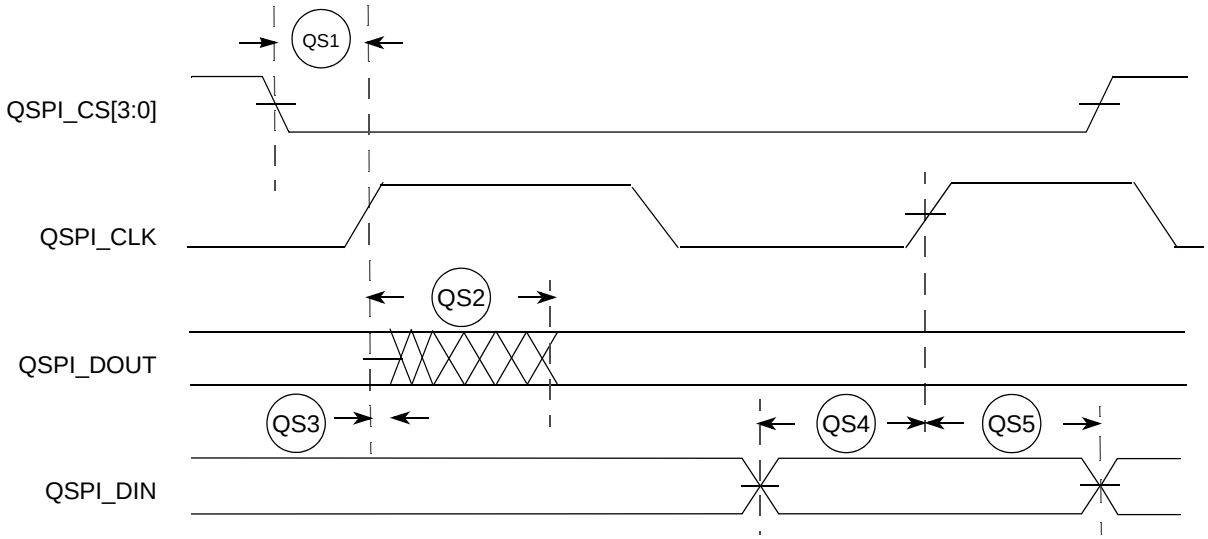


Figure 27. QSPI Timing

6 Revision History

Table 26. Revision History

Revision Number	Date	Substantive Changes
0	5/23/2005	• Initial Release
0.1	6/16/2005	• Corrected 144QFP pinout in Figure 1. Pins 139-142 incorrectly showed FEC functionality, which are actually UART 0/1 clear-to-send and request-to-send signals. • Changed maximum core frequency in Table 10, spec #2, from 240MHz to 166.67MHz. Also, changed symbols in table: f_{core} -> f_{sys} and f_{sys} -> $f_{sys/2}$ for consistency throughout document and reference manual.
0.2	8/26/2005	• Changed ball M9 from SD_VDD to EVDD in Figure 9. • Table 3: Pin 33 for 144 LQFP package should be EVDD instead of SD_VDD. $\overline{BE}/\overline{BWE}$[3:0] for 144 LQFP should be “20, 48, 18, 50“ instead of “18, 20, 48, 50” Cleaned up various electrical specifications: • Table 4: Added DDR/Memory pad supply voltage spec, changed “clock synthesizer supply voltage” to “PLL supply voltage”, changed min $PLLV_{DD}$ from -0.5 to -0.3, changed max V_{IN} from 4.0 to 3.6, changed minimum T_{stg} from -65 to -55, • Table 5: Changed TBD values in T_j entry to 105°C. • Table 7: Changed minimum core supply voltage from 1.35 to 1.4 and maximum from 1.65 to 1.6, added PLL supply voltage entry, added pad supply entries for mobile-DDR, DDR, and SDR, changed minimum input high voltage from 0.7xEV_{DD} to 2 and maximum from 3.65 to EV_{DD}+0.05, changed minimum input low voltage from VSS-0.3 to -0.05 and maximum from 0.35x$EV_{DD}$to 0.8, added input high/low voltage entries for DDR and mobile-DDR, removed high impedance leakage current entry, changed minimum output high voltage from EV_{DD}-0.5 to EV_{DD}-0.4, added DDR/bus output high/low voltage entries, removed load capacitance and DC injection current entries. • Added filtering circuits and voltage sequencing sections: Section 5.4.1, “PLL Power Filtering,” and Section 5.4.2, “Supply Voltage Sequencing and Separation Cautions.” • Removed “Operating Conditions” table from Section 5.6, “Oscillator and PLL Electrical Characteristics,” because it is redundant with Table 7. • Table 11: Changed minimum core frequency to TBD, removed external reference and on-chip PLL frequency specs to have only a CLKOUT frequency spec of TBD to 83.33MHz, removed loss of reference frequency and self-clocked mode frequency entries, in EXTAL input high/low voltage entries changed “All other modes (Dual controller (1:1), Bypass, External)” to “All other modes (External, Limp)”, removed XTAL output high/low voltage entries, removed power-up to lock time entry, removed last 5 entries (frequency un-lock range, frequency lock range, CLKOUT period jitter, frequency modulation range limit, and ICO frequency)
0.3	9/07/2005	• Corrected DRAMSEL footnote #3 in Table 3. • Updated Table 3 with 144MAPBGA pin locations. • Added 144MAPBGA ballmap to Section 4.3, “Pinout—144 MAPBGA.” • Changed J12 from PLL_VDD to IVDD in Figure 9.

Table 26. Revision History (continued)

Revision Number	Date	Substantive Changes
0.4	10/10/2005	• Figure 1 and Table 3: Changed pin 33 from EVDD to SD_VDD • Figure 4 and Table 3: Changed ball D10 from TEST to VSS • Figure 6 and Table 3: Changed pin 39 from EVDD to SD_VDD and pin 117 from TEST to VSS
0.5	3/29/2006	• Added “top view” and “bottom view” labels where appropriate to mechanical drawings and pinouts. • Updated mechanical drawings to latest available, and added note to Section 4, “Mechanicals and Pinouts.”
0.6	7/21/2006	• Corrected cross-reference to Figure 9 in Section 4.7, “Pinout—196 MAPBGA.” • Corrected L3 label in Figure 9 from SD_DR_DQS to SD_SDR_DQS. • Corrected L6 label in Figure 9 from SD_DQS0 to SD_DQS2 and H3 from SD_DQS1 to SD_DQS3. • Removed second sentence from Section 5.12.2, “MII Transmit Signal Timing (FEC_TXD[3:0], FEC_TXEN, FEC_TXER, FEC_TXCLK),” regarding no minimum frequency requirement for TXCLK. • Removed third and fourth paragraphs from Section 5.12.2, “MII Transmit Signal Timing (FEC_TXD[3:0], FEC_TXEN, FEC_TXER, FEC_TXCLK),” as this feature is not supported on this device.
1	3/28/2007	• Removed preliminary designation from Section 5, “Electrical Characteristics.” • Updated Section 5.2, “Thermal Characteristics.” • Updated Section 5.4, “DC Electrical Specifications.” • Added Section 5.5, “Current Consumption.” • Updated Section 5.6, “Oscillator and PLL Electrical Characteristics.” • Made some corrections to the drawings in Section 5.8, “SDRAM Bus.” • Edited for grammar, punctuation, spelling, style, and format. - JD
2	12/4/2008	• Updated FlexBus read and write timing diagrams in Figure 14 and Figure 15. Changed the following specs in Table 12 and Table 13: • Minimum frequency of operation from TBD to 60MHz • Maximum clock period from TBD to 16.67 ns
3	9/1/2009	• Changed doc type from Advance Information to Technical Data