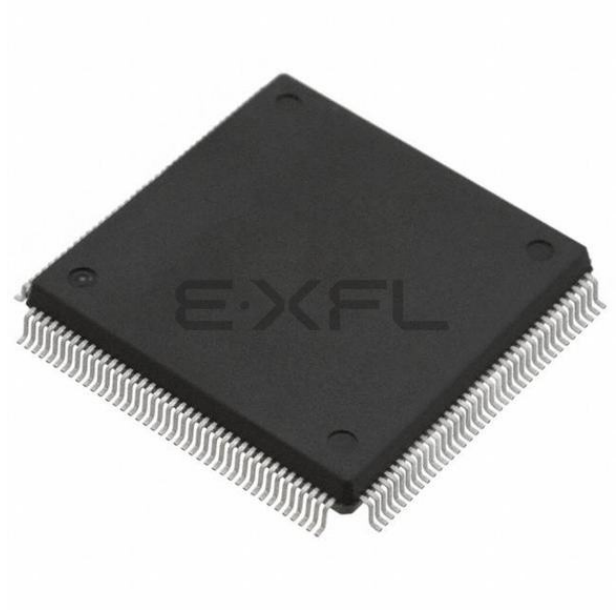

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | Coldfire V2 |
| Core Size | 32-Bit Single-Core |
| Speed | 166.67MHz |
| Connectivity | EBI/EMI, Ethernet, I²C, SPI, UART/USART |
| Peripherals | DMA, WDT |
| Number of I/O | 50 |
| Program Memory Size | - |
| Program Memory Type | ROMless |
| EEPROM Size | - |
| RAM Size | 16K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.4V ~ 3.6V |
| Data Converters | - |
| Oscillator Type | External |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 160-BQFP |
| Supplier Device Package | 160-QFP (28x28) |
| Purchase URL | https://www.e-xfl.com/product-detail/nxp-semiconductors/mcf5208cab166 |

# 1 MCF5207/8 Device Configurations

The following table compares the two devices described in this document:

**Table 1. MCF5207 & MCF5208 Configurations**

| Module | MCF5207 | MCF5208 |
|---|---|---|
| Version 2 ColdFire Core with EMAC (Enhanced Multiply-Accumulate Unit) | • | • |
| Core (System) Clock | up to 166.67 MHz | |
| Peripheral and External Bus Clock (Core clock ÷ 2) | up to 83.33 MHz | |
| Performance (Dhrystone/2.1 MIPS) | up to 159 | |
| Instruction/Data Cache | 8 Kbytes | |
| Static RAM (SRAM) | 16 Kbytes | |
| SDR/DDR SDRAM Controller | • | • |
| Fast Ethernet Controller (FEC) | — | • |
| Low-Power Management Module | • | • |
| UARTs | 3 | 3 |
| $I^2C$ | • | • |
| QSPI | • | • |
| 32-bit DMA Timers | 4 | 4 |
| Watchdog Timer (WDT) | • | • |
| Periodic Interrupt Timers (PIT) | 4 | 4 |
| Edge Port Module (EPORT) | • | • |
| Interrupt Controllers (INTC) | 1 | 1 |
| 16-channel Direct Memory Access (DMA) | • | • |
| FlexBus External Interface | • | • |
| General Purpose I/O Module (GPIO) | • | • |
| JTAG - IEEE® 1149.1 Test Access Port | • | • |
| Package | 144 LQFP<br>144 MAPBGA | 160 QFP<br>196 MAPBGA |

# 2 Ordering Information

**Table 2. Orderable Part Numbers**

| Freescale Part Number | Description | Speed | Temperature |
|---|---|---|---|
| MCF5207CAG166 | MCF5207 RISC Microprocessor, 144 LQFP | 166.67 MHz | –40° to +85° C |
| MCF5207CVM166 | MCF5207 RISC Microprocessor, 144 MAPBGA | 166.67 MHz | –40° to +85° C |
| MCF5208CAB166 | MCF5208 RISC Microprocessor, 160 QFP | 166.67 MHz | –40° to +85° C |
| MCF5208CVM166 | MCF5208 RISC Microprocessor, 196 MAPBGA | 166.67 MHz | –40° to +85° C |

# 3 Signal Descriptions

The following table lists all the MCF5208 pins grouped by function. The Dir column is the direction for the primary function of the pin only. Refer to Section 4, "Mechanicals and Pinouts" for package diagrams. For a more detailed discussion of the MCF5208 signals, consult the *MCF5208 Reference Manual* (MCF5208RM).

**NOTE**

In this table and throughout this document, a single signal within a group is designated without square brackets (i.e., A23), while designations for multiple signals within a group use brackets (i.e., A[23:21]) and is meant to include all signals within the two bracketed numbers when these numbers are separated by a colon.

**NOTE**

The primary functionality of a pin is not necessarily its default functionality. Pins that are muxed with GPIO default to their GPIO functionality.

**Table 3. MCF5207/8 Signal Information and Muxing**

| Signal Name | GPIO | Alternate 1 | Alternate 2 | Dir.[1] | Voltage Domain | MCF5207 144 LQFP | MCF5207 144 MAPBGA | MCF5208 160 QFP | MCF5208 196 MAPBGA |
|---|---|---|---|---|---|---|---|---|---|
| **Reset** | | | | | | | | | |
| $\overline{\text{RESET}}$[2] | — | — | — | I | EVDD | 82 | J10 | 90 | J14 |
| $\overline{\text{RSTOUT}}$ | — | — | — | O | EVDD | 74 | M12 | 82 | N14 |
| **Clock** | | | | | | | | | |
| EXTAL | — | — | — | I | EVDD | 78 | K12 | 86 | L14 |
| XTAL | — | — | — | O | EVDD | 80 | J12 | 88 | K14 |
| FB_CLK | — | — | — | O | SDVDD | 34 | L1 | 40 | N1 |
| **Mode Selection** | | | | | | | | | |
| $\overline{\text{RCON}}$[2] | — | — | — | I | EVDD | 144 | C4 | 160 | C3 |
| DRAMSEL | — | — | — | I | EVDD | 79 | H10 | 87 | K11 |
| **FlexBus** | | | | | | | | | |
| A[23:22] | — | $\overline{\text{FB\_CS}}$[5:4] | — | O | SDVDD | 118, 117 | B9, A10 | 126, 125 | B11, A11 |
| A[21:16] | — | — | — | O | SDVDD | 116–114, 112, 108, 107 | C9, A11, B10, A12, C11, B11 | 124, 123, 122, 120, 116, 115 | B12, A12, A13, B13, B14, C13 |
| A[15:14] | — | SD_BA[1:0][3] | — | O | SDVDD | 106, 105 | B12, C12 | 114, 113 | C14, D12 |
| A[13:11] | — | SD_A[13:11][3] | — | O | SDVDD | 104–102 | D11, E10, D12 | 112, 111, 110 | D13, D14, E11 |
| A10 | — | — | — | O | SDVDD | 101 | C10 | 109 | E12 |

**Table 3. MCF5207/8 Signal Information and Muxing (continued)**

| Signal Name | GPIO | Alternate 1 | Alternate 2 | Dir.[1] | Voltage Domain | MCF5207 144 LQFP | MCF5207 144 MAPBGA | MCF5208 160 QFP | MCF5208 196 MAPBGA |
|---|---|---|---|---|---|---|---|---|---|
| **QSPI** | | | | | | | | | |
| QSPI_CS2 | PQSPI3 | $\overline{\text{DACK0}}$ | $\overline{\text{U2RTS}}$ | O | EVDD | 126 | A8 | 132 | D10 |
| QSPI_CLK | PQSPI0 | I2C_SCL[2] | — | O | EVDD | 127 | C7 | 133 | A9 |
| QSPI_DOUT | PQSPI1 | I2C_SDA[2] | — | O | EVDD | 128 | A7 | 134 | B9 |
| QSPI_DIN | PQSPI2 | $\overline{\text{DREQ0}}$[2] | $\overline{\text{U2CTS}}$ | I | EVDD | 129 | B7 | 135 | C9 |
| **Note:** The QSPI_CS1 and QSPI_CS0 signals are available on the $\overline{\text{U1CTS}}$, $\overline{\text{U1RTS}}$, $\overline{\text{U0CTS}}$, or $\overline{\text{U0RTS}}$ pins for the 196 and 160-pin packages. | | | | | | | | | |
| **UARTs** | | | | | | | | | |
| $\overline{\text{U1CTS}}$ | PUARTL7 | DT1IN | QSPI_CS1 | I | EVDD | — | — | 136 | D9 |
| $\overline{\text{U1RTS}}$ | PUARTL6 | DT1OUT | QSPI_CS1 | O | EVDD | — | — | 137 | C8 |
| U1TXD | PUARTL5 | — | — | O | EVDD | 131 | A6 | 139 | A8 |
| U1RXD | PUARTL4 | — | — | I | EVDD | 130 | D6 | 138 | B8 |
| $\overline{\text{U0CTS}}$ | PUARTL3 | DT0IN | QSPI_CS0 | I | EVDD | — | — | 76 | N12 |
| $\overline{\text{U0RTS}}$ | PUARTL2 | DT0OUT | QSPI_CS0 | O | EVDD | — | — | 77 | P12 |
| U0TXD | PUARTL1 | — | — | O | EVDD | 71 | L10 | 79 | P13 |
| U0RXD | PUARTL0 | — | — | I | EVDD | 70 | M10 | 78 | N13 |
| **Note:** The UART2 signals are multiplexed on the DMA Timers, QSPI, FEC, and I2C pins. For the MCF5207 devices, the UART0 and UART1 control signals are multiplexed internally on the FEC signals. | | | | | | | | | |
| **DMA Timers** | | | | | | | | | |
| DT3IN | PTIMER3 | DT3OUT | $\overline{\text{U2CTS}}$ | I | EVDD | 135 | B5 | 143 | B7 |
| DT2IN | PTIMER2 | DT2OUT | $\overline{\text{U2RTS}}$ | I | EVDD | 136 | C5 | 144 | A7 |
| DT1IN | PTIMER1 | DT1OUT | U2RXD | I | EVDD | 137 | A4 | 145 | A6 |
| DT0IN | PTIMER0 | DT0OUT | U2TXD | I | EVDD | 138 | A3 | 146 | B6 |
| **BDM/JTAG[6]** | | | | | | | | | |
| JTAG_EN[7] | — | — | — | I | EVDD | 83 | J11 | 91 | J13 |
| DSCLK | — | $\overline{\text{TRST}}$[2] | — | I | EVDD | 76 | K11 | 84 | L12 |
| PSTCLK | — | TCLK[2] | — | O | EVDD | 64 | M7 | 70 | P9 |
| $\overline{\text{BKPT}}$ | — | TMS[2] | — | I | EVDD | 75 | L12 | 83 | M14 |
| DSI | — | TDI[2] | — | I | EVDD | 77 | H9 | 85 | K12 |
| DSO | — | TDO | — | O | EVDD | 69 | M9 | 75 | M12 |
| DDATA[3:0] | — | — | — | O | EVDD | — | K9, L9, M11, M8 | — | P11, N11, M11, P10 |
| PST[3:0] | — | — | — | O | EVDD | — | L11, L8, K10, K8 | — | N10, M10, L10, L9 |

# 4.3 Pinout—144 MAPBGA

The pinout of the MCF5207CVM166 device is shown below.

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A | SD_CS | U1RTS | DT0IN | DT1IN | IRQ7 | U1TXD | QSPI_DOUT | QSPI_CS2 | FB_CS2 | A22 | A20 | A18 | A |
| B | D14 | D15 | TS | U1CTS | DT3IN | IRQ1 | QSPI_DIN | FB_CS0 | A23 | A19 | A16 | A15 | B |
| C | D12 | D13 | SD_CKE | RCON | DT2IN | IRQ4 | QSPI_CLK | FB_CS1 | A21 | A10 | A17 | A14 | C |
| D | D10 | D11 | SD_WE | IVDD | U0RTS | U1RXD | FB_CS3 | IVDD | A8 | VSS | A13 | A11 | D |
| E | D8 | D9 | BE/BWE1 | U0CTS | EVDD | EVDD | SD_VDD | SD_VDD | A4 | A12 | A9 | A7 | E |
| F | D31 | D30 | SD_DQS3 | BE/BWE3 | EVDD | VSS | VSS | SD_VDD | A0 | A6 | A5 | A3 | F |
| G | D29 | D28 | D26 | D27 | SD_VDD | VSS | VSS | EVDD | EVDD | A2 | TA | A1 | G |
| H | D25 | D24 | SD_SDR_DQS | IVDD | SD_VDD | SD_VDD | EVDD | EVDD | TDI/DSI | DRAM SEL | IVDD | PLL_VDD | H |
| J | SD_CLK | SD_RAS | SD_VDD | D18 | BE/BWE0 | D4 | D2 | OE | IVDD | RESET | JTAG_EN | XTAL | J |
| K | SD_CLK | D20 | D23 | D16 | D6 | R/W | D0 | PST0 | DDATA3 | PST1 | TRST/DSCLK | EXTAL | K |
| L | FB_CLK | D22 | D21 | BE/BWE2 | D7 | D5 | D1 | PST2 | DDATA2 | U0TXD | PST3 | TMS/BKPT | L |
| M | SD_A10 | SD_CAS | D19 | D17 | SD_DQS2 | D3 | TCLK/PSTCLK | DDATA0 | TDO/DSO | U0RXD | DDATA1 | RSTOUT | M |
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | |

**Figure 4. MCF5207CVM166 Pinout Top View (144 MAPBGA)**

## 4.6 Package Dimensions—160 QFP

The package dimensions of the MCF5208CAB166 device are shown in the figures below.

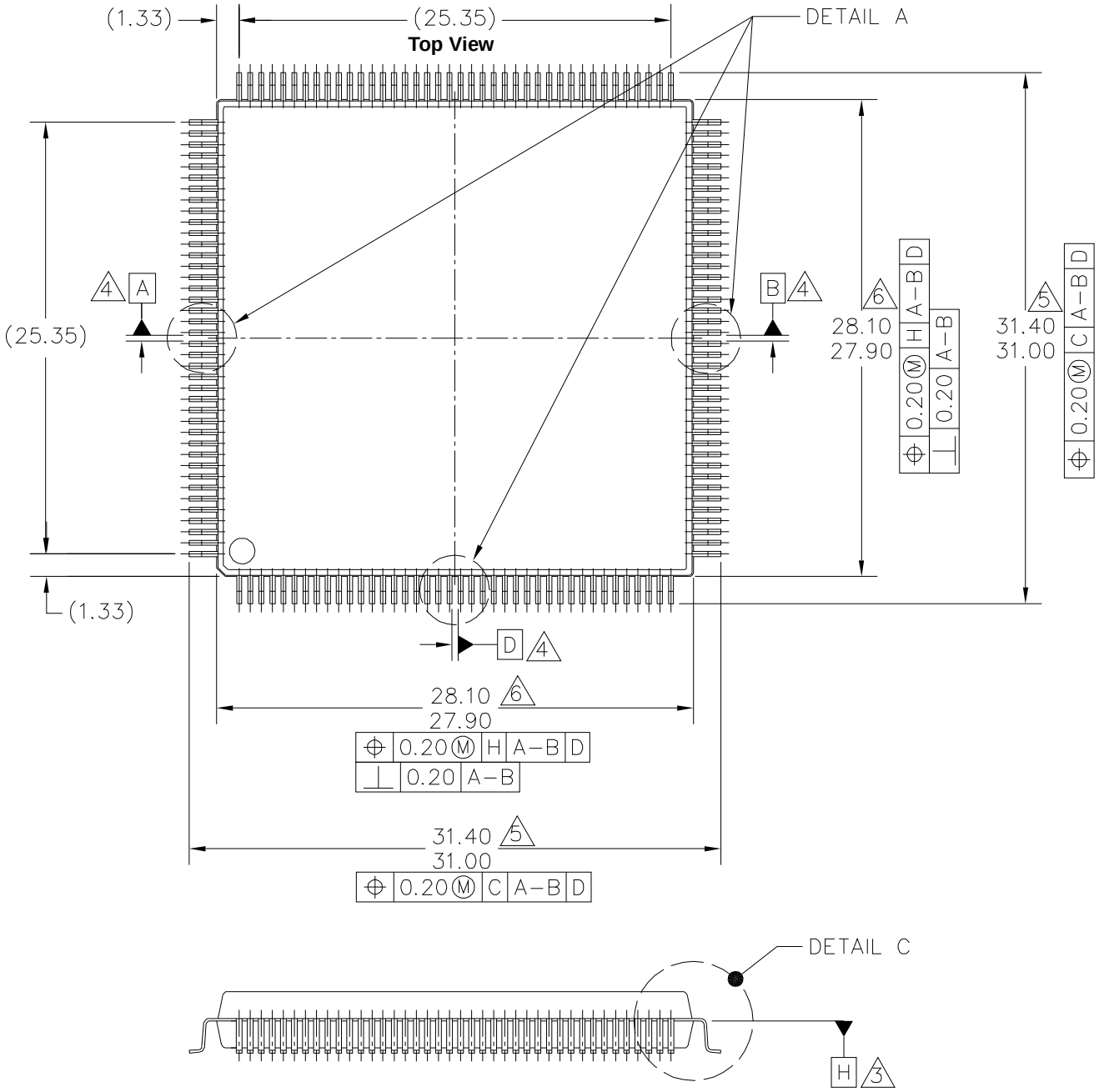
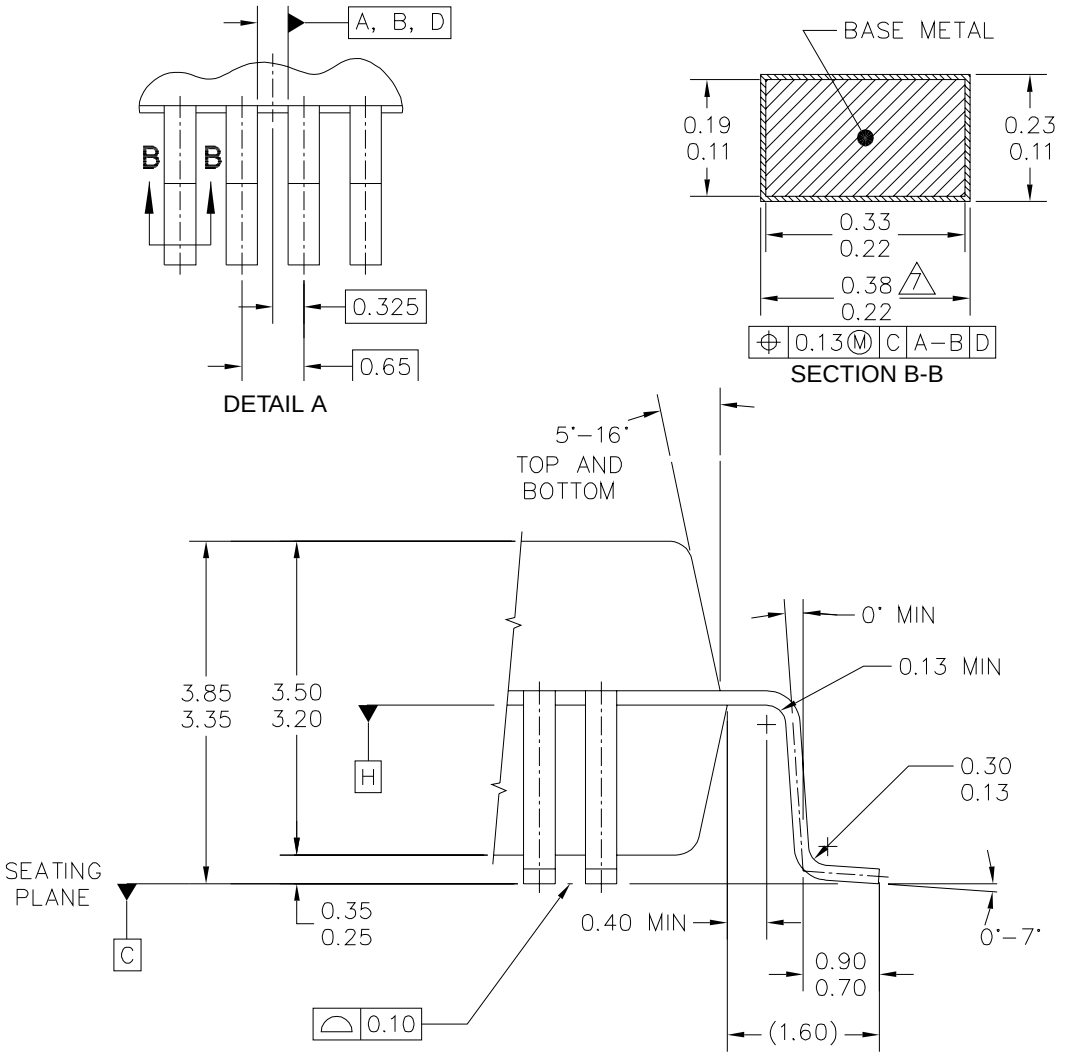



**Figure 7. MCF5208CAB166 Package Dimensions (Sheet 1 of 2)**




NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.

2. CONTROLLING DIMENSION: MILLIMETER.

3. DATUM PLANE IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.

4. DATUMS TO BE DETERMINED AT DATUM PLANE H.

5. DIMENSIONS TO BE DETERMINED AT SEATING PLANE C.

6. DIMENSIONS DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 PER SIDE. DIMENSIONS DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.

7. DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.

**Figure 8. MCF5208CAB166 Package Dimensions (Sheet 2 of 2)**

**Table 4. Absolute Maximum Ratings[1, 2] (continued)**

| | | | |
|---|---|---|---|
| Operating Temperature Range (Packaged) | $T_A$ ($T_L$ - $T_H$) | – 40 to 85 | °C |
| Storage Temperature Range | $T_{stg}$ | – 55 to 150 | °C |

NOTES:
1. Functional operating conditions are given in Section 5.4, "DC Electrical Specifications". Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Continued operation at these levels may affect device reliability or cause permanent damage to the device.
2. This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level ($V_{SS}$ or $EV_{DD}$).
3. Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.
4. All functional non-supply pins are internally clamped to $V_{SS}$ and $EV_{DD}$.
5. Power supply must maintain regulation within operating $EV_{DD}$ range during instantaneous and operating maximum current conditions. If positive injection current ($V_{in} > EV_{DD}$) is greater than $I_{DD}$, the injection current may flow out of $EV_{DD}$ and could result in external power supply going out of regulation. Ensure external $EV_{DD}$ load shunts current greater than maximum injection current. This is the greatest risk when the MCU is not consuming power (ex; no clock). Power supply must maintain regulation within operating $EV_{DD}$ range during instantaneous and operating maximum current conditions.

# 5.2 Thermal Characteristics

Table 5 lists thermal resistance values

**Table 5. Thermal Characteristics**

| Characteristic | | Symbol | 196MBGA | 144MBGA | 160QFP | 144LQFP | Unit |
|---|---|---|---|---|---|---|---|
| Junction to ambient, natural convection | Four layer board (2s2p) | $\theta_{JMA}$ | 47[1,2] | 47[1,2] | 49[1,2] | 65[1,2] | °C/W |
| Junction to ambient (@200 ft/min) | Four layer board (2s2p) | $\theta_{JMA}$ | 43[1,2] | 43[1,2] | 44[1,2] | 58[1,2] | °C/W |
| Junction to board | | $\theta_{JB}$ | 36[3] | 36[3] | 40[3] | 50[3] | °C/W |
| Junction to case | | $\theta_{JC}$ | 22[4] | 22[4] | 39[4] | 19[4] | °C/W |
| Junction to top of package | | $\Psi_{jt}$ | 6[1,5] | 6[1,5] | 12[1,6] | 5[1,7] | °C/W |
| Maximum operating junction temperature | | $T_j$ | 105 | 105 | 105 | 105 | °C |

NOTES:
1. $\theta_{JMA}$ and $\Psi_{jt}$ parameters are simulated in conformance with EIA/JESD Standard 51-2 for natural convection. Freescale recommends the use of $\theta_{JmA}$ and power dissipation specifications in the system design to prevent device junction temperatures from exceeding the rated specification. System designers should be aware that device junction temperatures can be significantly influenced by board layout and surrounding devices. Conformance to the device junction temperature specification can be verified by physical measurement in the customer's system using the $\Psi_{jt}$ parameter, the device power dissipation, and the method described in EIA/JESD Standard 51-2.
2. Per JEDEC JESD51-6 with the board horizontal.

**Table 7. DC Electrical Specifications (continued)**

| Characteristic | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Weak Internal Pull Up Device Current, tested at $V_{IL}$ Max.[1] | $I_{APU}$ | -10 | - 130 | µA |
| Input Capacitance [2]<br>All input-only pins<br>All input/output (three-state) pins | $C_{in}$ | <br>—<br>— | <br>7<br>7 | pF |

NOTES:
1 Refer to the signals section for pins having weak internal pull-up devices.
2 This parameter is characterized before qualification rather than 100% tested.

## 5.4.1 PLL Power Filtering

To further enhance noise isolation, an external filter is strongly recommended for PLL analog $V_{DD}$ pins. The filter shown in Figure 11 should be connected between the board $V_{DD}$ and the $PLLV_{DD}$ pins. The resistor and capacitors should be placed as close to the dedicated $PLLV_{DD}$ pin as possible.

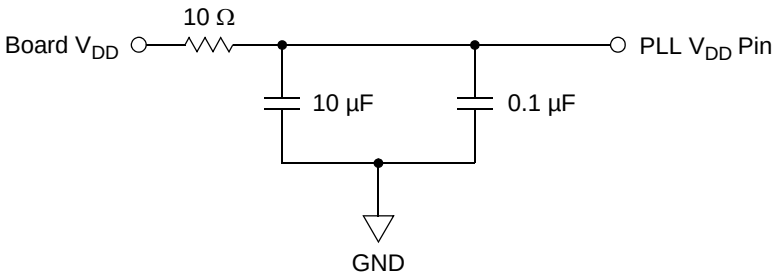



**Figure 11. System PLL $V_{DD}$ Power Filter**

## 5.4.2 Supply Voltage Sequencing and Separation Cautions

The relationship between $SDV_{DD}$ and $EV_{DD}$ is non-critical during power-up and power-down sequences. $SDV_{DD}$ (2.5V or 3.3V) and $EV_{DD}$ are specified relative to $IV_{DD}$.

### 5.4.2.1 Power Up Sequence

If $EV_{DD}/SDV_{DD}$ are powered up with $IV_{DD}$ at 0 V, the sense circuits in the I/O pads cause all pad output drivers connected to the $EV_{DD}/SDV_{DD}$ to be in a high impedance state. There is no limit on how long after $EV_{DD}/SDV_{DD}$ powers up before $IV_{DD}$ must power up. $IV_{DD}$ should not lead the $EV_{DD}$, $SDV_{DD}$, or $PLLV_{DD}$ by more than 0.4 V during power ramp-up or there will be high current in the internal ESD protection diodes. The rise times on the power supplies should be slower than 500 us to avoid turning on the internal ESD protection clamp diodes.

### 5.4.2.2 Power Down Sequence

If $IV_{DD}/PLLV_{DD}$ are powered down first, sense circuits in the I/O pads cause all output drivers to be in a high impedance state. There is no limit on how long after $IV_{DD}$ and $PLLV_{DD}$ power down before $EV_{DD}$ or $SDV_{DD}$ must power down. $IV_{DD}$ should not lag $EV_{DD}$, $SDV_{DD}$, or $PLLV_{DD}$ going low by more than

5 See the description of the low-power control register (LCPR) in the *MCF5208 Reference Manual* for more information on stop modes 0–3.

The figure below illustrates the power consumption in a graphical format.

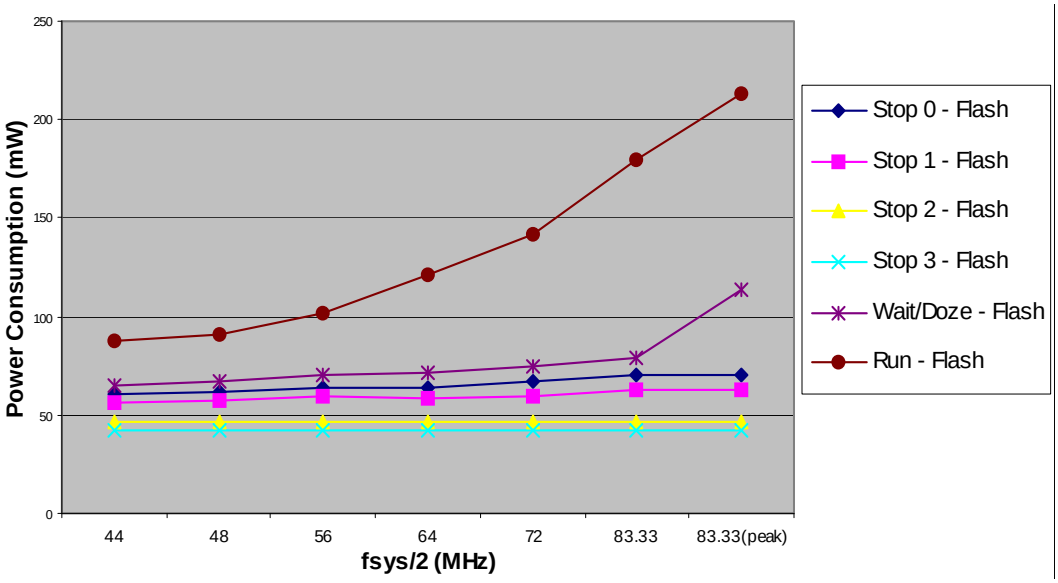



**Figure 12. Current Consumption in Low-Power Modes**

**Table 9. Typical Active Current Consumption Specifications[1]**

| $f_{sys/2}$ Frequency | Voltage (V) | Typical[2] Active (mA) | | Peak[3] Active (mA) |
|---|---|---|---|---|
| | | SRAM | Flash | |
| 1 MHz | 3.3 | 2.04 | 2.12 | 2.28 |
| | 2.5 | 15.24 | 15.32 | 15.24 |
| | 1.5 | 1.30 | 1.41 | 1.49 |
| 2 MHz | 3.3 | 2.23 | 2.40 | 3.57 |
| | 2.5 | 15.26 | 15.42 | 15.26 |
| | 1.5 | 1.71 | 1.92 | 2.09 |
| 4 MHz | 3.3 | 2.60 | 2.95 | 3.58 |
| | 2.5 | 15.30 | 15.61 | 15.30 |
| | 1.5 | 2.49 | 2.95 | 3.29 |
| 44 MHz | 3.3 | 7.61 | 17.67 | 25.34 |
| | 2.5 | 16.13 | 19.49 | 16.95 |
| | 1.5 | 24.04 | 28.72 | 39.02 |
| 48 MHz | 3.3 | 8.16 | 26.21 | 34.45 |
| | 2.5 | 16.28 | 20.06 | 17.17 |
| | 1.5 | 26.05 | 31.13 | 42.30 |

**Table 10. PLL Electrical Characteristics (continued)**

| Num | Characteristic | Symbol | Min. Value | Max. Value | Unit |
|---|---|---|---|---|---|
| 9 | XTAL Current | $I_{XTAL}$ | 1 | 3 | mA |
| 10 | Total on-chip stray capacitance on XTAL | $C_{S\_XTAL}$ | | 1.5 | pF |
| 11 | Total on-chip stray capacitance on EXTAL | $C_{S\_EXTAL}$ | | 1.5 | pF |
| 12 | Crystal capacitive load | $C_L$ | | See crystal spec | |
| 13 | Discrete load capacitance for XTAL | $C_{L\_XTAL}$ | | $2*C_L - C_{S\_XTAL} - C_{PCB\_XTAL}$ [7] | pF |
| 14 | Discrete load capacitance for EXTAL | $C_{L\_EXTAL}$ | | $2*C_L - C_{S\_EXTAL} - C_{PCB\_EXTAL}$ [7] | pF |
| 17 | CLKOUT Period Jitter, [3, 4, 7, 8, 9] Measured at $f_{SYS}$ Max<br>Peak-to-peak Jitter (Clock edge to clock edge)<br>Long Term Jitter | $C_{jitter}$ | <br>—<br>— | <br>10<br>TBD | <br>% $f_{sys/2}$<br>% $f_{sys/2}$ |
| 18 | Frequency Modulation Range Limit [3, 10, 11]<br>($f_{sys}$Max must not be exceeded) | $C_{mod}$ | 0.8 | 2.2 | %$f_{sys/2}$ |
| 19 | VCO Frequency. $f_{vco} = (f_{ref} * PFD)/4$ | $f_{vco}$ | 350 | 540 | MHz |

NOTES:
1. The maximum allowable input clock frequency when booting with the PLL enabled is 24 MHz. For higher input clock frequencies, the processor must boot in LIMP mode to avoid violating the maximum allowable CPU frequency.
2. All internal registers retain data at 0 Hz.
3. This parameter is guaranteed by characterization before qualification rather than 100% tested.
4. Proper PC board layout procedures must be followed to achieve specifications.
5. This parameter is guaranteed by design rather than 100% tested.
6. This specification is the PLL lock time only and does not include oscillator start-up time.
7. $C_{PCB\_EXTAL}$ and $C_{PCB\_XTAL}$ are the measured PCB stray capacitances on EXTAL and XTAL, respectively.
8. Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum $f_{sys}$. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the PLL circuitry via PLL $V_{DD}$, $EV_{DD}$, and $V_{SS}$ and variation in crystal oscillator frequency increase the Cjitter percentage for a given interval.
9. Values are with frequency modulation disabled. If frequency modulation is enabled, jitter is the sum of Cjitter+Cmod.
10. Modulation percentage applies over an interval of 10µs, or equivalently the modulation rate is 100KHz.
11. Modulation range determined by hardware design.

## 5.7 External Interface Timing Characteristics

Table 11 lists processor bus input timings.

**NOTE**

All processor bus timings are synchronous; that is, input setup/hold and output delay with respect to the rising edge of a reference clock. The reference clock is the FB_CLK output.

All other timing relationships can be derived from these values. Timings listed in Table 11 are shown in Figure 14 and Figure 15.

* The timings are also valid for inputs sampled on the negative clock edge.

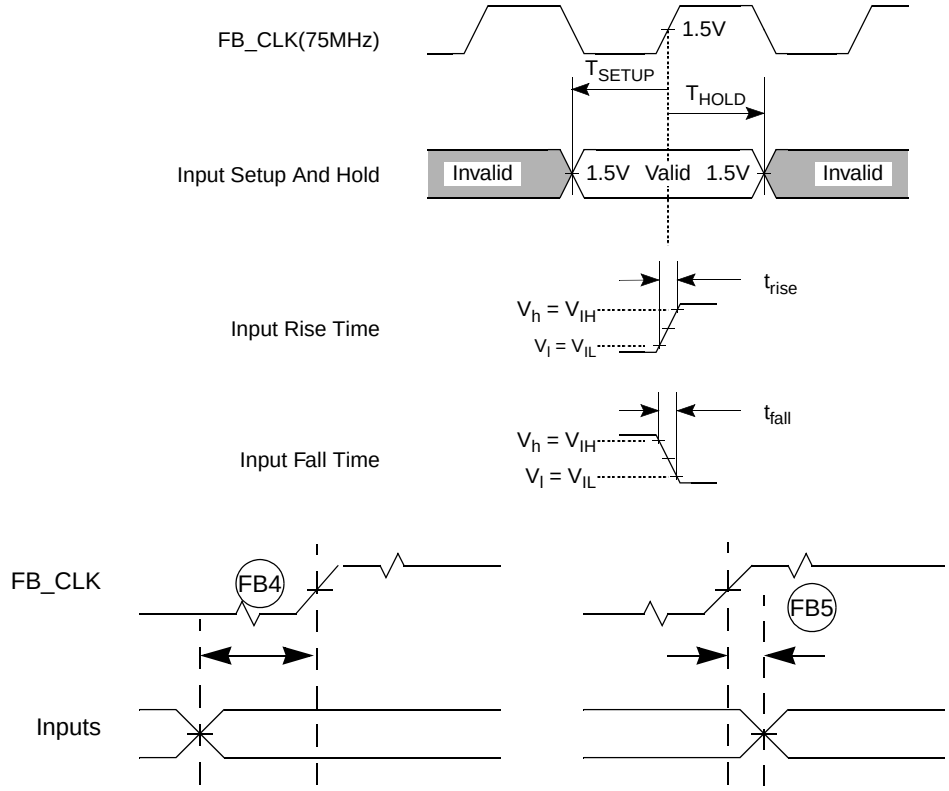



**Figure 13. General Input Timing Requirements**

## 5.7.1 FlexBus

FlexBus is a multi-function external bus interface provided to interface to slave-only devices up to a maximum bus frequency of 83.33 MHz. It can be directly connected to asynchronous or synchronous devices such as external boot ROMs, flash memories, gate-array logic, or other simple target (slave) devices with little or no additional circuitry. For asynchronous devices, a simple chip-select based interface can be used. The FlexBus interface has six general purpose chip-selects ($\overline{\text{FB\_CS}}$[5:0]) that can be configured to be distributed between the FlexBus or SDRAM memory interfaces. Chip-select $\overline{\text{FB\_CS}}$[0] can be dedicated to boot ROM access and can be programmed to be byte (8 bits), word (16 bits), or longword (32 bits) wide. Control signal timing is compatible with common ROM/flash memories.

7 This specification relates to the required hold time of today's DDR memories. MEM_DATA[31:24] is relative to MEM_DQS[3], MEM_DATA[23:16] is relative to MEM_DQS[2], MEM_DATA[15:8] is relative to MEM_DQS[1], and MEM_[7:0] is relative MEM_DQS[0].

8 Data input skew is derived from each DQS clock edge. It begins with a DQS transition and ends when the last data line becomes valid. This input skew must include DDR memory output skew and system level board skew (due to routing or other factors).

9 Data input hold is derived from each DQS clock edge. It begins with a DQS transition and ends when the first data line becomes invalid.

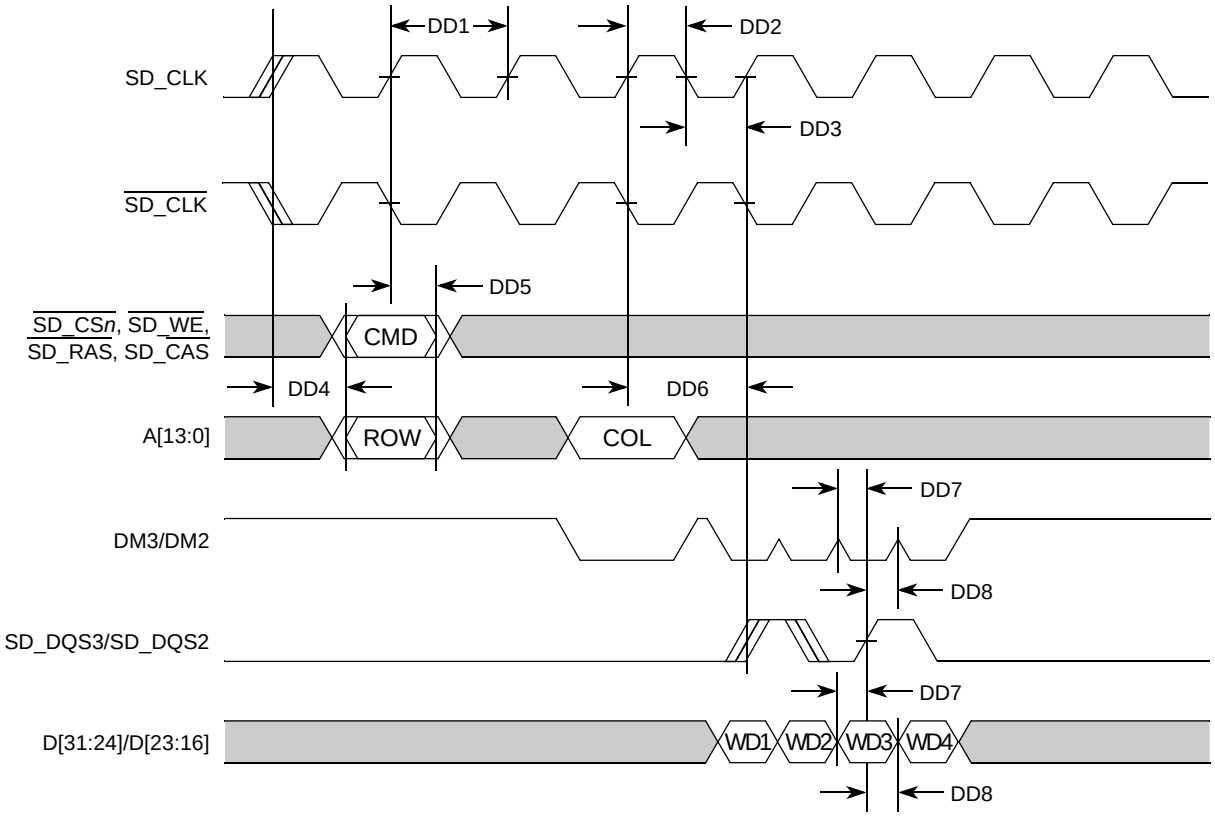



**Figure 18. DDR Write Timing**

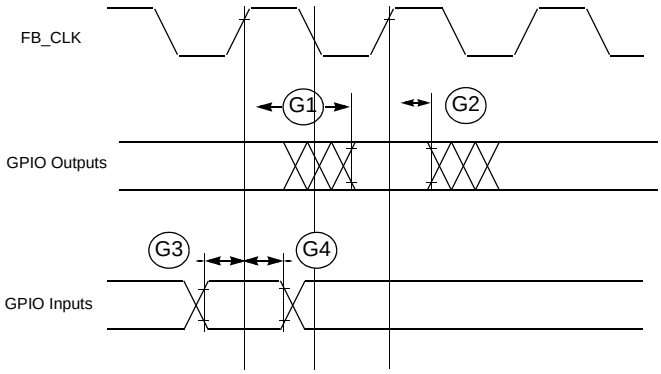



**Figure 20. GPIO Timing**

# 5.10 Reset and Configuration Override Timing

**Table 15. Reset and Configuration Override Timing**

| Num | Characteristic | Symbol | Min | Max | Unit |
|---|---|---|---|---|---|
| R1 | $\overline{\text{RESET}}$ Input valid to FB_CLK High | $t_{RVCH}$ | 9 | — | ns |
| R2 | FB_CLK High to $\overline{\text{RESET}}$ Input invalid | $t_{CHRI}$ | 1.5 | — | ns |
| R3 | $\overline{\text{RESET}}$ Input valid Time [1] | $t_{RIVT}$ | 5 | — | $t_{CYC}$ |
| R4 | FB_CLK High to $\overline{\text{RSTOUT}}$ Valid | $t_{CHROV}$ | — | 10 | ns |
| R5 | $\overline{\text{RSTOUT}}$ valid to Config. Overrides valid | $t_{ROVCV}$ | 0 | — | ns |
| R6 | Configuration Override Setup Time to $\overline{\text{RSTOUT}}$ invalid | $t_{COS}$ | 20 | — | $t_{CYC}$ |
| R7 | Configuration Override Hold Time after $\overline{\text{RSTOUT}}$ invalid | $t_{COH}$ | 0 | — | ns |
| R8 | $\overline{\text{RSTOUT}}$ invalid to Configuration Override High Impedance | $t_{ROICZ}$ | — | 1 | $t_{CYC}$ |

NOTES:
1 During low power STOP, the synchronizers for the $\overline{\text{RESET}}$ input are bypassed and $\overline{\text{RESET}}$ is asserted asynchronously to the system. Thus, $\overline{\text{RESET}}$ must be held a minimum of 100 ns.

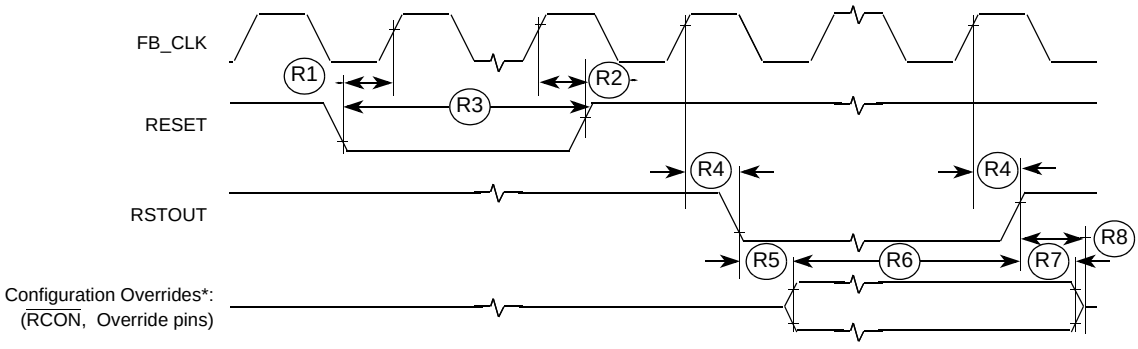



**Figure 21. $\overline{\text{RESET}}$ and Configuration Override Timing**

**NOTE**

Refer to the *MCF5208 Reference Manual* for more information.

## 5.11 I²C Input/Output Timing Specifications

Table 16 and Table 17 list specifications for the I²C input and output timing parameters.

**Table 16. I²C Input Timing Specifications between I2C_SCL and I2C_SDA**

| Num | Characteristic | Min | Max | Unit |
|---|---|---|---|---|
| I1 | Start condition hold time | 2 | — | $t_{cyc}$ |
| I2 | Clock low period | 8 | — | $t_{cyc}$ |
| I3 | I2C_SCL/I2C_SDA rise time ($V_{IL}$ = 0.5 V to $V_{IH}$ = 2.4 V) | — | 1 | ms |
| I4 | Data hold time | 0 | — | ns |
| I5 | I2C_SCL/I2C_SDA fall time ($V_{IH}$ = 2.4 V to $V_{IL}$ = 0.5 V) | — | 1 | ms |
| I6 | Clock high time | 4 | — | $t_{cyc}$ |
| I7 | Data setup time | 0 | — | ns |
| I8 | Start condition setup time (for repeated start condition only) | 2 | — | $t_{cyc}$ |
| I9 | Stop condition setup time | 2 | — | $t_{cyc}$ |

**Table 17. I²C Output Timing Specifications between I2C_SCL and I2C_SDA**

| Num | Characteristic | Min | Max | Unit |
|---|---|---|---|---|
| I1[1] | Start condition hold time | 6 | — | $t_{cyc}$ |
| I2 [1.] | Clock low period | 10 | — | $t_{cyc}$ |
| I3 [2] | I2C_SCL/I2C_SDA rise time ($V_{IL}$ = 0.5 V to $V_{IH}$ = 2.4 V) | — | — | µs |
| I4 [1.] | Data hold time | 7 | — | $t_{cyc}$ |
| I5 [3] | I2C_SCL/I2C_SDA fall time ($V_{IH}$ = 2.4 V to $V_{IL}$ = 0.5 V) | — | 3 | ns |
| I6 [1.] | Clock high time | 10 | — | $t_{cyc}$ |
| I7 [1.] | Data setup time | 2 | — | $t_{cyc}$ |
| I8 [1.] | Start condition setup time (for repeated start condition only) | 20 | — | $t_{cyc}$ |
| I9 [1.] | Stop condition setup time | 10 | — | $t_{cyc}$ |

NOTES:

1 Output numbers depend on the value programmed into the IFDR; an IFDR programmed with the maximum frequency (IFDR = 0x20) results in minimum output timings as shown in Table A-16. The I²C interface is designed to scale the actual data transition time to move it to the middle of the I2C_SCL low period. The actual position is affected by the prescale and division values programmed into the IFDR; however, the numbers given in Table A-16 are minimum values.

2 Because I2C_SCL and I2C_SDA are open-collector-type outputs, which the processor can only actively drive low, the time I2C_SCL or I2C_SDA take to reach a high level depends on external signal capacitance and pull-up resistor values.

3 Specified at a nominal 50-pF load.

## 5.13 32-Bit Timer Module AC Timing Specifications

Table 22 lists timer module AC timings.

**Table 22. Timer Module AC Timing Specifications**

| Name | Characteristic | Min | Max | Unit |
|---|---|---|---|---|
| T1 | DT0IN / DT1IN / DT2IN / DT3IN cycle time | 3 | — | $t_{CYC}$ |
| T2 | DT0IN / DT1IN / DT2IN / DT3IN pulse width | 1 | — | $t_{CYC}$ |

## 5.14 QSPI Electrical Specifications

Table 23 lists QSPI timings.

**Table 23. QSPI Modules AC Timing Specifications**

| Name | Characteristic | Min | Max | Unit |
|---|---|---|---|---|
| QS1 | QSPI_CS[3:0] to QSPI_CLK | 1 | 510 | tcyc |
| QS2 | QSPI_CLK high to QSPI_DOUT valid. | — | 10 | ns |
| QS3 | QSPI_CLK high to QSPI_DOUT invalid. (Output hold) | 1.5 | — | ns |
| QS4 | QSPI_DIN to QSPI_CLK (Input setup) | 9 | — | ns |
| QS5 | QSPI_DIN to QSPI_CLK (Input hold) | 9 | — | ns |

The values in Table 23 correspond to Figure 27.

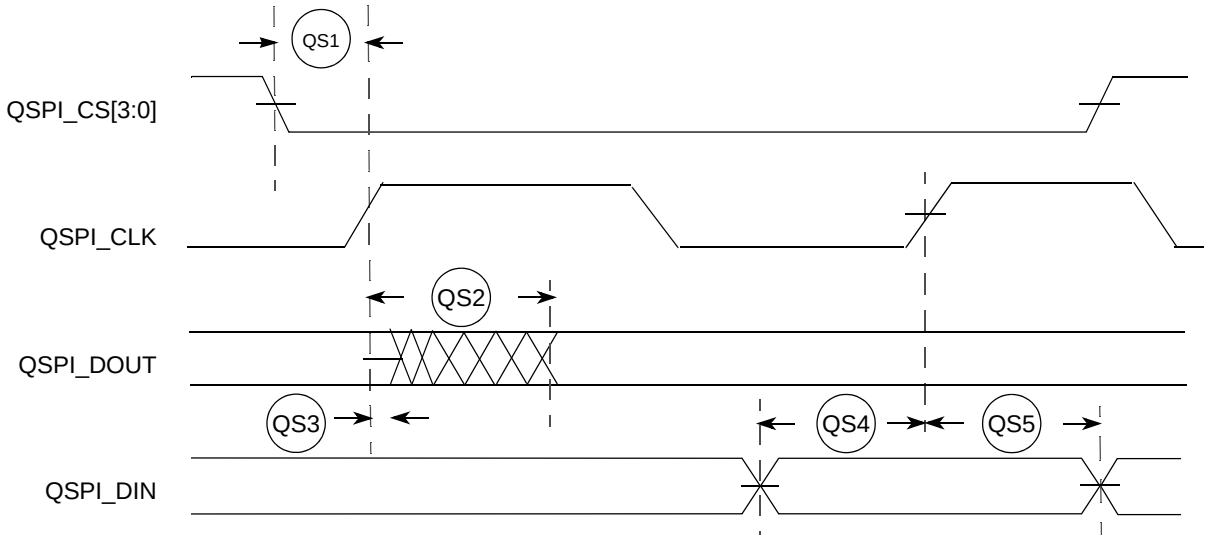



**Figure 27. QSPI Timing**

# 5.15 JTAG and Boundary Scan Timing

**Table 24. JTAG and Boundary Scan Timing**

| Num | Characteristics[1] | Symbol | Min | Max | Unit |
|---|---|---|---|---|---|
| J1 | TCLK Frequency of Operation | $f_{JCYC}$ | DC | 1/4 | $f_{sys/2}$ |
| J2 | TCLK Cycle Period | $t_{JCYC}$ | 4 | — | $t_{CYC}$ |
| J3 | TCLK Clock Pulse Width | $t_{JCW}$ | 26 | — | ns |
| J4 | TCLK Rise and Fall Times | $t_{JCRF}$ | 0 | 3 | ns |
| J5 | Boundary Scan Input Data Setup Time to TCLK Rise | $t_{BSDST}$ | 4 | — | ns |
| J6 | Boundary Scan Input Data Hold Time after TCLK Rise | $t_{BSDHT}$ | 26 | — | ns |
| J7 | TCLK Low to Boundary Scan Output Data Valid | $t_{BSDV}$ | 0 | 33 | ns |
| J8 | TCLK Low to Boundary Scan Output High Z | $t_{BSDZ}$ | 0 | 33 | ns |
| J9 | TMS, TDI Input Data Setup Time to TCLK Rise | $t_{TAPBST}$ | 4 | — | ns |
| J10 | TMS, TDI Input Data Hold Time after TCLK Rise | $t_{TAPBHT}$ | 10 | — | ns |
| J11 | TCLK Low to TDO Data Valid | $t_{TDODV}$ | 0 | 26 | ns |
| J12 | TCLK Low to TDO High Z | $t_{TDODZ}$ | 0 | 8 | ns |
| J13 | $\overline{TRST}$ Assert Time | $t_{TRSTAT}$ | 100 | — | ns |
| J14 | $\overline{TRST}$ Setup Time (Negation) to TCLK High | $t_{TRSTST}$ | 10 | — | ns |

NOTES:
1 JTAG_EN is expected to be a static signal. Hence, specific timing is not associated with it.

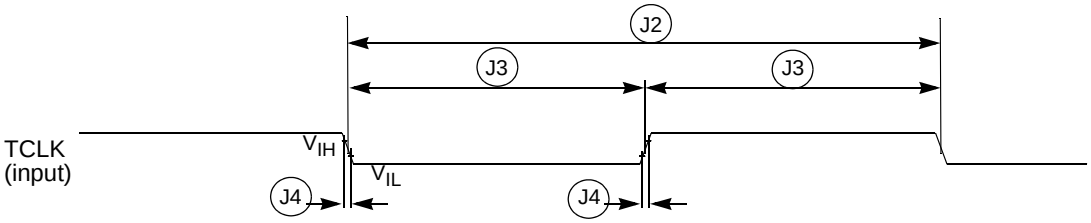



**Figure 28. Test Clock Input Timing**

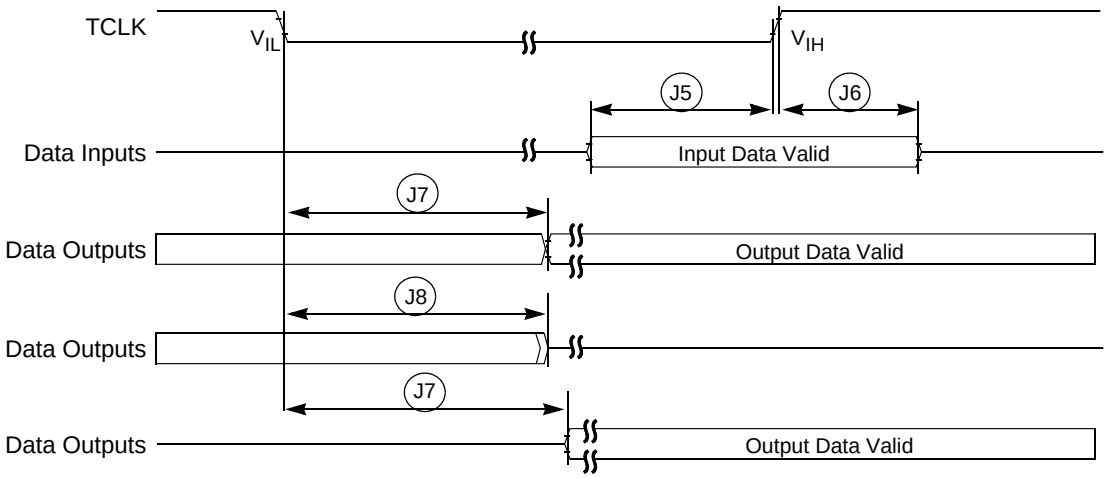



**Figure 29. Boundary Scan (JTAG) Timing**

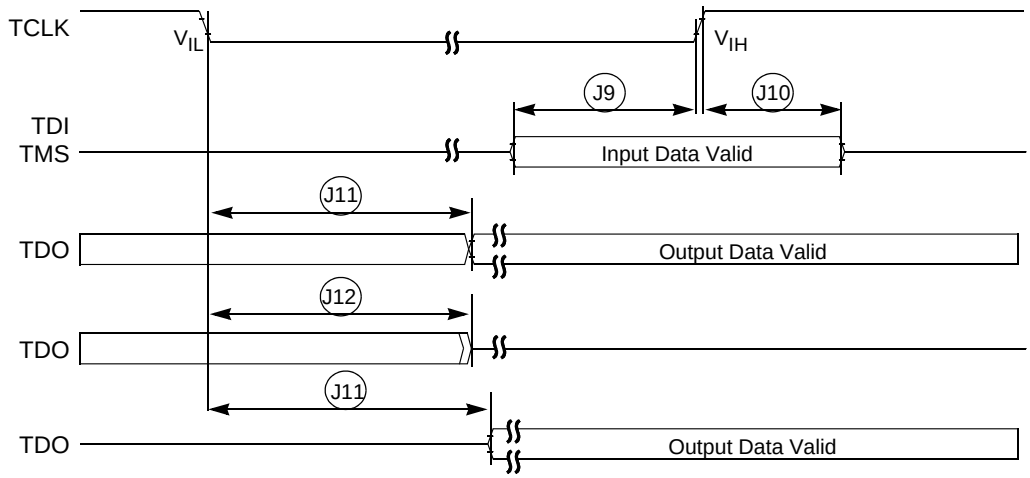



**Figure 30. Test Access Port Timing**

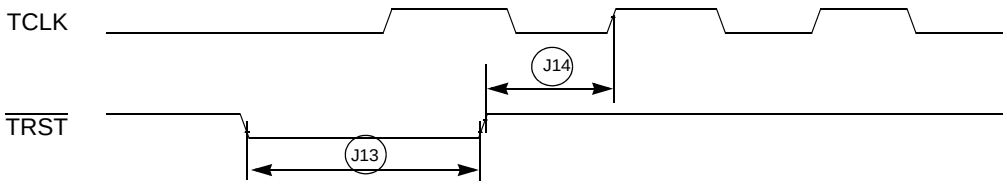



**Figure 31. $\overline{\text{TRST}}$ Timing**

# 5.16 Debug AC Timing Specifications

Table 25 lists specifications for the debug AC timing parameters shown in Figure 32.

**Table 25. Debug AC Timing Specification**

| Num | Characteristic | Min | Max | Unit |
|---|---|---|---|---|
| D0 | PSTCLK cycle time | 1 | 1 | $t_{SYS}$ |
| D1 | PSTCLK rising to PSTDDATA valid | — | 3.0 | ns |
| D2 | PSTCLK rising to PSTDDATA invalid | 1.5 | — | ns |
| D3 | DSI-to-DSCLK setup | 1 | — | PSTCLK |
| D4[1] | DSCLK-to-DSO hold | 4 | — | PSTCLK |
| D5 | DSCLK cycle time | 5 | — | PSTCLK |
| D6 | BKPT assertion time | 1 | — | PSTCLK |

NOTES:
1 DSCLK and DSI are synchronized internally. D4 is measured from the synchronized DSCLK input relative to the rising edge of PSTCLK.

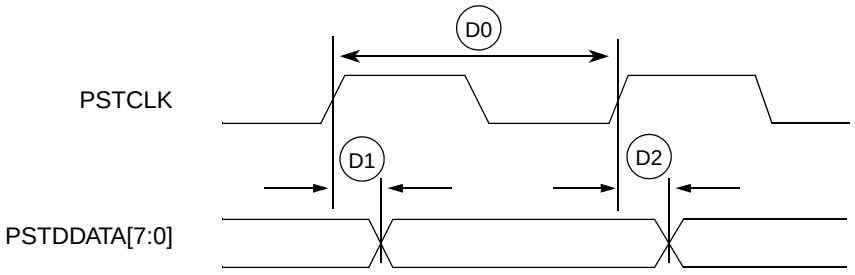



**Figure 32. Real-Time Trace AC Timing**

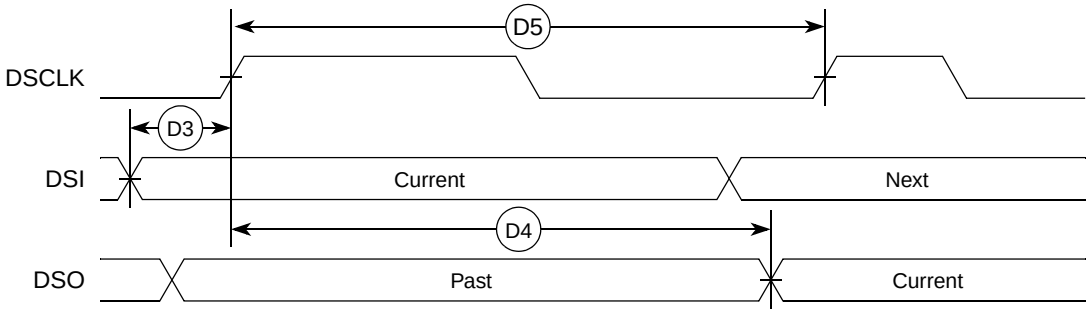



**Figure 33. BDM Serial Port AC Timing**

**Table 26. Revision History (continued)**

| Revision Number | Date | Substantive Changes |
|---|---|---|
| 0.4 | 10/10/2005 | • Figure 1 and Table 3: Changed pin 33 from EVDD to SD_VDD<br>• Figure 4 and Table 3: Changed ball D10 from TEST to VSS<br>• Figure 6 and Table 3: Changed pin 39 from EVDD to SD_VDD and pin 117 from TEST to VSS |
| 0.5 | 3/29/2006 | • Added “top view” and “bottom view” labels where appropriate to mechanical drawings and pinouts.<br>• Updated mechanical drawings to latest available, and added note to Section 4, “Mechanicals and Pinouts.” |
| 0.6 | 7/21/2006 | • Corrected cross-reference to Figure 9 in Section 4.7, “Pinout—196 MAPBGA.”<br>• Corrected L3 label in Figure 9 from SD_DR_DQS to SD_SDR_DQS.<br>• Corrected L6 label in Figure 9 from SD_DQS0 to SD_DQS2 and H3 from SD_DQS1 to SD_DQS3.<br>• Removed second sentence from Section 5.12.2, “MII Transmit Signal Timing (FEC_TXD[3:0], FEC_TXEN, FEC_TXER, FEC_TXCLK),” regarding no minimum frequency requirement for TXCLK.<br>• Removed third and fourth paragraphs from Section 5.12.2, “MII Transmit Signal Timing (FEC_TXD[3:0], FEC_TXEN, FEC_TXER, FEC_TXCLK),” as this feature is not supported on this device. |
| 1 | 3/28/2007 | • Removed preliminary designation from Section 5, “Electrical Characteristics.”<br>• Updated Section 5.2, “Thermal Characteristics.”<br>• Updated Section 5.4, “DC Electrical Specifications.”<br>• Added Section 5.5, “Current Consumption.”<br>• Updated Section 5.6, “Oscillator and PLL Electrical Characteristics.”<br>• Made some corrections to the drawings in Section 5.8, “SDRAM Bus.”<br>• Edited for grammar, punctuation, spelling, style, and format. - JD |
| 2 | 12/4/2008 | • Updated FlexBus read and write timing diagrams in Figure 14 and Figure 15.<br>Changed the following specs in Table 12 and Table 13:<br>• Minimum frequency of operation from TBD to 60MHz<br>• Maximum clock period from TBD to 16.67 ns |
| 3 | 9/1/2009 | • Changed doc type from Advance Information to Technical Data |

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