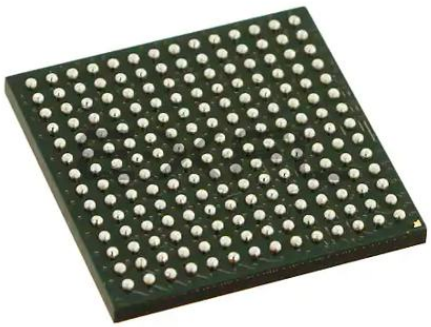

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	Coldfire V2
Core Size	32-Bit Single-Core
Speed	166.67MHz
Connectivity	EBI/EMI, Ethernet, I²C, SPI, UART/USART
Peripherals	DMA, WDT
Number of I/O	50
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.4V ~ 3.6V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	196-LBGA
Supplier Device Package	196-LBGA (15x15)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcf5208cvm166

Table 3. MCF5207/8 Signal Information and Muxing (continued)

Signal Name	GPIO	Alternate 1	Alternate 2	Dir.[1]	Voltage Domain	MCF5207 144 LQFP	MCF5207 144 MAPBGA	MCF5208 160 QFP	MCF5208 196 MAPBGA
A[9:0]	—	SD_A[9:0][3]	—	O	SDVDD	100–91	E11, D9, E12, F10, F11, E9, F12, G10, G12, F9	108–99	E13, E14, F11–F14, G11–G14
D[31:16]	—	SD_D[31:16][4]	—	I/O	SDVDD	21–28, 40–47	F1, F2, G1, G2, G4, G3, H1, H2, K3, L2, L3, K2, M3, J4, M4, K4	27–34, 46–53	J4–J1, K4–K1, M3, N3, M4, N4, P4, L5, M5, N5
D[15:0]	—	FB_D[31:16][4]	—	I/O	SDVDD	8–15, 51–58	B2, B1, C2, C1, D2, D1, E2, E1, L5, K5, L6, J6, M6, J7, L7, K7	16–23, 57–64	F3–F1, G4–G1, H1, N6, P6, L7, M7, N7, P7, N8, P8
$\overline{\text{BE/BWE}}$[3:0]	PBE[3:0]	$\overline{\text{SD\_DQM}}$[3:0][3]	—	O	SDVDD	20, 48, 18, 50	F4, L4, E3, J5	26, 54, 24, 56	H2, P5, H4, M6
$\overline{\text{OE}}$	PBUSCTL3	—	—	O	SDVDD	60	J8	66	M8
$\overline{\text{TA}}$[2]	PBUSCTL2	—	—	I	SDVDD	90	G11	98	H14
R/$\overline{\text{W}}$	PBUSCTL1	—	—	O	SDVDD	59	K6	65	L8
$\overline{\text{TS}}$	PBUSCTL0	$\overline{\text{DACK0}}$	—	O	SDVDD	4	B3	12	E3
Chip Selects									
$\overline{\text{FB\_CS}}$[3:2]	PCS[3:2]	—	—	O	SDVDD	119, 120	D7, A9	—	C11, A10
$\overline{\text{FB\_CS1}}$	PCS1	$\overline{\text{SD\_CS1}}$	—	O	SDVDD	121	C8	127	B10
$\overline{\text{FB\_CS0}}$	—	—	—	O	SDVDD	122	B8	128	C10
SDRAM Controller									
SD_A10	—	—	—	O	SDVDD	37	M1	43	N2
SD_CKE	—	—	—	O	SDVDD	6	C3	14	E1
SD_CLK	—	—	—	O	SDVDD	31	J1	37	L1
$\overline{\text{SD\_CLK}}$	—	—	—	O	SDVDD	32	K1	38	M1
$\overline{\text{SD\_CS0}}$	—	—	—	O	SDVDD	7	A1	15	F4
SD_DQS[3:2]	—	—	—	O	SDVDD	19, 49	F3, M5	25, 55	H3, L6
$\overline{\text{SD\_SCAS}}$	—	—	—	O	SDVDD	38	M2	44	P2
$\overline{\text{SD\_SRAS}}$	—	—	—	O	SDVDD	39	J2	45	P3
SD_SDR_DQS	—	—	—	O	SDVDD	29	H3	35	L3
$\overline{\text{SD\_WE}}$	—	—	—	O	SDVDD	5	D3	13	E2

Table 3. MCF5207/8 Signal Information and Muxing (continued)

Signal Name	GPIO	Alternate 1	Alternate 2	Dir.[1]	Voltage Domain	MCF5207 144 LQFP	MCF5207 144 MAPBGA	MCF5208 160 QFP	MCF5208 196 MAPBGA
External Interrupts Port[5]									
$\overline{\text{IRQ7}}$[2]	PIRQ7[2]	—	—	I	EVDD	134	A5	142	C7
$\overline{\text{IRQ4}}$[2]	PIRQ4[2]	$\overline{\text{DREQ0}}$[2]	—	I	EVDD	133	C6	141	D7
$\overline{\text{IRQ1}}$[2]	PIRQ1[2]	—	—	I	EVDD	132	B6	140	D8
FEC									
FEC_MDC	PFECI2C3	I2C_SCL[2]	U2TXD	O	EVDD	—	—	148	D6
FEC_MDIO	PFECI2C2	I2C_SDA[2]	U2RXD	I/O	EVDD	—	—	147	C6
FEC_TXCLK	PFECH7	—	—	I	EVDD	—	—	157	B3
—	PFECH6	—	$\overline{\text{U1RTS}}$	O	EVDD	142	A2	—	—
FEC_TXEN	PFECH6	—	$\overline{\text{U1RTS}}$	O	EVDD	—	—	158	A2
FEC_TXD0	PFECH5	—	—	O	EVDD	—	—	3	B1
FEC_COL	PFECH4	—	—	I	EVDD	—	—	7	D3
FEC_RXCLK	PFECH3	—	—	I	EVDD	—	—	154	B4
FEC_RXDV	PFECH2	—	—	I	EVDD	—	—	153	A4
FEC_RXD0	PFECH1	—	—	I	EVDD	—	—	152	D5
FEC_CRS	PFECH0	—	—	I	EVDD	—	—	8	D2
FEC_TXD[3:1]	PFECL[7:5]	—	—	O	EVDD	—	—	6–4	C1, C2, B2
—	PFECL4	—	$\overline{\text{U0RTS}}$	O	EVDD	141	D5	—	—
FEC_TXER	PFECL4	—	$\overline{\text{U0RTS}}$	O	EVDD	—	—	156	A3
FEC_RXD[3:2]	PFECL[3:2]	—	—	I	EVDD	—	—	149–150	A5, B5
—	PFECL1	—	$\overline{\text{U1CTS}}$	I	EVDD	139	B4	—	—
FEC_RXD1	PFECL1	—	$\overline{\text{U1CTS}}$	I	EVDD	—	—	151	C5
—	PFECL0	—	$\overline{\text{U0CTS}}$	I	EVDD	140	E4	—	—
FEC_RXER	PFECL0	—	$\overline{\text{U0CTS}}$	I	EVDD	—	—	155	C4
Note: The MCF5207 does not contain an FEC module. However, the UART0 and UART1 control signals (as well as their GPIO signals) are available by setting the appropriate FEC GPIO port registers.									
I²C									
I2C_SDA[2]	PFECI2C0[2]	U2RXD[2]	—	I/O	EVDD	—	—	—	D1
I2C_SCL[2]	PFECI2C1[2]	U2TXD[2]	—	I/O	EVDD	—	—	—	E4
DMA									
$\overline{\text{DACK0}}$ and $\overline{\text{DREQ0}}$ do not have a dedicated bond pads. Please refer to the following pins for muxing: $\overline{\text{TS}}$ and QSPI_CS2 for $\overline{\text{DACK0}}$, $\overline{\text{IRQ4}}$ and QSPI_DIN for $\overline{\text{DREQ0}}$.									

Table 3. MCF5207/8 Signal Information and Muxing (continued)

Signal Name	GPIO	Alternate 1	Alternate 2	Dir.[1]	Voltage Domain	MCF5207 144 LQFP	MCF5207 144 MAPBGA	MCF5208 160 QFP	MCF5208 196 MAPBGA
ALLPST	—	—	—	O	EVDD	67	—	73	—
Test									
TEST[7]	—	—	—	I	EVDD	109	—	—	C12
PLL_TEST	—	—	—	I	EVDD	—	—	—	M13
Power Supplies									
EVDD	—	—	—	—	—	1, 33, 63, 66, 72, 81, 87, 125	E5–E6, F5, G8–G9, H7–H8	2, 9, 69, 72, 80, 89, 95, 131	E5–E7, F5, F6, G5, H10, J9, J10, K8–K10, K13, M9
IVDD	—	—	—	—	—	30, 68, 84, 113, 143	D4, D8, H4, H11, J9	36, 74, 92, 121, 159	J12, D4, D11, H11, L4, L11,
PLL_VDD	—	—	—	—	—	86	H12	94	H13
SD_VDD	—	—	—	—	—	3, 17, 35, 61, 89, 110, 123	E7–E8, F8, G5, H5–H6, J3	11, 39, 41, 67, 97, 118, 129	E8–E10, F9, F10, G10, H5, J5, J6, K5–K7, L2
VSS	—	—	—	—	—	2, 16, 36, 62, 65, 73, 88, 111, 124	D10, F6–F7, G6–G7	1, 10, 42, 68, 71, 81, 96, 117, 119, 130	A1, A14, F7–F8, G6–G9, H6–H9, J7–J8, L13, M2, N9, P1, P14
PLL_VSS	—	—	—	—	—	85	—	93	H12

NOTES:
1 Refers to pin's primary function.
2 Pull-up enabled internally on this signal for this mode.
3 The SDRAM functions of these signals are not programmable by the user. They are dynamically switched by the processor when accessing SDRAM memory space and are included here for completeness.
4 Primary functionality selected by asserting the DRAMSEL signal (SDR mode). Alternate functionality selected by negating the DRAMSEL signal (DDR mode). The GPIO module is not responsible for assigning these pins.
5 GPIO functionality is determined by the edge port module. The GPIO module is only responsible for assigning the alternate functions.
6 If JTAG_EN is asserted, these pins default to Alternate 1 (JTAG) functionality. The GPIO module is not responsible for assigning these pins.
7 Pull-down enabled internally on this signal for this mode.

4 Mechanicals and Pinouts

Drawings in this section show the pinout and the packaging and mechanical characteristics of the MCF5207 and MCF5208 devices.

NOTE

The mechanical drawings are the latest revisions at the time of publication of this document. The most up-to-date mechanical drawings can be found at the product summary page located at http://www.freescale.com/coldfire.

4.1 Pinout—144 LQFP

Figure 1 shows a pinout of the MCF5207CAG166 device.

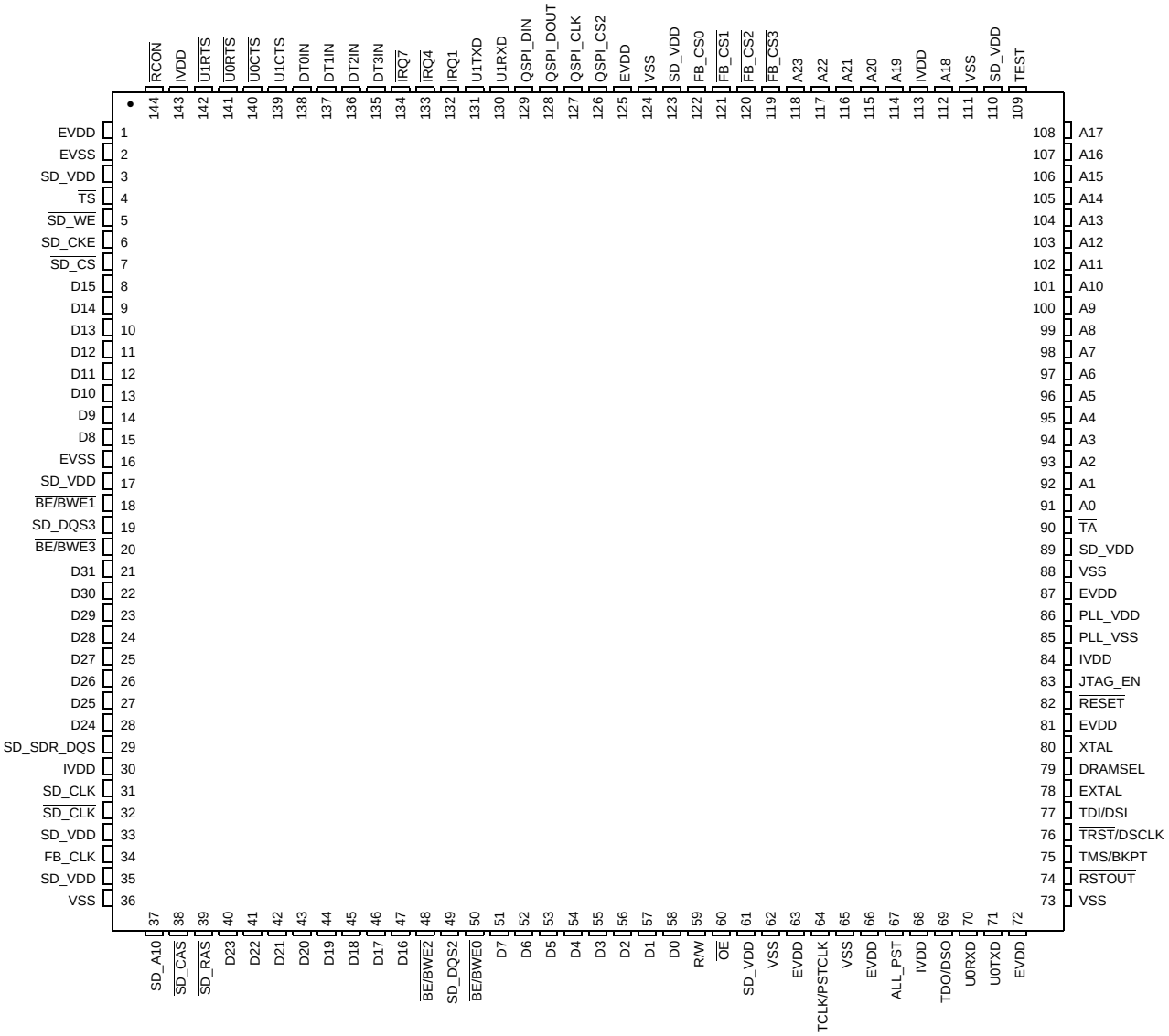
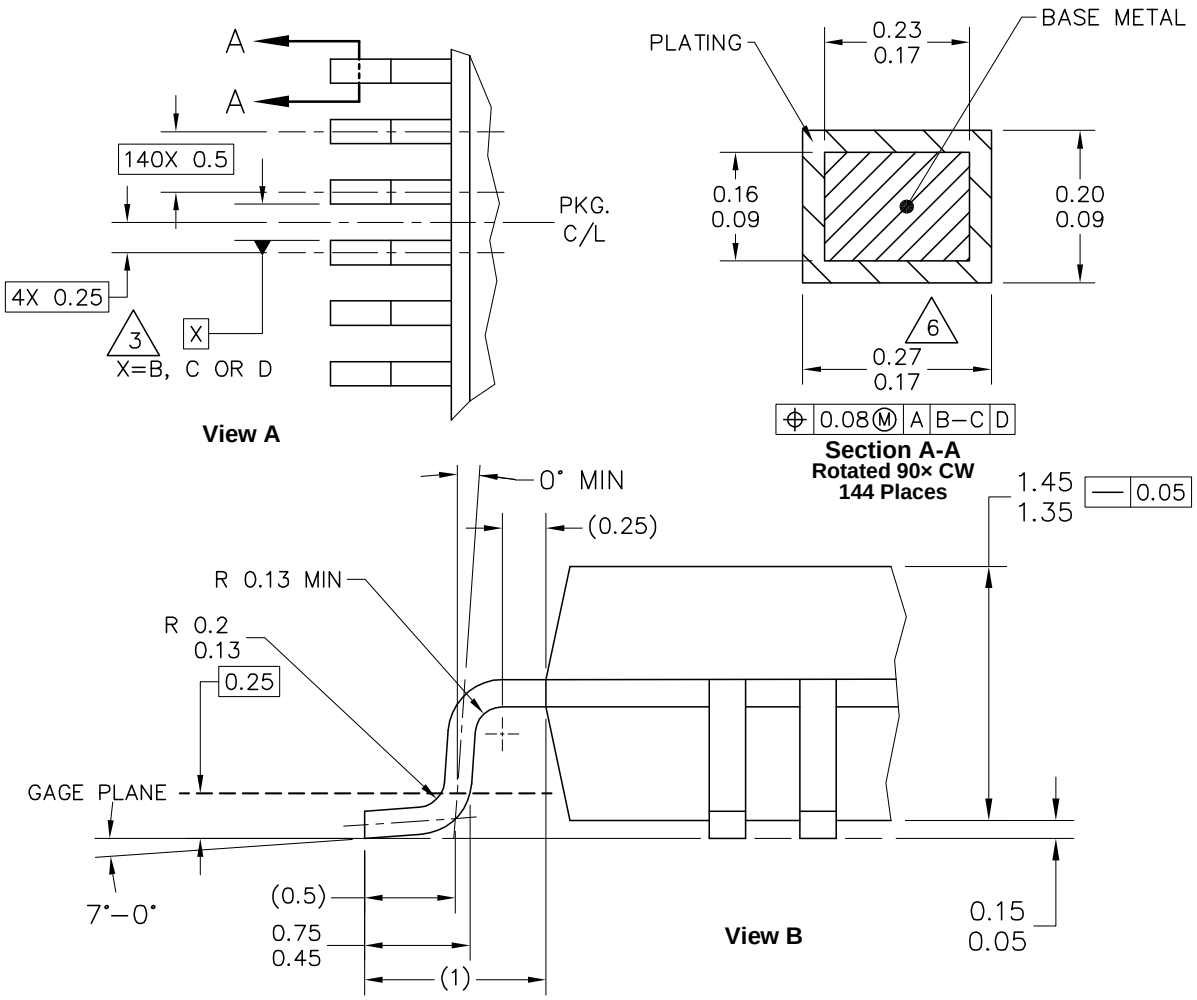


Figure 1. MCF5207CAG166 Pinout Top View (144 LQFP)



NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.

2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.

3. DATUMS B, C AND D TO BE DETERMINED AT DATUM PLANE H.

4. THE TOP PACKAGE BODY SIZE MAY BE SMALLER THAN THE BOTTOM PACKAGE SIZE BY A MAXIMUM OF 0.1 mm.

5. THIS DIMENSIONS DO NOT INCLUDE MOLD PROTRUSIONS. THE MAXIMUM ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. THIS DIMENSIONS ARE MAXIMUM BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.

6. THIS DIMENSION DOES NOT INCLUDE DAM BAR PROTRUSION. PROTRUSIONS SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.35. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD SHALL BE 0.07 MM.

7. THIS DIMENSIONS ARE DETERMINED AT THE SEATING PLANE, DATUM A.

Figure 3. MCF5207CAB166 Package Dimensions (Sheet 2 of 2)

4.3 Pinout—144 MAPBGA

The pinout of the MCF5207CVM166 device is shown below.

	1	2	3	4	5	6	7	8	9	10	11	12	
A	SD_CS	U1RTS	DT0IN	DT1IN	IRQ7	U1TXD	QSPI_DOUT	QSPI_CS2	FB_CS2	A22	A20	A18	A
B	D14	D15	TS	U1CTS	DT3IN	IRQ1	QSPI_DIN	FB_CS0	A23	A19	A16	A15	B
C	D12	D13	SD_CKE	RCON	DT2IN	IRQ4	QSPI_CLK	FB_CS1	A21	A10	A17	A14	C
D	D10	D11	SD_WE	IVDD	U0RTS	U1RXD	FB_CS3	IVDD	A8	VSS	A13	A11	D
E	D8	D9	BE/BWE1	U0CTS	EVDD	EVDD	SD_VDD	SD_VDD	A4	A12	A9	A7	E
F	D31	D30	SD_DQS3	BE/BWE3	EVDD	VSS	VSS	SD_VDD	A0	A6	A5	A3	F
G	D29	D28	D26	D27	SD_VDD	VSS	VSS	EVDD	EVDD	A2	TA	A1	G
H	D25	D24	SD_SDR_DQS	IVDD	SD_VDD	SD_VDD	EVDD	EVDD	TDI/DSI	DRAM SEL	IVDD	PLL_VDD	H
J	SD_CLK	SD_RAS	SD_VDD	D18	BE/BWE0	D4	D2	OE	IVDD	RESET	JTAG_EN	XTAL	J
K	SD_CLK	D20	D23	D16	D6	R/W	D0	PST0	DDATA3	PST1	TRST/DSCLK	EXTAL	K
L	FB_CLK	D22	D21	BE/BWE2	D7	D5	D1	PST2	DDATA2	U0TXD	PST3	TMS/BKPT	L
M	SD_A10	SD_CAS	D19	D17	SD_DQS2	D3	TCLK/PSTCLK	DDATA0	TDO/DSO	U0RXD	DDATA1	RSTOUT	M
	1	2	3	4	5	6	7	8	9	10	11	12	

Figure 4. MCF5207CVM166 Pinout Top View (144 MAPBGA)

4.7 Pinout—196 MAPBGA

Figure 9 shows a pinout of the MCF5208CVM166 device.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	
A	VSS	FEC_ TXEN	FEC_ TXER	FEC_ RXDV	FEC_ RXD3	DT1IN	DT2IN	U1TXD	QSPI_ CLK	FB_CS2	A22	A20	A19	VSS	A
B	FEC_ TXD0	FEC_ TXD1	FEC_ TXCLK	FEC_ RXCLK	FEC_ RXD2	DT0IN	DT3IN	U1RXD	QSPI_ DOUT	FB_CS1	A23	A21	A18	A17	B
C	FEC_ TXD3	FEC_ TXD2	RCON	FEC_ RXER	FEC_ RXD1	FEC_ MDIO	IRQ7	U1RTS	QSPI_ DIN	FB_CS0	FB_CS3	TEST	A16	A15	C
D	I2C_SDA	FEC_ CRS	FEC_ COL	IVDD	FEC_ RXD0	FEC_ MDC	IRQ4	IRQ1	U1CTS	QSPI_ CS2	IVDD	A14	A13	A12	D
E	SD_CKE	SD_WE	TS	I2C_SCL	EVDD	EVDD	EVDD	SD_VDD	SD_VDD	SD_VDD	A11	A10	A9	A8	E
F	D13	D14	D15	SD_CS	EVDD	EVDD	VSS	VSS	SD_VDD	SD_VDD	A7	A6	A5	A4	F
G	D9	D10	D11	D12	EVDD	VSS	VSS	VSS	VSS	SD_VDD	A3	A2	A1	A0	G
H	D8	BE/ BWE3	SD_ DQS3	BE/ BWE1	SD_VDD	VSS	VSS	VSS	VSS	EVDD	IVDD	PLL_ VSS	PLL_ VDD	TA	H
J	D28	D29	D30	D31	SD_VDD	SD_VDD	VSS	VSS	EVDD	EVDD	NC	IVDD	JTAG_ EN	RESET	J
K	D24	D25	D26	D27	SD_VDD	SD_VDD	SD_VDD	EVDD	EVDD	EVDD	DRAM SEL	TDI/ DSI	EVDD	XTAL	K
L	SD_CLK	SD_VDD	SD_SDR _DQS	IVDD	D18	SD_ DQS2	D5	R/W	PST0	PST1	IVDD	TRST/ DSCLK	VSS	EXTAL	L
M	SD_CLK	VSS	D23	D21	D17	BE/ BWE0	D4	OE	EVDD	PST2	DDATA1	TDO/ DSO	PLL_ TEST	TMS/ BKPT	M
N	FB_CLK	SD_A10	D22	D20	D16	D7	D3	D1	VSS	PST3	DDATA2	U0CTS	U0RXD	RSTOUT	N
P	VSS	SD_CAS	SD_RAS	D19	BE/ BWE2	D6	D2	D0	TCLK/ PSTCLK	DDATA0	DDATA3	U0RTS	U0TXD	VSS	P
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

Figure 9. MCF5208CVM166 Pinout Top View (196 MAPBGA)

4.8 Package Dimensions—196 MAPBGA

The package dimensions for the MCF5208CVM166 device is shown below.

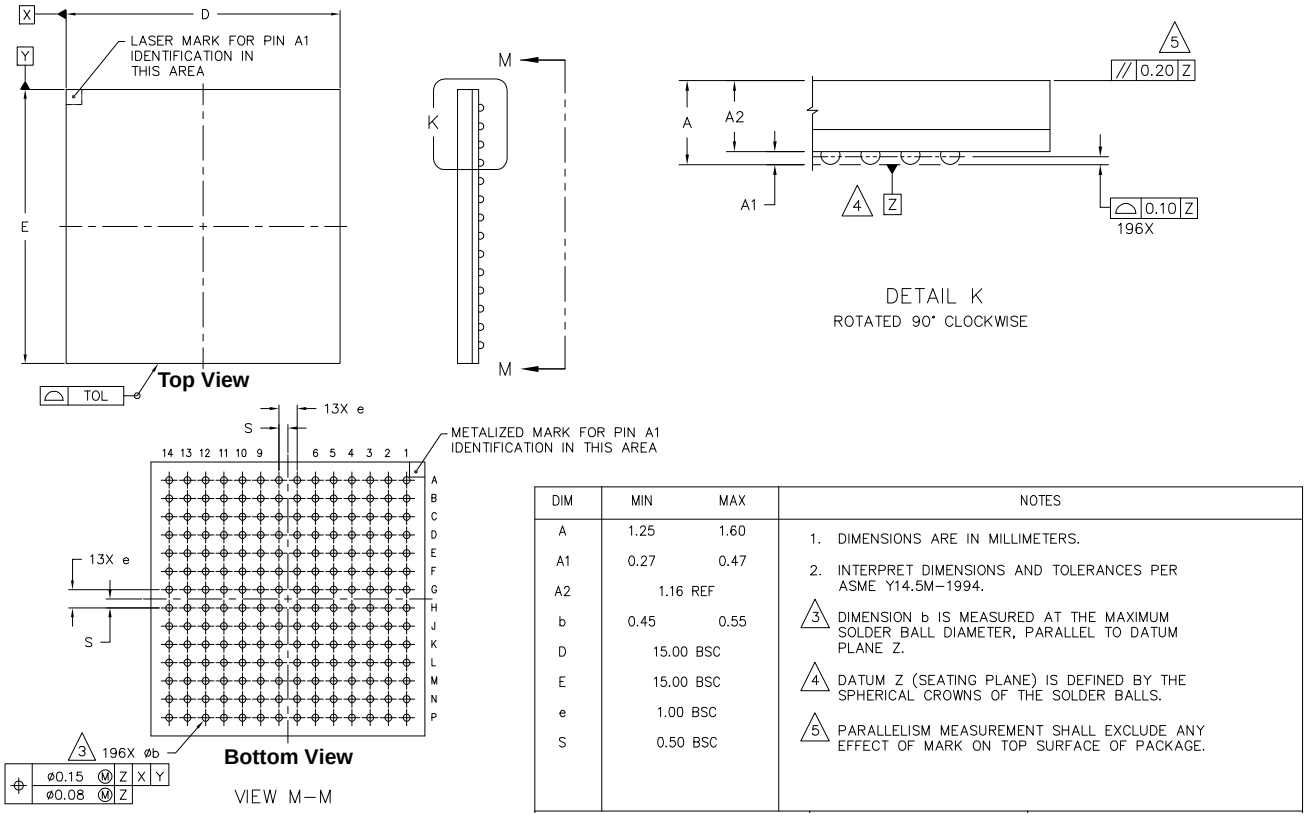


Figure 10. MCF5208CVM166 Package Dimensions (196 MAPBGA)

5 Electrical Characteristics

5.1 Maximum Ratings

Table 4. Absolute Maximum Ratings[1, 2]

Rating	Symbol	Value	Unit
Core Supply Voltage	IV_{DD}	– 0.5 to +2.0	V
CMOS Pad Supply Voltage	EV_{DD}	– 0.3 to +4.0	V
DDR/Memory Pad Supply Voltage	SDV_{DD}	– 0.3 to +4.0	V
PLL Supply Voltage	$PLLV_{DD}$	– 0.3 to +2.0	V
Digital Input Voltage [3]	V_{IN}	– 0.3 to +3.6	V
Instantaneous Maximum Current Single pin limit (applies to all pins) [3, 4, 5]	I_D	25	mA

Table 4. Absolute Maximum Ratings[1, 2] (continued)

Operating Temperature Range (Packaged)	T_A (T_L - T_H)	– 40 to 85	°C
Storage Temperature Range	T_{stg}	– 55 to 150	°C

NOTES:
1. Functional operating conditions are given in Section 5.4, "DC Electrical Specifications". Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Continued operation at these levels may affect device reliability or cause permanent damage to the device.
2. This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (V_{SS} or EV_{DD}).
3. Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.
4. All functional non-supply pins are internally clamped to V_{SS} and EV_{DD}.
5. Power supply must maintain regulation within operating EV_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{in} > EV_{DD}$) is greater than I_{DD}, the injection current may flow out of EV_{DD} and could result in external power supply going out of regulation. Ensure external EV_{DD} load shunts current greater than maximum injection current. This is the greatest risk when the MCU is not consuming power (ex; no clock). Power supply must maintain regulation within operating EV_{DD} range during instantaneous and operating maximum current conditions.

5.2 Thermal Characteristics

Table 5 lists thermal resistance values

Table 5. Thermal Characteristics

Characteristic		Symbol	196MBGA	144MBGA	160QFP	144LQFP	Unit
Junction to ambient, natural convection	Four layer board (2s2p)	θ_{JMA}	47[1,2]	47[1,2]	49[1,2]	65[1,2]	°C/W
Junction to ambient (@200 ft/min)	Four layer board (2s2p)	θ_{JMA}	43[1,2]	43[1,2]	44[1,2]	58[1,2]	°C/W
Junction to board		θ_{JB}	36[3]	36[3]	40[3]	50[3]	°C/W
Junction to case		θ_{JC}	22[4]	22[4]	39[4]	19[4]	°C/W
Junction to top of package		Ψ_{jt}	6[1,5]	6[1,5]	12[1,6]	5[1,7]	°C/W
Maximum operating junction temperature		T_j	105	105	105	105	°C

NOTES:
1. θ_{JMA} and Ψ_{jt} parameters are simulated in conformance with EIA/JESD Standard 51-2 for natural convection. Freescale recommends the use of θ_{JmA} and power dissipation specifications in the system design to prevent device junction temperatures from exceeding the rated specification. System designers should be aware that device junction temperatures can be significantly influenced by board layout and surrounding devices. Conformance to the device junction temperature specification can be verified by physical measurement in the customer's system using the Ψ_{jt} parameter, the device power dissipation, and the method described in EIA/JESD Standard 51-2.
2. Per JEDEC JESD51-6 with the board horizontal.

3 Thermal resistance between the die and the printed circuit board in conformance with JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

4 Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).

5 Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written in conformance with Psi-JT.

6 Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written in conformance with Psi-JT.

7 Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written in conformance with Psi-JT.

The average chip-junction temperature (T_J) in °C can be obtained from:

$$T_J = T_A + (P_D \times \Theta_{JMA}) \quad \textit{Eqn. 1}$$

Where:

T_A = Ambient Temperature, °C

Q_{JMA} = Package Thermal Resistance, Junction-to-Ambient, ×C/W

P_D = P_{INT} + $P_{I/O}$

P_{INT} = I_{DD} × IV_{DD}, Watts - Chip Internal Power

$P_{I/O}$ = Power Dissipation on Input and Output Pins — User Determined

For most applications $P_{I/O} < P_{INT}$ and can be ignored. An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = \frac{K}{(T_J + 273°C)} \quad \textit{Eqn. 2}$$

Solving equations 1 and 2 for K gives:

$$K = P_D \times (T_A \times 273°C) + Q_{JMA} \times P_D^2 \quad \textit{Eqn. 3}$$

where K is a constant pertaining to the particular part. K can be determined from Equation 3 by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving Equation 1 and Equation 2 iteratively for any value of T_A.

5.3 ESD Protection

Table 6. ESD Protection Characteristics[1, 2]

Characteristics	Symbol	Value	Unit
ESD Target for Human Body Model	HBM	2000	V

NOTES:
1 All ESD testing is in conformity with CDF-AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.

0.4 V during power down or there is an undesired high current in the ESD protection diodes. There are no requirements for the fall times of the power supplies.

The recommended power down sequence is:

1. Drop IV_{DD}/$PLLV_{DD}$ to 0 V.
2. Drop EV_{DD}/SDV_{DD} supplies.

5.5 Current Consumption

All of the below current consumption data is lab data measured on a single device using an evaluation board. Table 8 shows the typical current consumption in low-power modes at various $f_{sys/2}$ frequencies. Current measurements are taken after executing a STOP instruction.

Table 8. Current Consumption in Low-Power Mode[1,2]

Mode	Voltage (V)	Typical[3] (mA)					Peak[4] (mA)
		44 MHz	56 MHz	64 MHz	72 MHz	83.33 MHz	83.33 MHz
Stop Mode 3 (Stop 11)[5]	3.3	1.33					
	2.5	15.19					
	1.5	0.519					
Stop Mode 2 (Stop 10)[5]	3.3	1.93					
	2.5	15.19					
	1.5	1.25					
Stop Mode 1 (Stop 01)[5]	3.3	1.83					
	2.5	15.23					
	1.5	8.24	10.22	9.55	10.61	12.1	12.1
Stop Mode 0 (Stop 00)[5]	3.3	2.23	2.33	2.41	2.5	2.61	2.61
	2.5	16.2	16.47	16.62	16.91	17.24	17.24
	1.5	8.32	10.32	9.66	10.73	12.25	12.25
Wait/Doze	3.3	2.23	2.33	2.41	2..5	2.6	4.07
	2.5	16.2	16.48	16.62	16.91	17.24	18.77
	1.5	11.53	14.36	14.29	15.92	18.21	35.45
Run	3.3	6.79	9.02	14.56	19.54	29.12	30.43
	2.5	16.17	16.48	16.64	16.89	17.23	18.76
	1.5	16.29	20.36	21.13	23.57	27.0	44.1

NOTES:
1. All values are measured with a 3.30V EV_{DD}, 2.50V SDV_{DD}, and 1.5V IV_{DD} power supplies. Tests performed at room temperature with pins configured for high drive strength.
2. Refer to the Power Management chapter in the *MCF5208 Reference Manual* for more information on low-power modes.
3. All peripheral clocks except UART0, FlexBus, INTC, reset controller, PLL, and Edge Port off before entering low-power mode. All code executed from flash.
4. Peak current measured while running a while(1) loop with all modules active.

All other timing relationships can be derived from these values. Timings listed in Table 11 are shown in Figure 14 and Figure 15.

* The timings are also valid for inputs sampled on the negative clock edge.

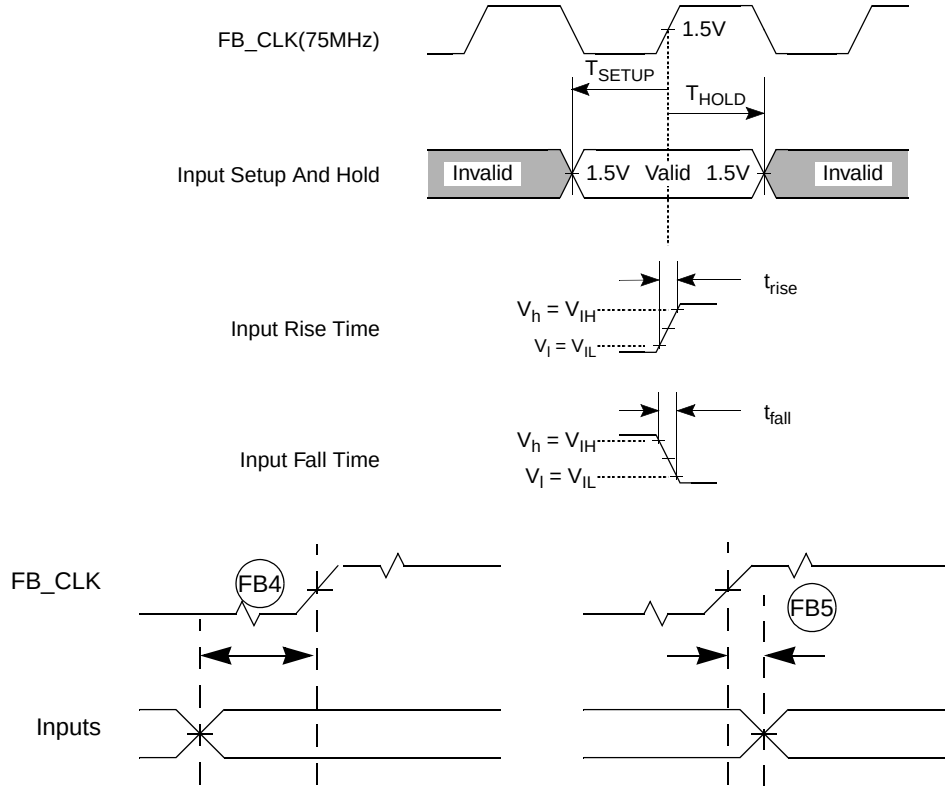


Figure 13. General Input Timing Requirements

5.7.1 FlexBus

FlexBus is a multi-function external bus interface provided to interface to slave-only devices up to a maximum bus frequency of 83.33 MHz. It can be directly connected to asynchronous or synchronous devices such as external boot ROMs, flash memories, gate-array logic, or other simple target (slave) devices with little or no additional circuitry. For asynchronous devices, a simple chip-select based interface can be used. The FlexBus interface has six general purpose chip-selects ($\overline{\text{FB\_CS}}$[5:0]) that can be configured to be distributed between the FlexBus or SDRAM memory interfaces. Chip-select $\overline{\text{FB\_CS}}$[0] can be dedicated to boot ROM access and can be programmed to be byte (8 bits), word (16 bits), or longword (32 bits) wide. Control signal timing is compatible with common ROM/flash memories.

5.8.2 DDR SDRAM AC Timing Characteristics

When using the SDRAM controller in DDR mode, the following timing numbers must be followed to properly latch or drive data onto the memory bus. All timing numbers are relative to the four DQS byte lanes. The following timing numbers are subject to change at anytime, and are only provided to aid in early board design. Please contact your local Freescale representative if questions develop.

Table 13. DDR Timing Specifications

Num	Characteristic	Symbol	Min	Max	Unit	Notes
—	Frequency of Operation	—	60	83.33	Mhz	1
DD1	Clock Period (SD_CLK)	t_{DDCK}	12	16.67	ns	2
DD2	Pulse Width High	t_{DDCKH}	0.45	0.55	SD_CLK	3
DD3	Pulse Width Low	t_{DDCKL}	0.45	0.55	SD_CLK	3
DD4	Address, SD_CKE, $\overline{\text{SD\_CAS}}$, $\overline{\text{SD\_RAS}}$, $\overline{\text{SD\_WE}}$, $\overline{\text{SD\_CS}}$[1:0] - Output Valid	$t_{SDCHACV}$	—	0.5 × SD_CLK + 1.0	ns	4
DD5	Address, SD_CKE, $\overline{\text{SD\_CAS}}$, $\overline{\text{SD\_RAS}}$, $\overline{\text{SD\_WE}}$, $\overline{\text{SD\_CS}}$[1:0] - Output Hold	$t_{SDCHACI}$	2.0	—	ns	—
DD6	Write Command to first DQS Latching Transition	t_{CMDVDQ}		1.25	SD_CLK	—
DD7	Data and Data Mask Output Setup (DQ-->DQS) Relative to DQS (DDR Write Mode)	t_{DQDMV}	1.5	—	ns	5 6
DD8	Data and Data Mask Output Hold (DQS-->DQ) Relative to DQS (DDR Write Mode)	t_{DQDMI}	1.0	—	ns	7
DD9	Input Data Skew Relative to DQS (Input Setup)	t_{DVDQ}	—	1	ns	8
DD10	Input Data Hold Relative to DQS.	t_{DIDQ}	0.25 × SD_CLK + 0.5ns	—	ns	9
DD11	DQS falling edge from SDCLK rising (output hold time)	$t_{DQLSDCH}$	0.5	—	ns	—
DD12	DQS input read preamble width (t_{RPRE})	t_{DQRPRE}	0.9	1.1	SD_CLK	—
DD13	DQS input read postamble width (t_{RPST})	t_{DQRPST}	0.4	0.6	SD_CLK	—
DD14	DQS output write preamble width (t_{WPRE})	t_{DQWPRE}	0.25	—	SD_CLK	—
DD15	DQS output write postamble width (t_{WPST})	t_{DQWPST}	0.4	0.6	SD_CLK	—

NOTES:
1. The frequency of operation is 2x or 4x the FB_CLK frequency of operation. FlexBus and SDRAM clock operate at the same frequency as the internal bus clock.
2. SD_CLK is one SDRAM clock in (ns).
3. Pulse width high plus pulse width low cannot exceed min and max clock period.
4. Command output valid should be 1/2 the memory bus clock (SD_CLK) plus some minor adjustments for process, temperature, and voltage variations.
5. This specification relates to the required input setup time of today's DDR memories. The device's output setup should be larger than the input setup of the DDR memories. If it is not larger, the input setup on the memory is in violation. MEM_DATA[31:24] is relative to MEM_DQS[3], MEM_DATA[23:16] is relative to MEM_DQS[2], MEM_DATA[15:8] is relative to MEM_DQS[1], and MEM_[7:0] is relative MEM_DQS[0].
6. The first data beat is valid before the first rising edge of DQS and after the DQS write preamble. The remaining data beats are valid for each subsequent DQS edge.

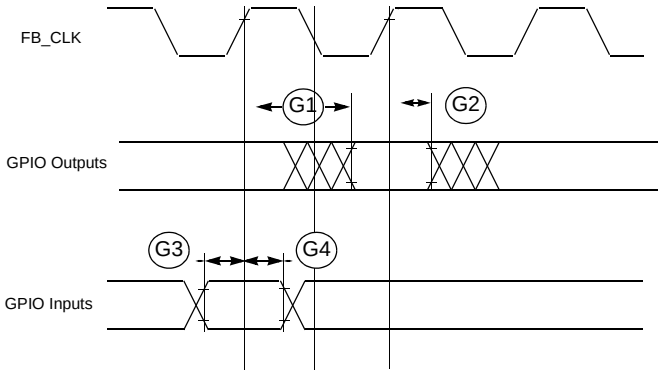


Figure 20. GPIO Timing

5.10 Reset and Configuration Override Timing

Table 15. Reset and Configuration Override Timing

Num	Characteristic	Symbol	Min	Max	Unit
R1	$\overline{\text{RESET}}$ Input valid to FB_CLK High	t_{RVCH}	9	—	ns
R2	FB_CLK High to $\overline{\text{RESET}}$ Input invalid	t_{CHRI}	1.5	—	ns
R3	$\overline{\text{RESET}}$ Input valid Time [1]	t_{RIVT}	5	—	t_{CYC}
R4	FB_CLK High to $\overline{\text{RSTOUT}}$ Valid	t_{CHROV}	—	10	ns
R5	$\overline{\text{RSTOUT}}$ valid to Config. Overrides valid	t_{ROVCV}	0	—	ns
R6	Configuration Override Setup Time to $\overline{\text{RSTOUT}}$ invalid	t_{COS}	20	—	t_{CYC}
R7	Configuration Override Hold Time after $\overline{\text{RSTOUT}}$ invalid	t_{COH}	0	—	ns
R8	$\overline{\text{RSTOUT}}$ invalid to Configuration Override High Impedance	t_{ROICZ}	—	1	t_{CYC}

NOTES:
1 During low power STOP, the synchronizers for the $\overline{\text{RESET}}$ input are bypassed and $\overline{\text{RESET}}$ is asserted asynchronously to the system. Thus, $\overline{\text{RESET}}$ must be held a minimum of 100 ns.

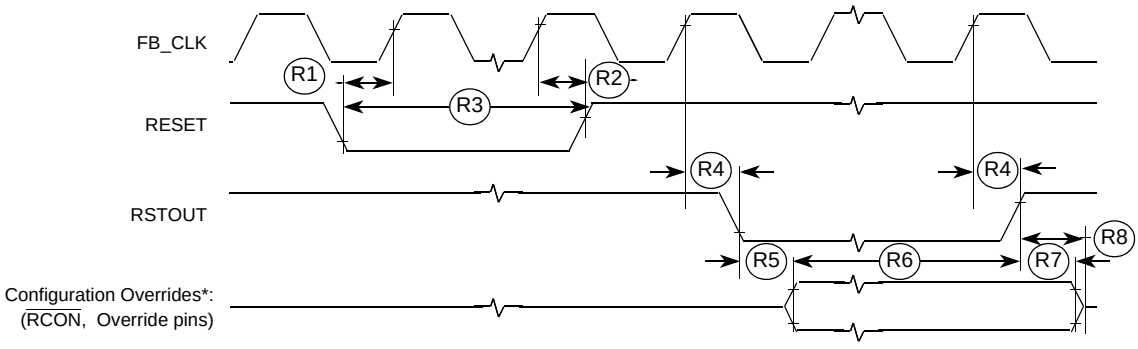


Figure 21. $\overline{\text{RESET}}$ and Configuration Override Timing

NOTE

Refer to the *MCF5208 Reference Manual* for more information.

5.11 I²C Input/Output Timing Specifications

Table 16 and Table 17 list specifications for the I²C input and output timing parameters.

Table 16. I²C Input Timing Specifications between I2C_SCL and I2C_SDA

Num	Characteristic	Min	Max	Unit
I1	Start condition hold time	2	—	t_{cyc}
I2	Clock low period	8	—	t_{cyc}
I3	I2C_SCL/I2C_SDA rise time (V_{IL} = 0.5 V to V_{IH} = 2.4 V)	—	1	ms
I4	Data hold time	0	—	ns
I5	I2C_SCL/I2C_SDA fall time (V_{IH} = 2.4 V to V_{IL} = 0.5 V)	—	1	ms
I6	Clock high time	4	—	t_{cyc}
I7	Data setup time	0	—	ns
I8	Start condition setup time (for repeated start condition only)	2	—	t_{cyc}
I9	Stop condition setup time	2	—	t_{cyc}

Table 17. I²C Output Timing Specifications between I2C_SCL and I2C_SDA

Num	Characteristic	Min	Max	Unit
I1[1]	Start condition hold time	6	—	t_{cyc}
I2 [1.]	Clock low period	10	—	t_{cyc}
I3 [2]	I2C_SCL/I2C_SDA rise time (V_{IL} = 0.5 V to V_{IH} = 2.4 V)	—	—	µs
I4 [1.]	Data hold time	7	—	t_{cyc}
I5 [3]	I2C_SCL/I2C_SDA fall time (V_{IH} = 2.4 V to V_{IL} = 0.5 V)	—	3	ns
I6 [1.]	Clock high time	10	—	t_{cyc}
I7 [1.]	Data setup time	2	—	t_{cyc}
I8 [1.]	Start condition setup time (for repeated start condition only)	20	—	t_{cyc}
I9 [1.]	Stop condition setup time	10	—	t_{cyc}

NOTES:

1 Output numbers depend on the value programmed into the IFDR; an IFDR programmed with the maximum frequency (IFDR = 0x20) results in minimum output timings as shown in Table A-16. The I²C interface is designed to scale the actual data transition time to move it to the middle of the I2C_SCL low period. The actual position is affected by the prescale and division values programmed into the IFDR; however, the numbers given in Table A-16 are minimum values.

2 Because I2C_SCL and I2C_SDA are open-collector-type outputs, which the processor can only actively drive low, the time I2C_SCL or I2C_SDA take to reach a high level depends on external signal capacitance and pull-up resistor values.

3 Specified at a nominal 50-pF load.

5.12.4 MII Serial Management Channel Timing (FEC_MDIO and FEC_MDC)

Table 21 lists MII serial management channel timings. The FEC functions correctly with a maximum MDC frequency of 2.5 MHz.

Table 21. MII Serial Management Channel Timing

Num	Characteristic	Min	Max	Unit
M10	FEC_MDC falling edge to FEC_MDIO output invalid (minimum propagation delay)	0	—	ns
M11	FEC_MDC falling edge to FEC_MDIO output valid (max prop delay)	—	25	ns
M12	FEC_MDIO (input) to FEC_MDC rising edge setup	10	—	ns
M13	FEC_MDIO (input) to FEC_MDC rising edge hold	0	—	ns
M14	FEC_MDC pulse width high	40%	60%	FEC_MDC period
M15	FEC_MDC pulse width low	40%	60%	FEC_MDC period

Figure 26 shows MII serial management channel timings listed in Table 21.

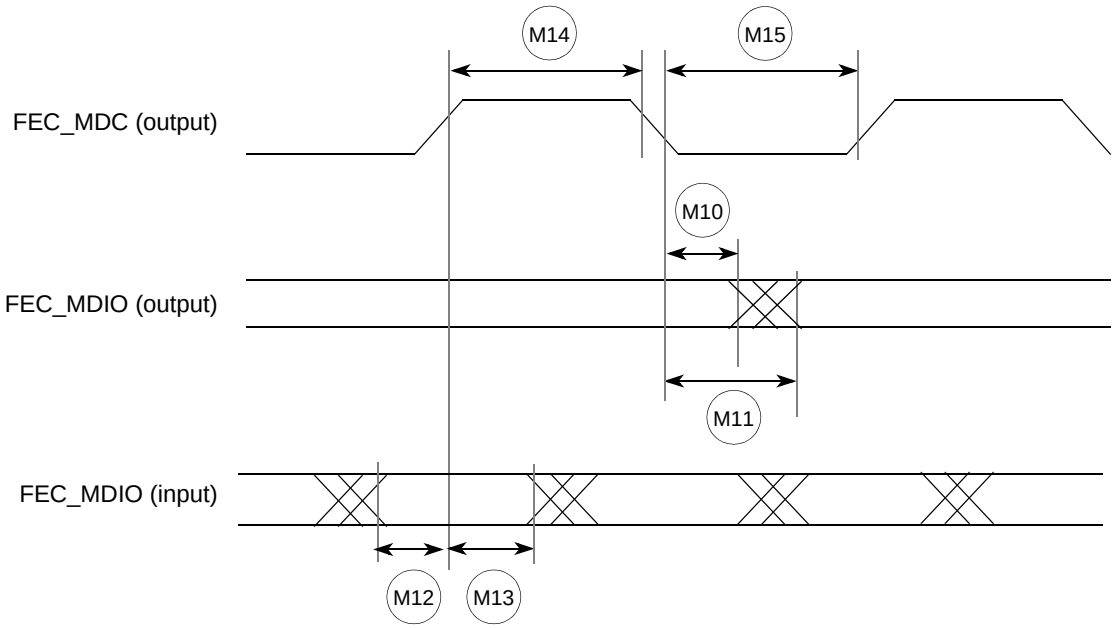


Figure 26. MII Serial Management Channel Timing Diagram

5.13 32-Bit Timer Module AC Timing Specifications

Table 22 lists timer module AC timings.

Table 22. Timer Module AC Timing Specifications

Name	Characteristic	Min	Max	Unit
T1	DT0IN / DT1IN / DT2IN / DT3IN cycle time	3	—	t_{CYC}
T2	DT0IN / DT1IN / DT2IN / DT3IN pulse width	1	—	t_{CYC}

5.14 QSPI Electrical Specifications

Table 23 lists QSPI timings.

Table 23. QSPI Modules AC Timing Specifications

Name	Characteristic	Min	Max	Unit
QS1	QSPI_CS[3:0] to QSPI_CLK	1	510	tcyc
QS2	QSPI_CLK high to QSPI_DOUT valid.	—	10	ns
QS3	QSPI_CLK high to QSPI_DOUT invalid. (Output hold)	1.5	—	ns
QS4	QSPI_DIN to QSPI_CLK (Input setup)	9	—	ns
QS5	QSPI_DIN to QSPI_CLK (Input hold)	9	—	ns

The values in Table 23 correspond to Figure 27.

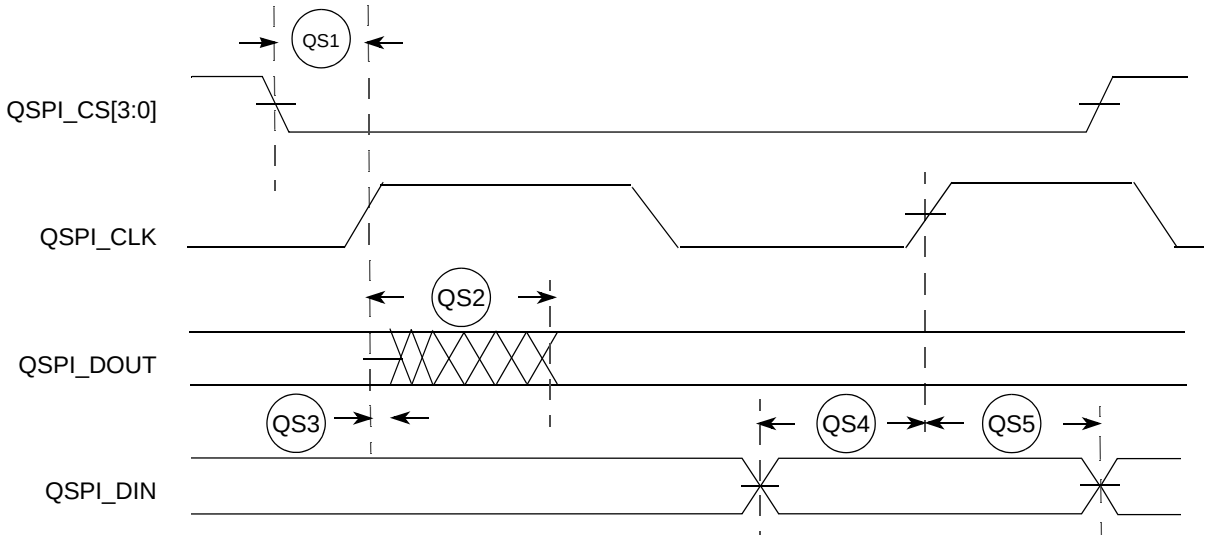


Figure 27. QSPI Timing

5.15 JTAG and Boundary Scan Timing

Table 24. JTAG and Boundary Scan Timing

Num	Characteristics[1]	Symbol	Min	Max	Unit
J1	TCLK Frequency of Operation	f_{JCYC}	DC	1/4	$f_{sys/2}$
J2	TCLK Cycle Period	t_{JCYC}	4	—	t_{CYC}
J3	TCLK Clock Pulse Width	t_{JCW}	26	—	ns
J4	TCLK Rise and Fall Times	t_{JCRF}	0	3	ns
J5	Boundary Scan Input Data Setup Time to TCLK Rise	t_{BSDST}	4	—	ns
J6	Boundary Scan Input Data Hold Time after TCLK Rise	t_{BSDHT}	26	—	ns
J7	TCLK Low to Boundary Scan Output Data Valid	t_{BSDV}	0	33	ns
J8	TCLK Low to Boundary Scan Output High Z	t_{BSDZ}	0	33	ns
J9	TMS, TDI Input Data Setup Time to TCLK Rise	t_{TAPBST}	4	—	ns
J10	TMS, TDI Input Data Hold Time after TCLK Rise	t_{TAPBHT}	10	—	ns
J11	TCLK Low to TDO Data Valid	t_{TDODV}	0	26	ns
J12	TCLK Low to TDO High Z	t_{TDODZ}	0	8	ns
J13	$\overline{TRST}$ Assert Time	t_{TRSTAT}	100	—	ns
J14	$\overline{TRST}$ Setup Time (Negation) to TCLK High	t_{TRSTST}	10	—	ns

NOTES:
1 JTAG_EN is expected to be a static signal. Hence, specific timing is not associated with it.

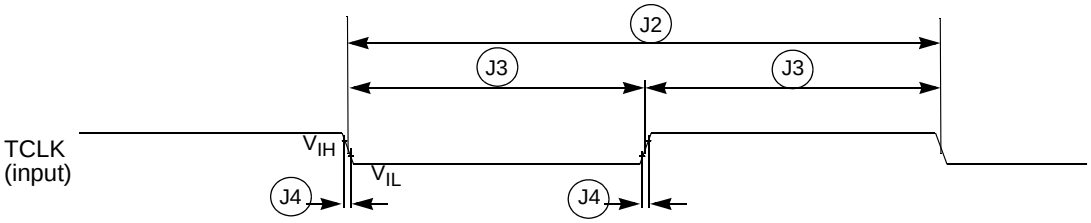


Figure 28. Test Clock Input Timing

5.16 Debug AC Timing Specifications

Table 25 lists specifications for the debug AC timing parameters shown in Figure 32.

Table 25. Debug AC Timing Specification

Num	Characteristic	Min	Max	Unit
D0	PSTCLK cycle time	1	1	t_{SYS}
D1	PSTCLK rising to PSTDDATA valid	—	3.0	ns
D2	PSTCLK rising to PSTDDATA invalid	1.5	—	ns
D3	DSI-to-DSCLK setup	1	—	PSTCLK
D4[1]	DSCLK-to-DSO hold	4	—	PSTCLK
D5	DSCLK cycle time	5	—	PSTCLK
D6	BKPT assertion time	1	—	PSTCLK

NOTES:
1 DSCLK and DSI are synchronized internally. D4 is measured from the synchronized DSCLK input relative to the rising edge of PSTCLK.

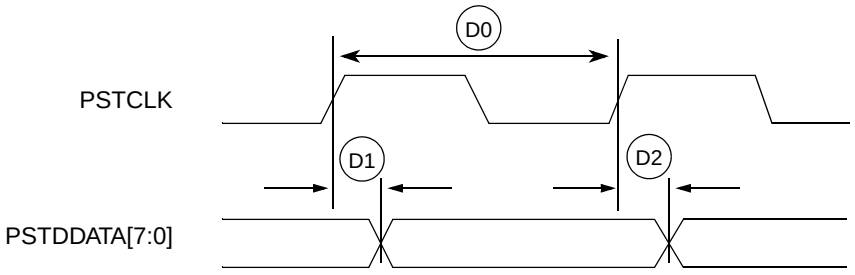


Figure 32. Real-Time Trace AC Timing

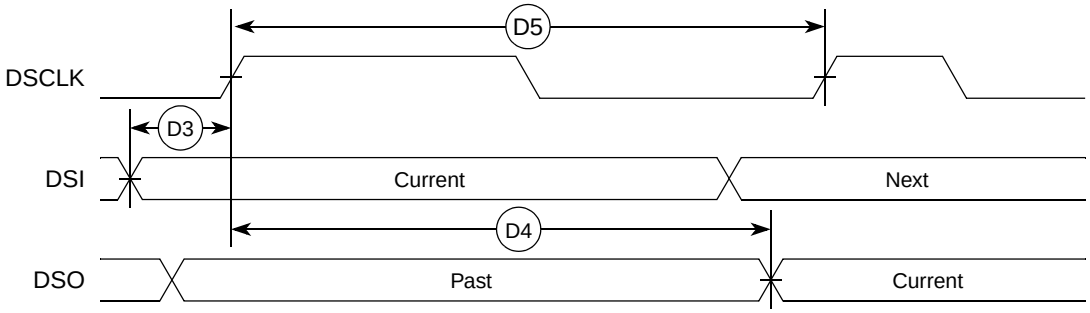


Figure 33. BDM Serial Port AC Timing

Table 26. Revision History (continued)

Revision Number	Date	Substantive Changes
0.4	10/10/2005	• Figure 1 and Table 3: Changed pin 33 from EVDD to SD_VDD • Figure 4 and Table 3: Changed ball D10 from TEST to VSS • Figure 6 and Table 3: Changed pin 39 from EVDD to SD_VDD and pin 117 from TEST to VSS
0.5	3/29/2006	• Added “top view” and “bottom view” labels where appropriate to mechanical drawings and pinouts. • Updated mechanical drawings to latest available, and added note to Section 4, “Mechanicals and Pinouts.”
0.6	7/21/2006	• Corrected cross-reference to Figure 9 in Section 4.7, “Pinout—196 MAPBGA.” • Corrected L3 label in Figure 9 from SD_DR_DQS to SD_SDR_DQS. • Corrected L6 label in Figure 9 from SD_DQS0 to SD_DQS2 and H3 from SD_DQS1 to SD_DQS3. • Removed second sentence from Section 5.12.2, “MII Transmit Signal Timing (FEC_TXD[3:0], FEC_TXEN, FEC_TXER, FEC_TXCLK),” regarding no minimum frequency requirement for TXCLK. • Removed third and fourth paragraphs from Section 5.12.2, “MII Transmit Signal Timing (FEC_TXD[3:0], FEC_TXEN, FEC_TXER, FEC_TXCLK),” as this feature is not supported on this device.
1	3/28/2007	• Removed preliminary designation from Section 5, “Electrical Characteristics.” • Updated Section 5.2, “Thermal Characteristics.” • Updated Section 5.4, “DC Electrical Specifications.” • Added Section 5.5, “Current Consumption.” • Updated Section 5.6, “Oscillator and PLL Electrical Characteristics.” • Made some corrections to the drawings in Section 5.8, “SDRAM Bus.” • Edited for grammar, punctuation, spelling, style, and format. - JD
2	12/4/2008	• Updated FlexBus read and write timing diagrams in Figure 14 and Figure 15. Changed the following specs in Table 12 and Table 13: • Minimum frequency of operation from TBD to 60MHz • Maximum clock period from TBD to 16.67 ns
3	9/1/2009	• Changed doc type from Advance Information to Technical Data