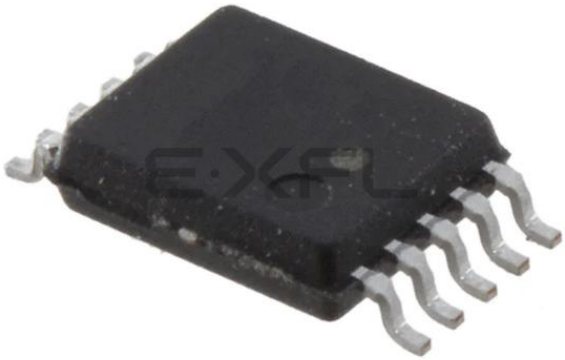

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	78K0S
Core Size	8-Bit
Speed	10MHz
Connectivity	-
Peripherals	LVD, POR, PWM, WDT
Number of I/O	7
Program Memory Size	2KB (2K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	A/D 4x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	10-LSSOP (0.225", 5.72mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd78f9201ma-cac-a

3.2 Processor Registers

The 78K0S/KU1+ provide the following on-chip processor registers.

3.2.1 Control registers

The control registers have special functions to control the program sequence statuses and stack memory. The control registers include a program counter, a program status word, and a stack pointer.

(1) Program counter (PC)

The program counter is a 16-bit register which holds the address information of the next program to be executed.

In normal operation, the PC is automatically incremented according to the number of bytes of the instruction to be fetched. When a branch instruction is executed, immediate data or register contents are set.

Reset signal generation sets the reset vector table values at addresses 0000H and 0001H to the program counter.

Figure 3-7. Program Counter Configuration

	15															0
PC	PC15	PC14	PC13	PC12	PC11	PC10	PC9	PC8	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0

(2) Program status word (PSW)

The program status word is an 8-bit register consisting of various flags to be set/reset by instruction execution.

Program status word contents are stored in stack area upon interrupt request generation or PUSH PSW instruction execution and are restored upon execution of the RETI and POP PSW instructions.

Reset signal generation sets PSW to 02H.

Figure 3-8. Program Status Word Configuration

	7							0
PSW	IE	Z	0	AC	0	0	1	CY

Table 3-3. Special Function Registers (3/3)

Address	Symbol	Bit No.								R/W	Number of Bits Manipulated Simultaneously			After Reset	Reference page
		7	6	5	4	3	2	1	0		1	8	16		
FFA0H	PFCMD	REG7	REG6	REG5	REG4	REG3	REG2	REG1	REG0	W	–	√	–	Undefined	239
FFA1H	PFS	0	0	0	0	0	WEPRERR	VCERR	FPRERR	R/W	√	√	–	00H	239
FFA2H	FLPMC	0	PRSELF4	PRSELF3	PRSELF2	PRSELF1	PRSELF0	0	FLSPM		–	√	–	Undefined	238
FFA3H	FLCMD	0	0	0	0	0	FLCMD2	FLCMD1	FLCMD0		√	√	–	00H	241
FFA4H	FLAPL	FLAP7	FLAP6	FLAP5	FLAP4	FLAP3	FLAP2	FLAP1	FLAP0		√	√	–	00H	242
FFA5H	FLAPH	0	0	0	0	FLAP11	FLAP10	FLAP9	FLAP8		√	√	–		
FFA6H	FLAPHC	0	0	0	0	FLAPC11	FLAPC10	FLAPC9	FLAPC8		√	√	–	00H	242
FFA7H	FLAPLC	FLAPC7	FLAPC6	FLAPC5	FLAPC4	FLAPC3	FLAPC2	FLAPC1	FLAPC0		√	√	–		
FFA8H	FLW	FLW7	FLW6	FLW5	FLW4	FLW3	FLW2	FLW1	FLW0		–	√	–	00H	243
FFA9H to FFDFH	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
FFE0H	IF0	<ADIF> Note 1	<TMIF010> Note 1	<TMIF000> Note 1	<TMIFH1>	<PIF1>	<PIF0>	<LVIIF>	0	R/W	√	√	–	00H	179
FFE1H to FFE3H	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
FFE4H	MK0	<ADMK> Note 1	<TMMK010> Note 1	<TMMK000> Note 1	<TMMKH1>	<PMK1>	<PMK0>	<LVIMK>	1	R/W	√	√	–	FFH	180
FFE5H to FFEBH	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
FFECH	INTM0	0	0	ES11	ES10	ES01	ES00	0	0	R/W	–	√	–	00H	180
FFEDH to FFF2H	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
FFF3H	PPCC	0	0	0	0	0	0	PPCC1	PPCC0	R/W	√	√	–	02H	76
FFF4H	OSTS Note 1	0	0	0	0	0	0	OSTS1	OSTS0		–	√	–	Undefined Note 2	78, 188
FFF5H to FFFAH	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
FFFBH	PCC	0	0	0	0	0	0	PCC1	0	R/W	√	√	–	02H	76

<R>

Notes 1. μPD78F920x only

2. The oscillation stabilization time that elapses after release of reset is selected by the option byte. For details, refer to **CHAPTER 15 OPTION BYTE**.

Remark For a bit name enclosed in angle brackets (<>), the bit name is defined as a reserved word in the RA78K0S, and is defined as an sfr variable using the #pragma sfr directive in the CC78K0S.

3.4.6 Based addressing

[Function]

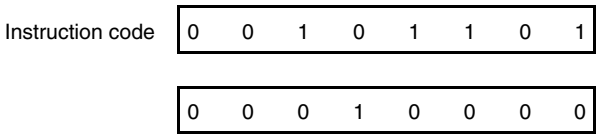
8-bit immediate data is added to the contents of the base register, that is, the HL register pair, and the sum is used to address the memory. Addition is performed by expanding the offset data as a positive number to 16 bits. A carry from the 16th bit is ignored. This addressing can be carried out for all the memory spaces.

[Operand format]

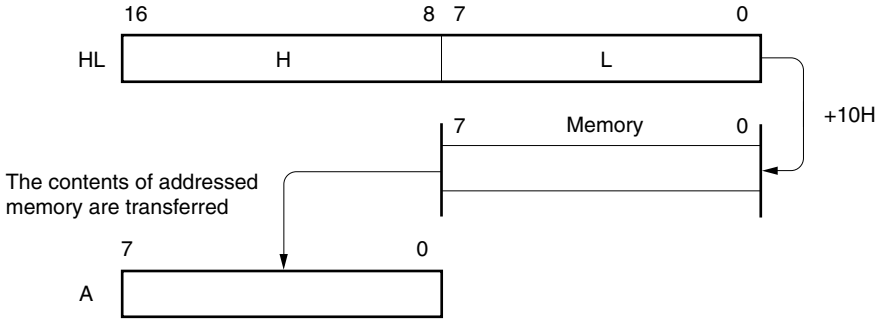
Identifier	Description
–	[HL+byte]

[Description example]

MOV A, [HL+10H]; When setting byte to 10H



[Illustration]



3.4.7 Stack addressing

[Function]

The stack area is indirectly addressed with the stack pointer (SP) contents.

This addressing method is automatically employed when the PUSH, POP, subroutine call, and return instructions are executed or the register is saved/restored upon interrupt request generation.

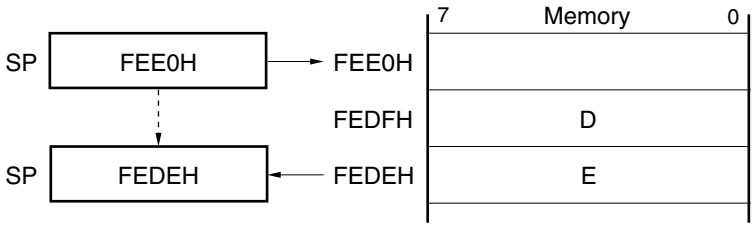
Stack addressing can be used to access the internal high-speed RAM area only.

[Description example]

In the case of PUSH DE

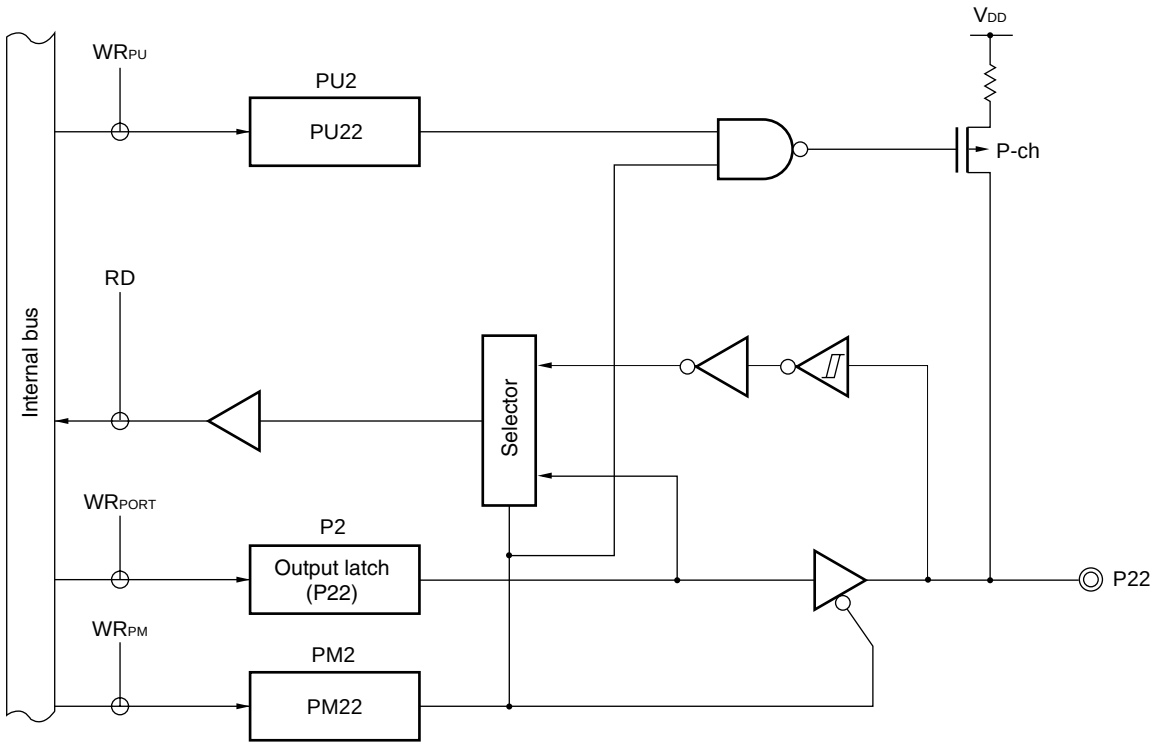
Instruction code	1	0	1	0	1	0	1	0

[Illustration]



<R>

Figure 4-6. Block Diagram of P22 (μPD78F950x)



P2: Port register 2
PU2: Pull-up resistor option register 2
PM2: Port mode register 2
RD: Read signal
WR××: Write signal

5.4 System Clock Oscillators

The following three types of system clock oscillators are available.

- High-speed internal oscillator: Internally oscillates a clock of 8 MHz (TYP.).
- Crystal/ceramic oscillator [Note 1]: Oscillates a clock of 2 MHz to 10 MHz.
- External clock input circuit: Supplies a clock of 2 MHz to 10 MHz to the X1 pin [Note 2].

<R> **Notes 1.** μPD78F920x only

<R> **2.** μPD78F920x: X1 pin, μPD78F950x: EXCLK pin

5.4.1 High-speed internal oscillator

The 78K0S/KU1+ include a high-speed internal oscillator (8 MHz (TYP.)).

If the high-speed internal oscillation is selected by the option byte as the clock source, the X1 and X2 pins in μPD78F920x, and the EXCLK pin in μPD78F950x can be used as I/O port pins.

For details of the option byte, refer to **CHAPTER 15 OPTION BYTE**. For details of I/O ports, refer to **CHAPTER 4 PORT FUNCTIONS**.

5.4.2 Crystal/ceramic oscillator (μPD78F920x only)

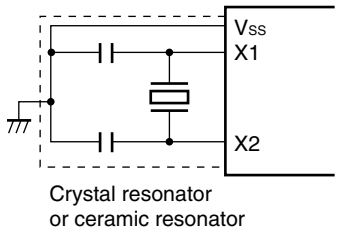
The crystal/ceramic oscillator oscillates using a crystal or ceramic resonator connected between the X1 and X2 pins.

If the crystal/ceramic oscillator is selected by the option byte as the system clock source, the X1 and X2 pins are used as crystal or ceramic resonator connection pins.

For details of the option byte, refer to **CHAPTER 15 OPTION BYTE**. For details of I/O ports, refer to **CHAPTER 4 PORT FUNCTIONS**.

Figure 5-6 shows the external circuit of the crystal/ceramic oscillator.

Figure 5-6. External Circuit of Crystal/Ceramic Oscillator (μPD78F920x Only)



Caution When using the crystal/ceramic oscillator, wire as follows in the area enclosed by the broken lines in Figure 5-6 to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines. Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as Vss. Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

Figure 6-10. Format of Port Mode Control Register 2 (PMC2)

Address: FF84H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
PMC2	0	0	0	0	PMC23	PMC22	PMC21	PMC20

PMC2n	Specification of operation mode (n = 0 to 3)
0	Port/Alternate-function (except A/D converter) mode
1	A/D converter mode

6.4 Operation of 16-Bit Timer/Event Counter 00

6.4.1 Interval timer operation

Setting 16-bit timer mode control register 00 (TMC00) and capture/compare control register 00 (CRC00) as shown in Figure 6-11 allows operation as an interval timer.

Setting

The basic operation setting procedure is as follows.

<1> Set the CRC00 register (see **Figure 6-11** for the set value).
<2> Set any value to the CR000 register.
<3> Set the count clock by using the PRM00 register.
<4> Set the TMC00 register to start the operation (see **Figure 6-11** for the set value).

Caution Changing the CR000 setting during TM00 operation may cause a malfunction. To change the setting, refer to 6.5 Cautions Related to 16-Bit Timer/Event Counter 00 (17) Changing compare register during timer operation.

Remark For how to enable the INTTM000 interrupt, see **CHAPTER 10 INTERRUPT FUNCTIONS**.

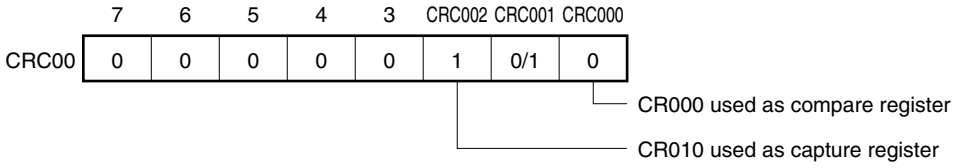
Interrupt requests are generated repeatedly using the count value set in 16-bit timer capture/compare register 000 (CR000) beforehand as the interval.

When the count value of 16-bit timer counter 00 (TM00) matches the value set to CR000, counting continues with the TM00 value cleared to 0 and the interrupt request signal (INTTM000) is generated.

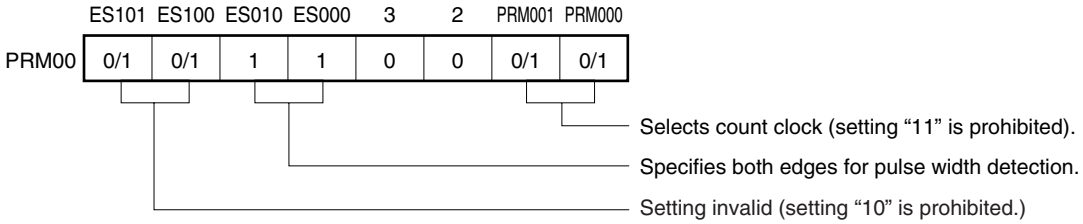
The count clock of the 16-bit timer/event counter can be selected using bits 0 and 1 (PRM000, PRM001) of prescaler mode register 00 (PRM00).

Figure 6-19. Control Register Settings for Pulse Width Measurement with Free-Running Counter and One Capture Register (When TI000 and CR010 Are Used)

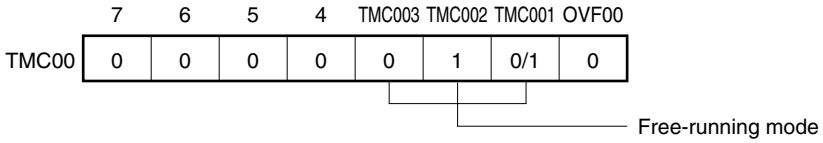
(a) Capture/compare control register 00 (CRC00)



(b) Prescaler mode register 00 (PRM00)



(c) 16-bit timer mode control register 00 (TMC00)



Remark 0/1: Setting 0 or 1 allows another function to be used simultaneously with pulse width measurement. See the description of the respective control registers for details.

Figure 6-20. Configuration Diagram for Pulse Width Measurement by Free-Running Counter

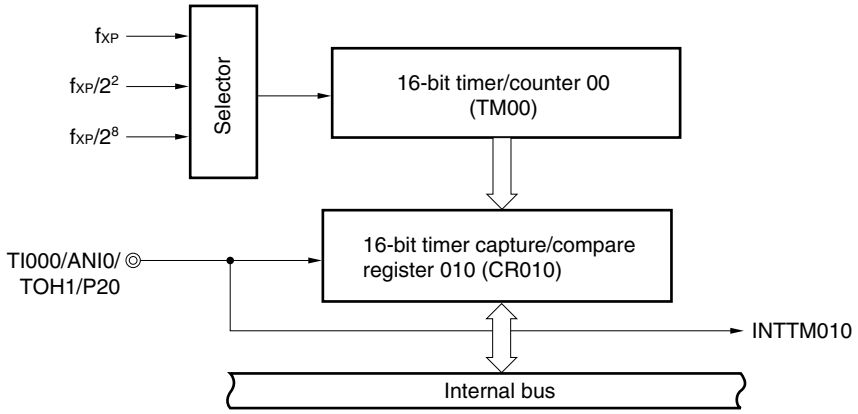
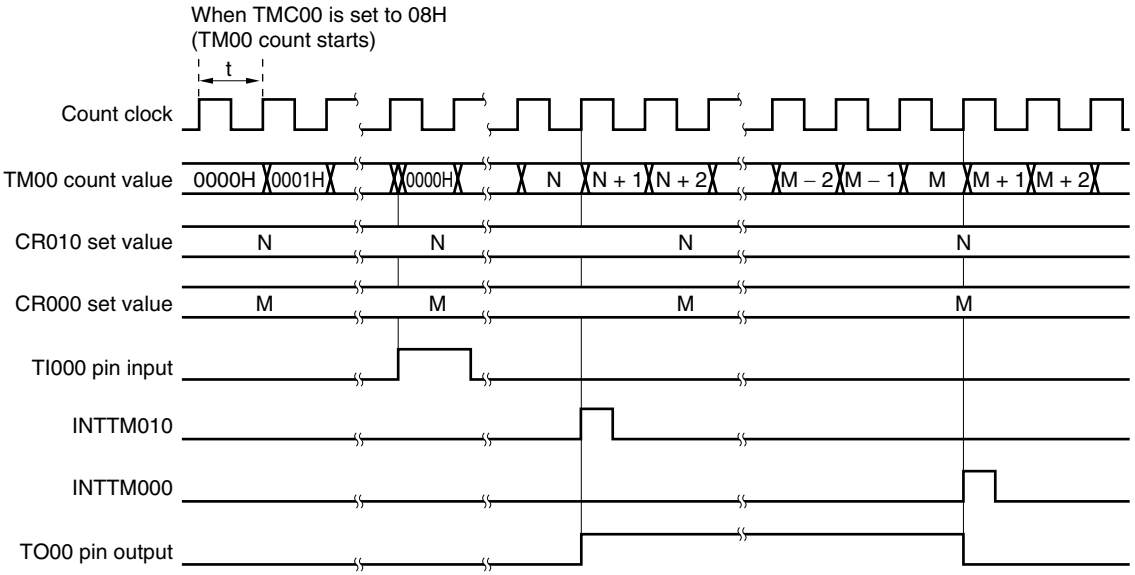


Figure 6-36. Timing of One-Shot Pulse Output Operation with External Trigger (with Rising Edge Specified)



Caution 16-bit timer counter 00 starts operating as soon as a value other than 00 (operation stop mode) is set to the TMC002 and TMC003 bits.

Remark N < M

<R> **(2) Port mode register 2 (PM2) and port mode control register 2 (PMC2)[Note]**

When using the P20/TOH1/TI000/ANI0 pin for timer output, clear PM20, the output latch of P20, and PMC20 to 0.

PM2 and PMC2 can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets PM2 to FFH, and clears PMC2 to 00H.

Note μPD78F920x only

Figure 7-5. Format of Port Mode Register 2 (PM2)

Address: FF22H After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
PM2	1	1	1	1	PM23	PM22	PM21	PM20

PM2n	P2n pin I/O mode selection (n = 0 to 3)
0	Output mode (output buffer on)
1	Input mode (output buffer off)

Figure 7-6. Format of Port Mode Control Register 2 (PMC2) (μPD78F920x Only)

Address: FF84H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
PMC2	0	0	0	0	PMC23	PMC22	PMC21	PMC20

PMC2n	Specification of operation mode (n = 0 to 3)
0	Port/Alternate-function (except A/D converter) mode
1	A/D converter mode

7.4 Operation of 8-Bit Timer H1

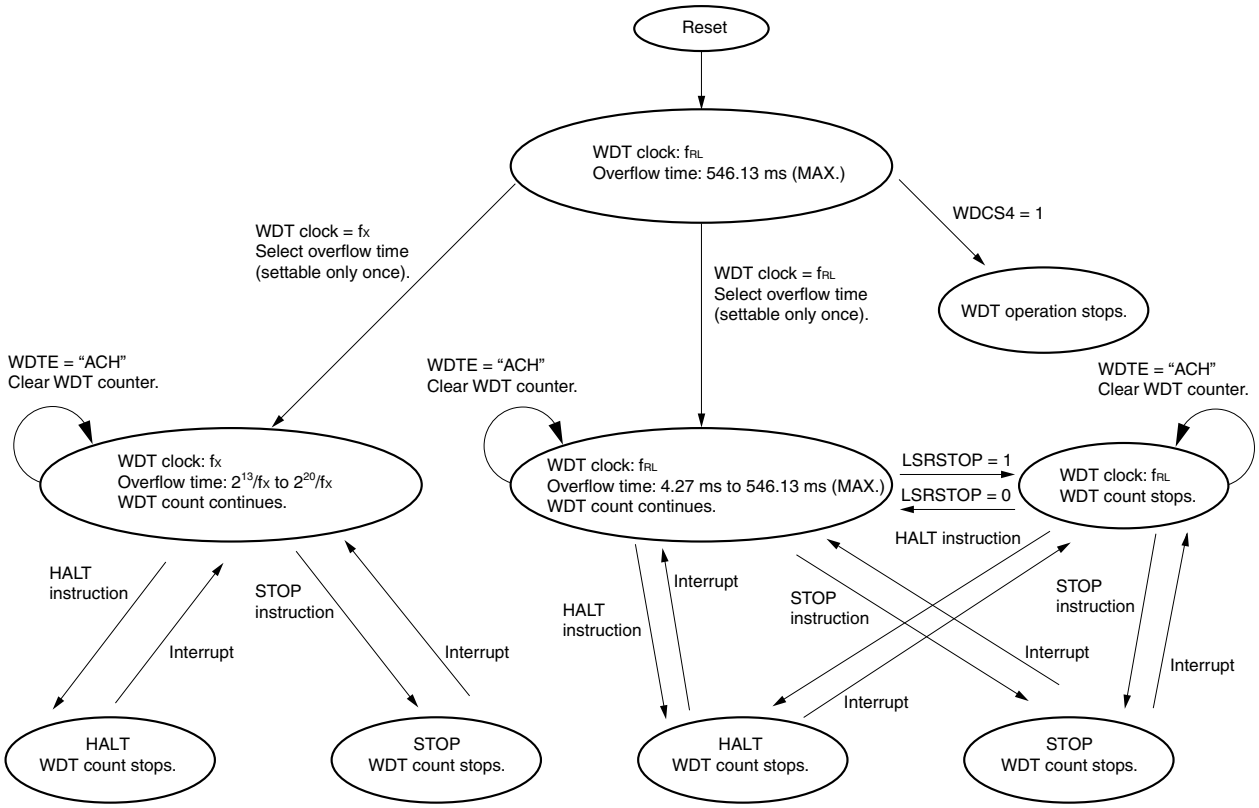
7.4.1 Operation as interval timer/square-wave output

When 8-bit timer counter H1 and compare register 01 (CMP01) match, an interrupt request signal (INTTMH1) is generated and 8-bit timer counter H1 is cleared to 00H.

Compare register 11 (CMP11) is not used in interval timer mode. Since a match of 8-bit timer counter H1 and the CMP11 register is not detected even if the CMP11 register is set, timer output is not affected.

By setting bit 0 (TOEN1) of timer H mode register 1 (TMHMD1) to 1, a square wave of any frequency (duty = 50%) is output from TOH1.

Figure 8-5. Status Transition Diagram When "Low-Speed Internal Oscillator Can Be Stopped by Software" Is Selected by Option Byte



11.2.2 STOP mode

(1) STOP mode setting and operating statuses

The STOP mode is set by executing the STOP instruction.

Caution Because an interrupt request signal is used to clear the standby mode, if there is an interrupt source with the interrupt request flag set and the interrupt mask flag reset, the standby mode is immediately cleared if set. Thus, in the STOP mode, the normal operation mode is restored after the STOP instruction is executed and then the operation is stopped for the duration of 34 μs (TYP.) (after an additional wait time for stabilizing oscillation set by the oscillation stabilization time select register (OSTS) has elapsed when crystal/ceramic oscillation is used).

The operating statuses in the STOP mode are shown below.

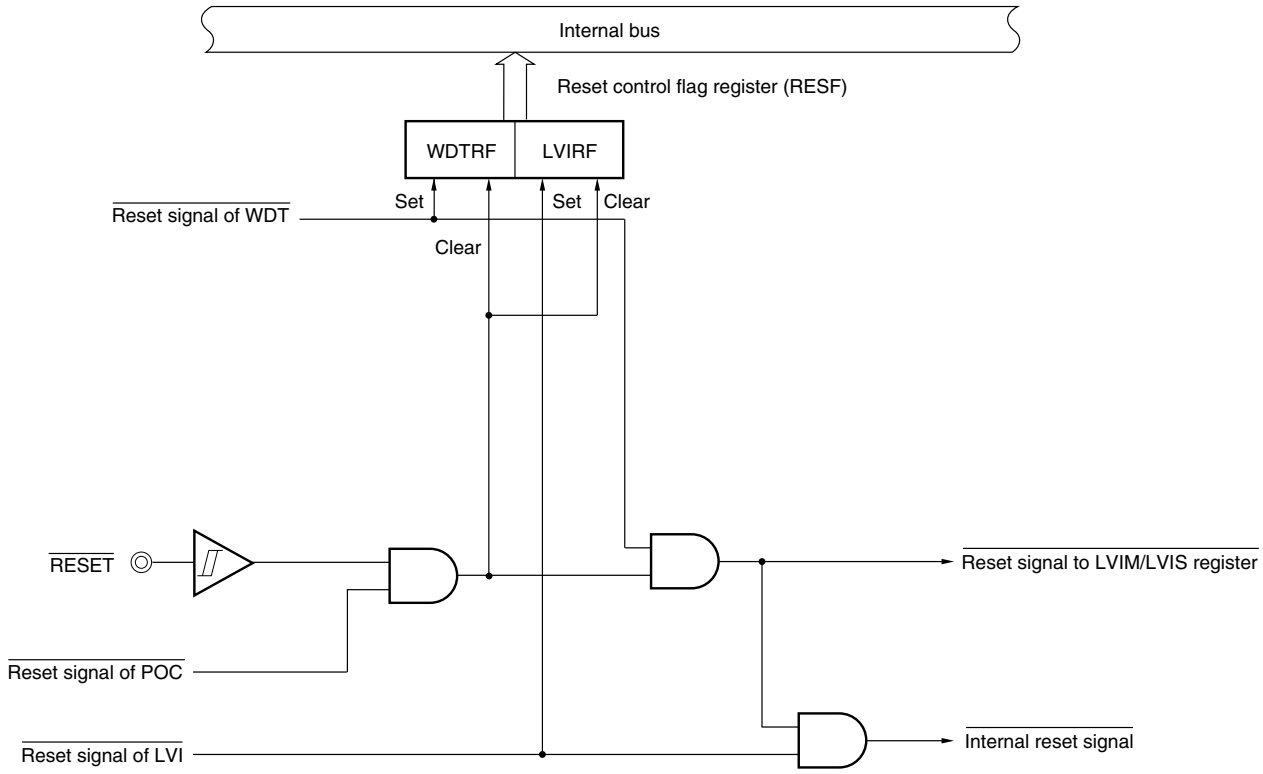
Table 11-4. Operating Statuses in STOP Mode

Setting of STOP Mode / Item		Low-Speed Internal Oscillator cannot be stopped[Note 1].	Low-Speed Internal Oscillator can be stopped[Note 1].	
			When Low-Speed Internal Oscillation Continues	When Low-Speed Internal Oscillation Stops
System clock		Oscillation stops.		
CPU		Operation stops.		
Port (latch)		Holds status before STOP mode was set.		
16-bit timer/event counter 00[Note 2]		Operation stops.		
8-bit timer H1	Sets count clock to f_{XP} to $f_{XP}/2^{12}$	Operation stops.		
	Sets count clock to $f_{RL}/2^{7}$	Operable	Operable	Operation stops.
Watchdog timer	"System clock" selected as operating clock	Setting disabled.	Operation stops.	
	"Low-speed internal oscillation clock" selected as operating clock	Operable (Operation continues)	Operation stops.	
A/D converter[Note 2]		Operation stops.		
Power-on-clear circuit		Always operates.		
Low-voltage detector		Operable		
External interrupt		Operable		

Notes 1. "Cannot be stopped" or "Stopped by software" is selected for low-speed internal oscillator by the option byte (for the option byte, see **CHAPTER 15 OPTION BYTE**).

<R> **2.** μPD78F920x only

Figure 12-1. Block Diagram of Reset Function



Caution The LVI circuit is not reset by the internal reset signal of the LVI circuit.

Remarks 1. LVIM: Low-voltage detect register

2. LVIS: Low-voltage detection level select register

CHAPTER 13 POWER-ON-CLEAR CIRCUIT

13.1 Functions of Power-on-Clear Circuit

The power-on-clear circuit (POC) has the following functions.

- Generates internal reset signal at power on.
- Compares supply voltage (V_{DD}) and detection voltage (V_{POC} = 2.1 V ±0.1 V), and generates internal reset signal when $V_{DD} < V_{POC}$.
- Compares supply voltage (V_{DD}) and detection voltage (V_{POC} = 2.1 V ±0.1 V), and releases internal reset signal when $V_{DD} \geq V_{POC}$.

Cautions 1. If an internal reset signal is generated in the POC circuit, the reset control flag register (RESF) is cleared to 00H.

2. Because the detection voltage (V_{POC}) of the POC circuit is in a range of 2.1 V ±0.1 V, use a voltage in the range of 2.2 to 5.5 V.

Remark This product incorporates multiple hardware functions that generate an internal reset signal. A flag that indicates the reset cause is located in the reset control flag register (RESF) for when an internal reset signal is generated by the watchdog timer (WDT) or low-voltage-detection (LVI) circuit. RESF is not cleared to 00H and the flag is set to 1 when an internal reset signal is generated by WDT or LVI.
For details of RESF, see **CHAPTER 12 RESET FUNCTION**.

CHAPTER 14 LOW-VOLTAGE DETECTOR

14.1 Functions of Low-Voltage Detector

The low-voltage detector (LVI) has following functions.

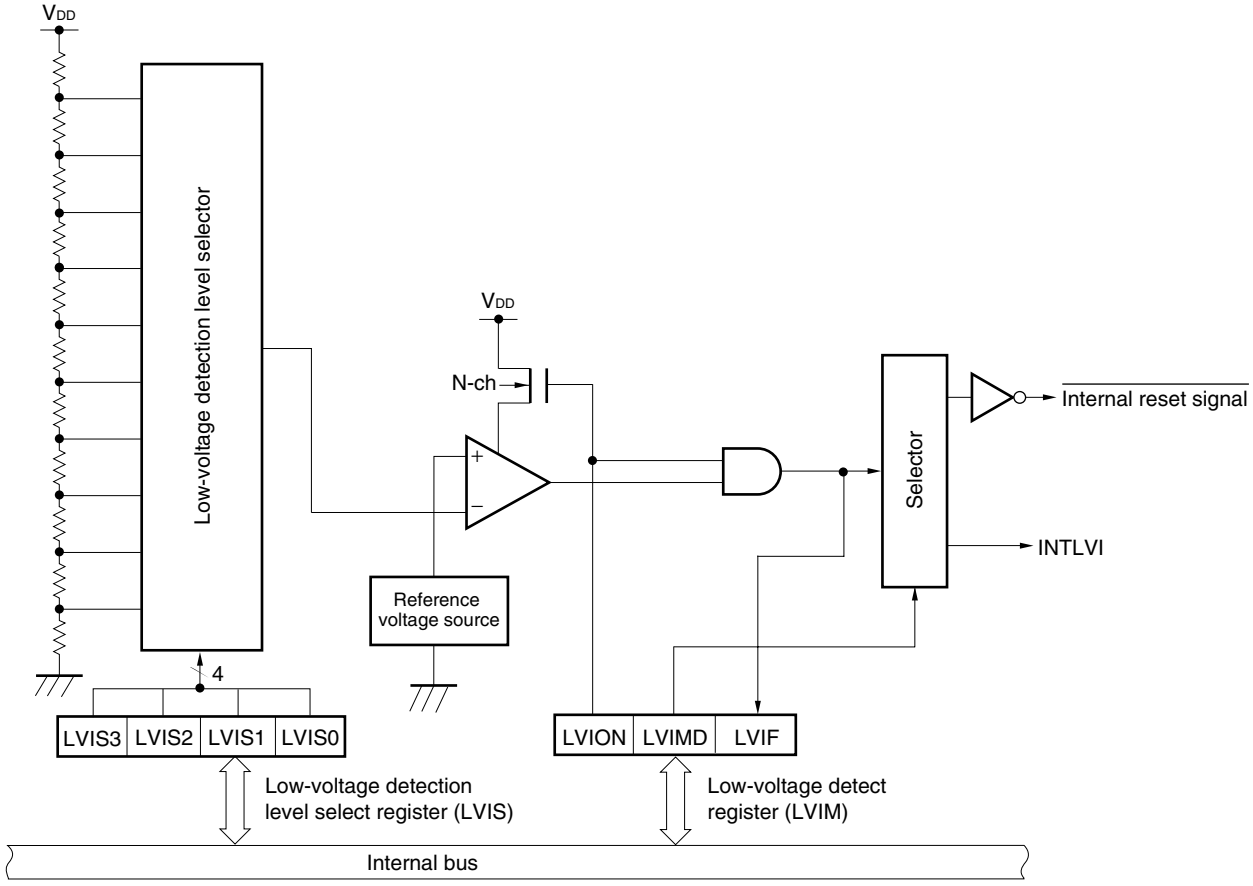
- Compares supply voltage (V_{DD}) and detection voltage (V_{LVI}), and generates an internal interrupt signal or internal reset signal when $V_{DD} < V_{LVI}$.
- Detection levels (ten levels) of supply voltage can be changed by software.
- Interrupt or reset function can be selected by software.
- Operable in STOP mode.

When the low-voltage detector is used to reset, bit 0 (LVIRF) of the reset control flag register (RESF) is set to 1 if reset occurs. For details of RESF, refer to **CHAPTER 12 RESET FUNCTION**.

14.2 Configuration of Low-Voltage Detector

The block diagram of the low-voltage detector is shown in Figure 14-1.

Figure 14-1. Block Diagram of Low-Voltage Detector



(2) When used as interrupt

- When starting operation

<1> Mask the LVI interrupt (LVIMK = 1).

<2> Set the detection voltage using bits 3 to 0 (LVIS3 to LVIS0) of the low-voltage detection level select register (LVIS).

<3> Set bit 7 (LVION) of LVIM to 1 (enables LVI operation).

<4> Use software to instigate a wait of at least 0.2 ms.

<5> Wait until "supply voltage (V_{DD}) ≥ detection voltage (V_{LVI})" at bit 0 (LVIF) of LVIM is confirmed.

<6> Clear the interrupt request flag of LVI (LVIIF) to 0.

<7> Release the interrupt mask flag of LVI (LVIMK).

<8> Execute the EI instruction (when vector interrupts are used).

Figure 14-5 shows the timing of generating the interrupt signal of the low-voltage detector. Numbers <1> to <7> in this figure correspond to <1> to <7> above.

- When stopping operation

  Either of the following procedures must be executed.

  - When using 8-bit memory manipulation instruction: Write 00H to LVIM.
  - When using 1-bit memory manipulation instruction: Clear LVION to 0.

An example of a program when the command execution time (from erasure to black check) should be minimized in self programming mode is shown below.

```
;---------------------------------------------------------------------
;START
;---------------------------------------------------------------------
       MOV      MK0,#11111111B   ; Masks all interrupts
       MOV      FLCMD,#00H       ; Clears FLCMD register

       DI

ModeOnLoop:                      ; Configure settings so that the CPU clock ≥ 1 MHz
       MOV      PFS,#00H         ; Clears flash status register
       MOV      PFCMD,#0A5H      ; PFCMD register control
       MOV      FLPMC,#01H       ; FLPMC register control (sets value)
       MOV      FLPMC,#0FEH      ; FLPMC register control (inverts set value)
       MOV      FLPMC,#01H       ; Sets self programming mode with FLPMC register control (sets
                                 ; value)

       NOP
       HALT
       BT PFS.0,$ModeOnLoop      ; Checks completion of write to specific registers
                                 ; Repeats the same processing when an error occurs.
FlashBlockErase:
       MOV      FLCMD,#03H       ; Sets flash control command (block erase)
       MOV      FLAPH,#07H       ; Sets number of block to be erased (block 7 is specified
                                 ; here)
       MOV      FLAPL,#00H       ; Fixes FLAPL to “00H”
       MOV      FLAPHC,#07H      ; Sets erase block compare number (same value as that of
                                 ; FLAPH)
       MOV      FLAPLC,#00H      ; Fixes FLAPLC to “00H”

       MOV      WDTE,#0ACH       ; Clears & restarts WDT
       HALT                      ; Self programming is started
       MOV      A,PFS
       CMP      A,#00H
       BNZ      $StatusError     ; Checks erase error
                                 ; Performs abnormal termination processing when an error
                                 ; occurs.

FlashBlockBlankCheck:
       MOV      FLCMD,#04H       ; Sets flash control command (block blank check)
       MOV      FLAPH,#07H       ; Sets number of block for blank check (block 7 is specified
                                 ; here)
       MOV      FLAPL,#00H       ; Fixes FLAPL to “00H”

       MOV      FLAPHC,#07H      ; Sets blank check block compare number (same value as of
                                 ; FLAPH)
```

Mnemonic	Operand	Bytes	Clocks	Operation	Flag		
					Z	AC	CY
CALL	!addr16	3	6	$(SP-1) \leftarrow (PC+3)_H$, $(SP-2) \leftarrow (PC+3)_L$, $PC \leftarrow$ addr16, $SP \leftarrow SP-2$			
CALLT	[addr5]	1	8	$(SP-1) \leftarrow (PC+1)_H$, $(SP-2) \leftarrow (PC+1)_L$, $PC_H \leftarrow$ (00000000, addr5 + 1), $PC_L \leftarrow$ (00000000, addr5), $SP \leftarrow SP-2$			
RET		1	6	$PC_H \leftarrow (SP+1)$, $PC_L \leftarrow (SP)$, $SP \leftarrow SP+2$			
RETI		1	8	$PC_H \leftarrow (SP+1)$, $PC_L \leftarrow (SP)$, PSW $\leftarrow (SP+2)$, $SP \leftarrow SP+3$, NMIS $\leftarrow 0$	R	R	R
PUSH	PSW	1	2	$(SP-1) \leftarrow$ PSW, $SP \leftarrow SP-1$			
	rp	1	4	$(SP-1) \leftarrow rp_H$, $(SP-2) \leftarrow rp_L$, $SP \leftarrow SP-2$			
POP	PSW	1	4	PSW $\leftarrow (SP)$, $SP \leftarrow SP+1$	R	R	R
	rp	1	6	$rp_H \leftarrow (SP+1)$, $rp_L \leftarrow (SP)$, $SP \leftarrow SP+2$			
MOVW	SP, AX	2	8	$SP \leftarrow$ AX			
	AX, SP	2	6	AX $\leftarrow$ SP			
BR	!addr16	3	6	PC $\leftarrow$ addr16			
	$addr16	2	6	PC $\leftarrow$ PC + 2 + jdisp8			
	AX	1	6	$PC_H \leftarrow$ A, $PC_L \leftarrow$ X			
BC	$saddr16	2	6	PC $\leftarrow$ PC + 2 + jdisp8 if CY = 1			
BNC	$saddr16	2	6	PC $\leftarrow$ PC + 2 + jdisp8 if CY = 0			
BZ	$saddr16	2	6	PC $\leftarrow$ PC + 2 + jdisp8 if Z = 1			
BNZ	$saddr16	2	6	PC $\leftarrow$ PC + 2 + jdisp8 if Z = 0			
BT	saddr.bit, $addr16	4	10	PC $\leftarrow$ PC + 4 + jdisp8 if (saddr.bit) = 1			
	sfr.bit, $addr16	4	10	PC $\leftarrow$ PC + 4 + jdisp8 if sfr.bit = 1			
	A.bit, $addr16	3	8	PC $\leftarrow$ PC + 3 + jdisp8 if A.bit = 1			
	PSW.bit, $addr16	4	10	PC $\leftarrow$ PC + 4 + jdisp8 if PSW.bit = 1			
BF	saddr.bit, $addr16	4	10	PC $\leftarrow$ PC + 4 + jdisp8 if (saddr.bit) = 0			
	sfr.bit, $addr16	4	10	PC $\leftarrow$ PC + 4 + jdisp8 if sfr.bit = 0			
	A.bit, $addr16	3	8	PC $\leftarrow$ PC + 3 + jdisp8 if A.bit = 0			
	PSW.bit, $addr16	4	10	PC $\leftarrow$ PC + 4 + jdisp8 if PSW.bit = 0			
DBNZ	B, $addr16	2	6	B $\leftarrow$ B – 1, then PC $\leftarrow$ PC + 2 + jdisp8 if B $\neq 0$			
	C, $addr16	2	6	C $\leftarrow$ C – 1, then PC $\leftarrow$ PC + 2 + jdisp8 if C $\neq 0$			
	saddr, $addr16	3	8	(saddr) $\leftarrow$ (saddr) – 1, then PC $\leftarrow$ PC + 3 + jdisp8 if (saddr) $\neq 0$			
NOP		1	2	No Operation			
EI		3	6	IE $\leftarrow$ 1 (Enable Interrupt)			
DI		3	6	IE $\leftarrow$ 0 (Disable Interrupt)			
HALT		1	2	Set HALT Mode			
STOP		1	2	Set STOP Mode			

Remark One instruction clock cycle is one CPU clock cycle (f_{CPU}) selected by the processor clock control register (PCC).

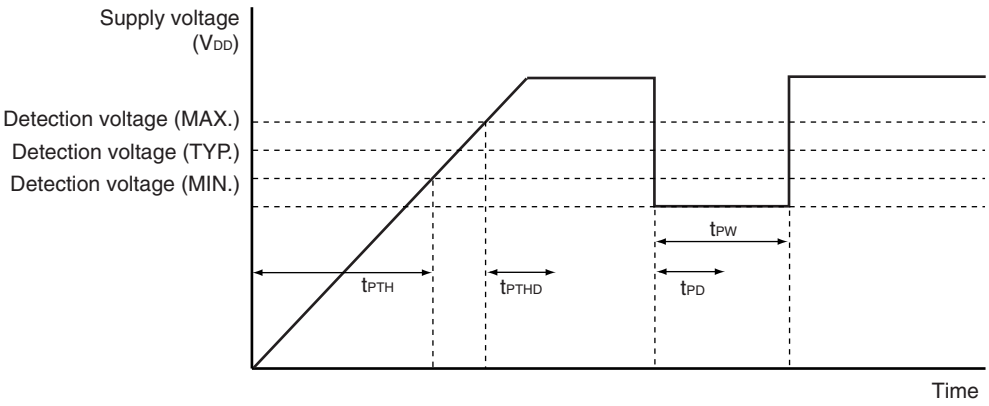
POC Circuit Characteristics (T_A = –40 to +85°C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	V_{POC}		2.0	2.1	2.2	V
Power supply rise time	t_{PTH}	V_{DD}: 0 V → 2.1 V	1.5			μs
Response delay time 1[Note 1]	t_{PTHD}	When power supply rises, after reaching detection voltage (MAX.)			3.0	ms
Response delay time 2[Note 2]	t_{PD}	When power supply falls			1.0	ms
Minimum pulse width	t_{PW}		0.2			ms

Notes 1. Time required from voltage detection to internal reset release.

2. Time required from voltage detection to internal reset signal generation.

POC Circuit Timing



<R> E.2 Revision History up to Previous Editions

The following table shows the revision history up to this edition. The “Applied to:” column indicates the chapters of each edition in which the revision was applied.

(1/2)

Edition	Description	Applied to:
2nd edition	Modification of **1.1 Features**	**CHAPTER 1 OVERVIEW**
	Addition of **Note 2** to **5** in **1.4 78K0S/Kx1+ Product Lineup**	
	9.1 Functions of A/D Converter • Addition of **Notes 4** to **Table 9-1 Sampling Time and A/D Conversion Time**	**CHAPTER 9 A/D CONVERTER**
	9.3 Registers Used by A/D Converter • Addition of **Note 5** to **Figure 9-3 Format of A/D Converter Mode Register (ADM)**	
	9.6 Cautions for A/D Converter • Addition of description to **(6) Input impedance of ANI0 to ANI3 pins**	
	Modification of **Caution 3**	**CHAPTER 12 RESET FUNCTION**
	16.4 Writing with Flash Memory Programmer • Addition of FlashPro5 to Dedicated flash memory programmer • Deletion of PG-FPL2 from Dedicated flash memory programmer • Modification of **Remark**	**CHAPTER 16 FLASH MEMORY**
	16.5 Programming Environment • Modification of **Figure 16-2 Environment for Writing Program to Flash Memory (FlashPro4/FlashPro5/QB-MINI2)** and addition of **Note** • Modification of **Table 16-2 Wiring Between 78K0S/KU1+ and FlashPro4/FlashPro5/QB-MINI2** and Addition of **Note 2** • Modification of **Figure 16-3 Wiring diagram with FlashPro4/FlashPro5/QB-MINI2** • Deletion of PG-FPL2 from dedicated flash memory programmer	
	Modification of **Figure 16-5 PG-FP5 GUI Software Setting Example**	
	Modification of **Figure 16-7 Communication Commands**	
	Addition of **Note** in **Table 16-10 Self Programming Controlling Commands**	
	Addition of this chapter	**CHAPTER 17 ON-CHIP DEBUG FUNCTION**
	• Modification of **X1 Oscillator Characteristics** • Addition of setting range of CPU clock and peripheral clock frequency to **AC Characteristics**	**CHAPTER 19 ELECTRICAL SPECIFICATIONS**
	Modification of **Figure A-1 Development Tools**	**APPENDIX A DEVELOPMENT TOOLS**
	A.4 Flash Memory Writing Tools • Addition of FlashPro5 • Deletion of PG-FPL2	
	A.5.1 When using in-circuit emulator QB-78K0SKX1 • Deletion of description of under development	
	Deletion of **A.5.3 When using in-circuit emulator IE-78K0S-NS or IE-78K0S-NS-A** and **A.5.4 When using in-circuit emulator QB-78K0SKX1MINI** in old edition	
	Modification of **A.6 Debugging Tools (Software)**	