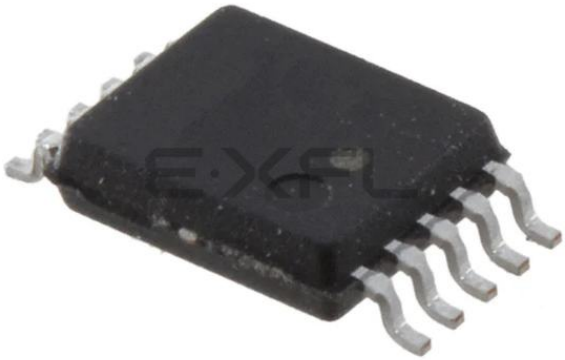

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	78K0S
Core Size	8-Bit
Speed	10MHz
Connectivity	-
Peripherals	LVD, POR, PWM, WDT
Number of I/O	7
Program Memory Size	4KB (4K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	A/D 4x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	10-LSSOP (0.225", 5.72mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd78f9202ma-cac-a

3.3.4 Register addressing 46
3.4 Operand Address Addressing 47
3.4.1 Direct addressing 47
3.4.2 Short direct addressing 48
3.4.3 Special function register (SFR) addressing 49
3.4.4 Register addressing 50
3.4.5 Register indirect addressing 51
3.4.6 Based addressing 52
3.4.7 Stack addressing 53

CHAPTER 4 PORT FUNCTIONS 54

4.1 Functions of Ports 54
4.2 Port Configuration 55
4.2.1 Port 2 56
4.2.2 Port 3 64
4.2.3 Port 4 66
4.3 Registers Controlling Port Functions 66
4.4 Operation of Port Function 71
4.4.1 Writing to I/O port 71
4.4.2 Reading from I/O port 71
4.4.3 Operations on I/O port 71

CHAPTER 5 CLOCK GENERATORS 72

5.1 Functions of Clock Generators 72
5.1.1 System clock oscillators 72
5.1.2 Clock oscillator for interval time generation 72
5.2 Configuration of Clock Generators 73
5.3 Registers Controlling Clock Generators 76
5.4 System Clock Oscillators 79
5.4.1 High-speed internal oscillator 79
5.4.2 Crystal/ceramic oscillator (μPD78F920x only) 79
5.4.3 External clock input circuit 81
5.4.4 Prescaler 81
5.5 Operation of CPU Clock Generator 82
5.6 Operation of Clock Generator Supplying Clock to Peripheral Hardware 88

CHAPTER 6 16-BIT TIMER/EVENT COUNTER 00 (μPD78F920x ONLY) 90

6.1 Functions of 16-Bit Timer/Event Counter 00 90
6.2 Configuration of 16-Bit Timer/Event Counter 00 91
6.3 Registers to Control 16-Bit Timer/Event Counter 00 95
6.4 Operation of 16-Bit Timer/Event Counter 00 101
6.4.1 Interval timer operation 101
6.4.2 External event counter operation 103
6.4.3 Pulse width measurement operations 106
6.4.4 Square-wave output operation 114

CHAPTER 1 OVERVIEW

1.1 Features

O 78K0S CPU core

O ROM and RAM capacities

Part number \ Item	Program Memory (Flash Memory)	Memory (Internal High-Speed RAM)
<R> μPD78F9200, 78F9500	1 KB	128 bytes
<R> μPD78F9201, 78F9501	2 KB	
<R> μPD78F9202, 78F9502	4 KB	

O Minimum instruction execution time: 0.2 μs (with 10 MHz@4.0 to 5.5 V operation)

O Clock

- High-speed system clock … Selected from the following three sources
  - Ceramic/crystal resonator: 2 to 10 MHz
  - External clock: 2 to 10 MHz
  - High-speed internal oscillator
    - μPD78F920x: 8 MHz ±3% (−10 to +70°C), 8 MHz ±5% (−40 to +85°C)
    - μPD78F950x: 8 MHz ±2% (−10 to +85°C), 8 MHz ±5% (−40 to +85°C)
- Low-speed internal oscillator 240 kHz (TYP.) … Watchdog timer, timer clock in intermittent operation

O I/O ports: 8 (CMOS I/O: 7, CMOS input: 1)

O Timer: 3 channels

- 16-bit timer/event counter[Note]: 1 channel … Timer output × 1, capture input × 2
- 8-bit timer: 1 channel … PWM output × 1
- Watchdog timer: 1 channel … Operable with low-speed internal oscillation clock

O 10-bit resolution A/D converter[Note]: 4 channels

O On-chip power-on-clear (POC) circuit (A reset is automatically generated when the voltage drops to 2.1 V (TYP.) or below)

O On-chip low voltage detector (LVI) circuit (An interrupt/reset (selectable) is generated when the detection voltage is reached)

- Detection voltage: Selectable from ten levels between 2.35 and 4.3 V

O Single-power-supply flash memory

- Flash self programming enabled
- Software protection function: Protected from outside party copying (no flash reading command)
- Time required for writing by dedicated flash memory programmer: Approximately 3 seconds (4 KB)
  - ∗ Flash programming on mass production lines supported

O Safety function

- Watchdog timer operated by clock independent from CPU
  - … A hang-up can be detected even if the system clock stops
- Supply voltage drop detectable by LVI
  - … Appropriate processing can be executed before the supply voltage drops below the operation voltage
- Equipped with option byte function
  - … Important system operation settings set in hardware

Note μPD78F920x only

CHAPTER 2 PIN FUNCTIONS

2.1 Pin Function List

2.1.1 μPD78F920x

(1) Port pins

Pin Name	I/O	Function		After Reset	Alternate-Function Pin
P20	I/O	Port 2. 4-bit I/O port. Can be set to input or output mode in 1-bit units. An on-chip pull-up resistor can be connected by setting software.		Input	ANI0/TI000/TOH1
P21					ANI1/TI010/ TO00/INTP0
P22[Note 1]					X2/ANI2[Note 1]
P23[Note 1]					X1/ANI3[Note 1]
P32	I/O	Port 3	Can be set to input or output mode in 1-bit units. An on-chip pull-up resistor can be connected by setting software.	Input	INTP1
P34[Note 1]	Input		Input only	Input	$\overline{\text{RESET}}$[Note 1]
P40, P43[Note 2]	I/O	Port 4. 2-bit I/O port. Can be set to input or output mode in 1-bit units. An on-chip pull-up resistor can be connected by setting software.		Input	–

Notes 1. For the setting method for pin functions, see **CHAPTER 15 OPTION BYTE**.

2. At program initialization, set PM41, PM42, and PM44 to PM47 to "0".

Caution The P22/X2/ANI2 and P23/X1/ANI3 pins are pulled down during reset.

3.3.2 Immediate addressing

[Function]

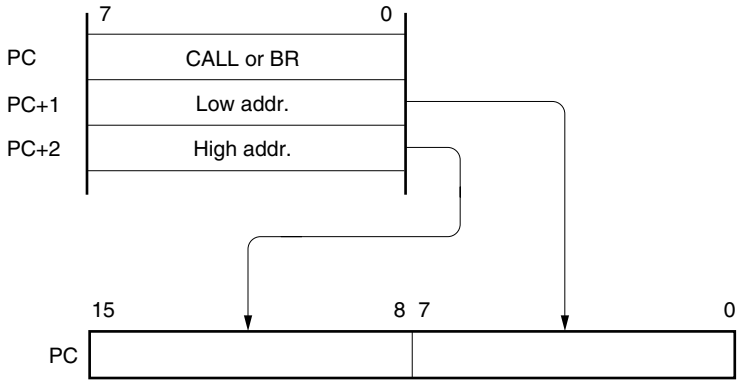
Immediate data in the instruction word is transferred to the program counter (PC) to branch.

This function is carried out when the CALL !addr16 and BR !addr16 instructions are executed.

CALL !addr16 and BR !addr16 instructions can be used to branch to all the memory spaces.

[Illustration]

In case of CALL !addr16 and BR !addr16 instructions



3.3.3 Table indirect addressing

[Function]

The table contents (branch destination address) of the particular location to be addressed by the immediate data of an instruction code from bit 1 to bit 5 are transferred to the program counter (PC) to branch.

Table indirect addressing is carried out when the CALLT [addr5] instruction is executed. This instruction can be used to branch to all the memory spaces according to the address stored in the memory table 40H to 7FH.

[Illustration]

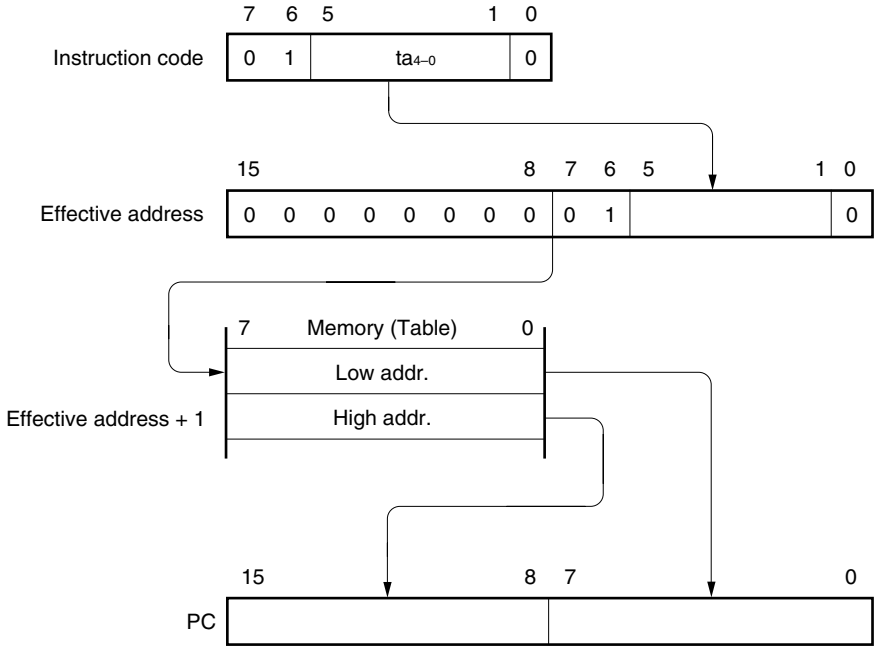
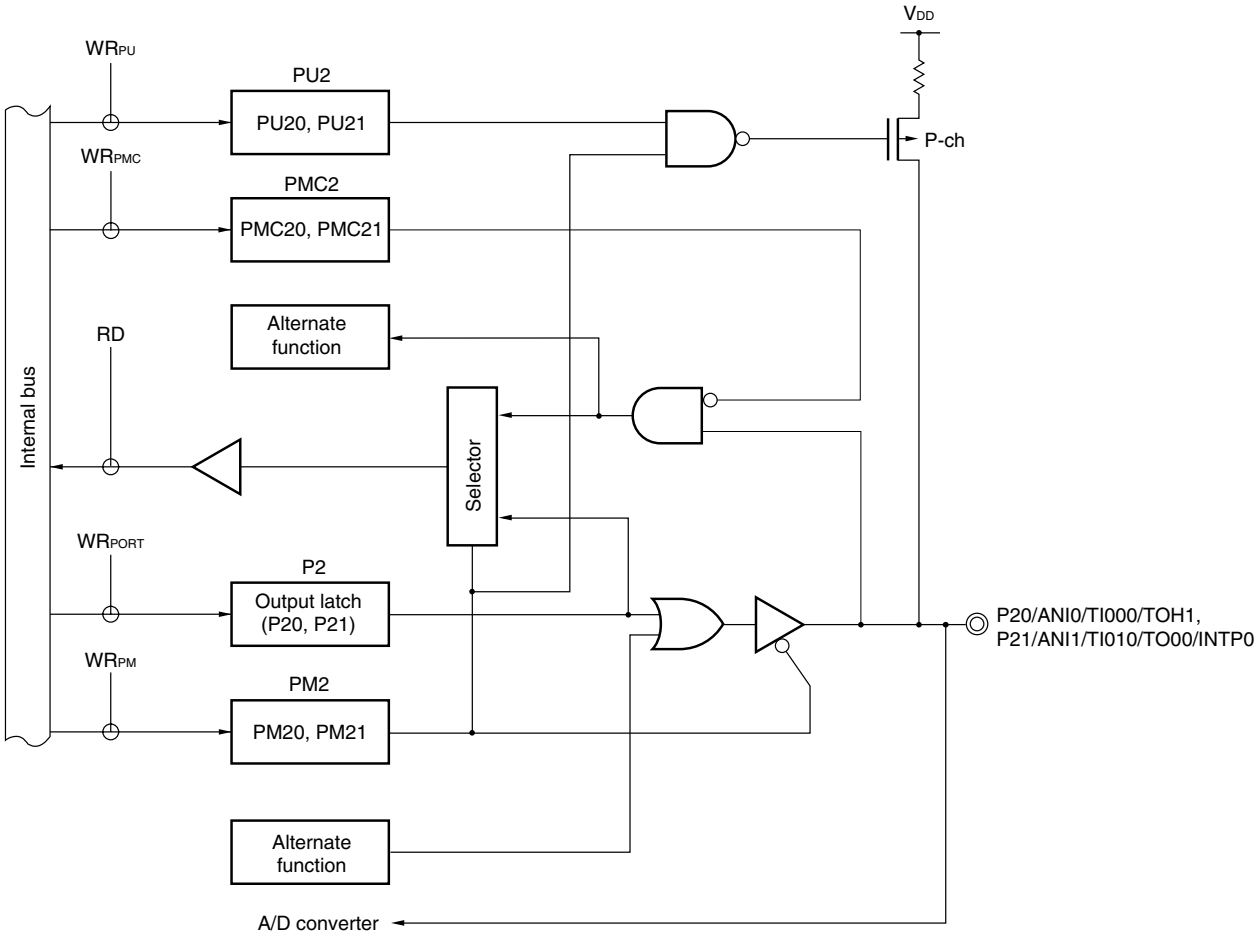


Figure 4-2. Block Diagram of P20 and P21 (μPD78F920x)



P2: Port register 2
PU2: Pull-up resistor option register 2
PM2: Port mode register 2
PMC2: Port mode control register 2
RD: Read signal
WR××: Write signal

Remark TM00: 16-bit timer counter 00
CR000: 16-bit timer capture/compare register 000
CR010: 16-bit timer capture/compare register 010

(2) Capture/compare control register 00 (CRC00)

This register controls the operation of the 16-bit capture/compare registers (CR000, CR010).
CRC00 is set by a 1-bit or 8-bit memory manipulation instruction.
Reset signal generation sets the value of CRC00 to 00H.

Figure 6-6. Format of Capture/Compare Control Register 00 (CRC00)

Address: FF62H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
CRC00	0	0	0	0	0	CRC002	CRC001	CRC000

CRC002	CR010 operating mode selection
0	Operate as compare register
1	Operate as capture register

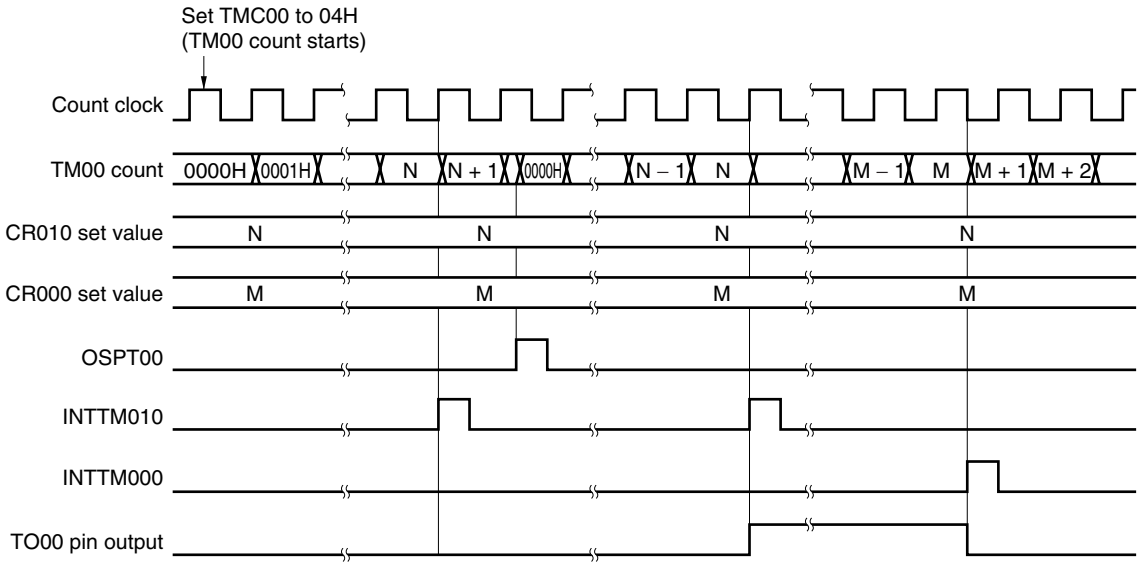
CRC001	CR000 capture trigger selection
0	Capture on valid edge of TI010 pin
1	Capture on valid edge of TI000 pin by reverse phase[Note]

CRC000	CR000 operating mode selection
0	Operate as compare register
1	Operate as capture register

Note When the CRC001 bit value is 1, capture is not performed if both the rising and falling edges have been selected as the valid edges of the TI000 pin.

Cautions 1. The timer operation must be stopped before setting CRC00.
2. When the clear & start mode entered on a match between TM00 and CR000 is selected by 16-bit timer mode control register 00 (TMC00), CR000 should not be specified as a capture register.
3. To ensure the reliability of the capture operation, the capture trigger requires a pulse longer than two cycles of the count clock selected by prescaler mode register 00 (PRM00) (refer to Figure 6-18).

Figure 6-34. Timing of One-Shot Pulse Output Operation with Software Trigger



Caution 16-bit timer counter 00 starts operating as soon as a value other than 00 (operation stop mode) is set to the TMC003 and TMC002 bits.

Remark N < M

(2) One-shot pulse output with external trigger

A one-shot pulse can be output from the TO00 pin by setting 16-bit timer mode control register 00 (TMC00), capture/compare control register 00 (CRC00), and 16-bit timer output control register 00 (TOC00) as shown in Figure 6-35, and by using the valid edge of the TI000 pin as an external trigger.

The valid edge of the TI000 pin is specified by bits 4 and 5 (ES000, ES010) of prescaler mode register 00 (PRM00). The rising, falling, or both the rising and falling edges can be specified.

When the valid edge of the TI000 pin is detected, the 16-bit timer/event counter is cleared and started, and the output becomes active at the count value set in advance to 16-bit timer capture/compare register 010 (CR010). After that, the output becomes inactive at the count value set in advance to 16-bit timer capture/compare register 000 (CR000)[Note].

Note The case where N < M is described here. When N > M, the output becomes active with the CR000 register and inactive with the CR010 register. Do not set N to M.

Caution Do not input the external trigger again while the one-shot pulse is output.
To output the one-shot pulse again, wait until the current one-shot pulse output is completed.

(5) Successive approximation register (SAR)

This register compares the sampled analog voltage and the voltage of the D/A converter, and converts the result, starting from the most significant bit (MSB).

When the voltage value is converted into a digital value down to the least significant bit (LSB) (end of A/D conversion), the contents of the SAR register are transferred to the A/D conversion result register (ADCR).

(6) 10-bit A/D conversion result register (ADCR)

The result of A/D conversion is loaded from the successive approximation register to this register each time A/D conversion is completed, and the ADCR register holds the result of A/D conversion in its lower 10 bits (the higher 6 bits are fixed to 0).

(7) 8-bit A/D conversion result register (ADCRH)

The result of A/D conversion is loaded from the successive approximation register to this register each time A/D conversion is completed, and the ADCRH register holds the result of A/D conversion in its higher 8 bits.

(8) Controller

When A/D conversion has been completed, INTAD is generated.

(9) V_{DD} pin

This is the positive power supply pin.

In the 78K0S/KU1+, V_{DD} functions alternately as the A/D converter reference voltage input. When using the A/D converter, stabilize V_{DD} at the supply voltage used (2.7 to 5.5 V).

(10) V_{SS} pin

This is the ground potential pin.

In the 78K0S/KU1+, V_{SS} functions alternately as the ground potential of the A/D converter. Be sure to connect V_{SS} to a stabilized GND (= 0 V).

(11) A/D converter mode register (ADM)

This register is used to set the conversion time of the analog input signal to be converted, and to start or stop the conversion operation.

(12) Analog input channel specification register (ADS)

This register is used to specify the port that inputs the analog voltage to be converted into a digital signal.

(13) Port mode control register 2 (PMC2)

This register is used when the P20/ANI0/TI000/TOH1, P21/ANI1/TI010/TO00/INTP0, P22/ANI2, and P23/ANI3 pins are used as the analog input pins of the A/D converter.

11.2 Standby Function Operation

11.2.1 HALT mode

(1) HALT mode

The HALT mode is set by executing the HALT instruction.

The operating statuses in the HALT mode are shown below.

Caution Because an interrupt request signal is used to clear the standby mode, if there is an interrupt source with the interrupt request flag set and the interrupt mask flag clear, the standby mode is immediately cleared if set.

Table 11-2. Operating Statuses in HALT Mode

Setting of HALT Mode / Item		Low-Speed Internal Oscillator cannot be stopped[Note 1].	Low-Speed Internal Oscillator can be stopped[Note 1].	
			When Low-Speed Internal Oscillation Continues	When Low-Speed Internal Oscillation Stops
System clock		Clock supply to CPU is stopped.		
CPU		Operation stops.		
Port (latch)		Holds status before HALT mode was set.		
16-bit timer/event counter 00[Note 2]		Operable		
8-bit timer H1	Sets count clock to f_{XP} to $f_{XP}/2^{12}$	Operable		
	Sets count clock to $f_{RL}/2^{7}$	Operable	Operable	Operation stops.
Watchdog timer	“System clock” selected as operating clock	Setting disabled.	Operation stops.	
	“Low-speed internal oscillation clock” selected as operating clock	Operable (Operation continues)	Operation stops.	
A/D converter[Note 2]		Operable		
Power-on-clear circuit		Always operates.		
Low-voltage detector		Operable		
External interrupt		Operable		

Notes 1. “Cannot be stopped” or “Stopped by software” is selected for low-speed internal oscillator by the option byte (for the option byte, see **CHAPTER 15 OPTION BYTE**).

<R> **2.** μPD78F920x only

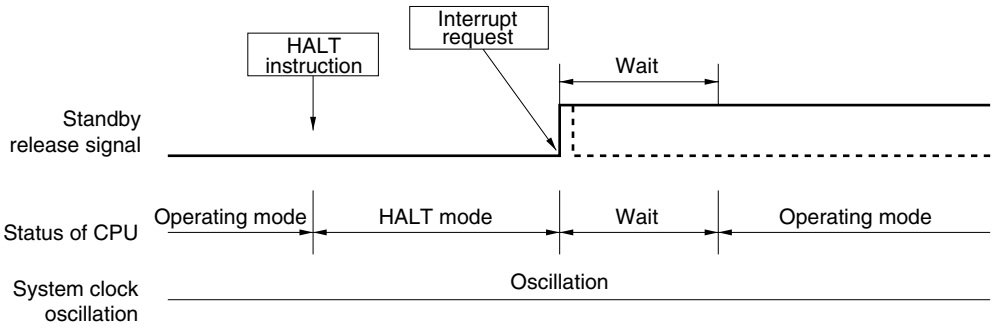
(2) HALT mode release

The HALT mode can be released by the following two sources.

(a) Release by unmasked interrupt request

When an unmasked interrupt request is generated, the HALT mode is released. If interrupt acknowledgement is enabled, vectored interrupt servicing is carried out. If interrupt acknowledgement is disabled, the next address instruction is executed.

Figure 11-2. HALT Mode Release by Interrupt Request Generation



Remarks 1. The broken lines indicate the case when the interrupt request which has released the standby mode is acknowledged.

2. The wait time is as follows:

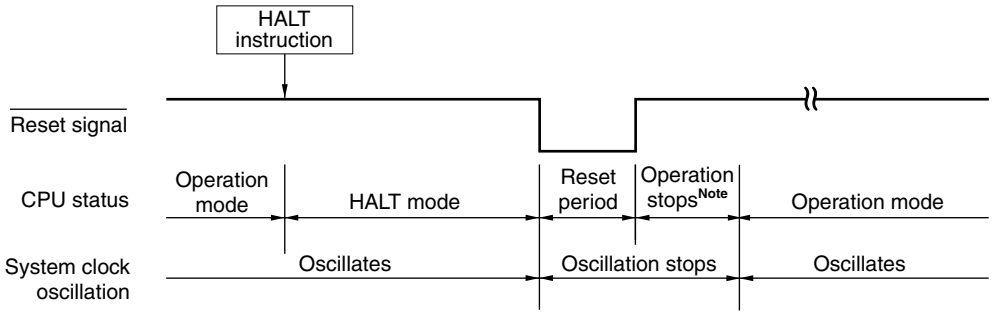
- When vectored interrupt servicing is carried out: 11 to 13 clocks
- When vectored interrupt servicing is not carried out: 3 to 5 clocks

(b) Release by reset signal generation

When the reset signal is input, HALT mode is released, and then, as in the case with a normal reset operation, the program is executed after branching to the reset vector address.

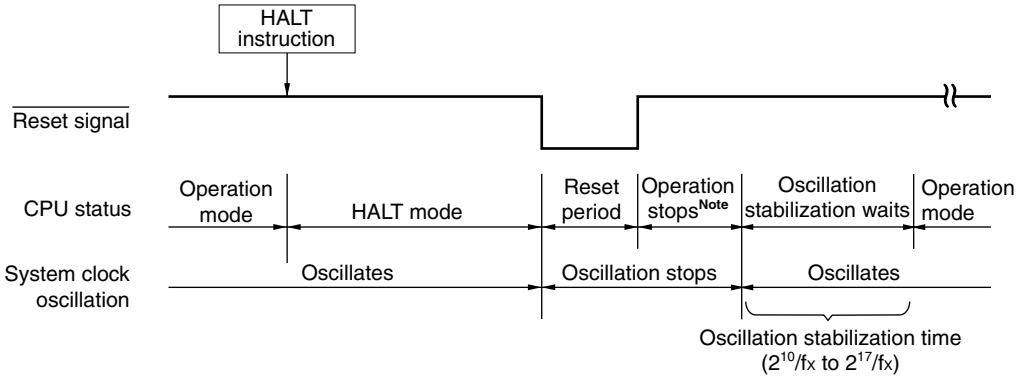
Figure 11-3. HALT Mode Release by Reset Signal Generation

(1) When CPU clock is high-speed internal oscillation clock or external input clock



Note Operation is stopped (277 μs (MIN.), 544 μs (TYP.), 1.075 ms (MAX.)) because the option byte is referenced.

<R> **(2) When CPU clock is crystal/ceramic oscillation clock (μPD78F920x only)**



Note Operation is stopped (276 μs (MIN.), 544 μs (TYP.), 1.074 ms (MAX.)) because the option byte is referenced.

Remark fx: System clock oscillation frequency

Table 11-3. Operation in Response to Interrupt Request in HALT Mode

Release Source	MK××	IE	Operation
Maskable interrupt request	0	0	Next address instruction execution
	0	1	Interrupt servicing execution
	1	×	HALT mode held
Reset signal generation	–	×	Reset processing

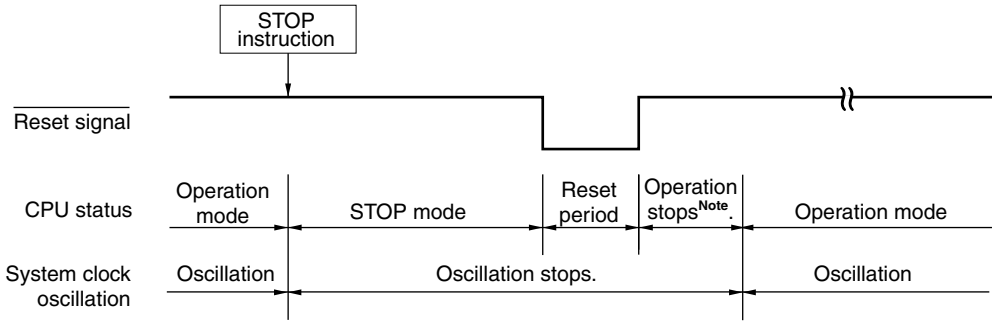
×: don't care

(b) Release by reset signal generation

When the reset signal is input, STOP mode is released and a reset operation is performed after the oscillation stabilization time has elapsed.

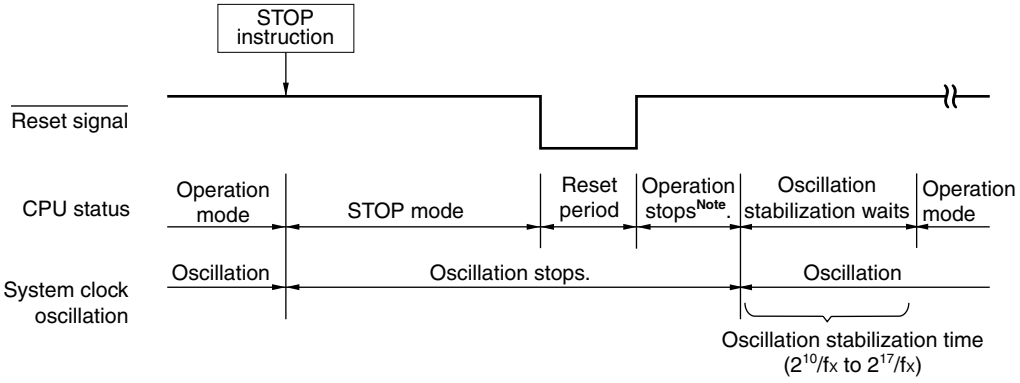
Figure 11-6. STOP Mode Release by Reset signal generation

(1) If CPU clock is high-speed internal oscillation clock or external input clock



Note Operation is stopped (277 μs (MIN.), 544 μs (TYP.), 1.075 ms (MAX.)) because the option byte is referenced.

<R> **(2) If CPU clock is crystal/ceramic oscillation clock (μPD78F920x only)**



Note Operation is stopped (276 μs (MIN.), 544 μs (TYP.), 1.074 ms (MAX.)) because the option byte is referenced.

Remark fx: System clock oscillation frequency

Table 11-5. Operation in Response to Interrupt Request in STOP Mode

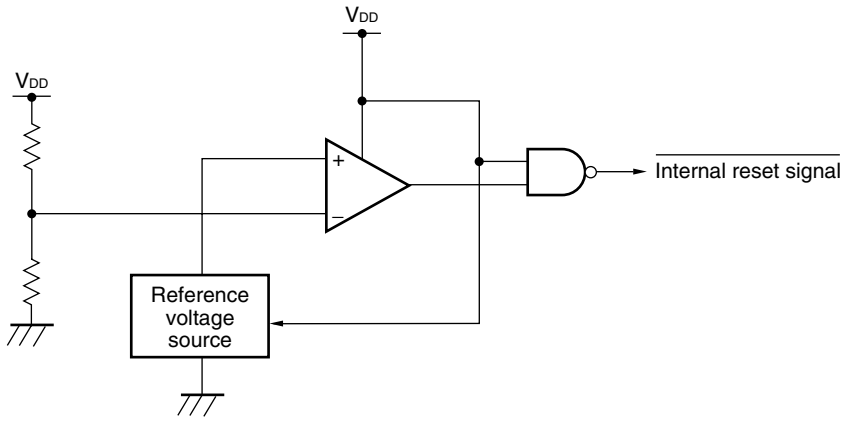
Release Source	MK××	IE	Operation
Maskable interrupt request	0	0	Next address instruction execution
	0	1	Interrupt servicing execution
	1	×	STOP mode held
Reset signal generation	–	×	Reset processing

×: don't care

13.2 Configuration of Power-on-Clear Circuit

The block diagram of the power-on-clear circuit is shown in Figure 13-1.

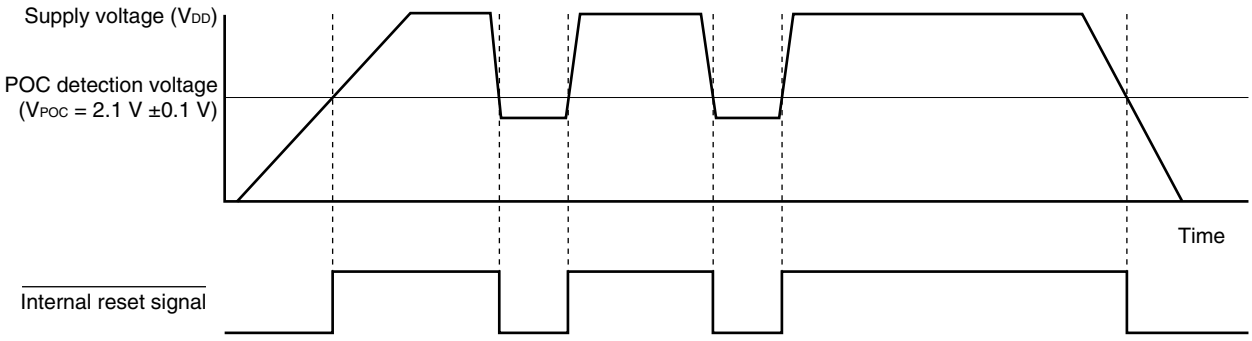
Figure 13-1. Block Diagram of Power-on-Clear Circuit



13.3 Operation of Power-on-Clear Circuit

In the power-on-clear circuit, the supply voltage (V_{DD}) and detection voltage (V_{POC} = 2.1 V ±0.1 V) are compared, and an internal reset signal is generated when $V_{DD} < V_{POC}$, and an internal reset is released when $V_{DD} \geq V_{POC}$.

Figure 13-2. Timing of Internal Reset Signal Generation in Power-on-Clear Circuit



15.2 Format of Option Byte

Format of option bytes is shown below.

15.2.1 μPD78F920x

Figure 15-3. Format of Option Byte (μPD78F920x) (1/2)

Address: 0080H

7	6	5	4	3	2	1	0
1	DEFOSTS1	DEFOSTS0	1	RMCE	OSCSEL1	OSCSEL0	LIOCP

DEFOSTS1	DEFOSTS0	Oscillation stabilization time on power application or after reset release
0	0	2^{10}/fx (102.4 μs)
0	1	2^{12}/fx (409.6 μs)
1	0	2^{15}/fx (3.27 ms)
1	1	2^{17}/fx (13.1 ms)

Caution The setting of this option is valid only when the crystal/ceramic oscillation clock is selected as the system clock source. No wait time elapses if the high-speed internal oscillation clock or external clock input is selected as the system clock source.

RMCE	Control of $\overline{\text{RESET}}$ pin
1	$\overline{\text{RESET}}$ pin is used as is.
0	$\overline{\text{RESET}}$ pin is used as input port pin (P34).

Caution Because the option byte is referenced after reset release, if a low level is input to the $\overline{\text{RESET}}$ pin before the option byte is referenced, then the reset state is not released.
Also, when setting 0 to RMCE, connect the pull-up resistor.

OSCSEL1	OSCSEL0	Selection of system clock source
0	0	Crystal/ceramic oscillation clock
0	1	External clock input
1	×	High-speed internal oscillation clock

Caution Because the X1 and X2 pins are also used as the P23/ANI3 and P22/ANI2 pins, the conditions under which the X1 and X2 pins can be used differ depending on the selected system clock source.

(1) Crystal/ceramic oscillation clock is selected
The X1 and X2 pins cannot be used as I/O port pins or analog input pins of A/D converter because they are used as clock input pins.

(2) External clock input is selected
Because the X1 pin is used as an external clock input pin, P23/ANI3 cannot be used as an I/O port pin or an analog input pin of A/D converter.

(3) High-speed internal oscillation clock is selected
P23/ANI3 and P22/ANI2 pins can be used as I/O port pins or analog input pins of A/D converter.

Remark × : don't care

Figure 16-8. Block Diagram of Self Programming

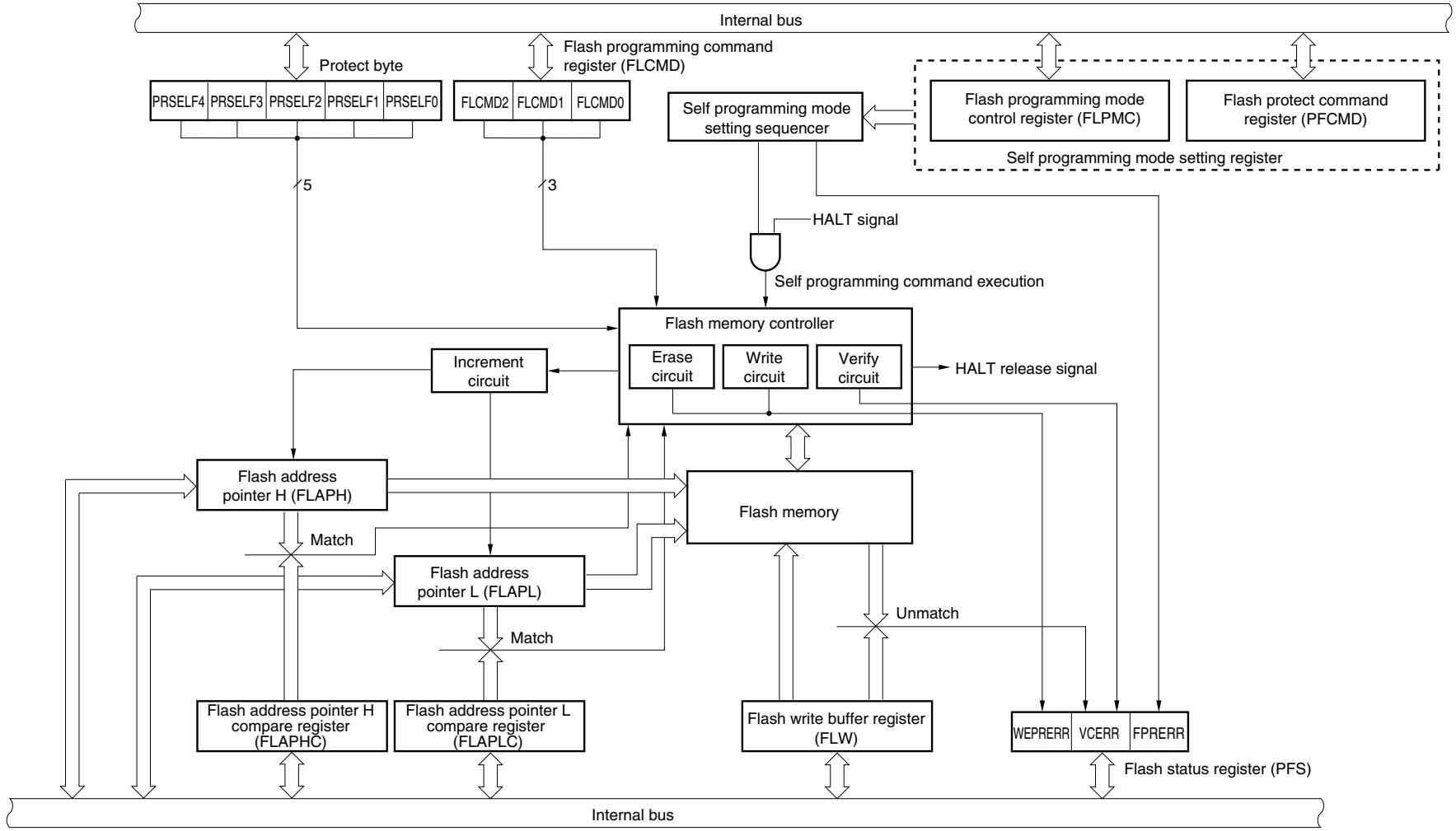
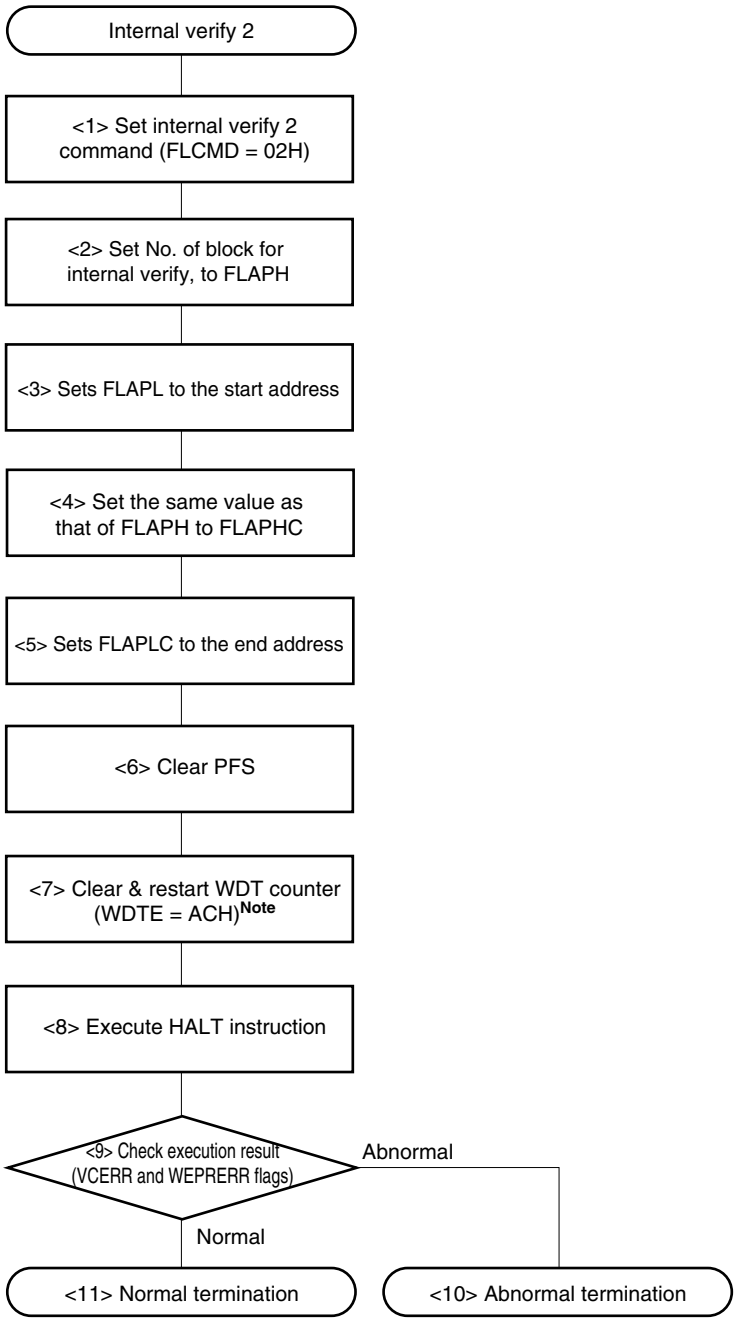


Figure 16-24. Example of Internal Verify 2 Operation in Self Programming Mode



Note This setting is not required when the watchdog timer is not used.

Remark <1> to <11> in Figure 16-24 correspond to Internal verify 2 <1> to <11> in **16.8.9** (the page before last).

```
        INCW    DE              ; Address at which data is to be written + 1
        BR      FlashWriteLoop

FlashVerify:
        MOVW    HL,#WriteAdr    ; Sets verify address

        MOV     FLCMD,#02H      ; Sets flash control command (internal verify 2)
        MOV     A,H
        MOV     FLAPH,A         ; Sets verify start address
        MOV     A,L
        MOV     FLAPL,A         ; Sets verify start address
        MOV     A,D
        MOV     FLAPHC,A        ; Sets verify end address
        MOV     A,E
        MOV     FLAPLC,A        ; Sets verify end address

        MOV     WDTE,#0ACH      ; Clears & restarts WDT
        HALT                    ; Self programming is started
        MOV     A,PFS
        CMP     A,#00H
        BNZ     $StatusError    ; Checks internal verify error
                                ; Performs abnormal termination processing when an error
                                ; occurs.

        MOV     FLCMD,#00H      ; Clears FLCMD register
ModeOffLoop:
        MOV     PFS,#00H        ; Clears flash status register
        MOV     PFCMD,#0A5H     ; PFCMD register control
        MOV     FLPMC,#00H      ; FLPMC register control (sets value)
        MOV     FLPMC,#0FFH     ; FLPMC register control (inverts set value)
        MOV     FLPMC,#00H      ; Sets normal mode via FLPMC register control (sets value)

        BT PFS.0,$ModeOffLoop   ; Checks completion of write to specific registers
                                ; Repeats the same processing when an error occurs.
                                ; After the specific sequence is correctly executed, restore
                                ; the CPU clock to its setting before the self programming
        MOV     MK0,#INT_MK0    ; Restores interrupt mask flag

        EI

        BR      StatusNormal

;---------------------------------------------------------------------
;END (abnormal termination processing); Perform processing to shift to
      normal mode in order to return to normal processing
;---------------------------------------------------------------------
StatusError:
```

Notes 2. This is the pin connection when the X1 and X2 pins are not used in the target system. When using the X1 and X2 pins, refer to **17.1.2 Connection of X1 and X2 pins**.

3. No problem will occur if the dashed line portions are connected.

4. This pin is connected to enhance the accuracy of time measurement between run and break during debugging. Debugging is possible even if this pin is left open, but measurement error occurs in several ms units.

5. The INTP1 pin is used for communication between QB-MINI2 and the target device during debugging. When debugging is performed with QB-MINI2, therefore, the INTP1 pin and its alternate-function pin cannot be used. For INTP1 pin connection, refer to **17.1.1 Connection of INTP1 pin**.

Pins for communication depend on whether the monitor program has been written or not. (refer to **Table 17-1**) X1 and X2 pins can be used as I/O port pins or the pins for oscillation, after the monitor program has been written.

Table 17-1. Pins for communication with QB-MINI2

Before writing the monitor program	After writing the monitor program
X1[Note 1], X2[Note 2], $\overline{\text{RESET}}$, INTP1, V_{DD}, V_{SS}	$\overline{\text{RESET}}$, INTP1, V_{DD}, V_{SS}

<R> **Notes 1. μPD78F920x: X1/P23/ANI3, μPD78F950x: EXCLK/P23**

<R> **2. μPD78F920x: X2/P22/ANI2, μPD78F950x: P22**

17.1.1 Connection of INTP1 pin

The INTP1 pin is used only for communication between QB-MINI2 and the target device during debugging. Design circuits appropriately according to the relevant case among the cases shown below.

(1) INTP1 pin is not used in target system (as is illustrated in **Figure 17-1. Recommended Circuit Connection**)
→ See **Figure 17-2**.

(2) QB-MINI2 is used only for programming, not for debugging
→ See **Figure 17-3**.

(3) QB-MINI2 is used for debugging and debugging of the INTP1 pin is performed only with a real machine
→ See **Figure 17-4**.

Figure 17-2. Circuit Connection for the Case Where INTP1 Pin Is Not Used in Target System

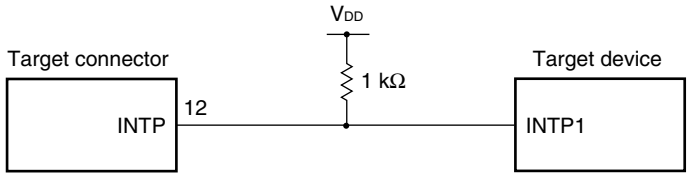


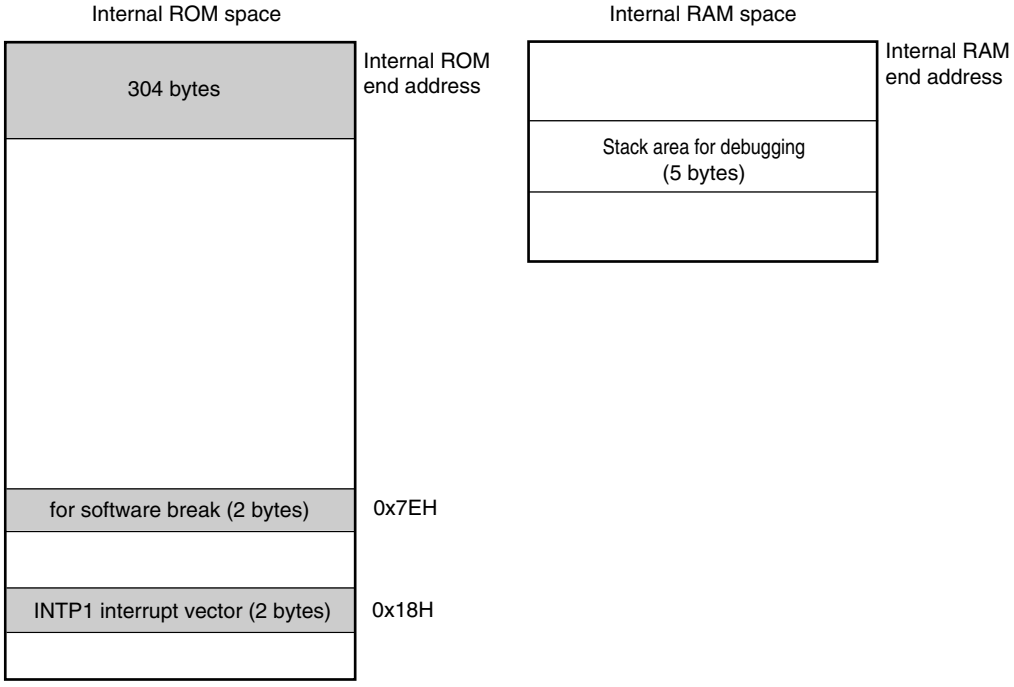
Figure 17-3. Circuit Connection for the Case Where QB-MINI2 Is Used Only for Programming

17.2 Securing of user resources

The user must prepare the following to perform communication between QB-MINI2 and the target device and implement each debug function. For details of the setting, refer to QB-MINI2 User's Manual (U18371E).

- Securement of memory space
  The shaded portions in Figure 17-6 are the areas reserved for placing the debug monitor program, so user programs cannot be allocated in these spaces.

Figure 17-6. Memory Spaces Where Debug Monitor Programs Are Allocated



- Securement of serial interface for communication
  The register settings, concerning the INTP1 pin used for communication between QB-MINI2 and the target device, performed by the debug monitor program must not be changed.

(8/15)

Chapter	Classification	Function	Details of Function	Cautions	Page
Chapter 9	Soft	A/D converter (μPD78F920x only)	ADM: A/D converter mode register	If a bit other than ADCS of ADM is manipulated while A/D conversion is stopped (ADCS = 0) and then A/D conversion is started, execute two NOP instructions or an instruction equivalent to two machine cycles, and set ADCS to 1.	p. 163 ☐
				A/D conversion must be stopped (ADCS = 0) before rewriting bits FR0 to FR2.	p. 163 ☐
				Be sure to clear bits 6, 2, and 1 to 0.	p. 163 ☐
			ADS: Analog input channel specification register	Be sure to clear bits 2 to 7 of ADS to 0.	p. 164 ☐
			ADCR: 10-bit A/D conversion result register	When writing to the A/D converter mode register (ADM) and analog input channel specification register (ADS), the contents of ADCR may become undefined. Read the conversion result following conversion completion before writing to ADM and ADS. Using timing other than the above may cause an incorrect conversion result to be read.	p. 164 ☐
			PMC2: Port mode control register 2	If PMC20 to PMC23 are set to 1, the P20/ANI0/TI000/TOH1, P21/ANI1/TIO10/TO00/INTP0, P22/ANI2, and P23/ANI3 pins cannot be used for any purpose other than the A/D converter function. Be sure to set 0 to the Pull-up resistor option register of the pin set in A/D converter mode.	p. 165 ☐
			A/D converter operations	Make sure the period of <1> to <4> is 1 μs or more.	pp. 166, 170 ☐
				It is no problem if the order of <1> and <2> is reversed.	pp. 166, 170 ☐
				<1> can be omitted. However, ignore the data resulting from the first conversion after <4> in this case.	p. 170 ☐
				The period from <5> to <8> differs from the conversion time set using bits 5 to 3 (FR2 to FR0) of ADM. The period from <7> to <8> is the conversion time set using FR2 to FR0.	p. 170 ☐
	Hard		Operating current in STOP mode	To satisfy the DC characteristics of supply current in STOP mode, clear bit 7 (ADCS) and bit 0 (ADCE) of the A/D converter mode register (ADM) to 0 before executing the STOP instruction.	p. 173 ☐
			Input range of ANI0 to ANI3	Observe the rated range of the ANI0 to ANI3 input voltage. If a voltage of V_{DD} or higher and V_{SS} or lower (even in the range of absolute maximum ratings) is input to an analog input channel, the converted value of that channel becomes undefined. In addition, the converted values of the other channels may also be affected.	p. 173 ☐
	Soft		Conflicting operations	Conflict between A/D conversion result register (ADCR, ADCRH) write and ADCR, ADCRH read by instruction upon the end of conversion ADCR, ADCRH read has priority. After the read operation, the new conversion result is written to ADCR, ADCRH.	p. 173 ☐
				Conflict between ADCR, ADCRH write and A/D converter mode register (ADM) write or analog input channel specification register (ADS) write upon the end of conversion ADM or ADS write has priority. ADCR, ADCRH write is not performed, nor is the conversion end interrupt signal (INTAD) generated.	p. 173 ☐