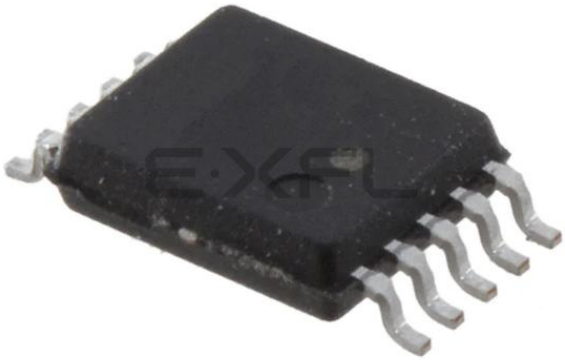

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	78K0S
Core Size	8-Bit
Speed	10MHz
Connectivity	-
Peripherals	LVD, POR, PWM, WDT
Number of I/O	7
Program Memory Size	2KB (2K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	10-LSSOP (0.225", 5.72mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd78f9501ma-cac-a

2.3 Pin I/O Circuits and Connection of Unused Pins

Tables 2-1 and 2-2 show I/O circuit type of each pin and the connections of unused pins.
For the configuration of the I/O circuit of each type, refer to **Figure 2-1**.

Table 2-1. Types of Pin I/O Circuits and Connection of Unused Pins (μPD78F920x)

Pin Name	I/O Circuit Type	I/O	Recommended Connection of Unused Pin
P20/ANI0/TI000/TOH1	11	I/O	Input: Individually connect to V_{DD} or V_{SS} via resistor. Output: Leave open.
P21/ANI1/TI010/TO00/INTP0			
P22/ANI2/X2	36		Input: Individually connect to V_{SS} via resistor. Output: Leave open.
P23/ANI3/X1			
P32/INTP1	8-A		Input: Individually connect to V_{DD} or V_{SS} via resistor. Output: Leave open.
P34/$\overline{\text{RESET}}$	2	Input	Connect to V_{DD} via resistor.
P40 and P43	8-A	I/O	Input: Individually connect to V_{DD} or V_{SS} via resistor. Output: Leave open.

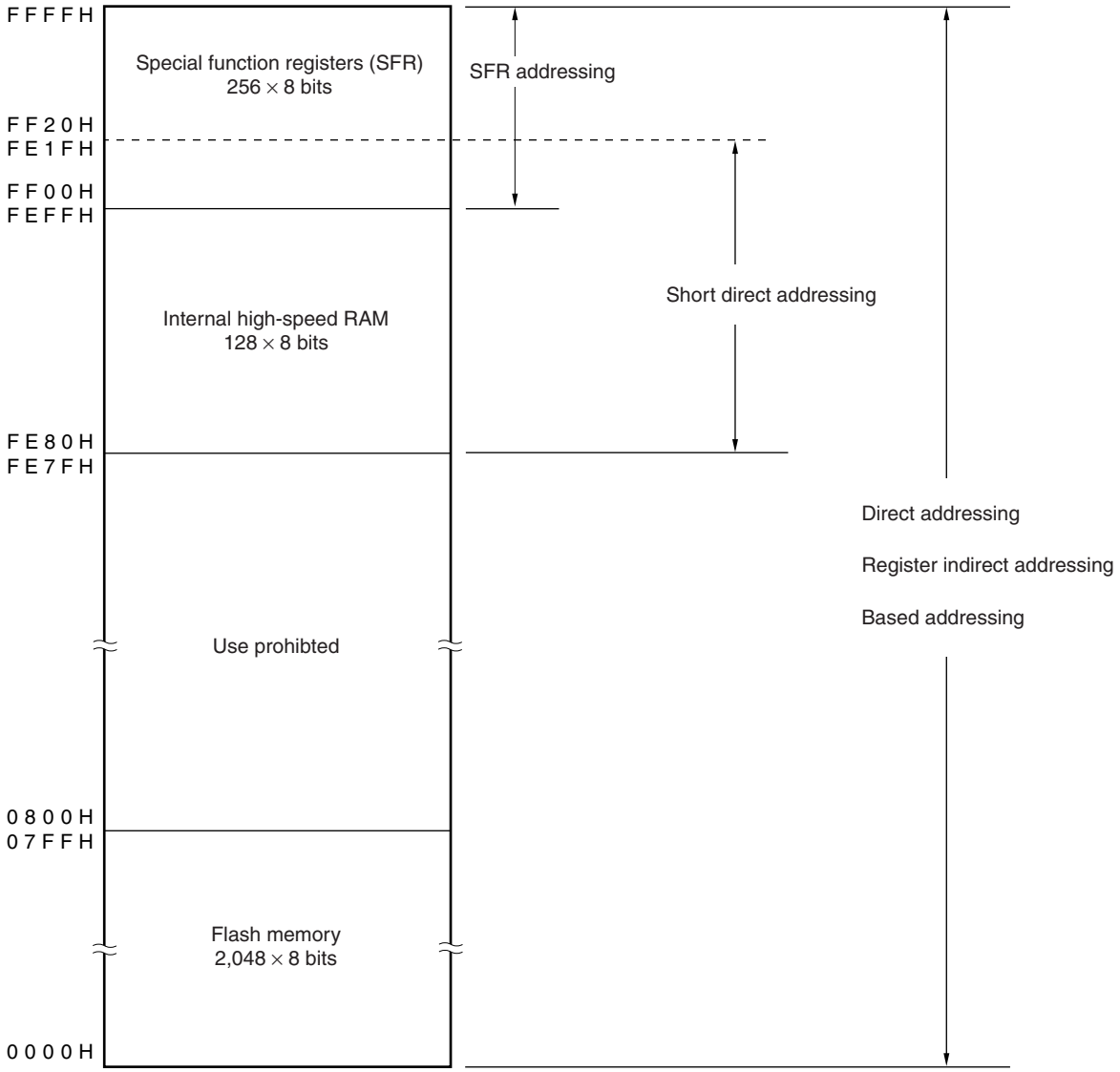
<R>

Table 2-2. Types of Pin I/O Circuits and Connection of Unused Pins (μPD78F950x)

Pin Name	I/O Circuit Type	I/O	Recommended Connection of Unused Pin
P20/TOH1	8-A	I/O	Input: Individually connect to V_{DD} or V_{SS} via resistor. Output: Leave open.
P21/INTP0			
P22			
P23/EXCLK			
P32/INTP1			
P34/$\overline{\text{RESET}}$	2-A	Input	Set ENPU34 to “1” on the option byte, and leave the pin open.
P40 and P43	8-A	I/O	Input: Individually connect to V_{DD} or V_{SS} via resistor. Output: Leave open.

<R>

Figure 3-5. Data Memory Addressing (μPD78F9201, 78F9501)



3.2.3 Special function registers (SFRs)

Unlike the general-purpose registers, each special function register has a special function.

The special function registers are allocated to the 256-byte area FF00H to FFFFH.

The special function registers can be manipulated, like the general-purpose registers, with operation, transfer, and bit manipulation instructions. Manipulatable bit units (1, 8, and 16) differ depending on the special function register type.

Each manipulation bit unit can be specified as follows.

- 1-bit manipulation
  Describes a symbol reserved by the assembler for the 1-bit manipulation instruction operand (sfr.bit). This manipulation can also be specified with an address and bit.

- 8-bit manipulation
  Describes a symbol reserved by the assembler for the 8-bit manipulation instruction operand (sfr). This manipulation can also be specified with an address.

- 16-bit manipulation
  Describes a symbol reserved by the assembler for the 16-bit manipulation instruction operand. When specifying an address, describe an even address.

Table 3-3 lists the special function registers. The meanings of the symbols in this table are as follows:

- Symbol
  Indicates the addresses of the implemented special function registers. It is defined as a reserved word in the RA78K0S, and is defined as an sfr variable using the #pragma sfr directive in the CC78K0S. Therefore, these symbols can be used as instruction operands if an assembler or integrated debugger is used.

- R/W
  Indicates whether the special function register can be read or written.
  R/W: Read/write
  R: Read only
  W: Write only

- Number of bits manipulated simultaneously
  Indicates the bit units (1, 8, and 16) in which the special function register can be manipulated.

- After reset
  Indicates the status of the special function register when a reset is input.

3.4.3 Special function register (SFR) addressing

[Function]

A memory-mapped special function register (SFR) is addressed with the 8-bit immediate data in an instruction word.

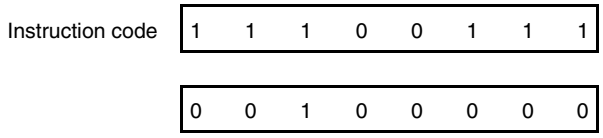
This addressing is applied to the 256-byte space FF00H to FFFFH. However, SFRs mapped at FF00H to FF1FH are accessed with short direct addressing.

[Operand format]

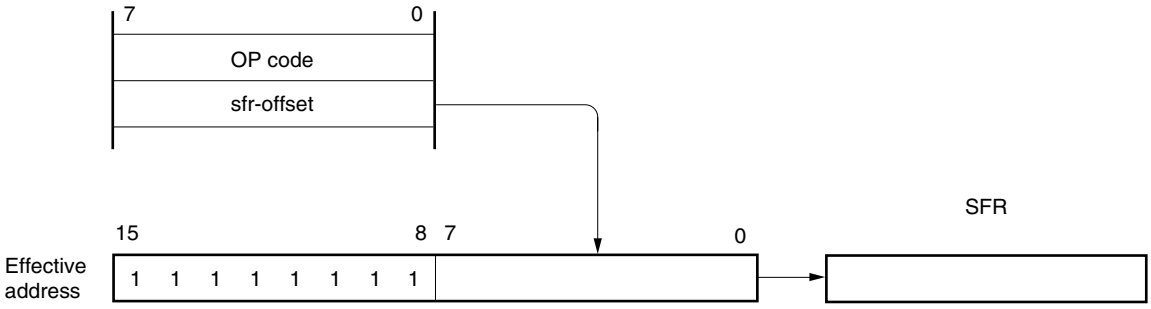
Identifier	Description
sfr	Special function register name

[Description example]

MOV PM0, A; When selecting PM0 for sfr



[Illustration]



CHAPTER 4 PORT FUNCTIONS

4.1 Functions of Ports

The 78K0S/KU1+ has the ports shown in Figure 4-1, which can be used for various control operations. Table 4-1 shows the functions of each port.

In addition to digital I/O port functions, each of these ports has an alternate function. For details, refer to **CHAPTER 2 PIN FUNCTIONS**.

Figure 4-1. Port Functions

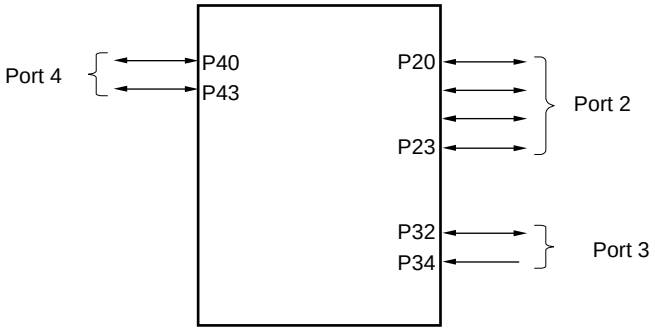


Table 4-1. Port Functions (μPD78F920x)

Pin Name	I/O	Function		After Reset	Alternate-Function Pin
P20	I/O	Port 2. 4-bit I/O port. Can be set to input or output mode in 1-bit units. On-chip pull-up resistor can be connected by setting software.		Input	ANI0/TI000/TOH1
P21					ANI1/TI010/TO00/INTP0
P22[Note 1]					X2/ANI2[Note 1]
P23[Note 1]					X1/ANI3[Note 1]
P32	I/O	Port 3	Can be set to input or output mode in 1-bit units. On-chip pull-up resistor can be connected by setting software.	Input	INTP1
P34[Note 1]	Input		Input only	Input	$\overline{\text{RESET}}$[Note 1]
P40 and P43[Note 2]	I/O	Port 4. 2-bit I/O port. Can be set to input or output mode in 1-bit units. On-chip pull-up resistor can be connected setting software.		Input	–

Notes 1. For the setting method for pin functions, see **CHAPTER 15 OPTION BYTE**.

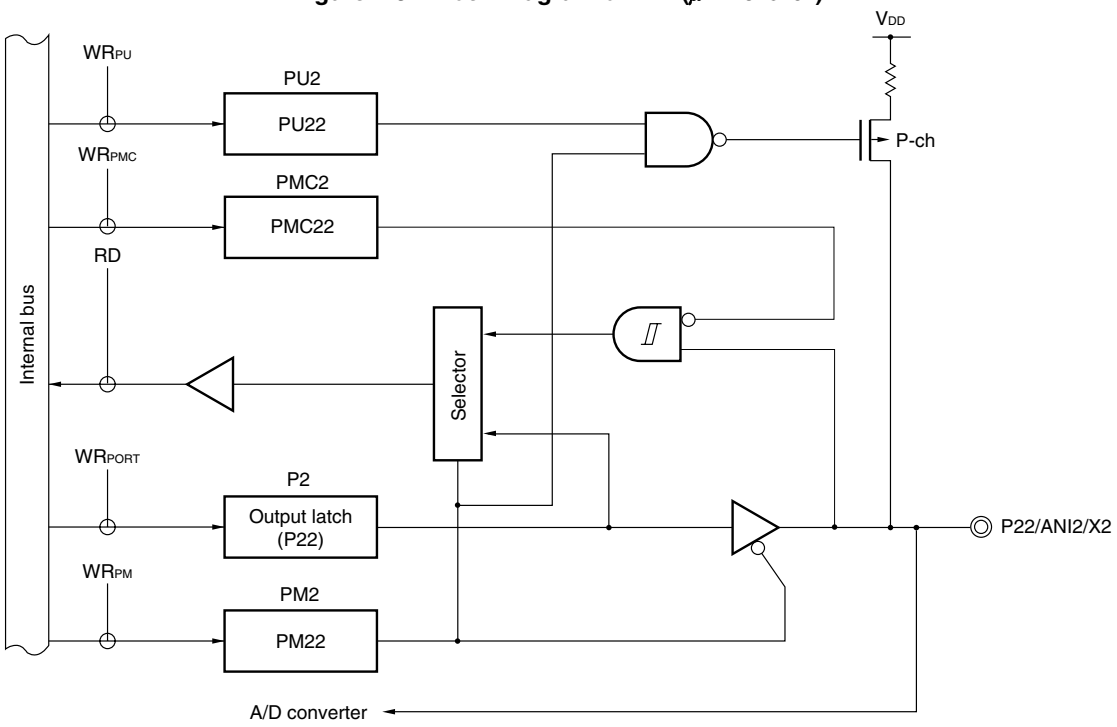
2. At program initialization, set PM41, PM42, and PM44 to PM47 to "0".

Caution The P22/X2/ANI2 and P23/X1/ANI3 pins are pulled down during reset.

Remarks 1. P22 and P23 can be allocated when the high-speed internal oscillation is selected as the system clock.

2. P22 can be allocated when an external clock input is selected as the system clock.

Figure 4-3. Block Diagram of P22 (μPD78F920x)



P2: Port register 2
PU2: Pull-up resistor option register 2
PM2: Port mode register 2
PMC2: Port mode control register 2
RD: Read signal
WR××: Write signal

CHAPTER 5 CLOCK GENERATORS

5.1 Functions of Clock Generators

The clock generators include a circuit that generates a clock (system clock) to be supplied to the CPU and peripheral hardware, and a circuit that generates a clock (interval time generation clock) to be supplied to the watchdog timer and 8-bit timer H1 (TMH1).

5.1.1 System clock oscillators

The following three types of system clock oscillators are used.

- High-speed internal oscillator
  This circuit internally oscillates a clock of 8 MHz (TYP.). Its oscillation can be stopped by execution of the STOP instruction.
<R> If the High-speed internal oscillator is selected to supply the system clock, the X1 and X2 pins in μPD78F920x, and the EXCLK pin in μPD78F950x can be used as I/O port pins.

- Crystal/ceramic oscillator[Note 1]
  This circuit oscillates a clock with a crystal/ceramic oscillator connected across the X1 and X2 pins. It can oscillate a clock of 2 MHz to 10 MHz. Oscillation of this circuit can be stopped by execution of the STOP instruction.

- External clock input circuit
  This circuit supplies a clock from an external IC to the X1 pin[Note 2]. A clock of 2 MHz to 10 MHz can be supplied. Internal clock supply can be stopped by execution of the STOP instruction.
  If the external clock input is selected as the system clock, the X2 pin can be used as an I/O port pin.[Note 1]

The system clock source is selected by using the option byte. For details, refer to **CHAPTER 15 OPTION BYTE**.

<R> When using the X1 and X2 pins in μPD78F920x, and the EXCLK pin in μPD78F950x as I/O port pins, refer to **CHAPTER 4 PORT FUNCTIONS** for details.

<R> **Notes 1.** μPD78F920x only

<R> **2.** μPD78F920x: X1 pin, μPD78F950x: EXCLK pin

5.1.2 Clock oscillator for interval time generation

The following circuit is used as a clock oscillator for interval time generation.

- Low-speed internal oscillator
  This circuit oscillates a clock of 240 kHz (TYP.). Its oscillation can be stopped by using the low-speed internal oscillation mode register (LSRCM) when it is specified by the option byte that its oscillation can be stopped by software.

(3) 16-bit timer output control register 00 (TOC00)

This register controls the operation of the 16-bit timer/event counter output controller. It sets timer output F/F set/reset, output inversion enable/disable, 16-bit timer/event counter 00 timer output enable/disable, one-shot pulse output operation enable/disable, and output trigger of one-shot pulse by software.

TOC00 is set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets the value of TOC00 to 00H.

Figure 6-7. Format of 16-Bit Timer Output Control Register 00 (TOC00)

Address: FF63H After reset: 00H R/W

Symbol	7	<6>	<5>	4	<3>	<2>	1	<0>
TOC00	0	OSPT00	OSPE00	TOC004	LVS00	LVR00	TOC001	TOE00

OSPT00	One-shot pulse output trigger control via software
0	No one-shot pulse output trigger
1	One-shot pulse output trigger

OSPE00	One-shot pulse output operation control
0	Successive pulse output mode
1	One-shot pulse output mode[Note]

TOC004	Timer output F/F control using match of CR010 and TM00
0	Disables inversion operation
1	Enables inversion operation

LVS00	LVR00	Timer output F/F status setting
0	0	No change
0	1	Timer output F/F reset (0)
1	0	Timer output F/F set (1)
1	1	Setting prohibited

TOC001	Timer output F/F control using match of CR000 and TM00
0	Disables inversion operation
1	Enables inversion operation

TOE00	Timer output control
0	Disables output (output fixed to level 0)
1	Enables output

Note The one-shot pulse output mode operates correctly only in the free-running mode and the mode in which clear & start occurs at the TI000 pin valid edge. In the mode in which clear & start occurs on a match between TM00 and CR000, one-shot pulse output is not possible because an overflow does not occur.

Cautions 1. Timer operation must be stopped before setting other than OSPT00.

2. If LVS00 and LVR00 are read, 0 is read.

3. OSPT00 is automatically cleared after data is set, so 0 is read.

4. Do not set OSPT00 to 1 other than in one-shot pulse output mode.

5. A write interval of two cycles or more of the count clock selected by prescaler mode register 00 (PRM00) is required, when OSPT00 is set to 1 successively.

Caution 6. When the TOE00 is 0, set the TOE00, LVS00, and LVR00 at the same time with the 8-bit memory manipulation instruction. When the TOE00 is 1, the LVS00 and LVR00 can be set with the 1-bit memory manipulation instruction.

(4) Prescaler mode register 00 (PRM00)

This register is used to set the 16-bit timer counter 00 (TM00) count clock and the TI000, TI010 pin input valid edges.

PRM00 is set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets the value of PRM00 to 00H.

Figure 6-8. Format of Prescaler Mode Register 00 (PRM00)

Address: FF61H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
PRM00	ES110	ES100	ES010	ES000	0	0	PRM001	PRM000

ES110	ES100	TI010 pin valid edge selection
0	0	Falling edge
0	1	Rising edge
1	0	Setting prohibited
1	1	Both falling and rising edges

ES010	ES000	TI000 pin valid edge selection
0	0	Falling edge
0	1	Rising edge
1	0	Setting prohibited
1	1	Both falling and rising edges

PRM001	PRM000	Count clock (f_{sam}) selection
0	0	f_{XP} (10 MHz)
0	1	$f_{XP}/2^2$ (2.5 MHz)
1	0	$f_{XP}/2^8$ (39.06 kHz)
1	1	TI000 pin valid edge[Note]

Remarks 1. f_{XP}: Oscillation frequency of clock supplied to peripheral hardware

2. ( ): f_{XP} = 10 MHz

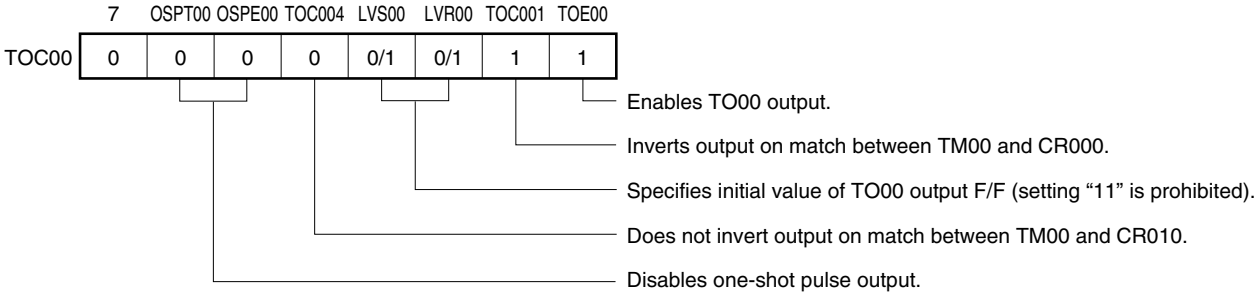
Note The external clock requires a pulse longer than two cycles of the internal count clock (f_{XP}).

Cautions 1. Always set data to PRM00 after stopping the timer operation.

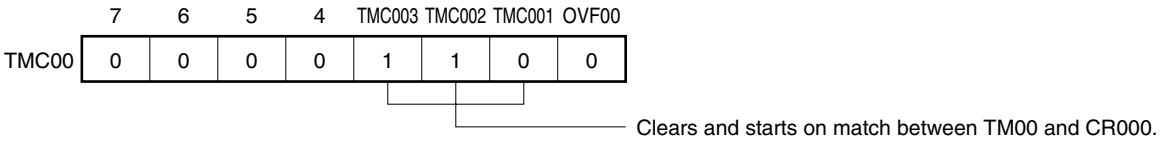
2. If the valid edge of the TI000 pin is to be set as the count clock, do not set the clear/start mode and the capture trigger at the valid edge of the TI000 pin.

Figure 6-28. Control Register Settings in Square-Wave Output Mode (2/2)

(c) 16-bit timer output control register 00 (TOC00)



(d) 16-bit timer mode control register 00 (TMC00)



Remark 0/1: Setting 0 or 1 allows another function to be used simultaneously with square-wave output. See the description of the respective control registers for details.

Figure 6-29. Square-Wave Output Operation Timing

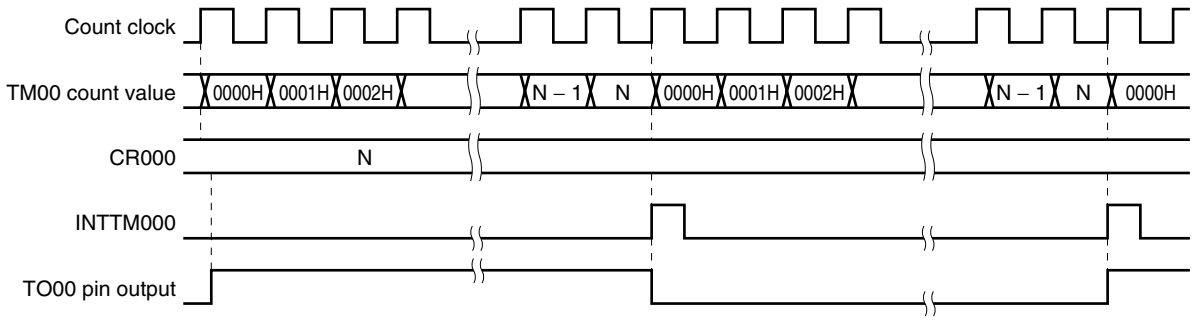
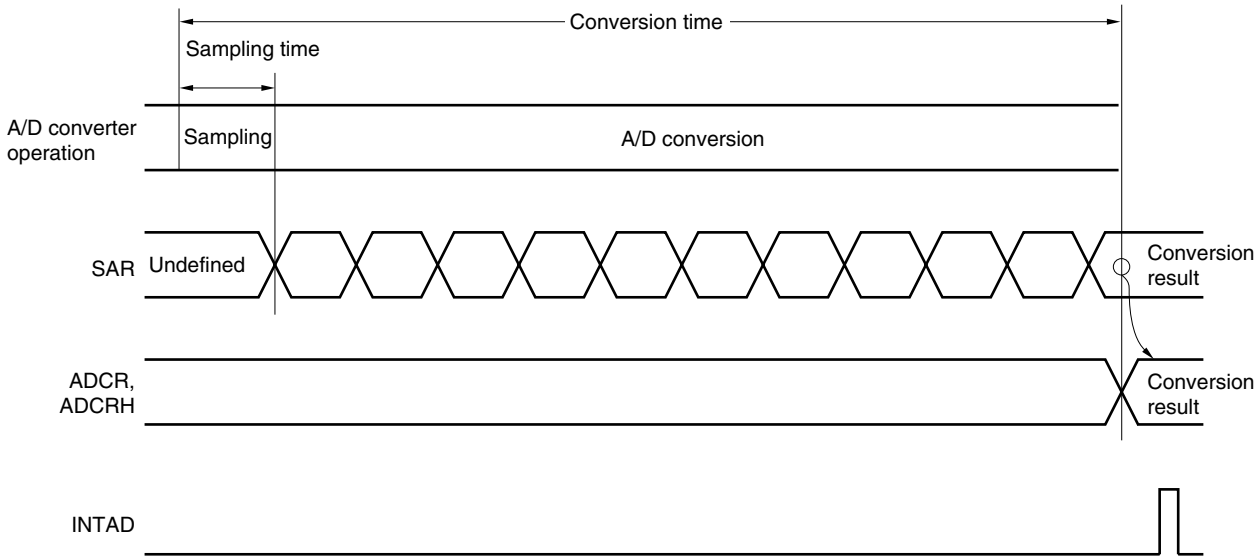


Figure 9-10. Basic Operation of A/D Converter



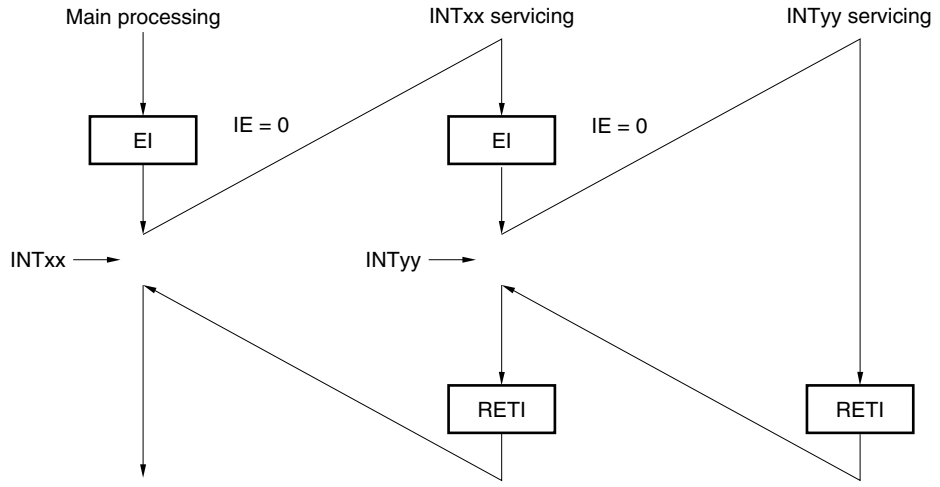
A/D conversion operations are performed continuously until bit 7 (ADCS) of the A/D converter mode register (ADM) is reset (0) by software.

If a write operation is performed to ADM or the analog input channel specification register (ADS) during an A/D conversion operation, the conversion operation is initialized, and if the ADCS bit is set (1), conversion starts again from the beginning.

Reset signal generation makes the A/D conversion result register (ADCR, ADCRH) undefined.

Figure 10-9. Example of Multiple Interrupts (1/2)

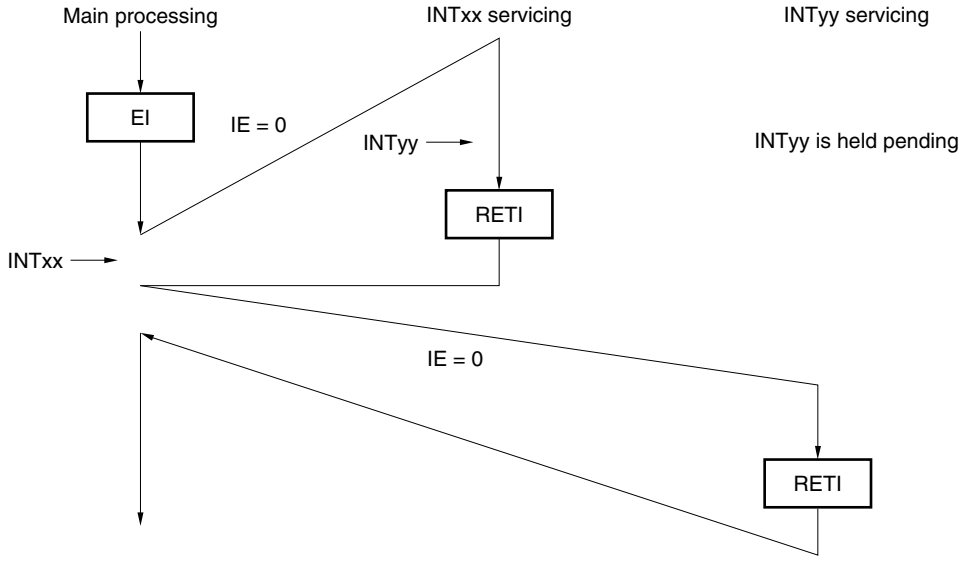
Example 1. Multiple interrupts are acknowledged



During interrupt INTxx servicing, interrupt request INTyy is acknowledged, and multiple interrupts are generated. Before each interrupt request acknowledgement, the EI instruction is issued, the interrupt mask is released, and the interrupt request acknowledgement enable state is set.

Caution Multiple interrupts can be acknowledged even for low-priority interrupts.

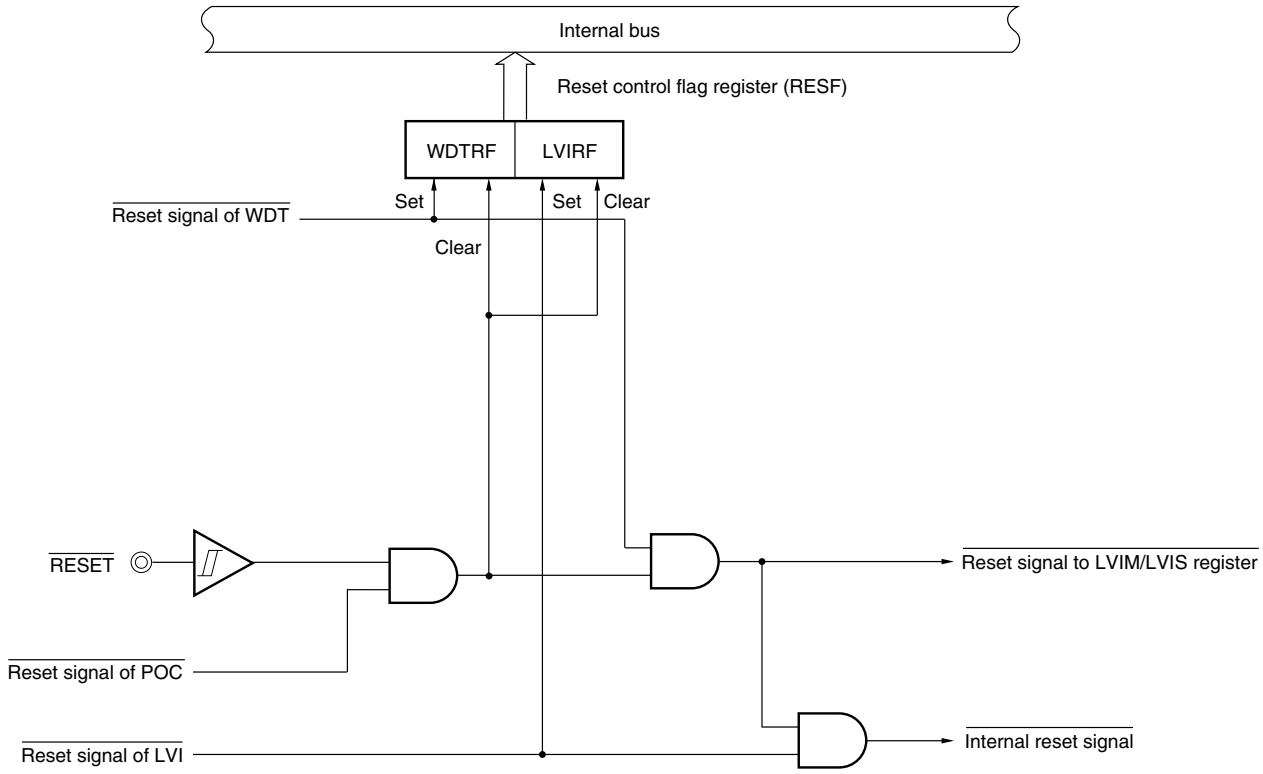
Example 2. Multiple interrupts are not generated because interrupts are not enabled



Because interrupts are not enabled in interrupt INTxx servicing (the EI instruction is not issued), interrupt request INTyy is not acknowledged, and multiple interrupts are not generated. The INTyy request is held pending and acknowledged after the INTxx servicing is performed.

IE = 0: Interrupt request acknowledgment disabled

Figure 12-1. Block Diagram of Reset Function



Caution The LVI circuit is not reset by the internal reset signal of the LVI circuit.

Remarks 1. LVIM: Low-voltage detect register

2. LVIS: Low-voltage detection level select register

14.4 Operation of Low-Voltage Detector

The low-voltage detector can be used in the following two modes.

- Used as reset
  Compares the supply voltage (V_{DD}) and detection voltage (V_{LVI}), and generates an internal reset signal when $V_{DD} < V_{LVI}$, and releases internal reset when $V_{DD} \geq V_{LVI}$.

- Used as interrupt
  Compares the supply voltage (V_{DD}) and detection voltage (V_{LVI}), and generates an interrupt signal (INTLVI) when $V_{DD} < V_{LVI}$.

The operation is set as follows.

(1) When used as reset

- When starting operation

<1> Mask the LVI interrupt (LVIMK = 1).
<2> Set the detection voltage using bits 3 to 0 (LVIS3 to LVIS0) of the low-voltage detection level select register (LVIS).
<3> Set bit 7 (LVION) of LVIM to 1 (enables LVI operation).
<4> Use software to instigate a wait of at least 0.2 ms.
<5> Wait until "supply voltage (V_{DD}) ≥ detection voltage (V_{LVI})" at bit 0 (LVIF) of LVIM is confirmed.
<6> Set bit 1 (LVIMD) of LVIM to 1 (generates internal reset signal when supply voltage (V_{DD}) < detection voltage (V_{LVI})).

Figure 14-4 shows the timing of generating the internal reset signal of the low-voltage detector. Numbers <1> to <6> in this figure correspond to <1> to <6> above.

Cautions 1. <1> must always be executed. When LVIMK = 0, an interrupt may occur immediately after the processing in <3>.

2. If supply voltage (V_{DD}) ≥ detection voltage (V_{LVI}) when LVIMD is set to 1, an internal reset signal is not generated.

- When stopping operation
  Either of the following procedures must be executed.
  - When using 8-bit memory manipulation instruction: Write 00H to LVIM.
  - When using 1-bit memory manipulation instruction: Clear LVIMD to 0 and LVION to 0 in that order.

Figure 16-9. Self Programming State Transition Diagram

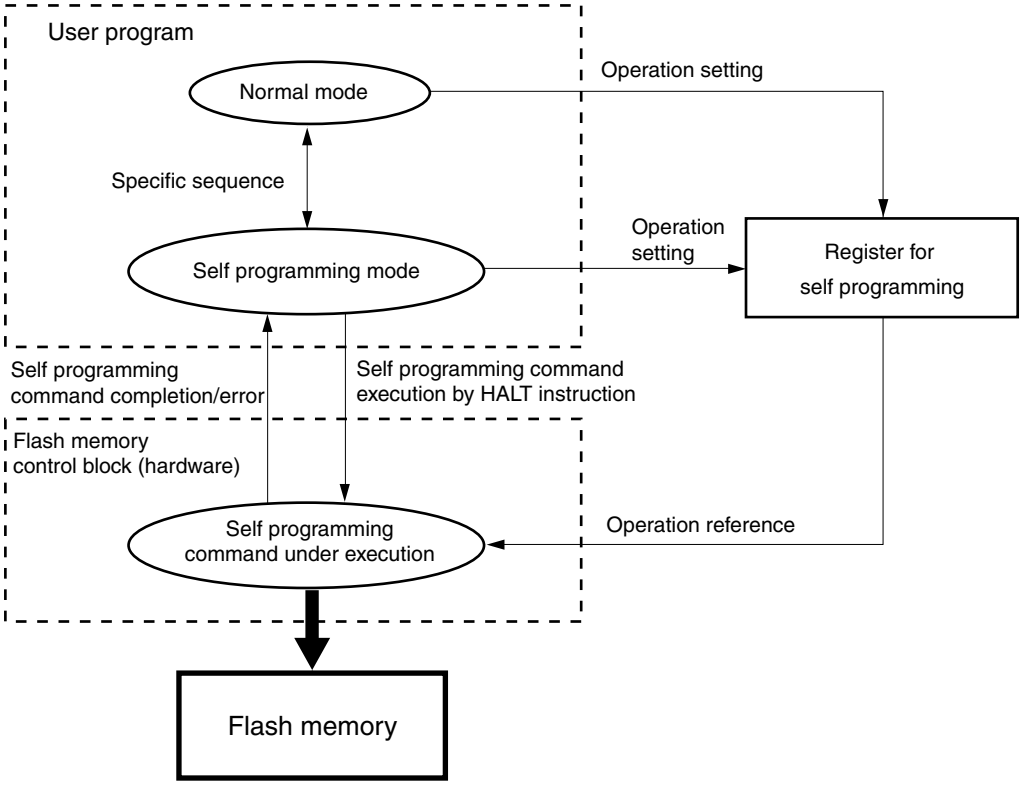


Table 16-10. Self Programming Controlling Commands

Command Name	Function	Time Taken from HALT Instruction Execution to Command Execution End
Internal verify 1	This command is used to check if data has been correctly written to the flash memory. It is used to check whether data has been written to an entire block.	Internal verify for 1 block (internal verify command executed once): 6.8 ms
Internal verify 2	This command is used to check if data has been correctly written to the flash memory. It is used to check whether data has been written in the same block.	Internal verify for 1 byte: 27 μs
Block erasure[Note]	This command is used to erase a specified block. Specify the block number before execution.	8.5 ms
Block blank check	This command is used to check if data in a specified block has been erased. Specify the block number, then execute this command.	480 μs
Byte write	This command is used to write 1-byte data to the specified address in the flash memory. Specify the write address and write data, then execute this command.	150 μs

Note Set the number of retrials larger than the block erasure time divided by the time (8.5 ms) for one erase, in accordance with the time (MAX. value) required for flash memory block erasures.

Remark The command internal verify 1 can be executed by specifying an address in the same block but internal verify 2 is recommended if data is written to two or more addresses in the same block.

(2) Flash protect command register (PFCMD)

If the application system stops inadvertently due to malfunction caused by noise or program hang-up, an operation to write the flash programming mode control register (FLPMC) may have a serious effect on the system. PFCMD is used to protect FLPMC from being written, so that the application system does not stop inadvertently.

Writing FLPMC is enabled only when a write operation is performed in the following specific sequence.

<1> Write a specific value to PFCMD (A5H)
<2> Write the value to be set to bit 0 (FLSPM) of the FLPMC (writing in this step is invalid)
<3> Write the inverted value of the value to be set to bit 0 (FLSPM) of the FLPMC (writing in this step is invalid)
<4> Write the value to be set to bit 0 (FLSPM) of the FLPMC (writing in this step is valid)

Caution Interrupt servicing cannot be executed in self-programming mode. Disable interrupt servicing (by executing the DI instruction while MK0 = FFH) before executing the specific sequence that sets self-programming mode and after executing the specific sequence that changes the mode to the normal mode.

This rewrites the value of the register, so that the register cannot be written illegally.

Occurrence of an illegal store operation can be checked by bit 0 (FPRERR) of the flash status register (PFS). Check FPRERR using a 1-bit memory manipulation instruction.

A5H must be written to PFCMD each time the value of FLPMC is changed.

PFCMD can be set by an 8-bit memory manipulation instruction.

Reset signal generation makes PFCMD undefined.

Figure 16-11. Format of Flash Protect Command Register (PFCMD)

Address: FFA0H After reset: Undefined W

Symbol	7	6	5	4	3	2	1	0
PFCMD	REG7	REG6	REG5	REG4	REG3	REG2	REG1	REG0

(3) Flash status register (PFS)

If data is not written to the flash programming mode control register (FLPMC), which is protected, in the correct sequence (writing the flash protect command register (PFCMD)), FLPMC is not written and a protection error occurs. If this happens, bit 0 of PFS (FPRERR) is set to 1.

When FPRERR is 1, it can be cleared to 0 by writing 0 to it.

Errors that may occur during self-programming are reflected in bit 1 (VCERR) and bit 2 (WEPRERR) of PFS. VCERR or WEPRERR can be cleared by writing 0 to them.

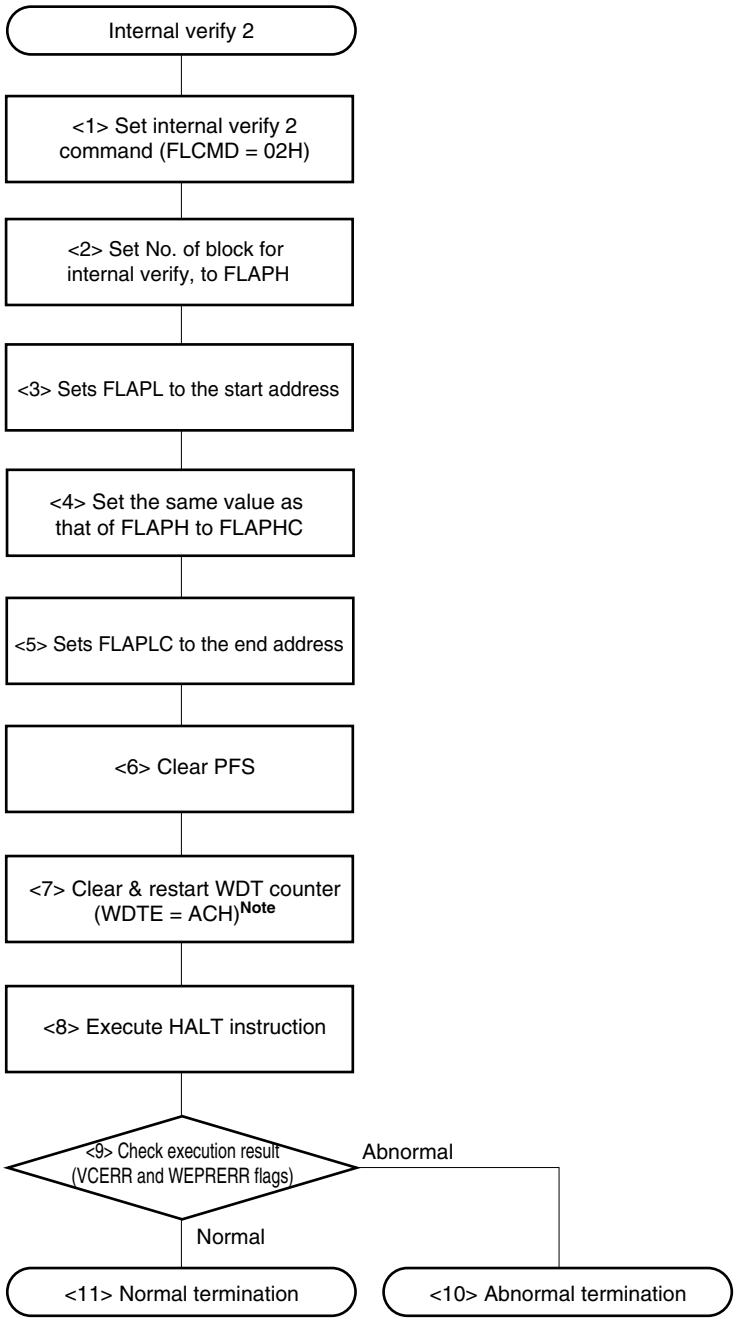
All the flags of the PFS register must be pre-cleared to 0 to check if the operation is performed correctly.

PFS can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears PFS to 00H.

Caution Check FPRERR using a 1-bit memory manipulation instruction.

Figure 16-24. Example of Internal Verify 2 Operation in Self Programming Mode



Note This setting is not required when the watchdog timer is not used.

Remark <1> to <11> in Figure 16-24 correspond to Internal verify 2 <1> to <11> in **16.8.9** (the page before last).

Notes 2. This is the pin connection when the X1 and X2 pins are not used in the target system. When using the X1 and X2 pins, refer to **17.1.2 Connection of X1 and X2 pins**.

3. No problem will occur if the dashed line portions are connected.

4. This pin is connected to enhance the accuracy of time measurement between run and break during debugging. Debugging is possible even if this pin is left open, but measurement error occurs in several ms units.

5. The INTP1 pin is used for communication between QB-MINI2 and the target device during debugging. When debugging is performed with QB-MINI2, therefore, the INTP1 pin and its alternate-function pin cannot be used. For INTP1 pin connection, refer to **17.1.1 Connection of INTP1 pin**.

Pins for communication depend on whether the monitor program has been written or not. (refer to **Table 17-1**) X1 and X2 pins can be used as I/O port pins or the pins for oscillation, after the monitor program has been written.

Table 17-1. Pins for communication with QB-MINI2

Before writing the monitor program	After writing the monitor program
X1[Note 1], X2[Note 2], $\overline{\text{RESET}}$, INTP1, V_{DD}, V_{SS}	$\overline{\text{RESET}}$, INTP1, V_{DD}, V_{SS}

<R> **Notes 1. μPD78F920x: X1/P23/ANI3, μPD78F950x: EXCLK/P23**

<R> **2. μPD78F920x: X2/P22/ANI2, μPD78F950x: P22**

17.1.1 Connection of INTP1 pin

The INTP1 pin is used only for communication between QB-MINI2 and the target device during debugging. Design circuits appropriately according to the relevant case among the cases shown below.

(1) INTP1 pin is not used in target system (as is illustrated in **Figure 17-1. Recommended Circuit Connection**)
→ See **Figure 17-2**.

(2) QB-MINI2 is used only for programming, not for debugging
→ See **Figure 17-3**.

(3) QB-MINI2 is used for debugging and debugging of the INTP1 pin is performed only with a real machine
→ See **Figure 17-4**.

Figure 17-2. Circuit Connection for the Case Where INTP1 Pin Is Not Used in Target System

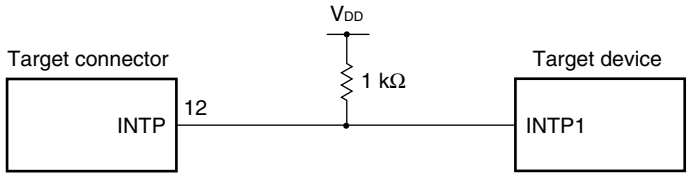
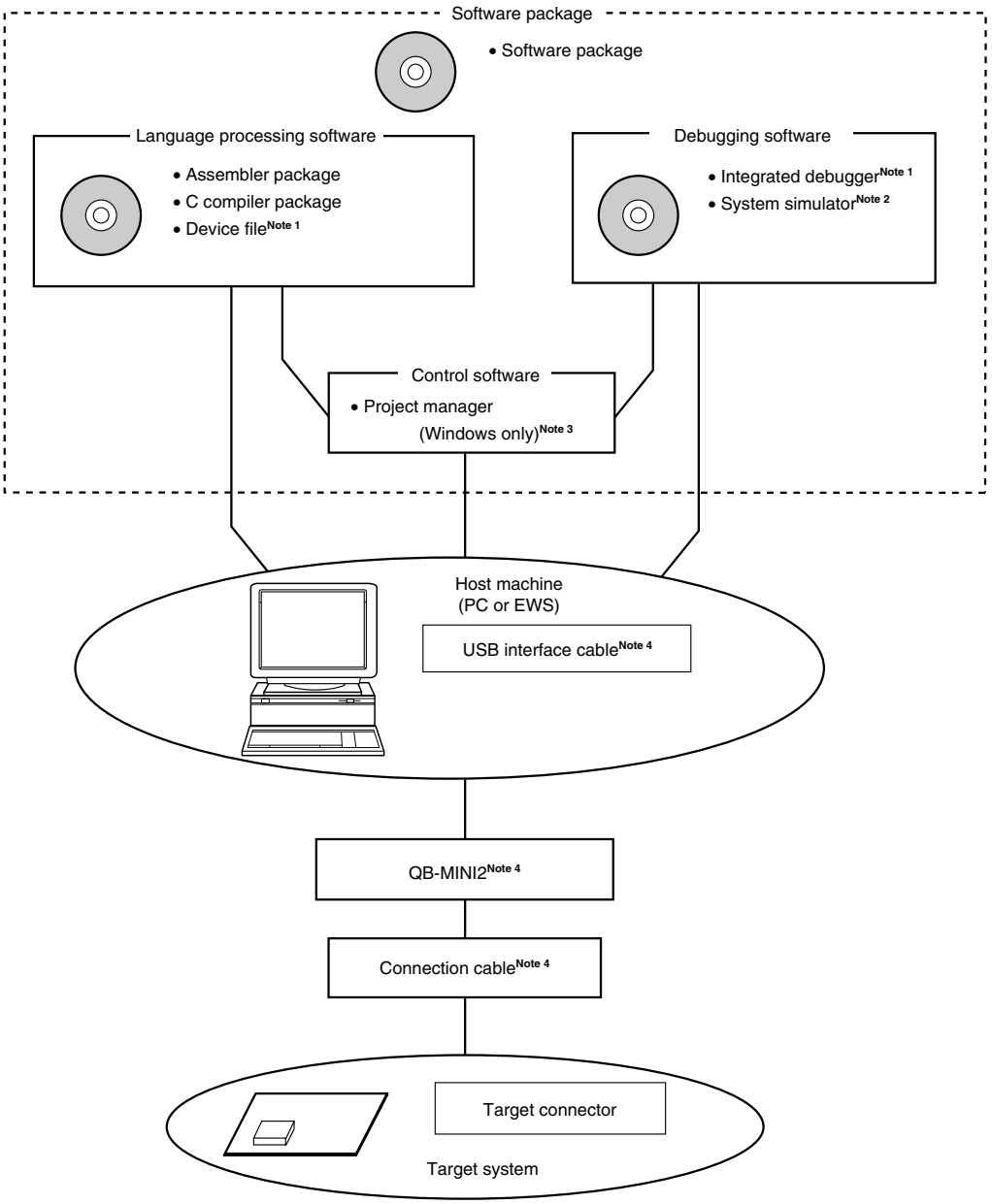


Figure 17-3. Circuit Connection for the Case Where QB-MINI2 Is Used Only for Programming

Figure A-1. Development Tools (2/2)

(2) When using the on-chip debug emulator with programming function QB-MINI2



Notes 1. Download the device file for 78K0S/Kx1+ microcontrollers (DF789234) and the integrated debugger ID78K0S-QB from the download site for development tools (http://www.necel.com/micro/en/ods/).

2. SM+ for 78K0S (instruction simulation version) is included in the software package. SM+ for 78K0S/Kx1+ (instruction + peripheral simulation version) is not included.

3. The project manager PM+ is included in the assembler package.
PM+ cannot be used other than with Windows.

4. QB-MINI2 is supplied with USB interface cable and connection cable. Any other products are sold separately. In addition, download the software for operating the QB-MINI2 from the download site for development tools (http://www.necel.com/micro/en/ods/).

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