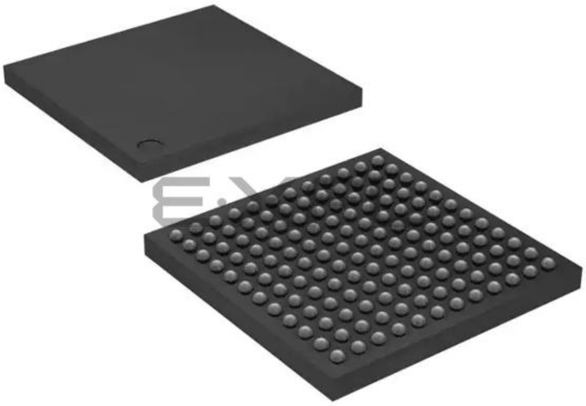

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, I²C, IrDA, SPI, UART/USART, USB, USB OTG
Peripherals	DMA, I²S, LVD, POR, PWM, WDT
Number of I/O	100
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 42x16b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LBGA
Supplier Device Package	144-MAPBGA (13x13)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mk21fn1m0avmd12

- Three analog comparators (CMP)
- Voltage reference

Ordering Information [1]

Part Number	Memory		Maximum number of I\O's
	Flash (KB)	SRAM (KB)	
MK21FX512VLQ12	512 KB	128	104
MK21FN1M0VLQ12	1 MB	128	104
MK21FX512VMD12	512 KB	128	104
MK21FN1M0VMD12	1 MB	128	104

1. To confirm current availability of ordererable part numbers, go to http://www.freescale.com and perform a part number search.

Related Resources

Type	Description	Resource
Selector Guide	The Freescale Solution Advisor is a web-based tool that features interactive application wizards and a dynamic product selector.	Solution Advisor
Product Brief	The Product Brief contains concise overview/summary information to enable quick evaluation of a device for design suitability.	K20PB[1]
Reference Manual	The Reference Manual contains a comprehensive description of the structure and function (operation) of a device.	K21P144M50SF5RM[1]
Data Sheet	The Data Sheet includes electrical characteristics and signal connections.	K21P144M50SF5[1]
Package drawing	Package dimensions are provided in package drawings.	• LQFP 144-pin: 98ASS23177W[1] • MAPBGA 144-pin: 98ASA00222D[1]

1. To find the associated resource, go to http://www.freescale.com and perform a search using this term.

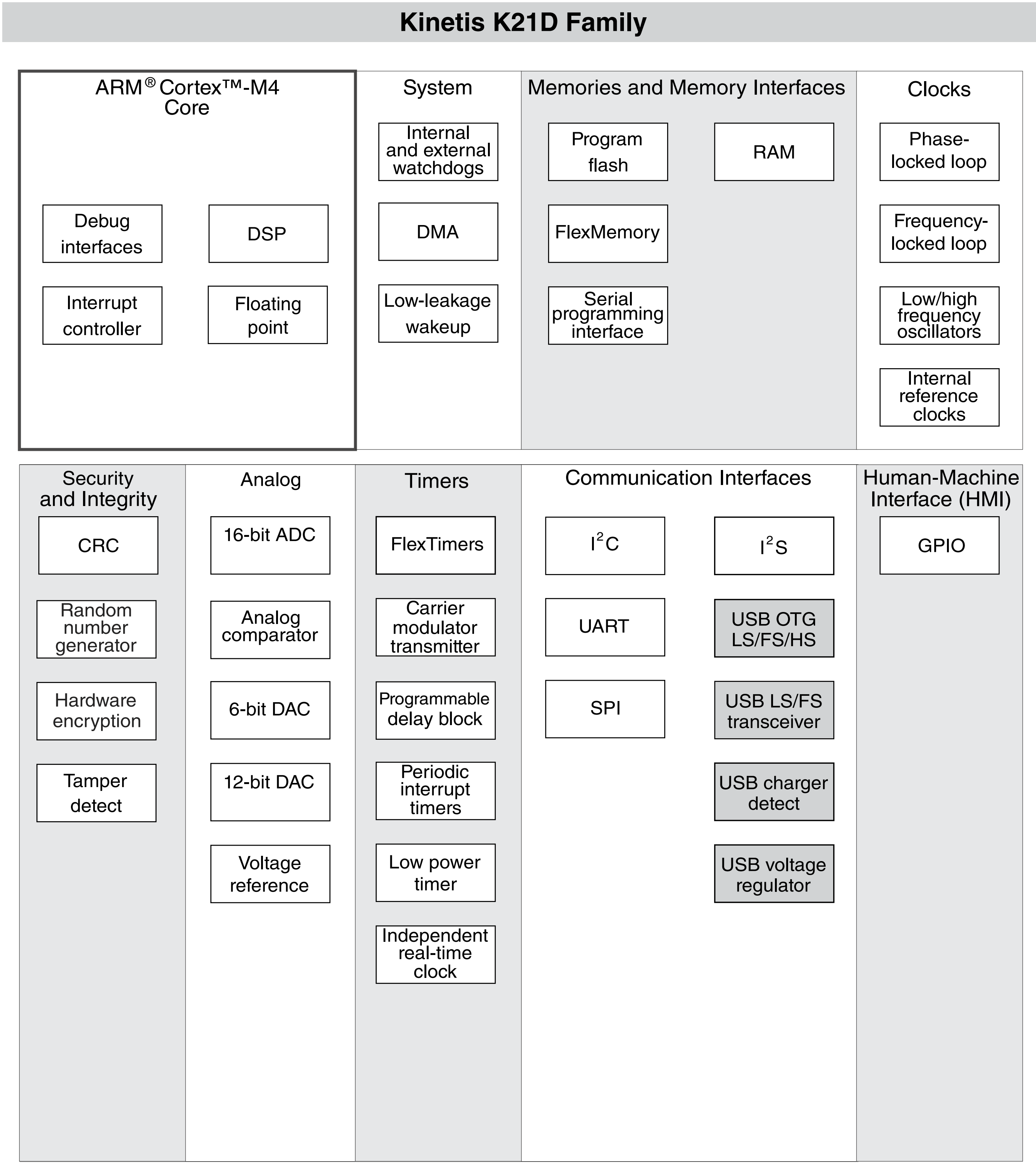


Figure 1. K20 block diagram

2.2.3 Voltage and current operating behaviors

Table 4. Voltage and current operating behaviors

Symbol	Description	Min.	Typ	Max.	Unit	Notes
V_{OH}	Output high voltage — high drive strength					
	• 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OH} = -8mA	V_{DD} – 0.5	—	—	V	
	• 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OH} = -3mA	V_{DD} – 0.5	—	—	V	
	Output high voltage — low drive strength					
	• 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OH} = -2mA	V_{DD} – 0.5	—	—	V	
	• 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OH} = -0.6mA	V_{DD} – 0.5	—	—	V	
I_{OHT}	Output high current total for all ports	—	—	100	mA	
V_{OH_Tamper}	Output high voltage — high drive strength	V_{BAT} – 0.5			V	
	• 2.7 V ≤ V_{BAT} ≤ 3.6 V, I_{OH} = -10mA	V_{BAT} – 0.5	—	—	V	
	• 1.71 V ≤ V_{BAT} ≤ 2.7 V, I_{OH} = -3mA		—	—		
	Output high voltage — low drive strength	V_{BAT} – 0.5			V	
	• 2.7 V ≤ V_{BAT} ≤ 3.6 V, I_{OH} = -2mA	V_{BAT} – 0.5	—	—	V	
	• 1.71 V ≤ V_{BAT} ≤ 2.7 V, I_{OH} = -0.6mA		—	—		
I_{OH_Tamper}	Output high current total for Tamper pins	—	—	100	mA	
V_{OL}	Output low voltage — high drive strength					1
	• 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OL} = 9mA	—	—	0.5	V	
	• 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OL} = 3mA	—	—	0.5	V	
	Output low voltage — low drive strength					
	• 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OL} = 2mA	—	—	0.5	V	
	• 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OL} = 0.6mA	—	—	0.5	V	
I_{OLT}	Output low current total for all ports	—	—	100	mA	
V_{OL_Tamper}	Output low voltage — high drive strength			0.5	V	
	• 2.7 V ≤ V_{BAT} ≤ 3.6 V, I_{OL} = 10mA	—	—	0.5	V	
	• 1.71 V ≤ V_{BAT} ≤ 2.7 V, I_{OL} = 3mA	—	—			
	Output low voltage — low drive strength			0.5	V	
	• 2.7 V ≤ V_{BAT} ≤ 3.6 V, I_{OL} = 2mA	—	—	0.5	V	
	• 1.71 V ≤ V_{BAT} ≤ 2.7 V, I_{OL} = 0.6mA	—	—			
I_{OL_Tamper}	Output low current total for Tamper pins	—	—	100	mA	
I_{IND}	Input leakage current, digital pins					2, 3
	• V_{SS} ≤ V_{IN} ≤ V_{IL}					
	• All digital pins	—	0.002	0.5	μA	

Table continues on the next page...

Table 4. Voltage and current operating behaviors (continued)

Symbol	Description	Min.	Typ	Max.	Unit	Notes
	• $V_{IN} = V_{DD}$ • All digital pins except PTD7 • PTD7	— —	0.002 0.004	0.5 1	μA μA	
I_{IND}	Input leakage current, digital pins • $V_{IL} < V_{IN} < V_{DD}$ • V_{DD} = 3.6 V • V_{DD} = 3.0 V • V_{DD} = 2.5 V • V_{DD} = 1.7 V	— — — —	18 12 8 3	26 19 13 6	μA μA μA μA	2
I_{IND}	Input leakage current, digital pins • $V_{DD} < V_{IN} < 5.5$ V	—	1	50	μA	
I_{IN_Tamper}	Input leakage current (per Tamper pin) for full temperature range	—	—	1	μA	
I_{IN_Tamper}	Input leakage current (per Tamper pin) at 25°C	—	—	0.025	μA	
I_{OZ}	Hi-Z (off-state) leakage current (per pin)	—	—	0.25	μA	
I_{OZ_Tamper}	Hi-Z (off-state) leakage current (per Tamper pin)	—	—	0.25	μA	
R_{PU}	Internal pullup resistors (except Tamper pins)	20	35	50	kΩ	4
R_{PD}	Internal pulldown resistors (except Tamper pins)	20	35	50	kΩ	5

1. Open drain outputs must be pulled to V_{DD}.
2. Measured at VDD=3.6V
3. Internal pull-up/pull-down resistors disabled.
4. Measured at V_{DD} supply voltage = V_{DD} min and Vinput = V_{SS}
5. Measured at V_{DD} supply voltage = V_{DD} min and Vinput = V_{DD}

2.2.4 Power mode transition operating behaviors

All specifications except t_{POR}, and VLLSx→RUN recovery times in the following table assume this clock configuration:

- CPU and system clocks = 100 MHz
- Bus clock = 50 MHz
- FlexBus clock = 50 MHz
- Flash clock = 25 MHz

- No GPIOs toggled
- Code execution from flash with cache enabled
- For the ALLOFF curve, all peripheral clocks are disabled except FTFE

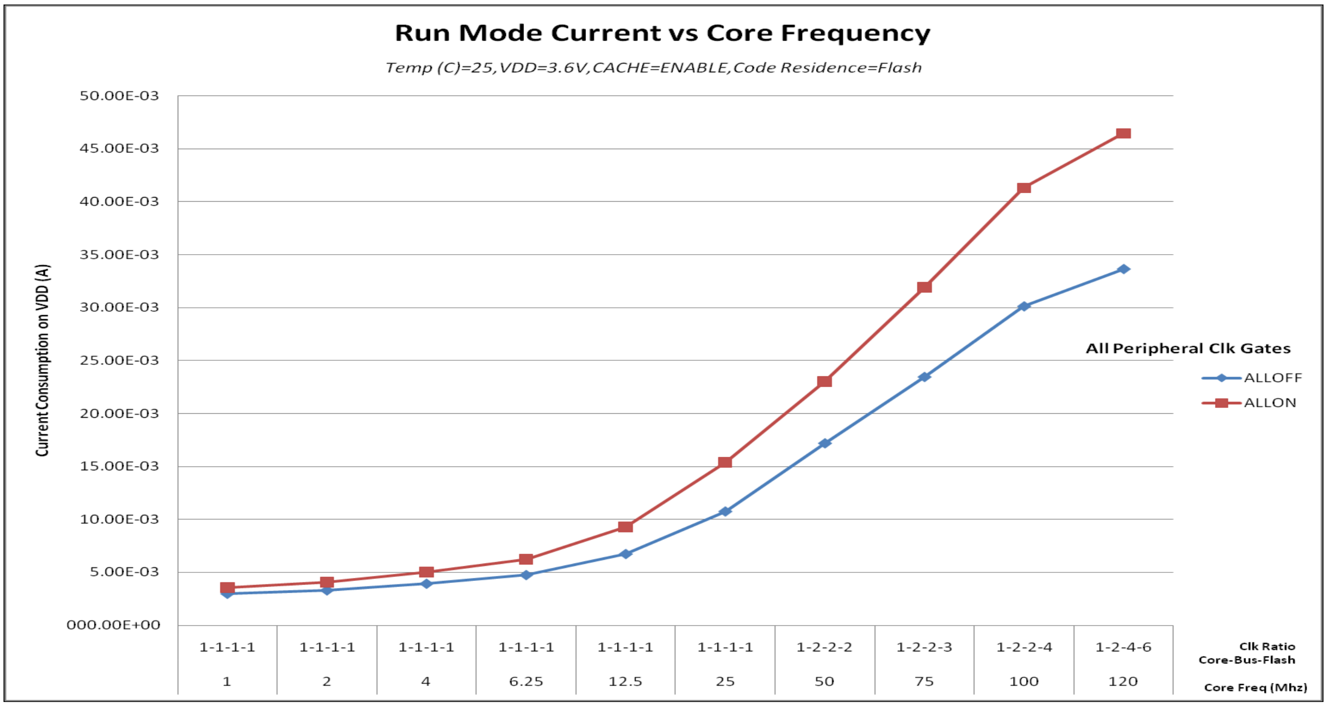


Figure 3. Run mode supply current vs. core frequency

Table 15. MCG specifications (continued)

Symbol	Description		Min.	Typ.	Max.	Unit	Notes
		$2197 \times f_{fll\_ref}$					
		High range (DRS=11) $2929 \times f_{fll\_ref}$	—	95.98	—	MHz	
J_{cyc_fll}	FLL period jitter • f_{DCO} = 48 MHz • f_{DCO} = 98 MHz		— —	180 150	— —	ps	
$t_{fll\_acquire}$	FLL target frequency acquisition time		—	—	1	ms	7
PLL							
f_{vco}	VCO operating frequency		48.0	—	120	MHz	
I_{pll}	PLL operating current • PLL @ 96 MHz ($f_{osc\_hi\_1}$ = 8 MHz, f_{pll_ref} = 2 MHz, VDIV multiplier = 48)		—	1060	—	µA	8
I_{pll}	PLL operating current • PLL @ 48 MHz ($f_{osc\_hi\_1}$ = 8 MHz, f_{pll_ref} = 2 MHz, VDIV multiplier = 24)		—	600	—	µA	8
f_{pll_ref}	PLL reference frequency range		2.0	—	4.0	MHz	
J_{cyc_pll}	PLL period jitter (RMS) • f_{vco} = 48 MHz • f_{vco} = 120 MHz		— —	120 75	— —	ps ps	9
J_{acc_pll}	PLL accumulated jitter over 1µs (RMS) • f_{vco} = 48 MHz • f_{vco} = 120 MHz		— —	1350 600	— —	ps ps	9
D_{lock}	Lock entry frequency tolerance		± 1.49	—	± 2.98	%	
D_{unl}	Lock exit frequency tolerance		± 4.47	—	± 5.97	%	
t_{pll_lock}	Lock detector detection time		—	—	$150 \times 10^{-6} + 1075(1/f_{pll\_ref})$	s	10

1. This parameter is measured with the internal reference (slow clock) being used as a reference to the FLL (FEI clock mode).
2. 2 V <= VDD <= 3.6 V.
3. These typical values listed are with the slow internal reference clock (FEI) using factory trim and DMX32=0.
4. The resulting system clock frequencies should not exceed their maximum specified values. The DCO frequency deviation (Δf_{dco_t}) over voltage and temperature should be considered.
5. These typical values listed are with the slow internal reference clock (FEI) using factory trim and DMX32=1.
6. The resulting clock frequency must not exceed the maximum specified clock frequency of the device.
7. This specification applies to any time the FLL reference source or reference divider is changed, trim value is changed, DMX32 bit is changed, DRS bits are changed, or changing from FLL disabled (BLPE, BLPI) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.
8. Excludes any oscillator currents that are also consuming power while PLL is in operation.
9. This specification was obtained using a Freescale developed PCB. PLL jitter is dependent on the noise characteristics of each PCB and results will vary.
10. This specification applies to any time the PLL VCO divider or reference divider is changed, or changing from PLL disabled (BLPE, BLPI) to PLL enabled (PBE, PEE). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

2. When transitioning from FEI or FBI to FBE mode, restrict the frequency of the input clock so that, when it is divided by FRDIV, it remains within the limits of the DCO input clock frequency.
3. Proper PC board layout procedures must be followed to achieve specifications.
4. Crystal startup time is defined as the time between the oscillator being enabled and the OSCINIT bit in the MCG_S register being set.

NOTE

The 32 kHz oscillator works in low power mode by default and cannot be moved into high power/gain mode.

3.3.3 32 kHz oscillator electrical characteristics

3.3.3.1 32 kHz oscillator DC electrical specifications

Table 18. 32kHz oscillator DC electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit
V_{BAT}	Supply voltage	1.71	—	3.6	V
R_F	Internal feedback resistor	—	100	—	MΩ
C_{para}	Parasitical capacitance of EXTAL32 and XTAL32	—	5	7	pF
V_{pp}[1]	Peak-to-peak amplitude of oscillation	—	0.6	—	V

1. When a crystal is being used with the 32 kHz oscillator, the EXTAL32 and XTAL32 pins should only be connected to required oscillator components and must not be connected to any other devices.

3.3.3.2 32 kHz oscillator frequency specifications

Table 19. 32 kHz oscillator frequency specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
f_{osc_lo}	Oscillator crystal	—	32.768	—	kHz	
t_{start}	Crystal start-up time	—	1000	—	ms	1
$v_{ec\_extal32}$	Externally provided input clock amplitude	700	—	V_{BAT}	mV	2, 3

1. Proper PC board layout procedures must be followed to achieve specifications.
2. This specification is for an externally supplied clock driven to EXTAL32 and does not apply to any other clock input. The oscillator remains enabled and XTAL32 must be left unconnected.
3. The parameter specified is a peak-to-peak value and V_{IH} and V_{IL} specifications do not apply. The voltage of the applied clock must be within the range of V_{SS} to V_{BAT}.

3.4 Memories and memory interfaces

2. Specification is valid for all FB_AD[31:0] and $\overline{\text{FB\_TA}}$.

Table 26. Flexbus full voltage range switching specifications

Num	Description	Min.	Max.	Unit	Notes
	Operating voltage	1.71	3.6	V	
	Frequency of operation	—	FB_CLK	MHz	
FB1	Clock period	1/FB_CLK	—	ns	
FB2	Address, data, and control output valid	—	13.5	ns	1
FB3	Address, data, and control output hold	0	—	ns	1
FB4	Data and $\overline{\text{FB\_TA}}$ input setup	13.7	—	ns	2
FB5	Data and $\overline{\text{FB\_TA}}$ input hold	0.5	—	ns	2

1. Specification is valid for all FB_AD[31:0], $\overline{\text{FB\_BE/BWE}n}$, $\overline{\text{FB\_CS}n}$, $\overline{\text{FB\_OE}}$, FB_R/$\overline{\text{W}}$,$\overline{\text{FB\_TBST}}$, FB_TSIZ[1:0], FB_ALE, and $\overline{\text{FB\_TS}}$.
2. Specification is valid for all FB_AD[31:0] and $\overline{\text{FB\_TA}}$.

Table 27. 16-bit ADC operating conditions (continued)

Symbol	Description	Conditions	Min.	Typ.[1]	Max.	Unit	Notes
		Continuous conversions enabled, subsequent conversion time					
C_{rate}	ADC conversion rate	16-bit mode No ADC hardware averaging Continuous conversions enabled, subsequent conversion time	37.037	—	461.467	Ksps	5

1. Typical values assume V_{DDA} = 3.0 V, Temp = 25 °C, f_{ADCK} = 1.0 MHz, unless otherwise stated. Typical values are for reference only, and are not tested in production.
2. DC potential difference.
3. This resistance is external to MCU. To achieve the best results, the analog source resistance must be kept as low as possible. The results in this data sheet were derived from a system that had < 8 Ω analog source resistance. The R_{AS}/C_{AS} time constant should be kept to < 1 ns.
4. To use the maximum ADC conversion clock frequency, CFG2[ADHSC] must be set and CFG1[ADLPC] must be clear.
5. For guidelines and examples of conversion rate calculation, download the ADC calculator tool.

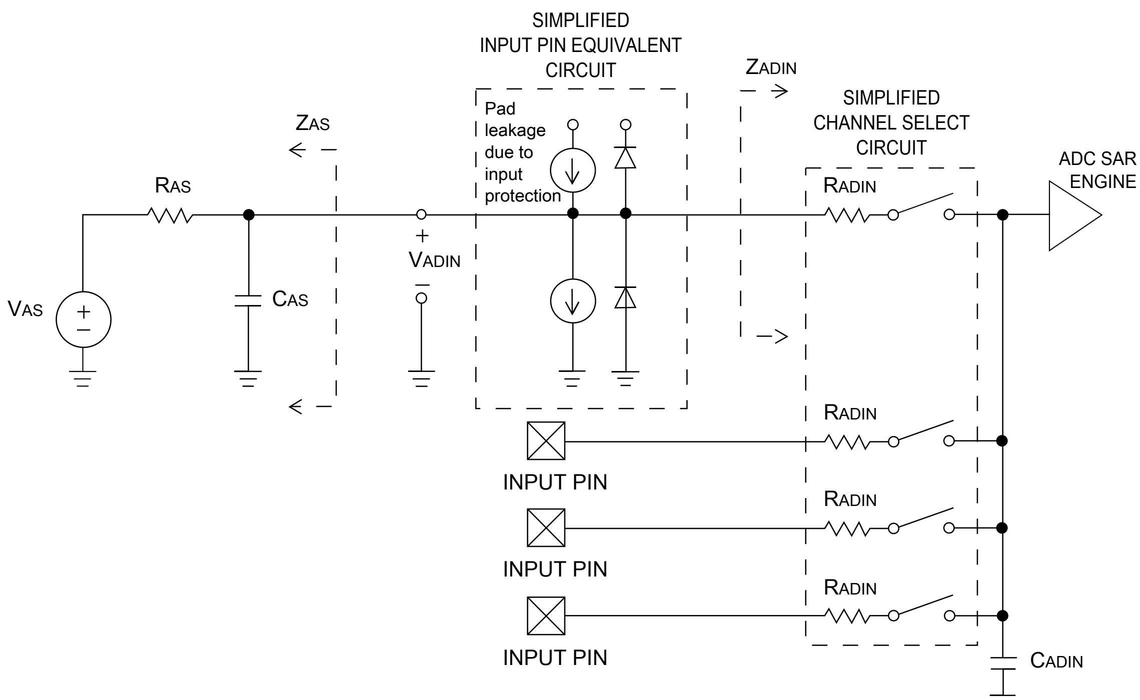


Figure 15. ADC input impedance equivalency diagram

3.6.1.2 16-bit ADC electrical characteristics

Table 28. 16-bit ADC characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$) (continued)

Symbol	Description	Conditions[1]	Min.	Typ.[2]	Max.	Unit	Notes
		• Avg = 32					
E_{IL}	Input leakage error			$I_{In} \times R_{AS}$		mV	I_{In} = leakage current (refer to the MCU's voltage and current operating ratings)
	Temp sensor slope	Across the full temperature range of the device	1.55	1.62	1.69	mV/°C	8
V_{TEMP25}	Temp sensor voltage	25 °C	706	716	726	mV	8

1. All accuracy numbers assume the ADC is calibrated with $V_{REFH} = V_{DDA}$
2. Typical values assume V_{DDA} = 3.0 V, Temp = 25 °C, f_{ADCK} = 2.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.
3. The ADC supply current depends on the ADC conversion clock speed, conversion rate and ADC_CFG1[ADLPC] (low power). For lowest power operation, ADC_CFG1[ADLPC] must be set, the ADC_CFG2[ADHSC] bit must be clear with 1 MHz ADC conversion clock speed.
4. 1 LSB = $(V_{REFH} - V_{REFL})/2^N$
5. ADC conversion clock < 16 MHz, Max hardware averaging (AVGE = %1, AVGS = %11)
6. Input data is 100 Hz sine wave. ADC conversion clock < 12 MHz.
7. Input data is 1 kHz sine wave. ADC conversion clock < 12 MHz.
8. ADC conversion clock < 3 MHz

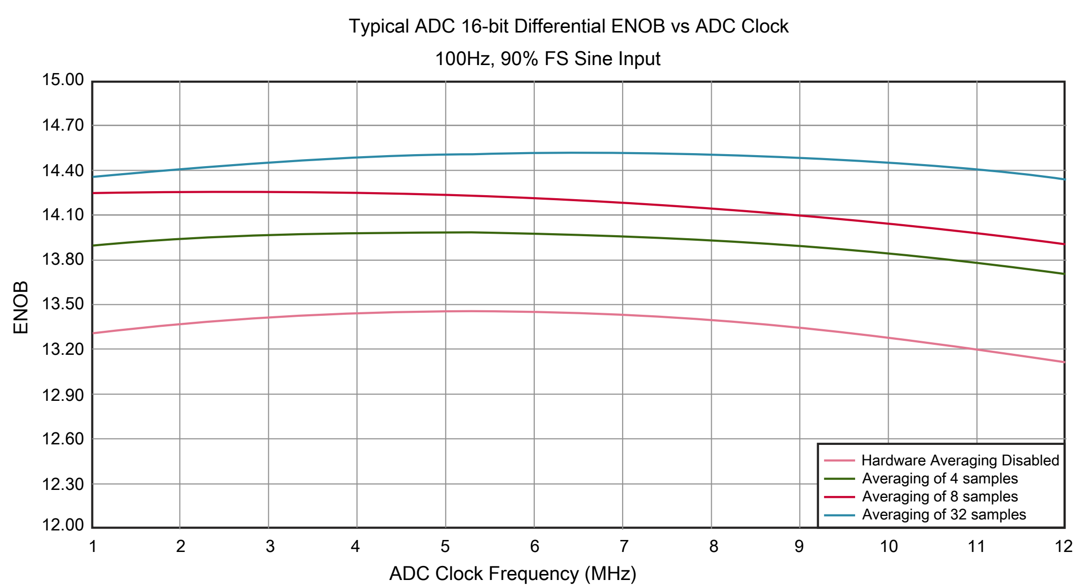


Figure 16. Typical ENOB vs. ADC_CLK for 16-bit differential mode

6. V_{DDA} = 3.0 V, reference select set for V_{DDA} (DACx_CO:DACRFS = 1), high power mode (DACx_C0:LPEN = 0), DAC set to 0x800, temperature range is across the full range of the device

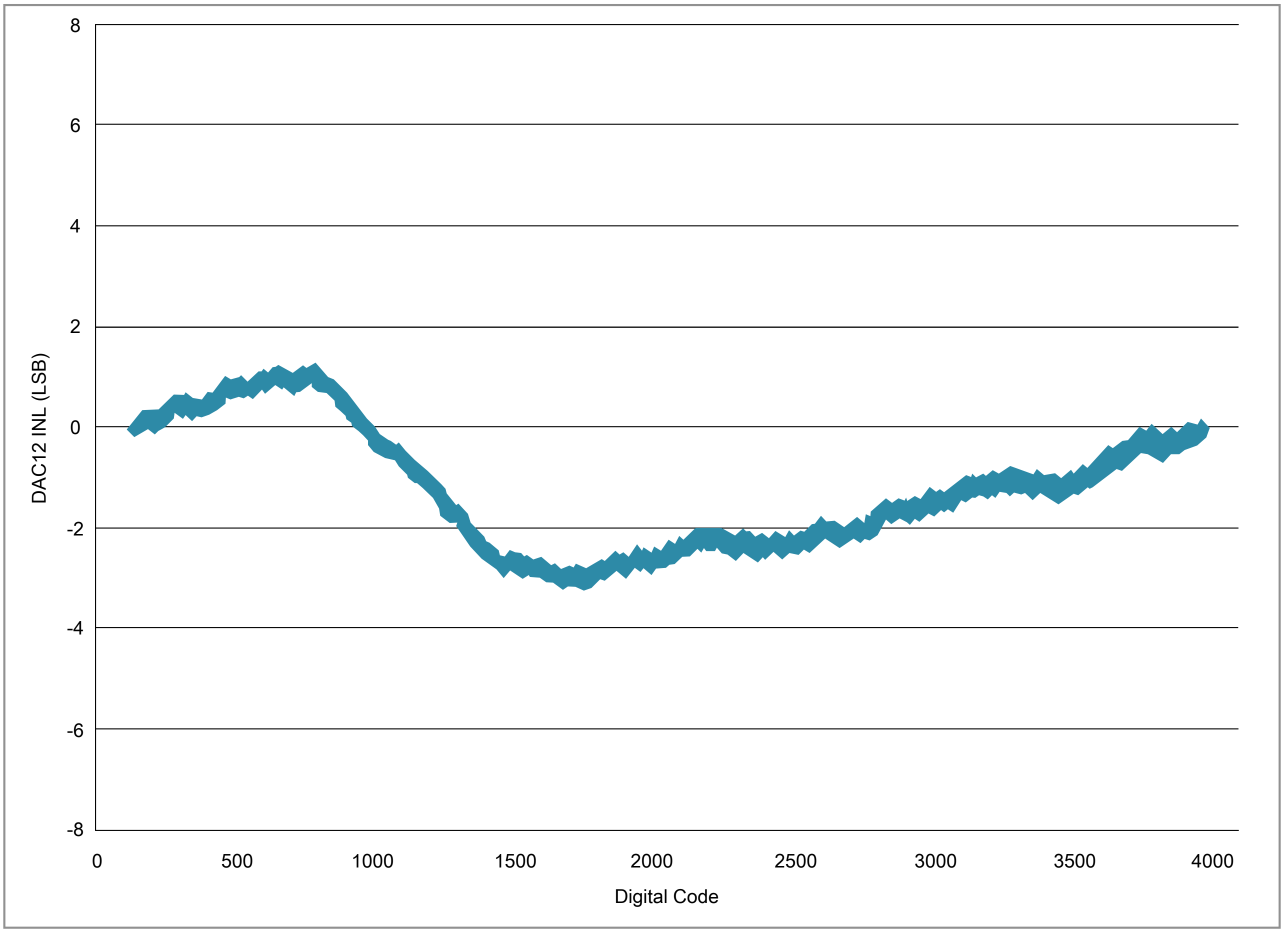


Figure 20. Typical INL error vs. digital code

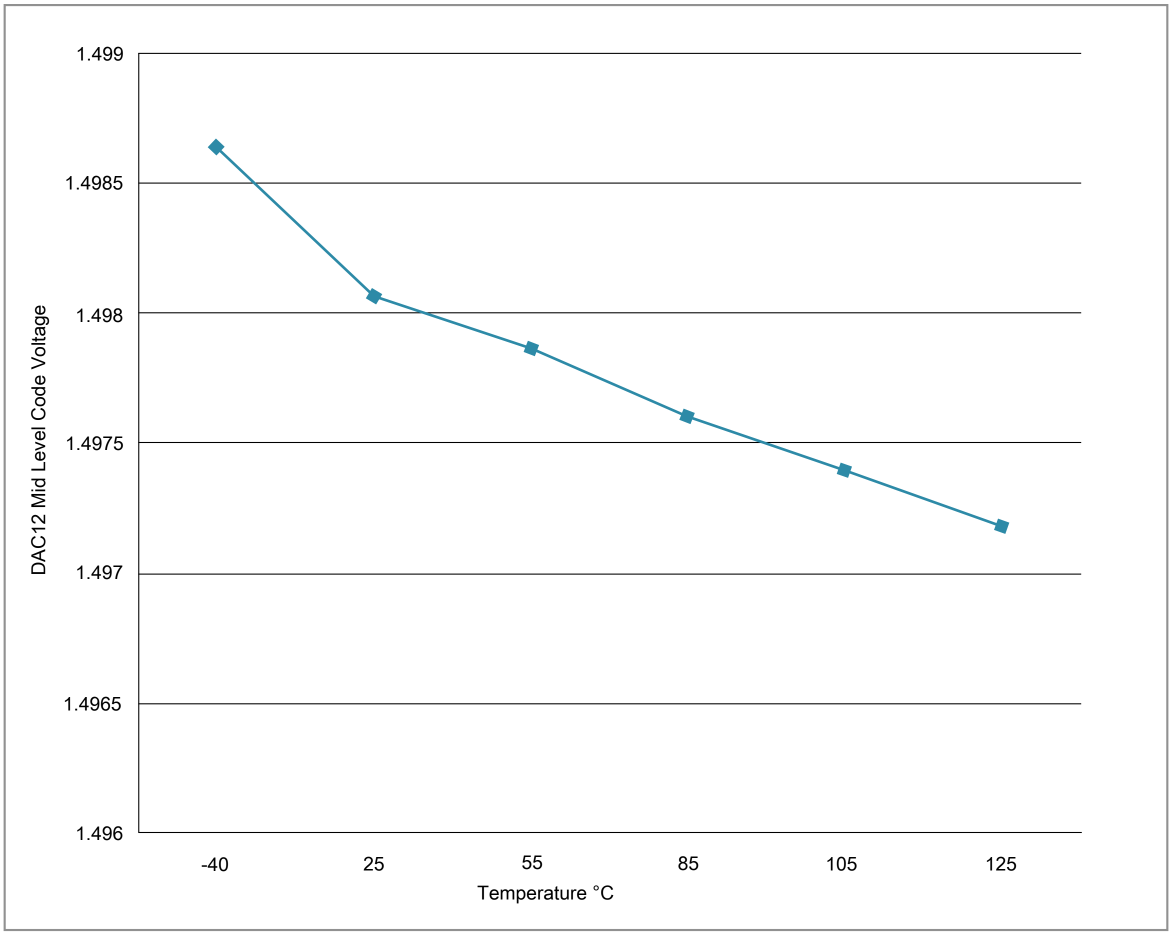


Figure 21. Offset at half scale vs. temperature

3.6.4 Voltage reference electrical specifications

Table 32. VREF full-range operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
V_{DDA}	Supply voltage	1.71	3.6	V	—
T_A	Temperature	Operating temperature range of the device		°C	—
C_L	Output load capacitance	100		nF	1, 2

1. C_L must be connected to VREF_OUT if the VREF_OUT functionality is being used for either an internal or external reference.
2. The load capacitance should not exceed +/-25% of the nominal specified C_L value over the operating temperature range of the device.

3.8.7 I²C switching specifications

See General switching specifications.

3.8.8 UART switching specifications

See General switching specifications.

3.8.9 SDHC specifications

The following timing specs are defined at the chip I/O pin and must be translated appropriately to arrive at timing specs/constraints for the physical interface. The following timing specifications assume a load of 50 pF.

Table 42. SDHC switching specifications

Num	Symbol	Description	Min.	Max.	Unit
		Operating voltage	1.71	3.6	V
	Card input clock				
SD1	fpp	Clock frequency (low speed)	0	400	kHz
	fpp	Clock frequency (SD\SDIO full speed\high speed)	0	25\50	MHz
	fpp	Clock frequency (MMC full speed\high speed)	0	20\50	MHz
	f_{OD}	Clock frequency (identification mode)	0	400	kHz
SD2	t_{WL}	Clock low time	7	—	ns
SD3	t_{WH}	Clock high time	7	—	ns
SD4	t_{TLH}	Clock rise time	—	3	ns
SD5	t_{THL}	Clock fall time	—	3	ns
	SDHC output / card inputs SDHC_CMD, SDHC_DAT (reference to SDHC_CLK)				
SD6	t_{OD}	SDHC output delay (output valid)	-5	8.3	ns
	SDHC input / card inputs SDHC_CMD, SDHC_DAT (reference to SDHC_CLK)				
SD7	t_{ISU}	SDHC input setup time	5	—	ns
SD8	t_{IH}	SDHC input hold time	0	—	ns

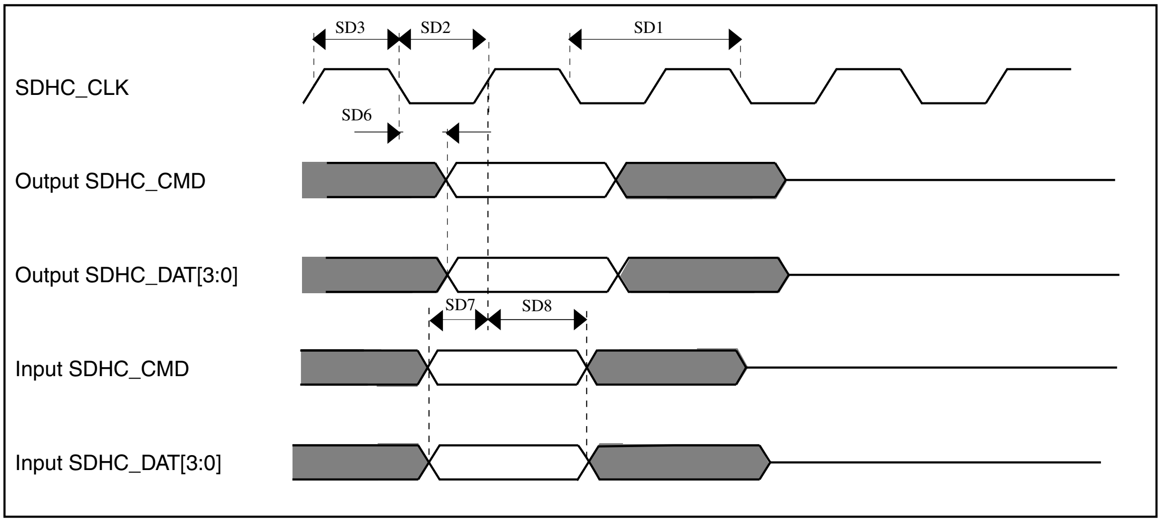


Figure 26. SDHC timing

3.8.10 I2S switching specifications

This section provides the AC timings for the I2S in master (clocks driven) and slave modes (clocks input). All timings are given for non-inverted serial clock polarity (TCR[TSCKP] = 0, RCR[RSCKP] = 0) and a non-inverted frame sync (TCR[TFSI] = 0, RCR[RFSI] = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timings remain valid by inverting the clock signal (I2S_BCLK) and/or the frame sync (I2S_FS) shown in the figures below.

Table 43. I2S master mode timing

Num	Description	Min.	Max.	Unit
	Operating voltage	2.7	3.6	V
S1	I2S_MCLK cycle time	40	—	ns
S2	I2S_MCLK pulse width high/low	45%	55%	MCLK period
S3	I2S_BCLK cycle time	80	—	ns
S4	I2S_BCLK pulse width high/low	45%	55%	BCLK period
S5	I2S_BCLK to I2S_FS output valid	—	15	ns
S6	I2S_BCLK to I2S_FS output invalid	0	—	ns
S7	I2S_BCLK to I2S_TXD valid	—	15	ns
S8	I2S_BCLK to I2S_TXD invalid	0	—	ns
S9	I2S_RXD/I2S_FS input setup before I2S_BCLK	15	—	ns
S10	I2S_RXD/I2S_FS input hold after I2S_BCLK	0	—	ns

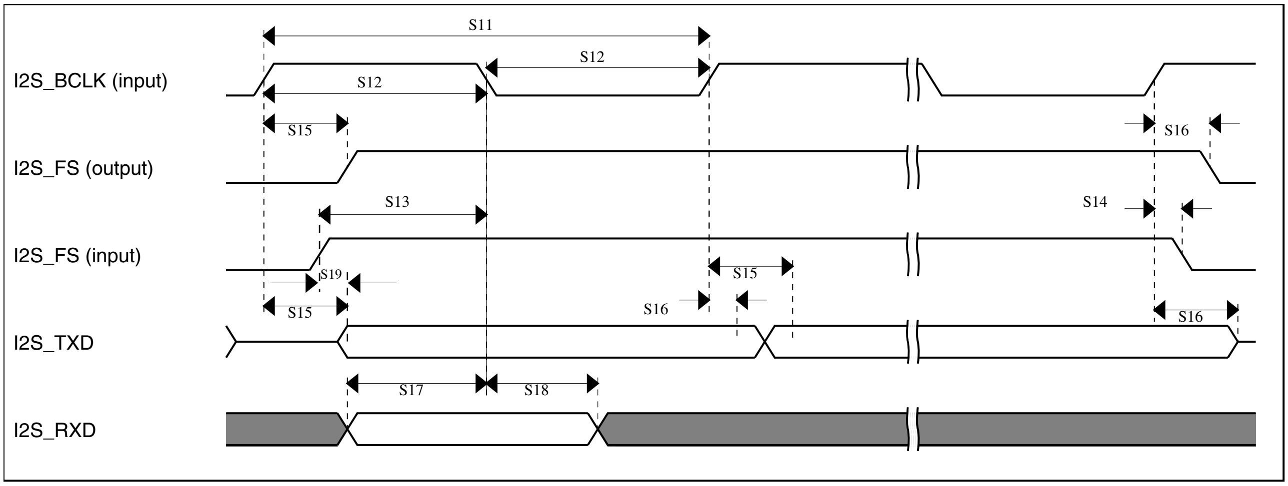


Figure 28. I²S timing — slave modes

3.8.10.1 Normal Run, Wait and Stop mode performance over the full operating voltage range

This section provides the operating performance over the full operating voltage for the device in Normal Run, Wait and Stop modes.

Table 45. I2S/SAI master mode timing

Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
S1	I2S_MCLK cycle time	40	—	ns
S2	I2S_MCLK (as an input) pulse width high/low	45%	55%	MCLK period
S3	I2S_TX_BCLK/I2S_RX_BCLK cycle time (output)	80	—	ns
S4	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low	45%	55%	BCLK period
S5	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output valid	—	15	ns
S6	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output invalid	-1	—	ns
S7	I2S_TX_BCLK to I2S_TXD valid	—	15	ns
S8	I2S_TX_BCLK to I2S_TXD invalid	0	—	ns
S9	I2S_RXD/I2S_RX_FS input setup before I2S_RX_BCLK	20.5	—	ns
S10	I2S_RXD/I2S_RX_FS input hold after I2S_RX_BCLK	0	—	ns

3.8.10.4.5 Small package marking

In an effort to save space, small package devices use special marking on the chip. These markings have the following format:

Q ## C F T PP

This table lists the possible values for each field in the part number for small packages (not all combinations are valid):

Field	Description	Values
Q	Qualification status	• M = Fully qualified, general market flow • P = Prequalification
##	Kinetis family	• 2# = K21/K22
C	Speed	• H = 120 MHz
F	Flash memory configuration	• K = 512 KB + Flex • 1 = 1 MB
T	Temperature range (°C)	• V = –40 to 105
PP	Package identifier	• LL = 100 LQFP • MC = 121 MAPBGA • LQ = 144 LQFP • MD = 144 MAPBGA • DC = 121 XFBGA

This tables lists some examples of small package marking along with the original part numbers:

Original part number	Alternate part number
MK21FN1M0VLQ12	M21H1VLQ
MK21FX512VMD12	M21HKVMD

3.8.10.5 Terminology and guidelines

3.8.10.5.1 Definition: Operating requirement

An *operating requirement* is a specified value or range of values for a technical characteristic that you must guarantee during operation to avoid incorrect operation and possibly decreasing the useful life of the chip.

3.8.10.5.1.1 Example

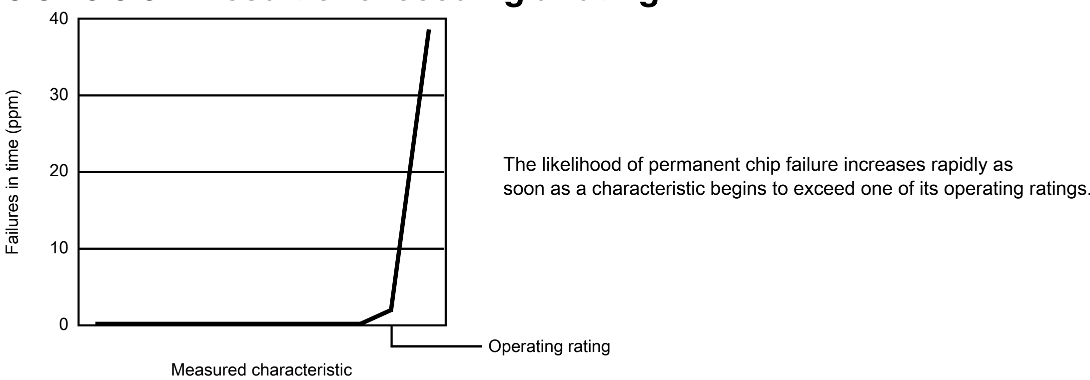
This is an example of an operating requirement:

3.8.10.5.4.1 Example

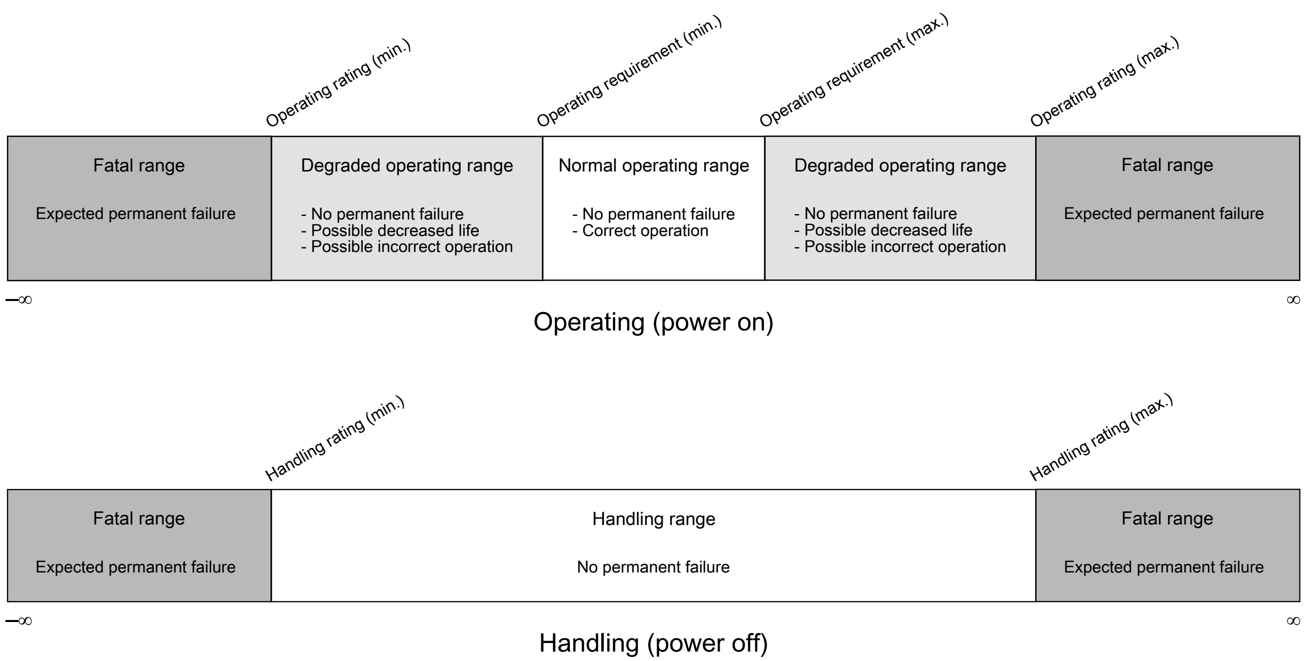
This is an example of an operating rating:

Symbol	Description	Min.	Max.	Unit
V_{DD}	1.0 V core supply voltage	–0.3	1.2	V

3.8.10.5.5 Result of exceeding a rating



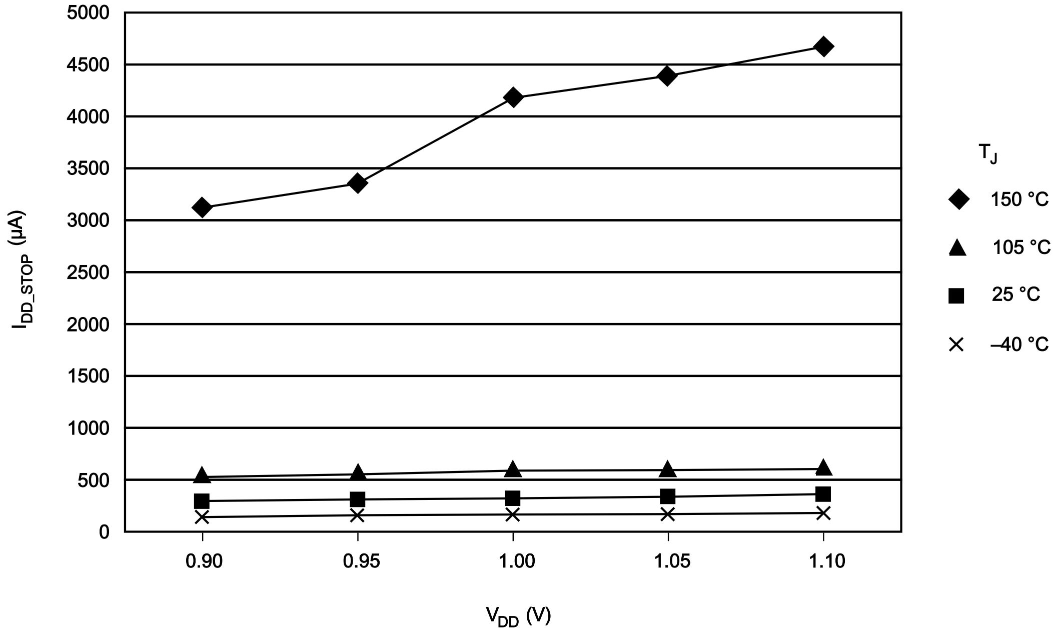
3.8.10.5.6 Relationship between ratings and operating requirements



3.8.10.5.7 Guidelines for ratings and operating requirements

Follow these guidelines for ratings and operating requirements:

- Never exceed any of the chip’s ratings.



3.8.10.5.9 Typical value conditions

Typical values assume you meet the following conditions (or other conditions as specified):

Symbol	Description	Value	Unit
T_A	Ambient temperature	25	°C
V_{DD}	3.3 V supply voltage	3.3	V

4 Dimensions

4.1 Obtaining package dimensions

Package dimensions are provided in package drawings.

To find a package drawing, go to freescale.com and perform a keyword search for the drawing's document number:

If you want the drawing for this package	Then use this document number
144-pin LQFP	98ASS23177W

Table continues on the next page...

144 MAP BGA	144 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
J5	50	PTA0	JTAG_TCLK/ SWD_CLK/ EZP_CLK		PTA0	UART0_ CTS_b	FTM0_CH5				JTAG_TCLK/ SWD_CLK	EZP_CLK
J6	51	PTA1	JTAG_TDI/ EZP_DI		PTA1	UART0_RX	FTM0_CH6				JTAG_TDI	EZP_DI
K6	52	PTA2	JTAG_TDO/ TRACE_ SWO/ EZP_DO		PTA2	UART0_TX	FTM0_CH7				JTAG_TDO/ TRACE_ SWO	EZP_DO
K7	53	PTA3	JTAG_TMS/ SWD_DIO		PTA3	UART0_ RTS_b	FTM0_CH0				JTAG_TMS/ SWD_DIO	
L7	54	PTA4/ LLWU_P3	NMI_b/ EZP_CS_b		PTA4/ LLWU_P3		FTM0_CH1				NMI_b	EZP_CS_b
M8	55	PTA5	DISABLED		PTA5	USB_CLKIN	FTM0_CH2		CMP2_OUT	I2S0_TX_ BCLK	JTAG_ TRST_b	
E7	56	VDD	VDD	VDD								
G7	57	VSS	VSS	VSS								
J7	58	PTA6	DISABLED		PTA6		FTM0_CH3		CLKOUT		TRACE_ CLKOUT	
J8	59	PTA7	ADC0_SE10	ADC0_SE10	PTA7		FTM0_CH4				TRACE_D3	
K8	60	PTA8	ADC0_SE11	ADC0_SE11	PTA8		FTM1_CH0			FTM1_QD_ PHA	TRACE_D2	
L8	61	PTA9	DISABLED		PTA9		FTM1_CH1			FTM1_QD_ PHB	TRACE_D1	
M9	62	PTA10	DISABLED		PTA10		FTM2_CH0			FTM2_QD_ PHA	TRACE_D0	
L9	63	PTA11	DISABLED		PTA11		FTM2_CH1		I2C2_SDA	FTM2_QD_ PHB		
K9	64	PTA12	CMP2_IN0	CMP2_IN0	PTA12	CAN0_TX	FTM1_CH0		I2C2_SCL	I2S0_TXD0	FTM1_QD_ PHA	
J9	65	PTA13/ LLWU_P4	CMP2_IN1	CMP2_IN1	PTA13/ LLWU_P4	CAN0_RX	FTM1_CH1		I2C2_SDA	I2S0_TX_FS	FTM1_QD_ PHB	
L10	66	PTA14	DISABLED		PTA14	SPI0_PCS0	UART0_TX		I2C2_SCL	I2S0_RX_ BCLK	I2S0_TXD1	
L11	67	PTA15	DISABLED		PTA15	SPI0_SCK	UART0_RX			I2S0_RXD0		
K10	68	PTA16	DISABLED		PTA16	SPI0_SOUT	UART0_ CTS_b			I2S0_RX_FS	I2S0_RXD1	
K11	69	PTA17	ADC1_SE17	ADC1_SE17	PTA17	SPI0_SIN	UART0_ RTS_b			I2S0_MCLK		
E8	70	VDD	VDD	VDD								
G8	71	VSS	VSS	VSS								
M12	72	PTA18	EXTAL0	EXTAL0	PTA18		FTM0_FLT2	FTM_CLKIN0				
M11	73	PTA19	XTAL0	XTAL0	PTA19		FTM1_FLT0	FTM_CLKIN1		LPTMR0_ ALT1		
L12	74	RESET_b	RESET_b	RESET_b								

144 MAP BGA	144 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
A5	127	PTD0/ LLWU_P12	DISABLED		PTD0/ LLWU_P12	SPI0_PCS0	UART2_ RTS_b	FTM3_CH0	FB_ALE/ FB_CS1_b/ FB_TS_b			
D4	128	PTD1	ADC0_SE5b	ADC0_SE5b	PTD1	SPI0_SCK	UART2_ CTS_b	FTM3_CH1	FB_CS0_b			
C4	129	PTD2/ LLWU_P13	DISABLED		PTD2/ LLWU_P13	SPI0_SOUT	UART2_RX	FTM3_CH2	FB_AD4		I2C0_SCL	
B4	130	PTD3	DISABLED		PTD3	SPI0_SIN	UART2_TX	FTM3_CH3	FB_AD3		I2C0_SDA	
A4	131	PTD4/ LLWU_P14	DISABLED		PTD4/ LLWU_P14	SPI0_PCS1	UART0_ RTS_b	FTM0_CH4	FB_AD2	EWM_IN		
A3	132	PTD5	ADC0_SE6b	ADC0_SE6b	PTD5	SPI0_PCS2	UART0_ CTS_b	FTM0_CH5	FB_AD1	EWM_OUT_ b		
A2	133	PTD6/ LLWU_P15	ADC0_SE7b	ADC0_SE7b	PTD6/ LLWU_P15	SPI0_PCS3	UART0_RX	FTM0_CH6	FB_AD0	FTM0_FLT0		
M10	134	VSS	VSS	VSS								
F8	135	VDD	VDD	VDD								
A1	136	PTD7	DISABLED		PTD7	CMT_IRO	UART0_TX	FTM0_CH7		FTM0_FLT1		
C9	137	PTD8	DISABLED		PTD8	I2C0_SCL	UART5_RX			FB_A16		
B9	138	PTD9	DISABLED		PTD9	I2C0_SDA	UART5_TX			FB_A17		
B3	139	PTD10	DISABLED		PTD10		UART5_ RTS_b			FB_A18		
B2	140	PTD11	DISABLED		PTD11	SPI2_PCS0	UART5_ CTS_b	SDHC0_ CLKIN		FB_A19		
B1	141	PTD12	DISABLED		PTD12	SPI2_SCK	FTM3_FLT0	SDHC0_D4		FB_A20		
C3	142	PTD13	DISABLED		PTD13	SPI2_SOUT		SDHC0_D5		FB_A21		
C2	143	PTD14	DISABLED		PTD14	SPI2_SIN		SDHC0_D6		FB_A22		
C1	144	PTD15	DISABLED		PTD15	SPI2_PCS1		SDHC0_D7		FB_A23		
M5	—	NC	NC	NC								
A10	—	NC	NC	NC								
B10	—	NC	NC	NC								
C10	—	NC	NC	NC								

5.2 K21 Pinouts

The below figure shows the pinout diagram for the devices supported by this document. Many signals may be multiplexed onto a single pin. To determine what signals can be used on which pin, see the previous section.