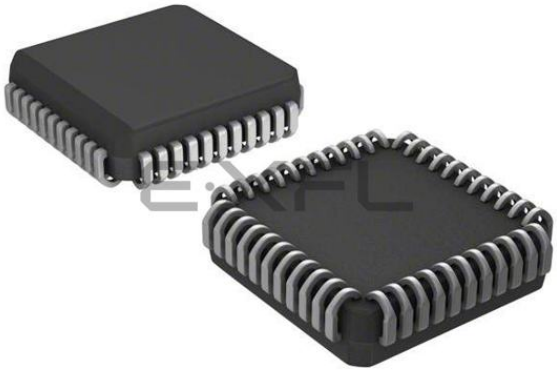

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Applications of "Embedded - Microcontrollers"

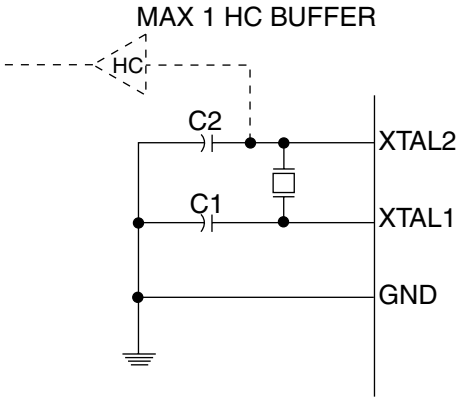
Details	
Product Status	Obsolete
Core Processor	AVR
Core Size	8-Bit
Speed	4MHz
Connectivity	SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	32
Program Memory Size	8KB (4K x 16)
Program Memory Type	FLASH
EEPROM Size	512 x 8
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 6V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C
Mounting Type	Surface Mount
Package / Case	44-LCC (J-Lead)
Supplier Device Package	44-PLCC (16.6x16.6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/at90ls8535-4jc

Clock Options

Crystal Oscillator

XTAL1 and XTAL2 are input and output, respectively, of an inverting amplifier which can be configured for use as an on-chip oscillator, as shown in Figure 2. Either a quartz crystal or a ceramic resonator may be used.

Figure 2. Oscillator Connections

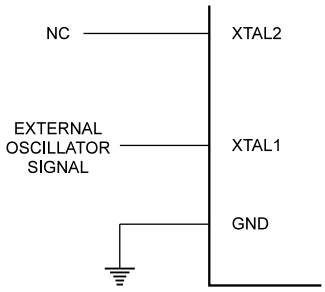


Note: When using the MCU Oscillator as a clock for an external device, an HC buffer should be connected as indicated in the figure.

External Clock

To drive the device from an external clock source, XTAL2 should be left unconnected while XTAL1 is driven as shown in Figure 3.

Figure 3. External Clock Drive Configuration

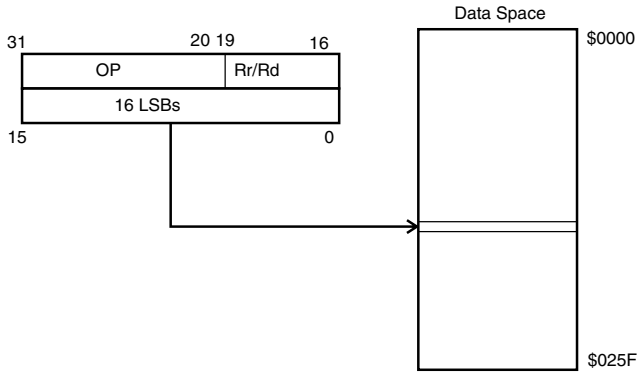


Timer Oscillator

For the Timer Oscillator pins, TOSC1 and TOSC2, the crystal is connected directly between the pins. No external capacitors are needed. The oscillator is optimized for use with a 32,768 Hz watch crystal. Applying an external clock source to TOSC1 is not recommended.

Data Direct

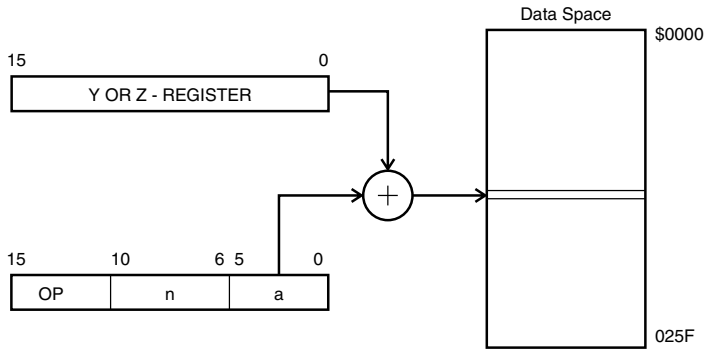
Figure 12. Direct Data Addressing



A 16-bit data address is contained in the 16 LSBs of a 2-word instruction. Rd/Rr specify the destination or source register.

Data Indirect with Displacement

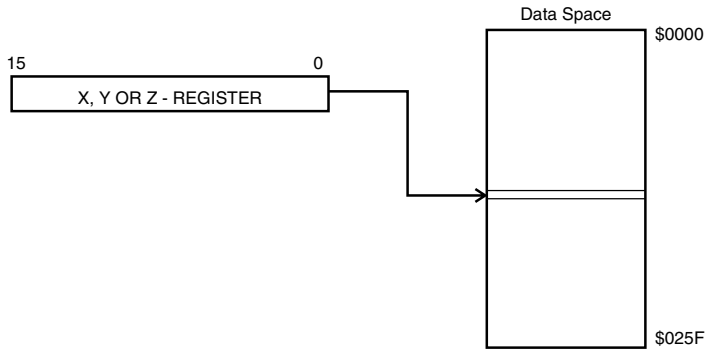
Figure 13. Data Indirect with Displacement



Operand address is the result of the Y- or Z-register contents added to the address contained in six bits of the instruction word.

Data Indirect

Figure 14. Data Indirect Addressing

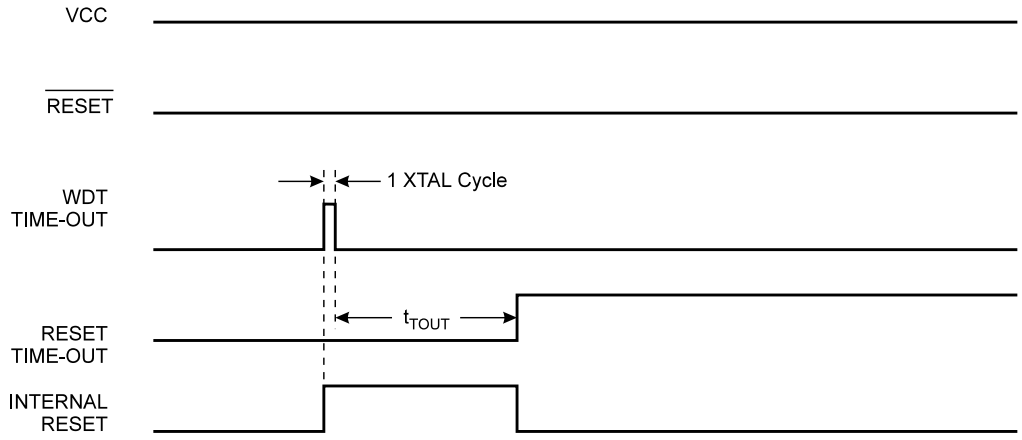


Operand address is the contents of the X-, Y-, or the Z-register.

Watchdog Reset

When the Watchdog times out, it will generate a short reset pulse of 1 XTAL cycle duration. On the falling edge of this pulse, the delay timer starts counting the Time-out period t_{TOUT}. Refer to page 49 for details on operation of the Watchdog.

Figure 27. Watchdog Reset during Operation



MCU Status Register – MCUSR

The MCU Status Register provides information on which reset source caused an MCU reset.

Bit	7	6	5	4	3	2	1	0	
$34 ($54)	–	–	–	–	–	–	EXTRF	PORF	MCUSR
Read/Write	R	R	R	R	R	R	R/W	R/W	
Initial Value	0	0	0	0	0	0	See Bit Description		

- **Bits 7..2 – Res: Reserved Bits**

These bits are reserved bits in the AT90S8535 and always read as zero.

- **Bit 1 – EXTRF: External Reset Flag**

After a power-on reset, this bit is undefined (X). It can only be set by an External Reset. A Watchdog Reset will leave this bit unchanged. The bit is cleared by writing a logical zero to the bit.

- **Bit 0 – PORF: Power-on Reset Flag**

This bit is only set by a Power-on Reset. A Watchdog Reset or an External Reset will leave this bit unchanged. The bit is cleared by writing a logical zero to the bit.

To summarize, Table 5 shows the value of these two bits after the three modes of reset.

Table 5. PORF and EXTRF Values after Reset

Reset Source	EXTRF	PORF
Power-on Reset	Undefined	1
External Reset	1	Unchanged
Watchdog Reset	Unchanged	Unchanged

To make use of these bits to identify a reset condition, the user software should clear both the PORF and EXTRF bits as early as possible in the program. Checking the PORF and EXTRF values is done before the bits are cleared. If the bit is cleared before an External or Watchdog Reset occurs, the source of reset can be found by using Table 6.

sponding interrupt of External Interrupt Request 0 is executed from program memory address $001. See also “External Interrupts.”

- **Bits 5.0 – Res: Reserved Bits**

These bits are reserved bits in the AT90S8535 and always read as zero.

General Interrupt Flag Register – GIFR

Bit	7	6	5	4	3	2	1	0	
$3A ($5A)	INTF1	INTF0	–	–	–	–	–	–	GIFR
Read/Write	R/W	R/W	R	R	R	R	R	R	
Initial Value	0	0	0	0	0	0	0	0	

- **Bit 7 – INTF1: External Interrupt Flag1**

When an edge or logical change on the INT1 pin triggers an interrupt request, INTF1 becomes set (one). This flag is always cleared (0) when the pin is configured for low-level interrupts, as the state of a low-level interrupt can be determined by reading the PIN register.

If the I-bit in SREG and the INT1 bit in GIMSK are set (one), the MCU will jump to the interrupt address $002. For edge and logic change interrupts, this flag is cleared when the interrupt routine is executed. Alternatively, the flag can be cleared by writing a logical “1” to it.

- **Bit 6 – INTF0: External Interrupt Flag0**

When an edge or logical change on the INT0 pin triggers an interrupt request, INTF0 becomes set (one). This flag is always cleared (0) when the pin is configured for low-level interrupts, as the state of a low-level interrupt can be determined by reading the PIN register.

If the I-bit in SREG and the INT0 bit in GIMSK are set (one), the MCU will jump to the interrupt address $001. For edge and logic change interrupts, this flag is cleared when the interrupt routine is executed. Alternatively, the flag can be cleared by writing a logical “1” to it.

- **Bits 5..0 – Res: Reserved Bits**

These bits are reserved bits in the AT90S8535 and always read as zero.

Timer/Counter Interrupt Mask Register – TIMSK

Bit	7	6	5	4	3	2	1	0	
$39 ($59)	OCIE2	TOIE2	TICIE1	OCIE1A	OCIE1B	TOIE1	–	TOIE0	TIMSK
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R	R/W	
Initial Value	0	0	0	0	0	0	0	0	

- **Bit 7 – OCIE2: Timer/Counter2 Output Compare Match Interrupt Enable**

When the OCIE2 bit is set (one) and the I-bit in the Status Register is set (one), the Timer/Counter2 Compare Match interrupt is enabled. The corresponding interrupt (at vector $003) is executed if a compare match in Timer/Counter2 occurs (i.e., when the OCF2 bit is set in the Timer/Counter Interrupt Flag Register [TIFR]).

- **Bit 6 – TOIE2: Timer/Counter2 Overflow Interrupt Enable**

When the TOIE2 bit is set (one) and the I-bit in the Status Register is set (one), the Timer/Counter2 Overflow interrupt is enabled. The corresponding interrupt (at vector $004) is executed if an overflow in Timer/Counter2 occurs (i.e., when the TOV2 bit is set in the Timer/Counter Interrupt Flag Register [TIFR]).

The clock source for Timer/Counter2 prescaler is named PCK2. PCK2 is by default connected to the main system clock (CK). By setting the AS2 bit in ASSR, Timer/Counter2 prescaler is asynchronously clocked from the PC6(TOSC1) pin. This enables use of Timer/Counter2 as a Real-time Clock (RTC). When AS2 is set, pins PC6(TOSC1) and PC7(TOSC2) are disconnected from Port C. A crystal can then be connected between the PC6(TOSC1) and PC7(TOSC2) pins to serve as an independent clock source for Timer/Counter2. The oscillator is optimized for use with a 32.768 kHz crystal. Applying an external clock source to TOSC1 is not recommended.

8-bit Timer/Counter0

Figure 30 shows the block diagram for Timer/Counter0.

The 8-bit Timer/Counter0 can select clock source from CK, prescaled CK or an external pin. In addition, it can be stopped as described in the specification for the Timer/Counter0 Control Register (TCCR0). The overflow status flag is found in the Timer/Counter Interrupt Flag Register (TIFR). Control signals are found in the Timer/Counter0 Control Register (TCCR0). The interrupt enable/disable settings for Timer/Counter0 are found in the Timer/Counter Interrupt Mask Register (TIMSK).

When Timer/Counter0 is externally clocked, the external signal is synchronized with the oscillator frequency of the CPU. To assure proper sampling of the external clock, the minimum time between two external clock transitions must be at least one internal CPU clock period. The external clock signal is sampled on the rising edge of the internal CPU clock.

The 8-bit Timer/Counter0 features both a high-resolution and a high-accuracy usage with the lower prescaling opportunities. Similarly, the high prescaling opportunities make the Timer/Counter0 useful for lower speed functions or exact timing functions with infrequent actions.

Figure 30. Timer/Counter0 Block Diagram

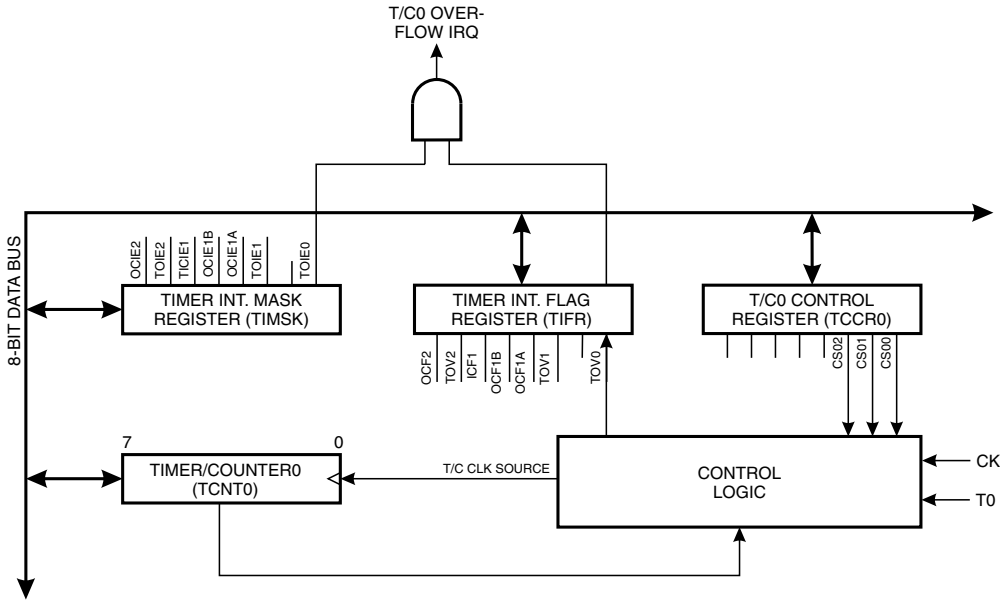
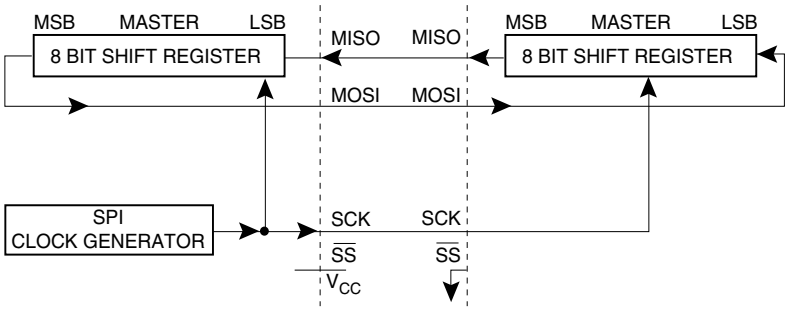


Figure 38. SPI Master-slave Interconnection



The system is single-buffered in the transmit direction and double-buffered in the receive direction. This means that bytes to be transmitted cannot be written to the SPI Data Register before the entire shift cycle is completed. When receiving data, however, a received byte must be read from the SPI Data Register before the next byte has been completely shifted in. Otherwise, the first byte is lost.

When the SPI is enabled, the data direction of the MOSI, MISO, SCK and $\overline{SS}$ pins is overridden according to Table 22.

Table 22. SPI Pin Overrides

Pin	Direction, Master SPI	Direction, Slave SPI
MOSI	User Defined	Input
MISO	Input	User Defined
SCK	User Defined	Input
$\overline{SS}$	User Defined	Input

Note: See “Alternate Functions of Port B” on page 79 for a detailed description of how to define the direction of the user-defined SPI pins.

Analog-to-Digital Converter

Feature list

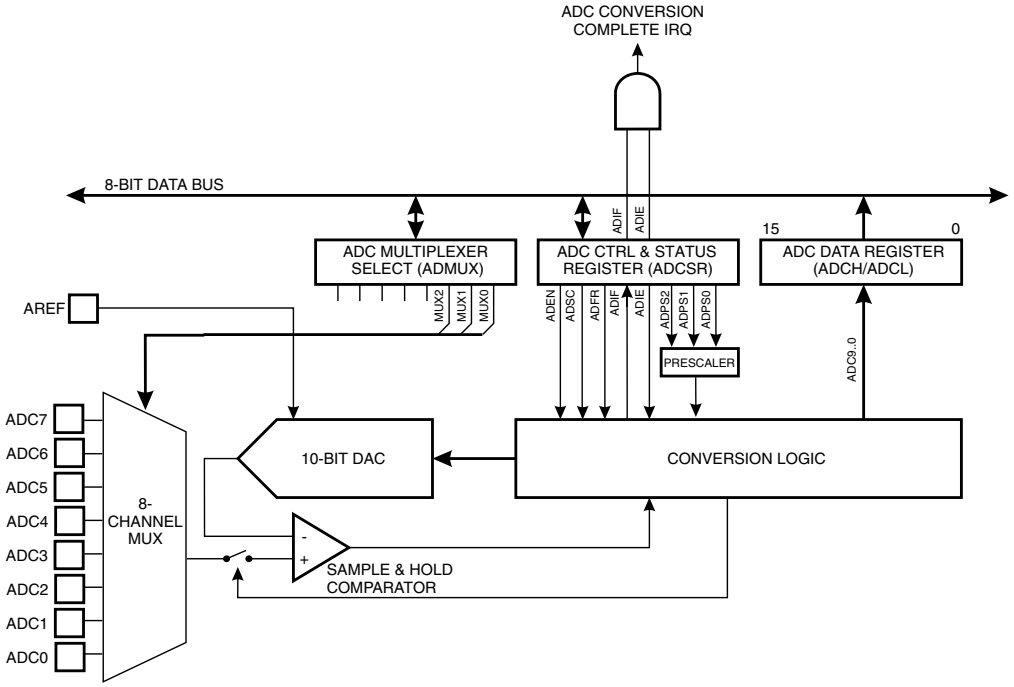
- **10-bit Resolution**
- **0.5 LSB Integral Non-linearity**
- **±2 LSB Absolute Accuracy**
- **65 - 260 µs Conversion Time**
- **Up to 15 kSPS at Maximum Resolution**
- **8 Multiplexed Input Channels**
- **Rail-to-Rail Input Range**
- **Free Running or Single Conversion Mode**
- **Interrupt on ADC Conversion Complete**
- **Sleep Mode Noise Canceler**

The AT90S8535 features a 10-bit successive approximation ADC. The ADC is connected to an 8-channel Analog Multiplexer that allows each pin of Port A to be used as an input for the ADC. The ADC contains a Sample and Hold Amplifier that ensures that the input voltage to the ADC is held at a constant level during conversion. A block diagram of the ADC is shown in Figure 45.

The ADC has two separate analog supply voltage pins, AVCC and AGND. AGND must be connected to GND and the voltage on AV_{CC} must not differ more than ±0.3V from V_{CC}. See “ADC Noise Canceling Techniques” on page 74 on how to connect these pins.

An external reference voltage must be applied to the AREF pin. This voltage must be in the range 2V - AV_{CC}.

Figure 45. Analog-to-Digital Converter Block Schematic



higher sampling rate. See “ADC Characteristics” on page 75 for more details. The ADC module contains a prescaler, which divides the system clock to an acceptable ADC clock frequency.

The ADPS2..0 bits in ADCSR are used to generate a proper ADC clock input frequency from any CPU frequency above 100 kHz. The prescaler starts counting from the moment the ADC is switched on by setting the ADEN bit in ADCSR. The prescaler keeps running for as long as the ADEN bit is set and is continuously reset when ADEN is low.

When initiating a conversion by setting the ADSC bit in ADCSR, the conversion starts at the following rising edge of the ADC clock cycle.

A normal conversion takes 13 ADC clock cycles. In certain situations, the ADC needs more clock cycles for initialization and to minimize offset errors. Extended conversions take 25 ADC clock cycles and occur as the first conversion after the ADC is switched on (ADEN in ADCSR is set).

The actual sample-and-hold takes place 1.5 ADC clock cycles after the start of a normal conversion and 13.5 ADC clock cycles after the start of an extended conversion. When a conversion is complete, the result is written to the ADC data registers and ADIF is set. In Single Conversion Mode, ADSC is cleared simultaneously. The software may then set ADSC again and a new conversion will be initiated on the first rising ADC clock edge. In Free Running Mode, a new conversion will be started immediately after the conversion completes, while ADSC remains high. Using Free Running Mode and an ADC clock frequency of 200 kHz gives the lowest conversion time with a maximum resolution, 65 µs, equivalent to 15 kSPS. For a summary of conversion times, see Table 26.

Figure 47. ADC Timing Diagram, Extended Conversion (Single Conversion Mode)

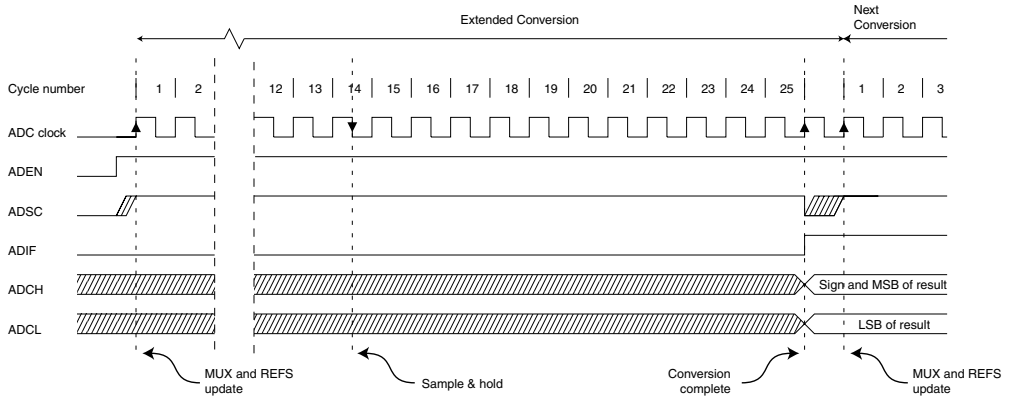


Figure 48. ADC Timing Diagram, Single Conversion

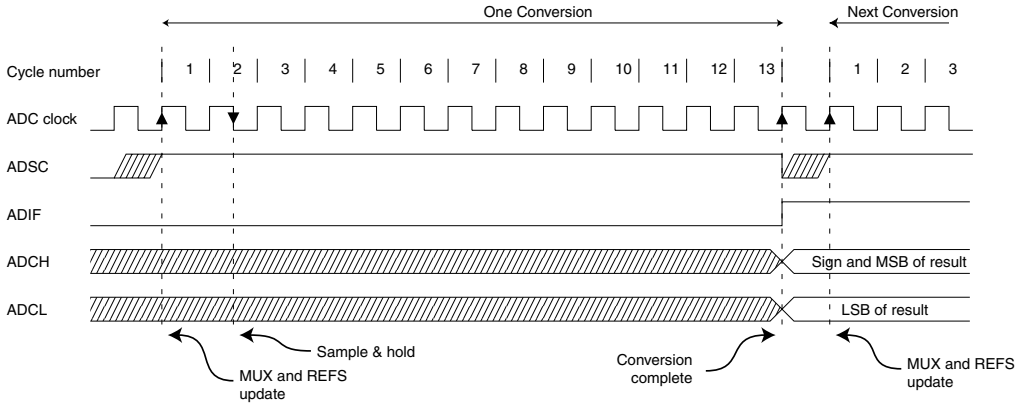


Figure 49. ADC Timing Diagram, Free Running Conversion

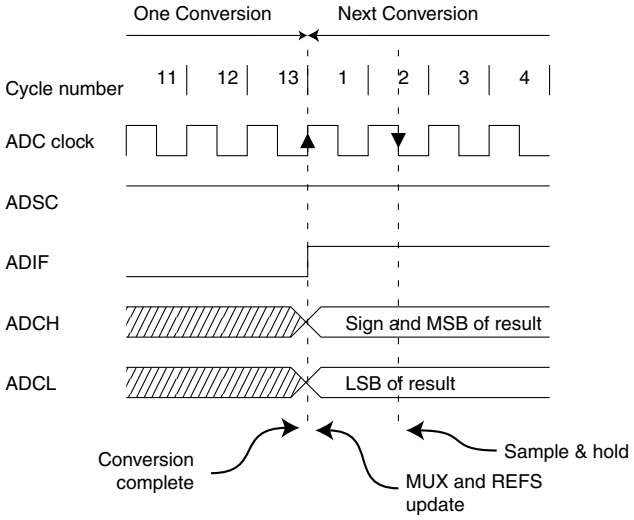


Table 26. ADC Conversion Time

Condition	Sample and Hold (Cycles from Start of Conversion)	Conversion Time (Cycles)	Conversion Time (µs)
Extended Conversion	14	25	125 - 500
Normal Conversion	14	26	130 - 520

ADC Noise Canceler Function

The ADC features a noise canceler that enables conversion during Idle Mode to reduce noise induced from the CPU core. To make use of this feature, the following procedure should be used:

1. Make sure that the ADC is enabled and is not busy converting. Single Conversion Mode must be selected and the ADC conversion complete interrupt must be enabled.

   ADEN = 1

   ADSC = 0

   ADFR = 0

   ADIE = 1

2. Enter Idle Mode. The ADC will start a conversion once the CPU has been halted.
3. If no other interrupts occur before the ADC conversion completes, the ADC interrupt will wake up the MCU and execute the ADC Conversion Complete Interrupt routine.

ADC Multiplexer Select Register – ADMUX

Bit	7	6	5	4	3	2	1	0	
$07 ($27)	–	–	–	–	–	MUX2	MUX1	MUX0	ADMUX
Read/Write	R	R	R	R	R	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

- **Bits 7..3 – Res: Reserved Bits**

These bits are reserved bits in the AT90S8535 and always read as zero.

- **Bits 2..0 – MUX2..MUX0: Analog Channel Select Bits 2-0**

The value of these three bits selects which analog input ADC7..0 is connected to the ADC. See Table 27 for details.

If these bits are changed during a conversion, the change will not go into effect until this conversion is complete (ADIF in ADCSR is set).

Table 27. Input Channel Selections

MUX2.0	Single-ended Input
000	ADC0
001	ADC1
010	ADC2
011	ADC3
100	ADC4
101	ADC5
110	ADC6
111	ADC7

ADC Control and Status Register – ADCSR

Bit	7	6	5	4	3	2	1	0	
$06 ($26)	ADEN	ADSC	ADFR	ADIF	ADIE	ADPS2	ADPS1	ADPS0	ADCSR
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

- **Bit 7 – ADEN: ADC Enable**

Writing a logical “1” to this bit enables the ADC. By clearing this bit to zero, the ADC is turned off. Turning the ADC off while a conversion is in progress will terminate this conversion.

- **Bit 6 – ADSC: ADC Start Conversion**

In Single Conversion Mode, a logical “1” must be written to this bit to start each conversion. In Free Running Mode, a logical “1” must be written to this bit to start the first conversion. The first time ADSC has been written after the ADC has been enabled or if ADSC is written at the same time as the ADC is enabled, an extended conversion will precede the initiated conversion. This extended conversion performs initialization of the ADC.

ADSC will read as one as long as a conversion is in progress. When the conversion is complete, it returns to zero. When a extended conversion precedes a real conversion, ADSC will stay high until the real conversion completes. Writing a “0” to this bit has no effect.

- **Bit 5 – ADFR: ADC Free Running Select**

When this bit is set (one), the ADC operates in Free Running Mode. In this mode, the ADC samples and updates the data registers continuously. Clearing this bit (zero) will terminate Free Running Mode.

- **Bit 4 – ADIF: ADC Interrupt Flag**

This bit is set (one) when an ADC conversion completes and the data registers are updated. The ADC Conversion Complete interrupt is executed if the ADIE bit and the I-bit in SREG are set (one). ADIF is cleared by hardware when executing the corresponding interrupt handling vector. Alternatively, ADIF is cleared by writing a logical “1” to the flag. Beware that if doing a read-modify-write on ADCSR, a pending interrupt can be disabled. This also applies if the SBI and CBI instructions are used.

- **Bit 3 – ADIE: ADC Interrupt Enable**

When this bit is set (one) and the I-bit in SREG is set (one), the ADC Conversion Complete interrupt is activated.

- **Bits 2..0 – ADPS2..ADPS0: ADC Prescaler Select Bits**

These bits determine the division factor between the XTAL frequency and the input clock to the ADC.

Table 28. ADC Prescaler Selections

ADPS2	ADPS1	ADPS0	Division Factor
0	0	0	2
0	0	1	2
0	1	0	4
0	1	1	8
1	0	0	16
1	0	1	32
1	1	0	64
1	1	1	128

ADC Data Register – ADCL AND ADCH

Bit	15	14	13	12	11	10	9	8	
$05 ($25)	–	–	–	–	–	–	ADC9	ADC8	ADCH
$04 ($24)	ADC7	ADC6	ADC5	ADC4	ADC3	ADC2	ADC1	ADC0	ADCL
	7	6	5	4	3	2	1	0	
Read/Write	R	R	R	R	R	R	R	R	
	R	R	R	R	R	R	R	R	
Initial Value	0	0	0	0	0	0	0	0	
	0	0	0	0	0	0	0	0	

When an ADC conversion is complete, the result is found in these two registers.

When ADCL is read, the ADC Data Register is not updated until ADCH is read. Consequently, it is essential that both registers are read and that ADCL is read before ADCH.

allows analog signals that are close to $V_{CC}/2$ to be present during power-down without causing excessive power consumption.

- **AIN0 – Port B, Bit 2**

AIN0, Analog Comparator Positive Input. When configured as an input (DDB2 is cleared [zero]) and with the internal MOS pull-up resistor switched off (PB2 is cleared [zero]), this pin also serves as the positive input of the on-chip Analog Comparator. During Power-down mode, the Schmitt trigger of the digital input is disconnected. This allows analog signals that are close to $V_{CC}/2$ to be present during power-down without causing excessive power consumption.

- **T1 – Port B, Bit 1**

T1, Timer/Counter1 counter source. See the timer description for further details.

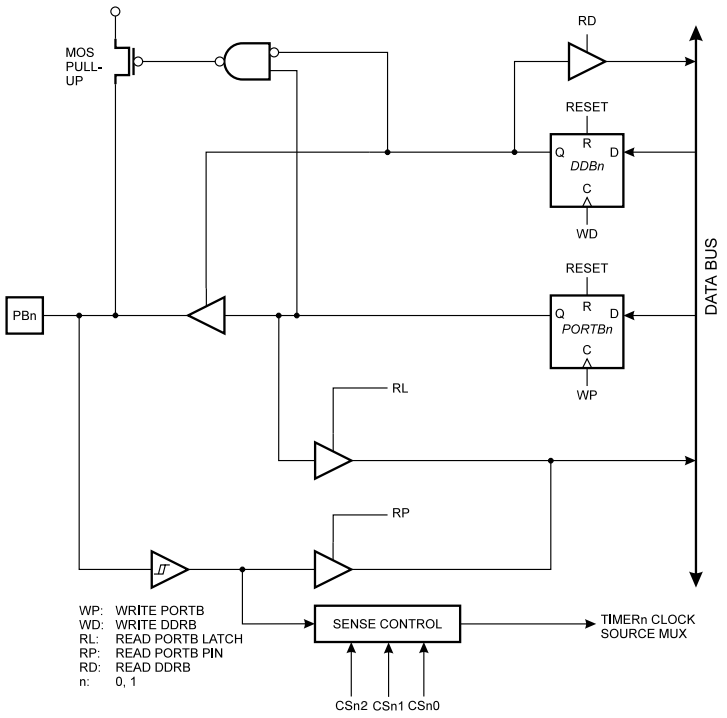
- **T0 – Port B, Bit 0**

T0: Timer/Counter0 counter source. See the timer description for further details.

Port B Schematics

Note that all port pins are synchronized. The synchronization latches are, however, not shown in the figures.

Figure 52. Port B Schematic Diagram (Pins PB0 and PB1)



Memory Programming

Program and Data Memory Lock Bits

The AT90S8535 MCU provides two Lock bits that can be left unprogrammed (“1”) or can be programmed (“0”) to obtain the additional features listed in Table 35. The Lock bits can only be erased with the Chip Erase command.

Table 35. Lock Bit Protection Modes

Memory Lock Bits			
Mode	**LB1**	**LB2**	**Protection Type**
1	1	1	No memory lock features enabled.
2	0	1	Further programming of the Flash and EEPROM is disabled.(1)
3	0	0	Same as mode 2 and verify is also disabled.

Note: 1. In Parallel Mode, further programming of the Fuse bits is also disabled. Program the Fuse bits before programming the Lock bits.

Fuse Bits

The AT90S8535 has two Fuse bits, SPIEN and FSTRT.

- When the SPIEN Fuse is programmed (“0”), Serial Program and Data Downloading is enabled. Default value is programmed (“0”). The SPIEN Fuse is not accessible in Serial Programming Mode.
- When the FSTRT Fuse is programmed (“0”), the short start-up time is selected. Default value is unprogrammed (“1”).

The status of the Fuse bits is not affected by Chip Erase.

Signature Bytes

All Atmel microcontrollers have a three-byte signature code that identifies the device. This code can be read in both Serial and Parallel modes. The three bytes reside in a separate address space.

1. $000: $1E (indicates manufactured by Atmel)
2. $001: $93 (indicates 8K bytes Flash memory)
3. $002: $03 (indicates AT90S8535 device when signature byte $001 is $93)

Note: 1. When both Lock bits are programmed (lock mode 3), the signature bytes cannot be read in Serial Mode. Reading the signature bytes will return: $00, $01 and $02.

Programming the Flash and EEPROM

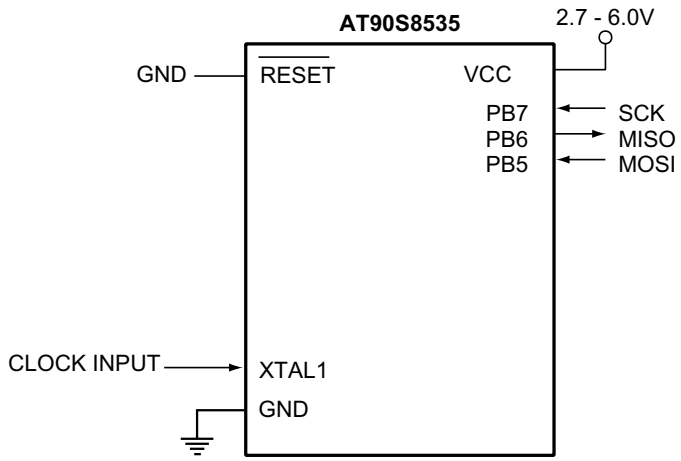
Atmel’s AT90S8535 offers 8K bytes of in-system reprogrammable Flash program memory and 512 bytes of EEPROM data memory.

The AT90S8535 is shipped with the On-chip Flash program and EEPROM data memory arrays in the erased state (i.e., contents = $FF) and ready to be programmed. This device supports a high-voltage (12V) Parallel Programming Mode and a low-voltage Serial Programming Mode. The +12V is used for programming enable only and no current of significance is drawn by this pin. The Serial Programming Mode provides a convenient way to download program and data into the AT90S8535 inside the user’s system.

The program and data memory arrays on the AT90S8535 are programmed byte-by-byte in either programming mode. For the EEPROM, an auto-erase cycle is provided within the self-timed write instruction in the Serial Programming Mode.

During programming, the supply voltage must be in accordance with Table 36.

Figure 71. Serial Programming and Verify



For the EEPROM, an auto-erase cycle is provided within the self-timed write instruction and there is no need to first execute the Chip Erase instruction. The Chip Erase instruction turns the content of every memory location in both the program and EEPROM arrays into $FF.

The program and EEPROM memory arrays have separate address spaces: $0000 to $0FFF for program memory and $0000 to $01FF for EEPROM memory.

Either an external clock is supplied at pin XTAL1 or a crystal needs to be connected across pins XTAL1 and XTAL2. The minimum low and high periods for the serial clock (SCK) input are defined as follows:

Low: > 2 XTAL1 clock cycles

High: > 2 XTAL1 clock cycles

Serial Programming Algorithm

When writing serial data to the AT90S8535, data is clocked on the rising edge of SCK.

When reading data from the AT90S8535, data is clocked on the falling edge of SCK. See Figure 72, Figure 73 and Table 43 for timing details.

To program and verify the AT90SS8535 in the Serial Programming Mode, the following sequence is recommended (see 4-byte instruction formats in Table 42):

1. Power-up sequence:

   Apply power between V_{CC} and GND while $\overline{\text{RESET}}$ and SCK are set to “0”. If a crystal is not connected across pins XTAL1 and XTAL2, apply a clock signal to the XTAL1 pin. In some systems, the programmer cannot guarantee that SCK is held low during power-up. In this case, $\overline{\text{RESET}}$ must be given a positive pulse of at least two XTAL1 cycles duration after SCK has been set to “0”.
2. Wait for at least 20 ms and enable serial programming by sending the Programming Enable serial instruction to the MOSI (PB5) pin.
3. The serial programming instructions will not work if the communication is out of synchronization. When in sync, the second byte ($53) will echo back when issuing the third byte of the Programming Enable instruction. Whether the echo is correct or not, all four bytes of the instruction must be transmitted. If the $53 did not echo back, give SCK a positive pulse and issue a new Programming Enable instruction. If the $53 is not seen within 32 attempts, there is no functional device connected.

Figure 78. Idle Supply Current vs. V_{CC}

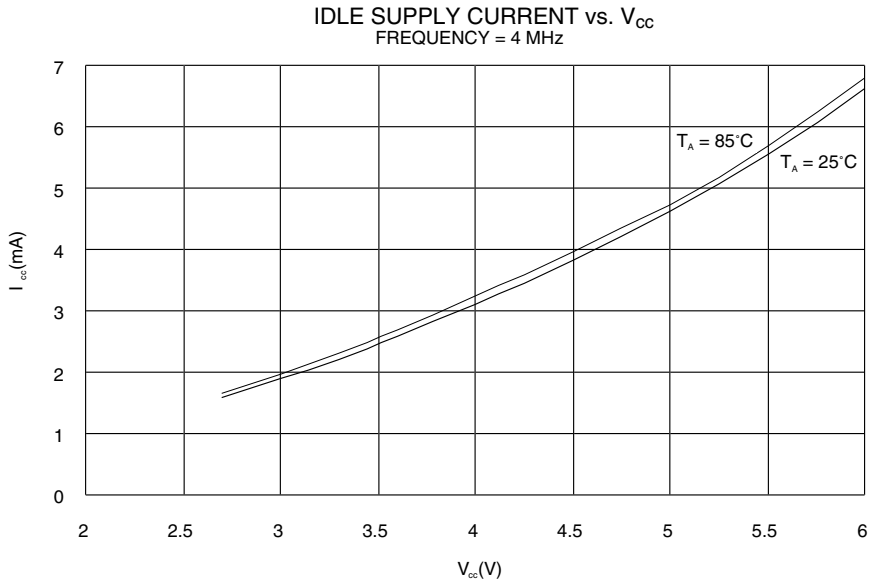


Figure 79. Power-down Supply Current vs. V_{CC}

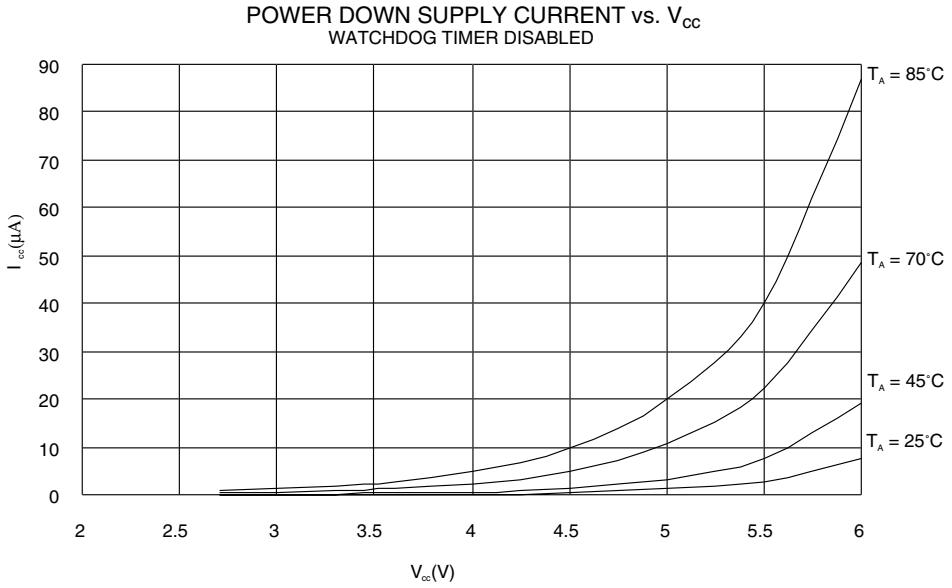


Figure 90. I/O Pin Source Current vs. Output Voltage

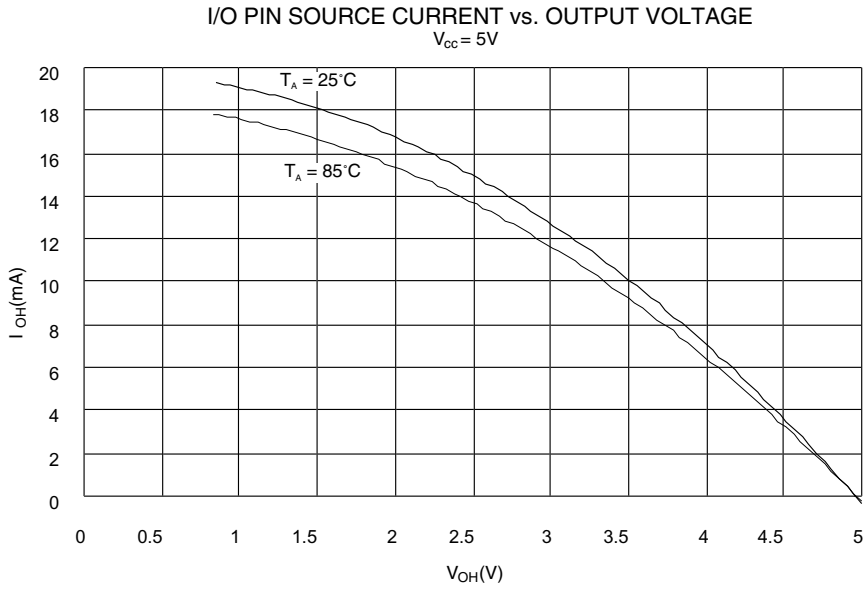


Figure 91. I/O Pin Sink Current vs. Output Voltage

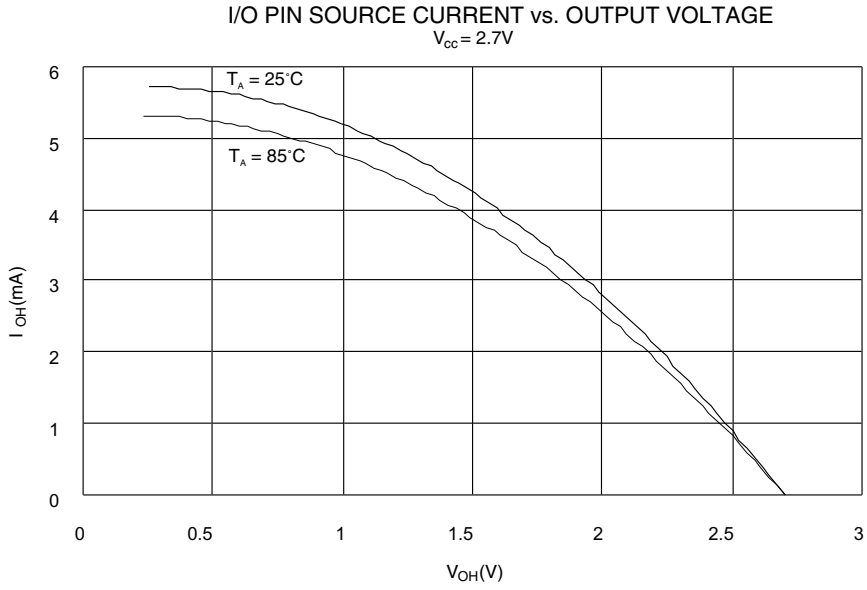


Figure 92. I/O Pin Source Current vs. Output Voltage

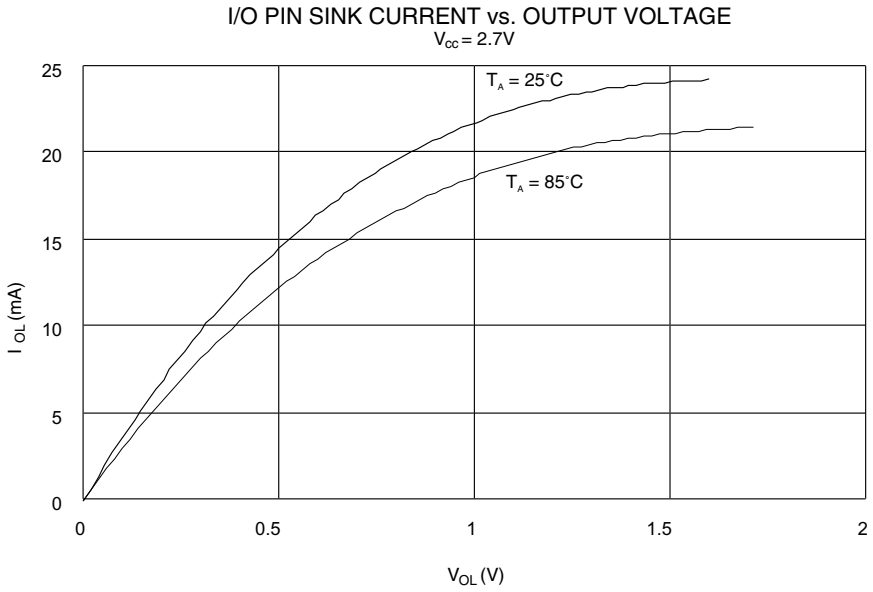


Figure 93. I/O Pin Input Threshold Voltage vs. V_{CC}

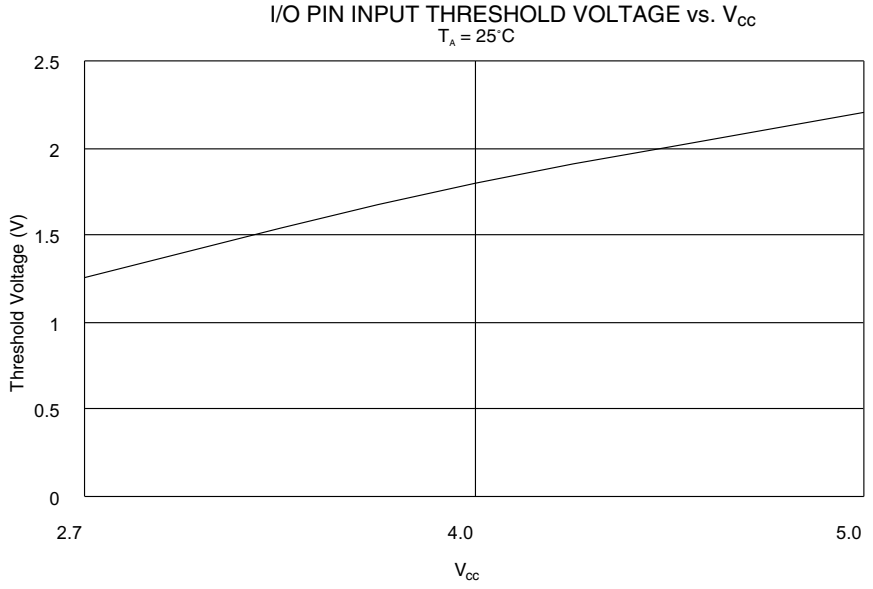
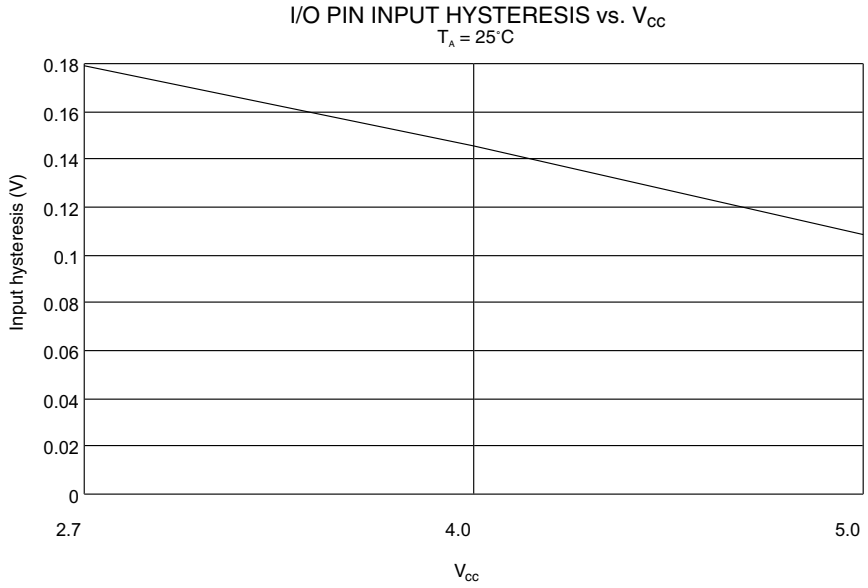


Figure 94. I/O Pin Input Hysteresis vs. V_{CC}

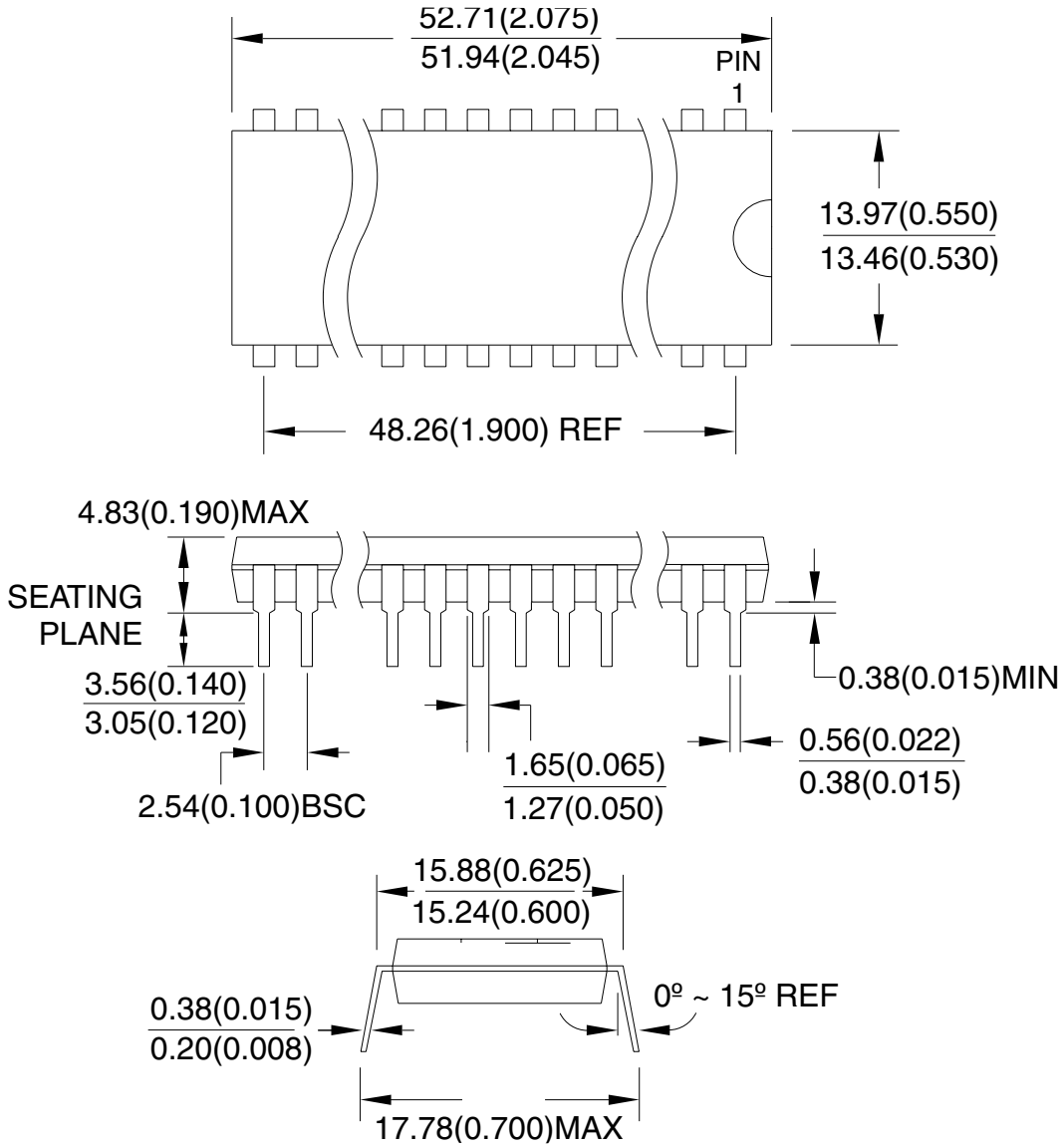


Register Summary

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Page
$3F ($5F)	SREG	I	T	H	S	V	N	Z	C	page 19
$3E ($5E)	SPH	-	-	-	-	-	-	SP9	SP8	page 20
$3D ($5D)	SPL	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0	page 20
$3C ($5C)	Reserved									
$3B ($5B)	GIMSK	INT1	INT0	-	-	-	-	-	-	page 25
$3A ($5A)	GIFR	INTF1	INTF0							page 26
$39 ($59)	TIMSK	OCIE2	TOIE2	TICIE1	OCIE1A	OCIE1B	TOIE1	-	TOIE0	page 26
$38 ($58)	TIFR	OCF2	TOV2	ICF1	OCF1A	OCF1B	TOV1	-	TOV0	page 27
$37 ($57)	Reserved									
$36 ($56)	Reserved									
$35 ($55)	MCUCR	-	SE	SM1	SM0	ISC11	ISC10	ISC01	ISC00	page 29
$34 ($54)	MCUSR	-	-	-	-	-	-	EXTRF	PORF	page 24
$33 ($53)	TCCR0	-	-	-	-	-	CS02	CS01	CS00	page 34
$32 ($52)	TCNT0	Timer/Counter0 (8 Bits)								page 34
$31 ($51)	Reserved									
$30 ($50)	Reserved									
$2F ($4F)	TCCR1A	COM1A1	COM1A0	COM1B1	COM1B0	-	-	PWM11	PWM10	page 36
$2E ($4E)	TCCR1B	ICNC1	ICES1	-	-	CTC1	CS12	CS11	CS10	page 37
$2D ($4D)	TCNT1H	Timer/Counter1 – Counter Register High Byte								page 38
$2C ($4C)	TCNT1L	Timer/Counter1 – Counter Register Low Byte								page 38
$2B ($4B)	OCR1AH	Timer/Counter1 – Output Compare Register A High Byte								page 39
$2A ($4A)	OCR1AL	Timer/Counter1 – Output Compare Register A Low Byte								page 39
$29 ($49)	OCR1BH	Timer/Counter1 – Output Compare Register B High Byte								page 39
$28 ($48)	OCR1BL	Timer/Counter1 – Output Compare Register B Low Byte								page 39
$27 ($47)	ICR1H	Timer/Counter1 – Input Capture Register High Byte								page 40
$26 ($46)	ICR1L	Timer/Counter1 – Input Capture Register Low Byte								page 40
$25 ($45)	TCCR2	-	PWM2	COM21	COM20	CTC2	CS22	CS21	CS20	page 43
$24 ($44)	TCNT2	Timer/Counter2 (8 Bits)								page 44
$23 ($43)	OCR2	Timer/Counter2 Output Compare Register								page 44
$22 ($42)	ASSR	-	-	-	-	AS2	TCN2UB	OCR2UB	TCR2UB	page 46
$21 ($41)	WDTCR	-	-	-	WDTOE	WDE	WDP2	WDP1	WDP0	page 49
$20 ($40)	Reserved									
$1F ($3F)	EEARH								EEAR8	page 51
$1E ($3E)	EEARL	EEAR7	EEAR6	EEAR5	EEAR4	EEAR3	EEAR2	EEAR1	EEAR0	page 51
$1D ($3D)	EEDR	EEPROM Data Register								page 51
$1C ($3C)	EECR	-	-	-	-	EERIE	EEMWE	EEWE	EERE	page 51
$1B ($3B)	PORTA	PORTA7	PORTA6	PORTA5	PORTA4	PORTA3	PORTA2	PORTA1	PORTA0	page 76
$1A ($3A)	DDRA	DDA7	DDA6	DDA5	DDA4	DDA3	DDA2	DDA1	DDA0	page 76
$19 ($39)	PINA	PINA7	PINA6	PINA5	PINA4	PINA3	PINA2	PINA1	PINA0	page 76
$18 ($38)	PORTB	PORTB7	PORTB6	PORTB5	PORTB4	PORTB3	PORTB2	PORTB1	PORTB0	page 78
$17 ($37)	DDRB	DDB7	DDB6	DDB5	DDB4	DDB3	DDB2	DDB1	DDB0	page 78
$16 ($36)	PINB	PINB7	PINB6	PINB5	PINB4	PINB3	PINB2	PINB1	PINB0	page 78
$15 ($35)	PORTC	PORTC7	PORTC6	PORTC5	PORTC4	PORTC3	PORTC2	PORTC1	PORTC0	page 84
$14 ($34)	DDRC	DDC7	DDC6	DDC5	DDC4	DDC3	DDC2	DDC1	DDC0	page 84
$13 ($33)	PINC	PINC7	PINC6	PINC5	PINC4	PINC3	PINC2	PINC1	PINC0	page 84
$12 ($32)	PORTD	PORTD7	PORTD6	PORTD5	PORTD4	PORTD3	PORTD2	PORTD1	PORTD0	page 87
$11 ($31)	DDRD	DDD7	DDD6	DDD5	DDD4	DDD3	DDD2	DDD1	DDD0	page 87
$10 ($30)	PIND	PIND7	PIND6	PIND5	PIND4	PIND3	PIND2	PIND1	PIND0	page 87
$0F ($2F)	SPDR	SPI Data Register								page 58
$0E ($2E)	SPSR	SPIF	WCOL	-	-	-	-	-	-	page 58
$0D ($2D)	SPCR	SPIE	SPE	DORD	MSTR	CPOL	CPHA	SPR1	SPR0	page 57
$0C ($2C)	UDR	UART I/O Data Register								page 62
$0B ($2B)	USR	RXC	TXC	UDRE	FE	OR	-	-	-	page 62
$0A ($2A)	UCR	RXCIE	TXCIE	UDRIE	RXEN	TXEN	CHR9	RXB8	TXB8	page 63
$09 ($29)	UBRR	UART Baud Rate Register								page 65
$08 ($28)	ACSR	ACD	-	ACO	ACI	ACIE	ACIC	ACIS1	ACIS0	page 66
$07 ($27)	ADMUX	-	-	-	-	-	MUX2	MUX1	MUX0	page 72
$06 ($26)	ADCSR	ADEN	ADSC	ADFR	ADIF	ADIE	ADPS2	ADPS1	ADPS0	page 72
$05 ($25)	ADCH	-	-	-	-	-	-	ADC9	ADC8	page 73
$04 ($24)	ADCL	ADC7	ADC6	ADC5	ADC4	ADC3	ADC2	ADC1	ADC0	page 73
$03 ($20)	Reserved									
$02 ($22)	Reserved									
$01 ($21)	Reserved									
$00 ($20)	Reserved									

40P6

40-lead, Plastic Dual Inline
Parkage (PDIP), 0.600" wide
Demension in Millimeters and (Inches)*
JEDEC STANDARD MS-011 AC



*Controlling dimension: Inches

REV. A 04/11/2001