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Details

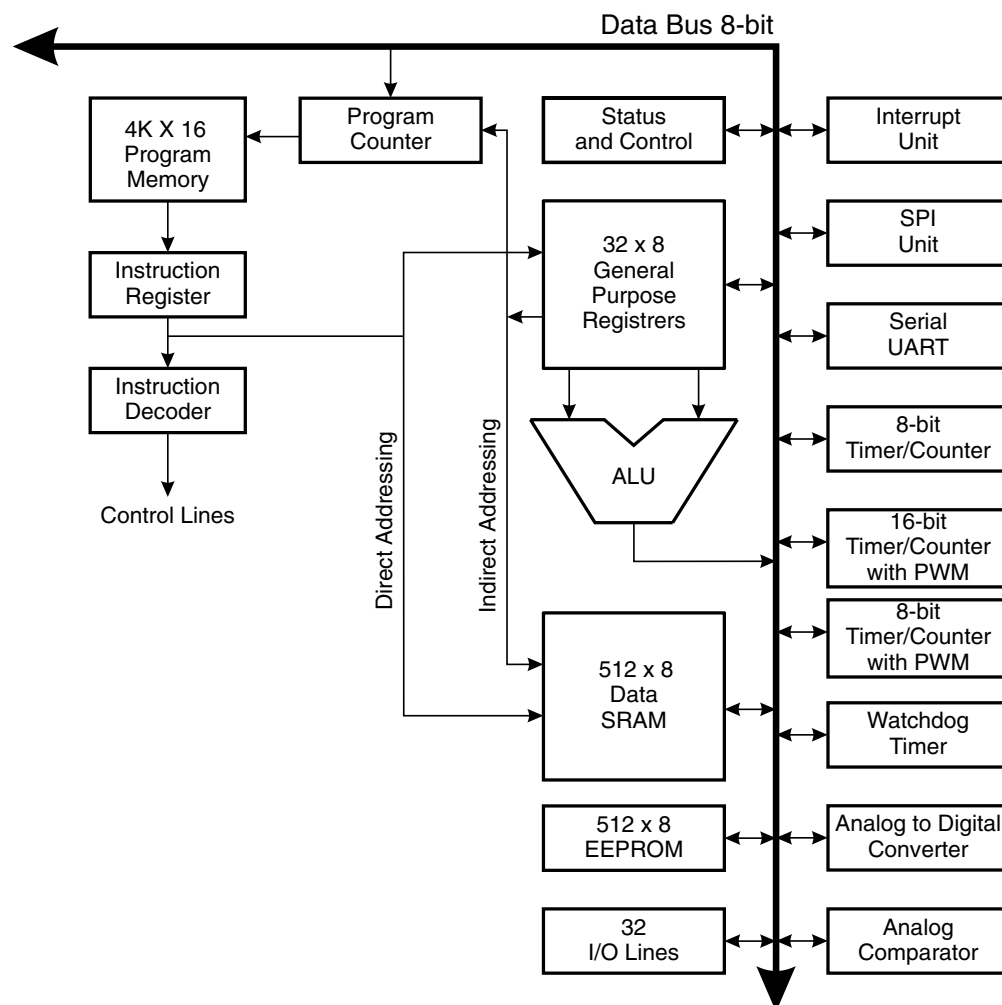
Product Status	Obsolete
Core Processor	AVR
Core Size	8-Bit
Speed	4MHz
Connectivity	SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	32
Program Memory Size	8KB (4K x 16)
Program Memory Type	FLASH
EEPROM Size	512 x 8
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 6V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C
Mounting Type	Through Hole
Package / Case	40-DIP (0.600", 15.24mm)
Supplier Device Package	40-PDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/at90ls8535-4pc

Architectural Overview

The fast-access register file concept contains 32 x 8-bit general-purpose working registers with a single clock cycle access time. This means that during one single clock cycle, one Arithmetic Logic Unit (ALU) operation is executed. Two operands are output from the register file, the operation is executed and the result is stored back in the register file – in one clock cycle.

Six of the 32 registers can be used as three 16-bit indirect address register pointers for Data Space addressing, enabling efficient address calculations. One of the three address pointers is also used as the address pointer for the constant table look-up function. These added function registers are the 16-bit X-register, Y-register, and Z-register.

Figure 4. The AT90S8535 AVR RISC Architecture

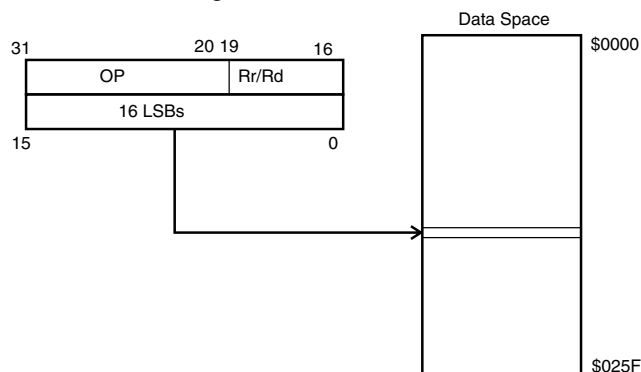


The ALU supports arithmetic and logic functions between registers or between a constant and a register. Single register operations are also executed in the ALU. Figure 4 shows the AT90S8535 AVR RISC microcontroller architecture.

In addition to the register operation, the conventional memory addressing modes can be used on the register file as well. This is enabled by the fact that the register file is

Data Direct

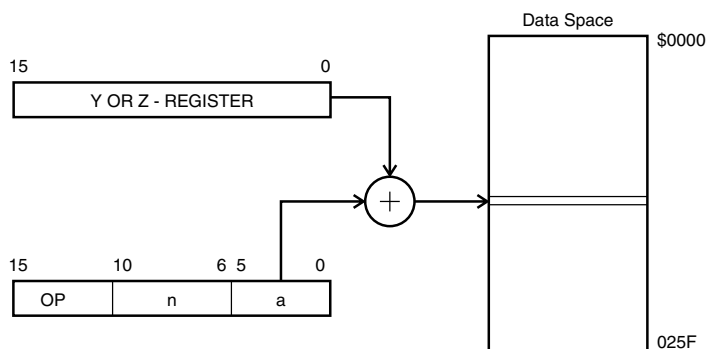
Figure 12. Direct Data Addressing



A 16-bit data address is contained in the 16 LSBs of a 2-word instruction. Rd/Rr specify the destination or source register.

Data Indirect with Displacement

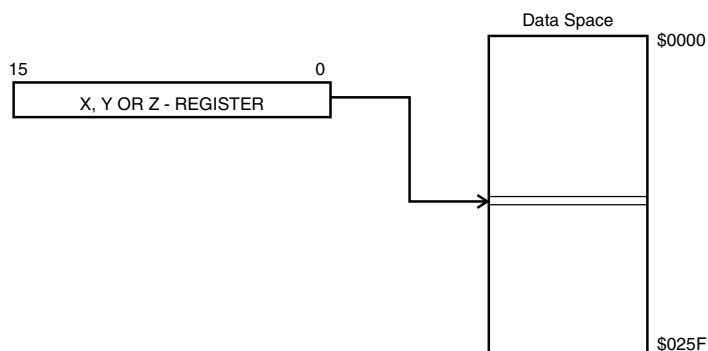
Figure 13. Data Indirect with Displacement



Operand address is the result of the Y- or Z-register contents added to the address contained in six bits of the instruction word.

Data Indirect

Figure 14. Data Indirect Addressing



Operand address is the contents of the X-, Y-, or the Z-register.

Stack Pointer – SP

The AT90S8535 Stack Pointer is implemented as two 8-bit registers in the I/O space locations \$3E (\$5E) and \$3D (\$5D). As the AT90S8535 data memory has \$25F locations, 10 bits are used.

Bit	15	14	13	12	11	10	9	8	
\$3E (\$5E)	–	–	–	–	–	–	SP9	SP8	SPH
\$3D (\$5D)	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0	SPL
	7	6	5	4	3	2	1	0	
Read/Write	R	R	R	R	R	R	R/W	R/W	
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	
	0	0	0	0	0	0	0	0	

The Stack Pointer points to the data SRAM stack area where the Subroutine and Interrupt stacks are located. This stack space in the data SRAM must be defined by the program before any subroutine calls are executed or interrupts are enabled. The Stack Pointer must be set to point above \$60. The Stack Pointer is decremented by 1 when data is pushed onto the stack with the PUSH instruction and it is decremented by 2 when an address is pushed onto the stack with subroutine calls and interrupts. The Stack Pointer is incremented by 1 when data is popped from the stack with the POP instruction and it is incremented by 2 when an address is popped from the stack with return from subroutine RET or return from interrupt RETI.

Reset and Interrupt Handling

The AT90S8535 provides 16 different interrupt sources. These interrupts and the separate reset vector each have a separate program vector in the program memory space. All interrupts are assigned individual enable bits that must be set (one) together with the I-bit in the Status Register in order to enable the interrupt.

The lowest addresses in the program memory space are automatically defined as the Reset and Interrupt vectors. The complete list of vectors is shown in Table 2. The list also determines the priority levels of the different interrupts. The lower the address, the higher the priority level. RESET has the highest priority, and next is INT0 (the External Interrupt Request 0), etc.

Table 2. Reset and Interrupt Vectors

Vector No.	Program Address	Source	Interrupt Definition
1	\$000	RESET	Hardware Pin, Power-on Reset and Watchdog Reset
2	\$001	INT0	External Interrupt Request 0
3	\$002	INT1	External Interrupt Request 1
4	\$003	TIMER2 COMP	Timer/Counter2 Compare Match
5	\$004	TIMER2 OVF	Timer/Counter2 Overflow
6	\$005	TIMER1 CAPT	Timer/Counter1 Capture Event
7	\$006	TIMER1 COMPA	Timer/Counter1 Compare Match A
8	\$007	TIMER1 COMPB	Timer/Counter1 Compare Match B
9	\$008	TIMER1 OVF	Timer/Counter1 Overflow
10	\$009	TIMER0 OVF	Timer/Counter0 Overflow
11	\$00A	SPI, STC	SPI Serial Transfer Complete
12	\$00B	UART, RX	UART, Rx Complete

placed at these locations. The circuit diagram in Figure 23 shows the reset logic. Table 3 defines the timing and electrical parameters of the reset circuitry.

Figure 23. Reset Logic

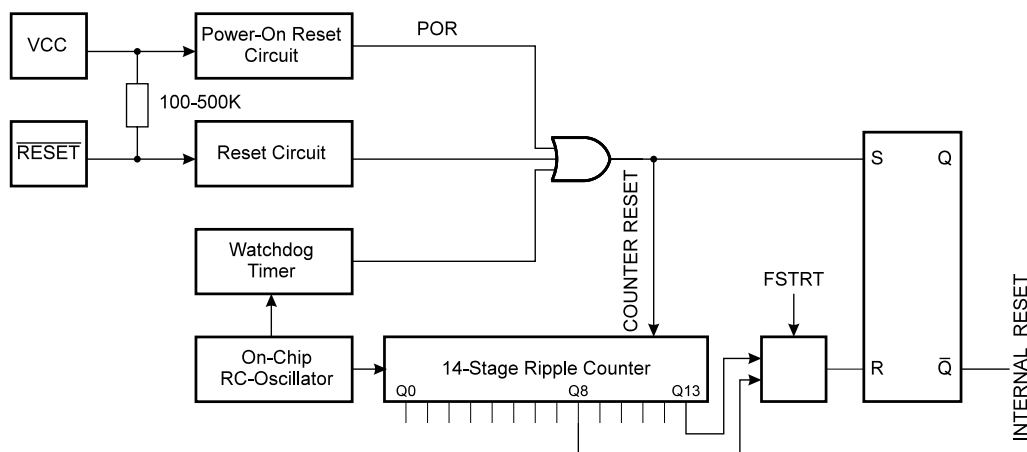


Table 3. Reset Characteristics ($V_{CC} = 5.0V$)

Symbol	Parameter	Min	Typ	Max	Units
$V_{POT}^{(1)}$	Power-on Reset Threshold (rising)	1.0	1.4	1.8	V
	Power-on Reset Threshold (falling)	0.4	0.6	0.8	V
V_{RST}	$\overline{RESET}$ Pin Threshold Voltage		0.6 V_{CC}		V
t_{TOUT}	Reset Delay Time-out Period FSTRT Unprogrammed	11.0	16.0	21.0	ms
t_{TOUT}	Reset Delay Time-out Period FSTRT Programmed	1.0	1.1	1.2	ms

Note: 1. The Power-on Reset will not work unless the supply voltage has been below V_{POT} (falling).

Table 4. Number of Watchdog Oscillator Cycles

FSTRT	Time-out at $V_{CC} = 5V$	Number of WDT Cycles
Programmed	1.1 ms	1K
Unprogrammed	16.0 ms	16K

Power-on Reset

A Power-on Reset (POR) circuit ensures that the device is reset from power-on. As shown in Figure 23, an internal timer clocked from the Watchdog Timer oscillator prevents the MCU from starting until after a certain period after V_{CC} has reached the Power-on Threshold voltage (V_{POT}), regardless of the V_{CC} rise time (see Figure 24).

The user can select the start-up time according to typical oscillator start-up time. The number of WDT oscillator cycles is shown in Table 4. The frequency of the Watchdog oscillator is voltage-dependent as shown in "Typical Characteristics" on page 107.

If the built-in start-up delay is sufficient, $\overline{RESET}$ can be connected to V_{CC} directly or via an external pull-up resistor. By holding the pin low for a period after V_{CC} has been applied, the Power-on Reset period can be extended. Refer to Figure 25 for a timing example of this.

Comparator Interrupt is not required, the Analog Comparator can be powered down by setting the ACD-bit in the Analog Comparator Control and Status Register (ACSR). This will reduce power consumption in Idle Mode. When the MCU wakes up from Idle Mode, the CPU starts program execution immediately.

Power-down Mode

When the SM1/SM0 bits are set to 10, the SLEEP instruction makes the MCU enter the Power-down mode. In this mode, the external oscillator is stopped while the external interrupts and the Watchdog (if enabled) continue operating. Only an external reset, a Watchdog reset (if enabled) or an external level interrupt can wake up the MCU.

Note that when a level-triggered interrupt is used for wake-up from power-down, the low level must be held for a time longer than the reset delay Time-out period t_{TOUT} .

When waking up from Power-down mode, a delay from the wake-up condition occurs until the wake-up becomes effective. This allows the clock to restart and become stable after having been stopped. The wake-up period is equal to the reset period, as shown in Table 3 on page 22.

If the wake-up condition disappears before the MCU wakes up and starts to execute, e.g., a low-level on is not held long enough, the interrupt causing the wake-up will not be executed.

Power Save Mode

When the SM1/SM0 bits are 11, the SLEEP instruction makes the MCU enter the Power Save Mode. This mode is identical to Power-down, with one exception: If Timer/Counter2 is clocked asynchronously, i.e., the AS2 bit in ASSR is set, Timer/Counter2 will run during sleep. In addition to the power-down wake-up sources, the device can also wake up from either a Timer Overflow or Output Compare event from Timer/Counter2 if the corresponding Timer/Counter2 interrupt enable bits are set in TIMSK and the global interrupt enable bit in SREG is set.

When waking up from Power Save Mode by an external interrupt, two instruction cycles are executed before the interrupt flags are updated. When waking up by the asynchronous timer, three instruction cycles are executed before the flags are updated. During these cycles, the processor executes instructions, but the interrupt condition is not readable and the interrupt routine has not started yet.

When waking up from Power Save Mode by an asynchronous timer interrupt, the part will wake up even if global interrupts are disabled. To ensure that the part executes the interrupt routine when waking up, also set the global interrupt enable bit in SREG.

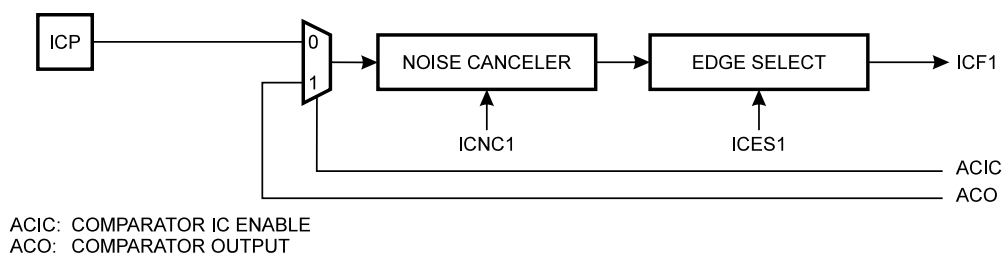
If the asynchronous timer is not clocked asynchronously, Power-down mode is recommended instead of Power Save Mode because the contents of the registers in the asynchronous timer should be considered undefined after wake-up in Power Save Mode, even if AS2 is 0.

the counter on compareA match and actions on the Output Compare pins on both compare matches.

Timer/Counter1 can also be used as an 8-, 9- or 10-bit Pulse Width Modulator. In this mode the counter and the OCR1A/OCR1B registers serve as a dual glitch-free stand-alone PWM with centered pulses. Refer to page 40 for a detailed description of this function.

The Input Capture function of Timer/Counter1 provides a capture of the Timer/Counter1 contents to the Input Capture Register (ICR1), triggered by an external event on the Input Capture Pin (ICP). The actual capture event settings are defined by the Timer/Counter1 Control Register (TCCR1B). In addition, the Analog Comparator can be set to trigger the input capture. Refer to “Analog Comparator” on page 66 for details on this. The ICP pin logic is shown in Figure 32.

Figure 32. ICP Pin Schematic Diagram



If the Noise Canceler function is enabled, the actual trigger condition for the capture event is monitored over four samples and all four must be equal to activate the capture flag. The input pin signal is sampled at XTAL clock frequency.

Timer/Counter1 Control Register A – TCCR1A

Bit	7	6	5	4	3	2	1	0	
\$2F (\$4F)	COM1A1	COM1A0	COM1B1	COM1B0	–	–	PWM11	PWM10	TCCR1A
Read/Write	R/W	R/W	R/W	R/W	R	R	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

• Bits 7, 6 – COM1A1, COM1A0: Compare Output Mode1A, Bits 1 and 0

The COM1A1 and COM1A0 control bits determine any output pin action following a compare match in Timer/Counter1. Any output pin actions affect pin OC1A (Output CompareA pin 1). This is an alternative function to an I/O port and the corresponding direction control bit must be set (one) to control an output pin. The control configuration is shown in Table 11.

• Bits 5, 4 – COM1B1, COM1B0: Compare Output Mode1B, Bits 1 and 0

The COM1B1 and COM1B0 control bits determine any output pin action following a compare match in Timer/Counter1. Any output pin actions affect pin OC1B (Output CompareB). This is an alternative function to an I/O port and the corresponding direction control bit must be set (one) to control an output pin. The control configuration is given in Table 11.

up-counting and down-counting values are reached simultaneously. When the prescaler is in use ($CS12..CS10 \neq 001$ or 000), the PWM output goes active when the counter reaches TOP value, but the down-counting compare match is not interpreted to be reached before the next time the counter reaches the TOP value, making a one-period PWM pulse.

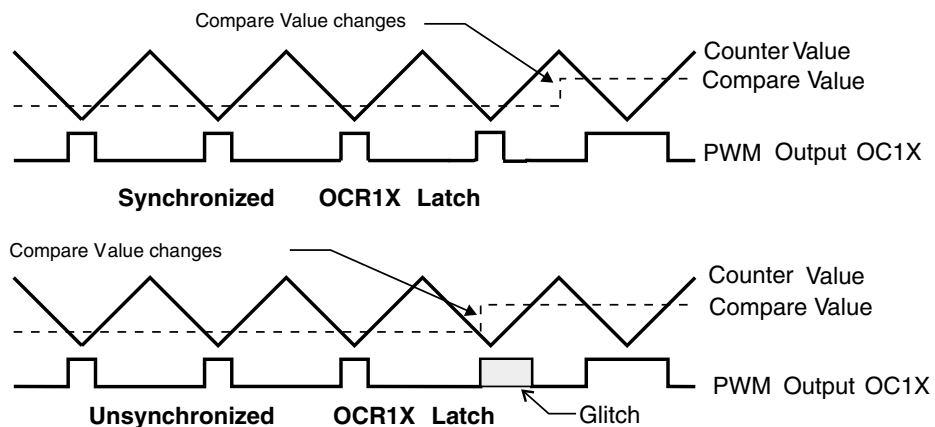
Table 15. Compare1 Mode Select in PWM Mode

COM1X1	COM1X0	Effect on OCX1
0	0	Not connected
0	1	Not connected
1	0	Cleared on compare match, up-counting. Set on compare match, down-counting (non-inverted PWM).
1	1	Cleared on compare match, down-counting. Set on compare match, up-counting (inverted PWM).

Note: X = A or B

Note that in the PWM mode, the 10 least significant OCR1A/OCR1B bits, when written, are transferred to a temporary location. They are latched when Timer/Counter1 reaches the value TOP. This prevents the occurrence of odd-length PWM pulses (glitches) in the event of an unsynchronized OCR1A/OCR1B write. See Figure 33 for an example.

Figure 33. Effects of Unsynchronized OCR1 Latching



Note: X = A or B

During the time between the write and the latch operations, a read from OCR1A or OCR1B will read the contents of the temporary location. This means that the most recently written value always will read out of OCR1A/B.

When the OCR1A/OCR1B contains \$0000 or TOP, the output OC1A/OC1B is updated to low or high on the next compare match according to the settings of COM1A1/COM1A0 or COM1B1/COM1B0. This is shown in Table 16.

Table 16. PWM Outputs OCR1X = \$0000 or TOP

COM1X1	COM1X0	OCR1X	Output OC1X
1	0	\$0000	L

Table 16. PWM Outputs OCR1X = \$0000 or TOP

COM1X1	COM1X0	OCR1X	Output OC1X
1	0	TOP	H
1	1	\$0000	H
1	1	TOP	L

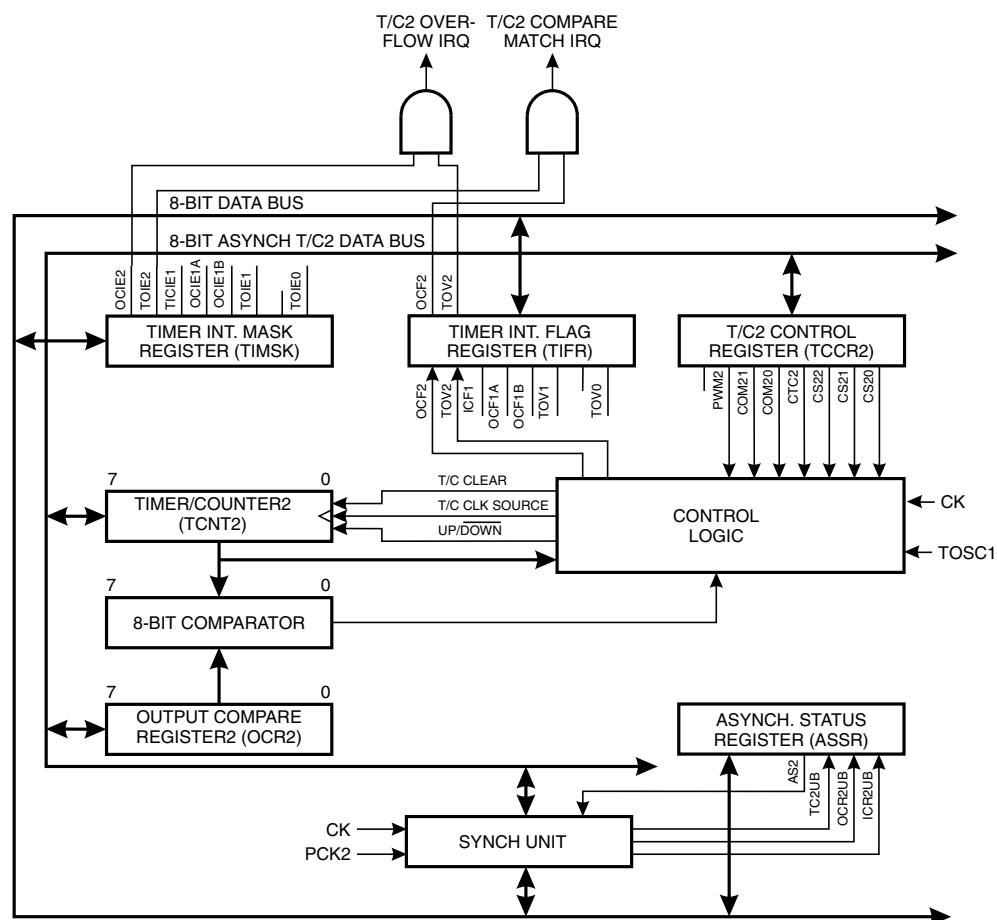
Note: X = A

In PWM mode, the Timer Overflow Flag1 (TOV1) is set when the counter advances from \$0000. Timer Overflow Interrupt1 operates exactly as in normal Timer/Counter mode, i.e., it is executed when TOV1 is set, provided that Timer Overflow Interrupt1 and global interrupts are enabled. This also applies to the Timer Output Compare1 flags and interrupts.

8-bit Timer/Counter2

Figure 34 shows the block diagram for Timer/Counter2.

Figure 34. Timer/Counter2 Block Diagram



The 8-bit Timer/Counter2 can select clock source from PCK2 or prescaled PCK2. It can also be stopped as described in the specification for the Timer/Counter Control Register (TCCR2).

The different status flags (Overflow and Compare Match) are found in the Timer/Counter Interrupt Flag Register (TIFR). Control signals are found in the

Table 20. PWM Outputs OCR2 = \$00 or \$FF

COM21	COM20	OCR2	Output PWM2
1	0	\$FF	H
1	1	\$00	H
1	1	\$FF	L

In PWM mode, the Timer Overflow Flag (TOV2) is set when the counter advances from \$00. Timer Overflow Interrupt2 operates exactly as in normal Timer/Counter mode, i.e., it is executed when TOV2 is set, provided that Timer Overflow Interrupt and global interrupts are enabled. This also applies to the Timer Output Compare flag and interrupt.

The frequency of the PWM will be Timer Clock Frequency divided by 510.

Asynchronous Status Register – ASSR

Bit	7	6	5	4	3	2	1	0	
\$22 (\$22)	–	–	–	–	AS2	TCN2UB	OCR2UB	TCR2UB	ASSR
Read/Write	R	R	R	R	R/W	R	R	R	
Initial Value	0	0	0	0	0	0	0	0	

• Bit 7..4 – Res: Reserved Bits

These bits are reserved bits in the AT90S8535 and always read as zero.

• Bit 3 – AS2: Asynchronous Timer/Counter2

When AS2 is set (one), Timer/Counter2 is clocked from the TOSC1 pin. Pins PC6 and PC7 become connected to a crystal oscillator and cannot be used as general I/O pins. When cleared (zero), Timer/Counter2 is clocked from the internal system clock, CK. When the value of this bit is changed, the contents of TCNT2, OCR2 and TCCR2 might get corrupted.

• Bit 2 – TCN2UB: Timer/Counter2 Update Busy

When Timer/Counter2 operates asynchronously and TCNT2 is written, this bit becomes set (one). When TCNT2 has been updated from the temporary storage register, this bit is cleared (zero) by hardware. A logical “0” in this bit indicates that TCNT2 is ready to be updated with a new value.

• Bit 1 – OCR2UB: Output Compare Register2 Update Busy

When Timer/Counter2 operates asynchronously and OCR2 is written, this bit becomes set (one). When OCR2 has been updated from the temporary storage register, this bit is cleared (zero) by hardware. A logical “0” in this bit indicates that OCR2 is ready to be updated with a new value.

• Bit 0 – TCR2UB: Timer/Counter Control Register2 Update Busy

When Timer/Counter2 operates asynchronously and TCCR2 is written, this bit becomes set (one). When TCCR2 has been updated from the temporary storage register, this bit is cleared (zero) by hardware. A logical “0” in this bit indicates that TCCR2 is ready to be updated with a new value.

If a write is performed to any of the three Timer/Counter2 registers while its Update Busy flag is set (one), the updated value might get corrupted and cause an unintentional interrupt to occur.

The mechanisms for reading TCNT2, OCR2 and TCCR2 are different. When reading TCNT2, the actual timer value is read. When reading OCR2 or TCCR2, the value in the temporary storage register is read.

least one before the processor can read the counter value. After wake-up, the MCU is halted for four cycles, it executes the interrupt routine, and resumes execution from the instruction following SLEEP.

- During asynchronous operation, the synchronization of the interrupt flags for the asynchronous timer takes three processor cycles plus one timer cycle. The timer is therefore advanced by at least 1 before the processor can read the timer value causing the setting of the interrupt flag. The output compare pin is changed on the timer clock and is not synchronized to the processor clock.

UART

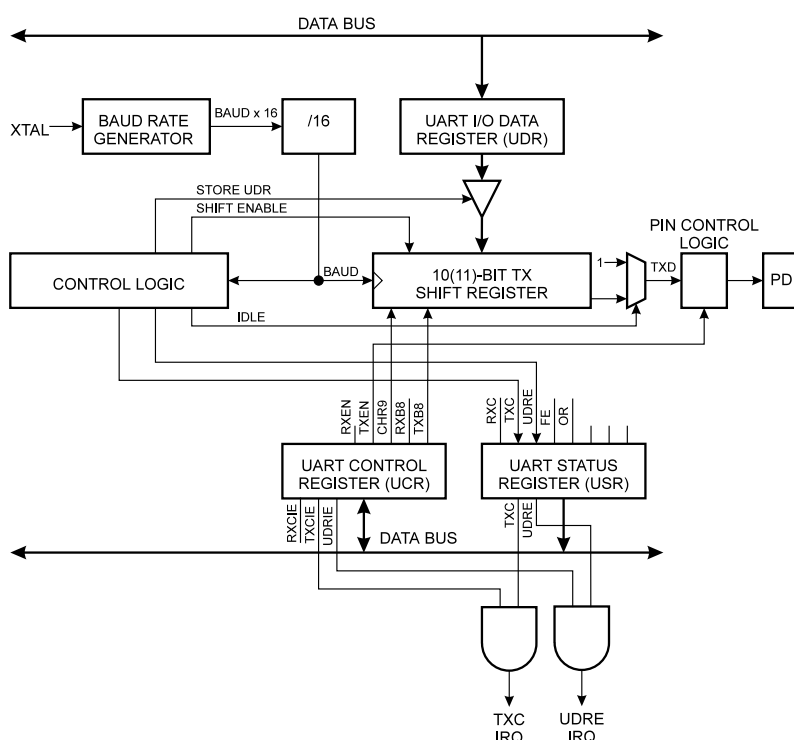
The AT90S8535 features a full duplex (separate receive and transmit registers) Universal Asynchronous Receiver and Transmitter (UART). The main features are:

- **Baud Rate Generator that can Generate a Large Number of Baud Rates (bps)**
- **High Baud Rates at Low XTAL Frequencies**
- **8 or 9 Bits Data**
- **Noise Filtering**
- **Overrun Detection**
- **Framing Error Detection**
- **False Start Bit Detection**
- **Three Separate Interrupts on TX Complete, TX Data Register Empty and RX Complete**
- **Buffered Transmit and Receive**

Data Transmission

A block schematic of the UART transmitter is shown in Figure 41.

Figure 41. UART Transmitter



Data transmission is initiated by writing the data to be transmitted to the UART I/O Data Register, UDR. Data is transferred from UDR to the Transmitter shift register when:

- A new character is written to UDR after the stop bit from the previous character has been shifted out. The shift register is loaded immediately.
- A new character is written to UDR before the stop bit from the previous character has been shifted out. The shift register is loaded when the stop bit of the character currently being transmitted is shifted out.

If the 10(11)-bit Transmitter shift register is empty, data is transferred from UDR to the shift register. The UDRE (UART Data Register Empty) bit in the UART Status Register, USR, is set. When this bit is set (one), the UART is ready to receive the next character. At the same time as the data is transferred from UDR to the 10(11)-bit shift register, bit 0 of the shift register is cleared (start bit) and bit 9 or 10 is set (stop bit). If 9-bit data word

Baud Rate Generator

The baud rate generator is a frequency divider which generates baud rates according to the following equation:

$$\text{BAUD} = \frac{f_{\text{CK}}}{16(\text{UBRR} + 1)}$$

- BAUD = Baud rate
- f_{CK} = Crystal clock frequency
- UBRR = Contents of the UART Baud Rate register, UBRR (0 - 255)

For standard crystal frequencies, the most commonly used baud rates can be generated by using the UBRR settings in Table 24. UBRR values that yield an actual baud rate differing less than 2% from the target baud rate are boldface in the table. However, using baud rates that have more than 1% error is not recommended. High error ratings give less noise resistance.

Table 24. UBRR Settings at Various Crystal Frequencies (Examples)

Baud Rate	1 MHz	%Error	1.8432 MHz	%Error	2 MHz	%Error	2.4576 MHz	%Error
2400	UBRR= 25	0.2	UBRR= 47	0.0	UBRR= 51	0.2	UBRR= 63	0.0
4800	UBRR= 12	0.2	UBRR= 23	0.0	UBRR= 25	0.2	UBRR= 31	0.0
9600	UBRR= 6	7.5	UBRR= 11	0.0	UBRR= 12	0.2	UBRR= 15	0.0
14400	UBRR= 3	7.8	UBRR= 7	0.0	UBRR= 8	3.7	UBRR= 10	3.1
19200	UBRR= 2	7.8	UBRR= 5	0.0	UBRR= 6	7.5	UBRR= 7	0.0
28800	UBRR= 1	7.8	UBRR= 3	0.0	UBRR= 3	7.8	UBRR= 4	6.3
38400	UBRR= 1	22.9	UBRR= 2	0.0	UBRR= 2	7.8	UBRR= 3	0.0
57600	UBRR= 0	7.8	UBRR= 1	0.0	UBRR= 1	7.8	UBRR= 2	12.5
76800	UBRR= 0	22.9	UBRR= 1	33.3	UBRR= 1	22.9	UBRR= 1	0.0
115200	UBRR= 0	84.3	UBRR= 0	0.0	UBRR= 0	7.8	UBRR= 0	25.0

Baud Rate	3.2768 MHz	%Error	3.6864 MHz	%Error	4 MHz	%Error	4.608 MHz	%Error
2400	UBRR= 84	0.4	UBRR= 95	0.0	UBRR= 103	0.2	UBRR= 119	0.0
4800	UBRR= 42	0.8	UBRR= 47	0.0	UBRR= 51	0.2	UBRR= 59	0.0
9600	UBRR= 20	1.6	UBRR= 23	0.0	UBRR= 25	0.2	UBRR= 29	0.0
14400	UBRR= 13	1.6	UBRR= 15	0.0	UBRR= 16	2.1	UBRR= 19	0.0
19200	UBRR= 10	3.1	UBRR= 11	0.0	UBRR= 12	0.2	UBRR= 14	0.0
28800	UBRR= 6	1.6	UBRR= 7	0.0	UBRR= 8	3.7	UBRR= 9	0.0
38400	UBRR= 4	6.3	UBRR= 5	0.0	UBRR= 6	7.5	UBRR= 7	6.7
57600	UBRR= 3	12.5	UBRR= 3	0.0	UBRR= 3	7.8	UBRR= 4	0.0
76800	UBRR= 2	12.5	UBRR= 2	0.0	UBRR= 2	7.8	UBRR= 3	6.7
115200	UBRR= 1	12.5	UBRR= 1	0.0	UBRR= 1	7.8	UBRR= 2	20.0

Baud Rate	7.3728 MHz	%Error	8 MHz	%Error	9.216 MHz	%Error	11.059 MHz	%Error
2400	UBRR= 191	0.0	UBRR= 207	0.2	UBRR= 239	0.0	UBRR= 287	-
4800	UBRR= 95	0.0	UBRR= 103	0.2	UBRR= 119	0.0	UBRR= 143	0.0
9600	UBRR= 47	0.0	UBRR= 51	0.2	UBRR= 59	0.0	UBRR= 71	0.0
14400	UBRR= 31	0.0	UBRR= 34	0.8	UBRR= 39	0.0	UBRR= 47	0.0
19200	UBRR= 23	0.0	UBRR= 25	0.2	UBRR= 29	0.0	UBRR= 35	0.0
28800	UBRR= 15	0.0	UBRR= 16	2.1	UBRR= 19	0.0	UBRR= 23	0.0
38400	UBRR= 11	0.0	UBRR= 12	0.2	UBRR= 14	0.0	UBRR= 17	0.0
57600	UBRR= 7	0.0	UBRR= 8	3.7	UBRR= 9	0.0	UBRR= 11	0.0
76800	UBRR= 5	0.0	UBRR= 6	7.5	UBRR= 7	6.7	UBRR= 8	0.0
115200	UBRR= 3	0.0	UBRR= 3	7.8	UBRR= 4	0.0	UBRR= 5	0.0

Note: Maximum baud rate to each frequency.

Operation

The ADC converts an analog input voltage to a 10-bit digital value through successive approximation. The minimum value represents AGND and the maximum value represents the voltage on the AREF pin minus one LSB. The analog input channel is selected by writing to the MUX bits in ADMUX. Any of the eight ADC input pins ADC7..0 can be selected as single-ended inputs to the ADC.

The ADC can operate in two modes – Single Conversion and Free Running. In Single Conversion Mode, each conversion will have to be initiated by the user. In Free Running Mode, the ADC is constantly sampling and updating the ADC Data Register. The ADFR bit in ADCSR selects between the two available modes.

The ADC is enabled by setting the ADC Enable bit, ADEN in ADCSR. Input channel selections will not go into effect until ADEN is set. The ADC does not consume power when ADEN is cleared, so it is recommended to switch off the ADC before entering power-saving sleep modes.

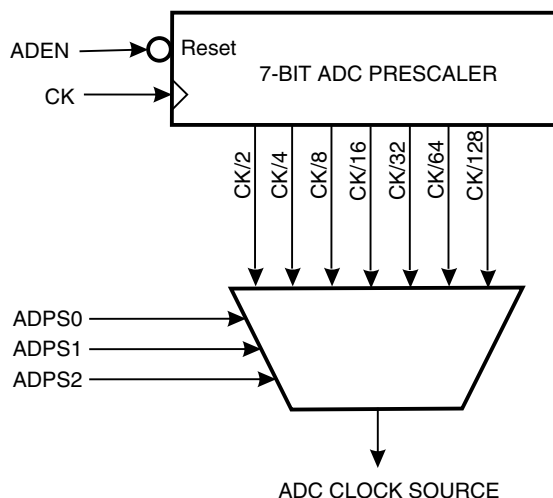
A conversion is started by writing a logical “1” to the ADC Start Conversion bit, ADSC. This bit stays high as long as the conversion is in progress and will be set to zero by hardware when the conversion is completed. If a different data channel is selected while a conversion is in progress, the ADC will finish the current conversion before performing the channel change.

The ADC generates a 10-bit result, which is presented in the ADC data register, ADCH and ADCL. When reading data, ADCL must be read first, then ADCH, to ensure that the content of the data register belongs to the same conversion. Once ADCL is read, ADC access to data register is blocked. This means that if ADCL has been read and a conversion completes before ADCH is read, neither register is updated and the result from the conversion is lost. Then ADCH is read, ADC access to the ADCH and ADCL register is re-enabled.

The ADC has its own interrupt that can be triggered when a conversion completes. When ADC access to the data registers is prohibited between reading of ADCH and ADCL, the interrupt will trigger even if the result is lost.

Prescaling

Figure 46. ADC Prescaler



The successive approximation circuitry requires an input clock frequency between 50 kHz and 200 kHz to achieve maximum resolution. If a resolution of lower than 10 bits is required, the input clock frequency to the ADC can be higher than 200 kHz to achieve a

Figure 55. Port B Schematic Diagram (Pin PB5)

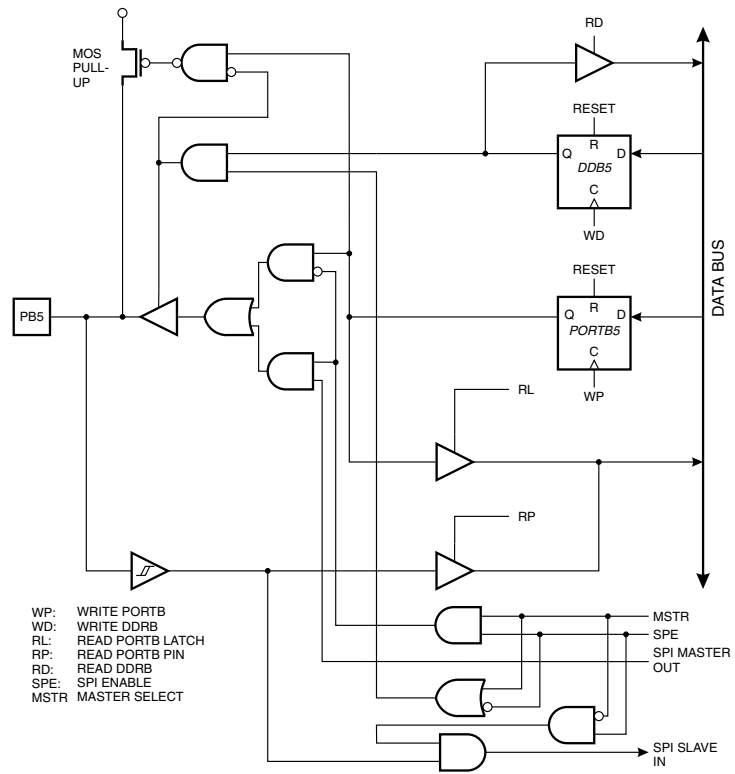


Figure 56. Port B Schematic Diagram (Pin PB6)

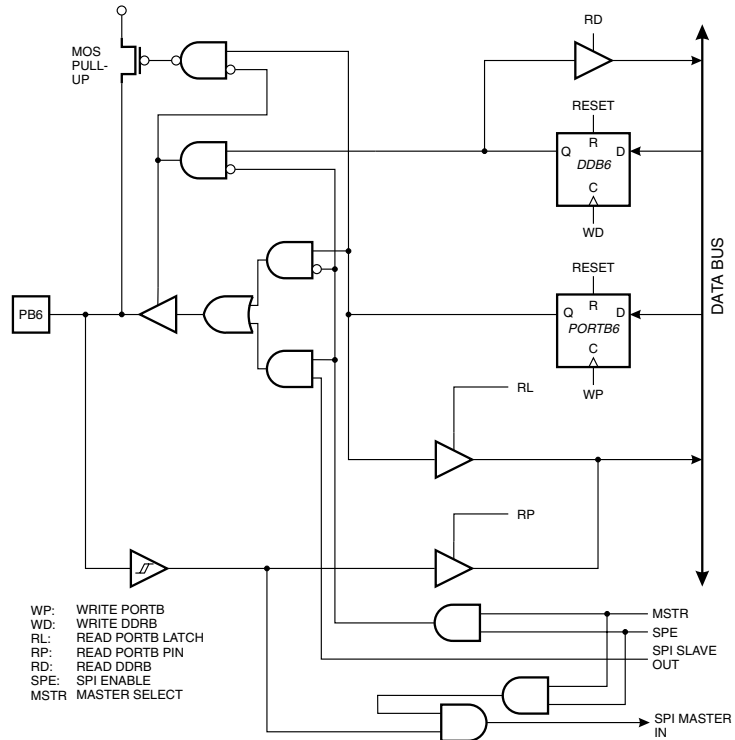


Table 37. Pin Name Mapping

Signal Name in Programming Mode	Pin Name	I/O	Function
RDY/BSY	PD1	O	0: Device is busy programming, 1: Device is ready for new command
$\overline{OE}$	PD2	I	Output Enable (Active low)
$\overline{WR}$	PD3	I	Write Pulse (Active low)
BS	PD4	I	Byte Select ("0" selects low byte, "1" selects high byte)
XA0	PD5	I	XTAL Action Bit 0
XA1	PD6	I	XTAL Action Bit 1
DATA	PB7 - 0	I/O	Bi-directional Data Bus (Output when $\overline{OE}$ is low)

Table 38. XA1 and XA0 Coding

XA1	XA0	Action when XTAL1 is Pulsed
0	0	Load Flash or EEPROM Address (high or low address byte determined by BS)
0	1	Load Data (High or low data byte for Flash determined by BS)
1	0	Load Command
1	1	No Action, Idle

Table 39. Command Byte Bit Coding

Command Byte	Command Executed
1000 0000	Chip Erase
0100 0000	Write Fuse Bits
0010 0000	Write Lock Bits
0001 0000	Write Flash
0001 0001	Write EEPROM
0000 1000	Read Signature Bytes
0000 0100	Read Lock and Fuse Bits
0000 0010	Read Flash
0000 0011	Read EEPROM

Enter Programming Mode

The following algorithm puts the device in Parallel Programming Mode:

1. Apply supply voltage according to Table 36, between V_{CC} and GND.
2. Set the $\overline{RESET}$ and BS pin to "0" and wait at least 100 ns.
3. Apply 11.5 - 12.5V to $\overline{RESET}$. Any activity on BS within 100 ns after +12V has been applied to $\overline{RESET}$, will cause the device to fail entering programming mode.

1. Set BS to “1”. This selects high data.
2. Give $\overline{WR}$ a negative pulse. This starts programming of the data byte. RDY/ $\overline{BSY}$ goes low.
3. Wait until RDY/ $\overline{BSY}$ goes high to program the next byte.

(See Figure 69 for signal waveforms.)

The loaded command and address are retained in the device during programming. For efficient programming, the following should be considered:

- The command needs only be loaded once when writing or reading multiple memory locations.
- Address high byte needs only be loaded before programming a new 256-word page in the Flash.
- Skip writing the data value \$FF, that is, the contents of the entire Flash and EEPROM after a Chip Erase.

These considerations also apply to EEPROM programming and Flash, EEPROM and signature byte reading.

Figure 68. Programming the Flash Waveforms

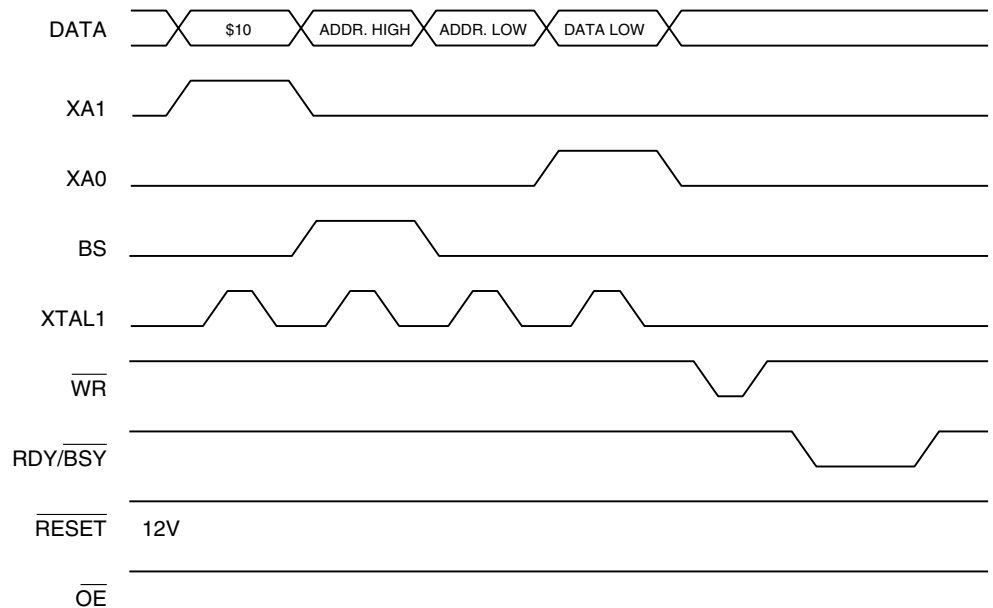


Figure 76. Active Supply Current vs. V_{CC}

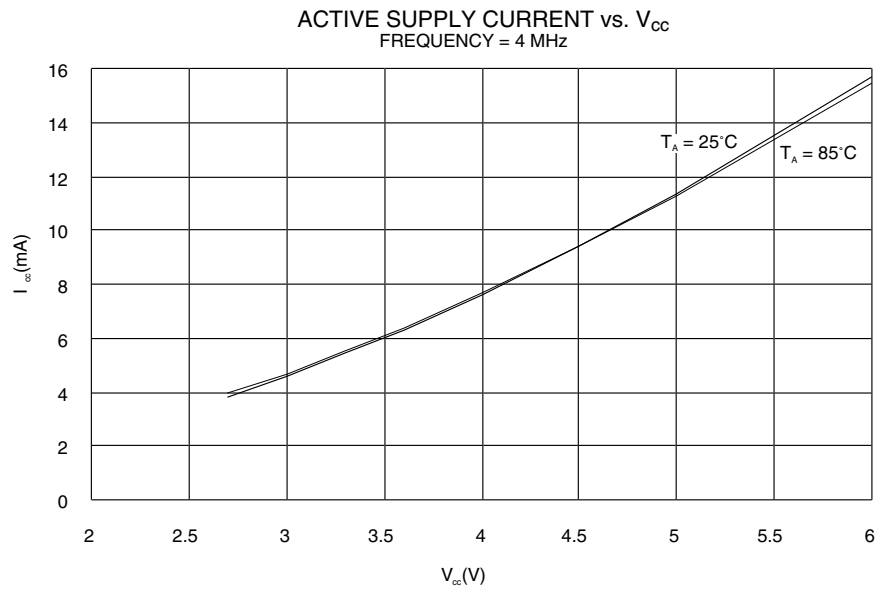


Figure 77. Idle Supply Current vs. Frequency

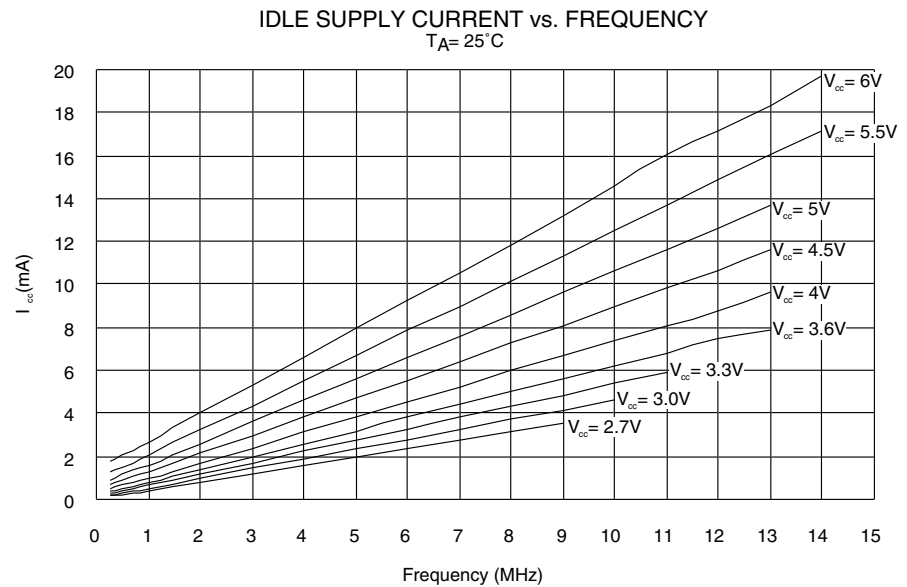
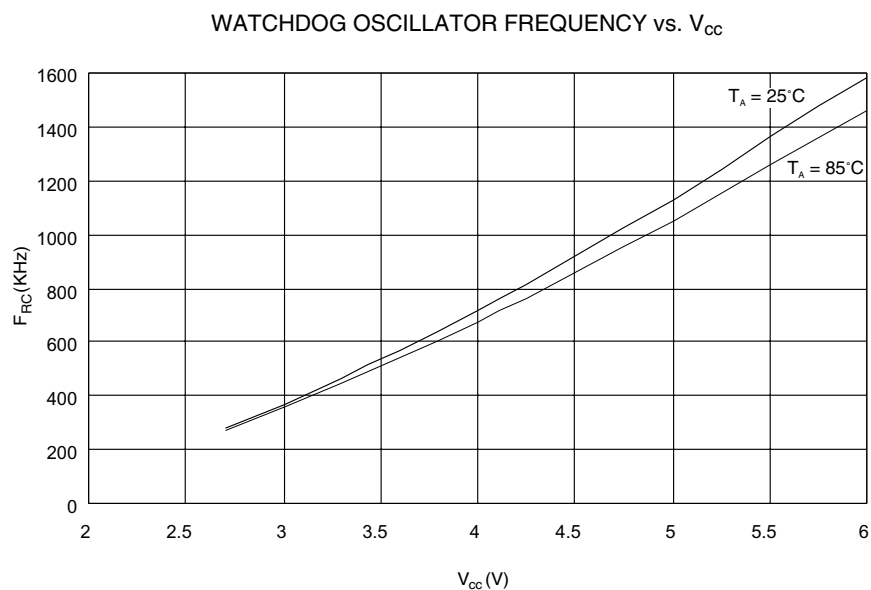


Figure 86. Watchdog Oscillator Frequency vs. V_{CC}



Note: Sink and source capabilities of I/O ports are measured on one pin at a time.

Figure 87. Pull-up Resistor Current vs. Input Voltage

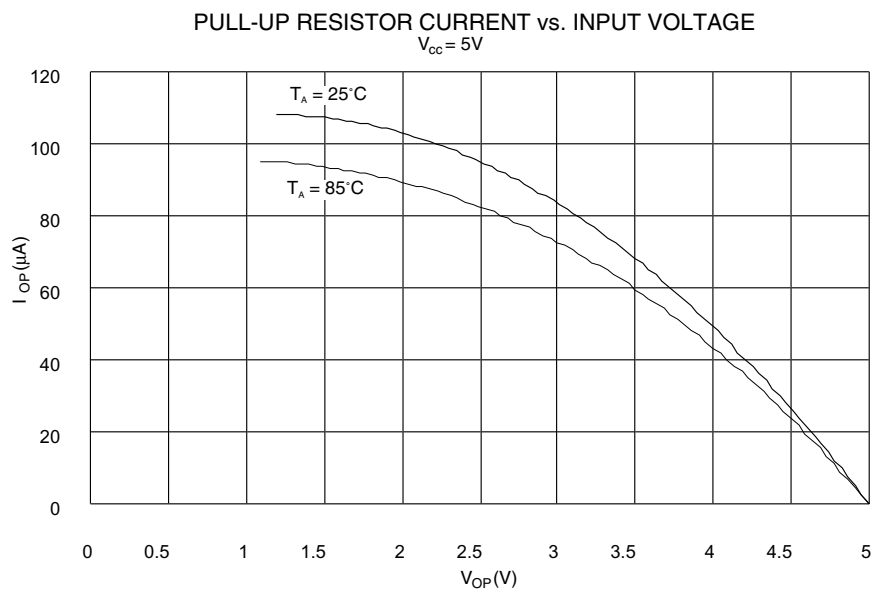
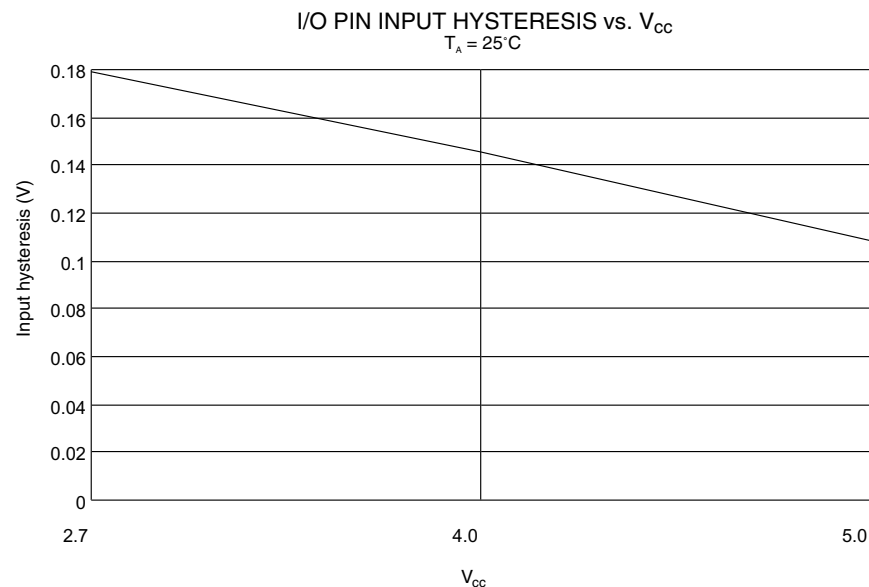


Figure 94. I/O Pin Input Hysteresis vs. V_{CC}



Instruction Set Summary

Mnemonic	Operands	Description	Operation	Flags	# Clocks
ARITHMETIC AND LOGIC INSTRUCTIONS					
ADD	Rd, Rr	Add Two Registers	$Rd \leftarrow Rd + Rr$	Z,C,N,V,H	1
ADC	Rd, Rr	Add with Carry Two Registers	$Rd \leftarrow Rd + Rr + C$	Z,C,N,V,H	1
ADIW	Rdl, K	Add Immediate to Word	$Rdh:Rdl \leftarrow Rdh:Rdl + K$	Z,C,N,V,S	2
SUB	Rd, Rr	Subtract Two Registers	$Rd \leftarrow Rd - Rr$	Z,C,N,V,H	1
SUBI	Rd, K	Subtract Constant from Register	$Rd \leftarrow Rd - K$	Z,C,N,V,H	1
SBC	Rd, Rr	Subtract with Carry Two Registers	$Rd \leftarrow Rd - Rr - C$	Z,C,N,V,H	1
SBCI	Rd, K	Subtract with Carry Constant from Reg.	$Rd \leftarrow Rd - K - C$	Z,C,N,V,H	1
SBIW	Rdl, K	Subtract Immediate from Word	$Rdh:Rdl \leftarrow Rdh:Rdl - K$	Z,C,N,V,S	2
AND	Rd, Rr	Logical AND Registers	$Rd \leftarrow Rd \bullet Rr$	Z,N,V	1
ANDI	Rd, K	Logical AND Register and Constant	$Rd \leftarrow Rd \bullet K$	Z,N,V	1
OR	Rd, Rr	Logical OR Registers	$Rd \leftarrow Rd \vee Rr$	Z,N,V	1
ORI	Rd, K	Logical OR Register and Constant	$Rd \leftarrow Rd \vee K$	Z,N,V	1
EOR	Rd, Rr	Exclusive OR Registers	$Rd \leftarrow Rd \oplus Rr$	Z,N,V	1
COM	Rd	One's Complement	$Rd \leftarrow \$FF - Rd$	Z,C,N,V	1
NEG	Rd	Two's Complement	$Rd \leftarrow \$00 - Rd$	Z,C,N,V,H	1
SBR	Rd, K	Set Bit(s) in Register	$Rd \leftarrow Rd \vee K$	Z,N,V	1
CBR	Rd, K	Clear Bit(s) in Register	$Rd \leftarrow Rd \bullet (\$FF - K)$	Z,N,V	1
INC	Rd	Increment	$Rd \leftarrow Rd + 1$	Z,N,V	1
DEC	Rd	Decrement	$Rd \leftarrow Rd - 1$	Z,N,V	1
TST	Rd	Test for Zero or Minus	$Rd \leftarrow Rd \bullet Rd$	Z,N,V	1
CLR	Rd	Clear Register	$Rd \leftarrow Rd \oplus Rd$	Z,N,V	1
SER	Rd	Set Register	$Rd \leftarrow \$FF$	None	1
BRANCH INSTRUCTIONS					
RJMP	k	Relative Jump	$PC \leftarrow PC + k + 1$	None	2
IJMP		Indirect Jump to (Z)	$PC \leftarrow Z$	None	2
RCALL	k	Relative Subroutine Call	$PC \leftarrow PC + k + 1$	None	3
ICALL		Indirect Call to (Z)	$PC \leftarrow Z$	None	3
RET		Subroutine Return	$PC \leftarrow STACK$	None	4
RETI		Interrupt Return	$PC \leftarrow STACK$	I	4
CPSE	Rd, Rr	Compare, Skip if Equal	if $(Rd = Rr)$ $PC \leftarrow PC + 2$ or 3	None	1/2/3
CP	Rd, Rr	Compare	$Rd - Rr$	Z,N,V,C,H	1
CPC	Rd, Rr	Compare with Carry	$Rd - Rr - C$	Z,N,V,C,H	1
CPI	Rd, K	Compare Register with Immediate	$Rd - K$	Z,N,V,C,H	1
SBRC	Rr, b	Skip if Bit in Register Cleared	if $(Rr(b) = 0)$ $PC \leftarrow PC + 2$ or 3	None	1/2/3
SBRs	Rr, b	Skip if Bit in Register is Set	if $(Rr(b) = 1)$ $PC \leftarrow PC + 2$ or 3	None	1/2/3
SBIC	P, b	Skip if Bit in I/O Register Cleared	if $(P(b) = 0)$ $PC \leftarrow PC + 2$ or 3	None	1/2/3
SBIS	P, b	Skip if Bit in I/O Register is Set	if $(P(b) = 1)$ $PC \leftarrow PC + 2$ or 3	None	1/2/3
BRBS	s, k	Branch if Status Flag Set	if $(SREG(s) = 1)$ then $PC \leftarrow PC + k + 1$	None	1/2
BRBC	s, k	Branch if Status Flag Cleared	if $(SREG(s) = 0)$ then $PC \leftarrow PC + k + 1$	None	1/2
BREQ	k	Branch if Equal	if $(Z = 1)$ then $PC \leftarrow PC + k + 1$	None	1/2
BRNE	k	Branch if Not Equal	if $(Z = 0)$ then $PC \leftarrow PC + k + 1$	None	1/2
BRCS	k	Branch if Carry Set	if $(C = 1)$ then $PC \leftarrow PC + k + 1$	None	1/2
BRCC	k	Branch if Carry Cleared	if $(C = 0)$ then $PC \leftarrow PC + k + 1$	None	1/2
BRSH	k	Branch if Same or Higher	if $(C = 0)$ then $PC \leftarrow PC + k + 1$	None	1/2
BRLO	k	Branch if Lower	if $(C = 1)$ then $PC \leftarrow PC + k + 1$	None	1/2
BRMI	k	Branch if Minus	if $(N = 1)$ then $PC \leftarrow PC + k + 1$	None	1/2
BRPL	k	Branch if Plus	if $(N = 0)$ then $PC \leftarrow PC + k + 1$	None	1/2
BRGE	k	Branch if Greater or Equal, Signed	if $(N \oplus V = 0)$ then $PC \leftarrow PC + k + 1$	None	1/2
BRLT	k	Branch if Less Than Zero, Signed	if $(N \oplus V = 1)$ then $PC \leftarrow PC + k + 1$	None	1/2
BRHS	k	Branch if Half-carry Flag Set	if $(H = 1)$ then $PC \leftarrow PC + k + 1$	None	1/2
BRHC	k	Branch if Half-carry Flag Cleared	if $(H = 0)$ then $PC \leftarrow PC + k + 1$	None	1/2
BRTS	k	Branch if T-flag Set	if $(T = 1)$ then $PC \leftarrow PC + k + 1$	None	1/2
BRTC	k	Branch if T-flag Cleared	if $(T = 0)$ then $PC \leftarrow PC + k + 1$	None	1/2
BRVS	k	Branch if Overflow Flag is Set	if $(V = 1)$ then $PC \leftarrow PC + k + 1$	None	1/2
BRVC	k	Branch if Overflow Flag is Cleared	if $(V = 0)$ then $PC \leftarrow PC + k + 1$	None	1/2
BRIE	k	Branch if Interrupt Enabled	if $(I = 1)$ then $PC \leftarrow PC + k + 1$	None	1/2
BRID	k	Branch if Interrupt Disabled	if $(I = 0)$ then $PC \leftarrow PC + k + 1$	None	1/2
DATA TRANSFER INSTRUCTIONS					
MOV	Rd, Rr	Move between Registers	$Rd \leftarrow Rr$	None	1
LDI	Rd, K	Load Immediate	$Rd \leftarrow K$	None	1
LD	Rd, X	Load Indirect	$Rd \leftarrow (X)$	None	2
LD	Rd, X+	Load Indirect and Post-inc.	$Rd \leftarrow (X), X \leftarrow X + 1$	None	2
LD	Rd, -X	Load Indirect and Pre-dec.	$X \leftarrow X - 1, Rd \leftarrow (X)$	None	2