



Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Obsolete
Core Processor	AVR
Core Size	8-Bit
Speed	8MHz
Connectivity	SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	32
Program Memory Size	8KB (4K x 16)
Program Memory Type	FLASH
EEPROM Size	512 x 8
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	4V ~ 6V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C
Mounting Type	Surface Mount
Package / Case	44-TQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/at90s8535-8ac

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Description

The AT90S8535 is a low-power CMOS 8-bit microcontroller based on the AVR RISC architecture. By executing powerful instructions in a single clock cycle, the AT90S8535 achieves throughputs approaching 1 MIPS per MHz allowing the system designer to optimize power consumption versus processing speed.

Block Diagram

Figure 1. The AT90S8535 Block Diagram





Vector No.	Program Address	Source	Interrupt Definition
13	\$00C	UART, UDRE	UART Data Register Empty
14	\$00D	UART, TX	UART, Tx Complete
15	\$00E	ADC	ADC Conversion Complete
16	\$00F	EE_RDY	EEPROM Ready
17	\$010	ANA_COMP	Analog Comparator

 Table 2.
 Reset and Interrupt Vectors (Continued)

The most typical and general program setup for the Reset and Interrupt vector addresses are:

Address Labels	Code		Comments
\$000	rjmp	RESET	; Reset Handler
\$001	rjmp	EXT_INT0	; IRQ0 Handler
\$002	rjmp	EXT_INT1	; IRQ1 Handler
\$003	rjmp	TIM2_COMP	; Timer2 Compare Handler
\$004	rjmp	TIM2_OVF	; Timer2 Overflow Handler
\$005	rjmp	TIM1_CAPT	; Timer1 Capture Handler
\$006	rjmp	TIM1_COMPA	; Timer1 CompareA Handler
\$007	rjmp	TIM1_COMPB	; Timer1 CompareB Handler
\$008	rjmp	TIM1_OVF	; Timer1 Overflow Handler
\$009	rjmp	TIM0_OVF	; Timer0 Overflow Handler
\$00a	rjmp	SPI_STC;	; SPI Transfer Complete Handler
\$00b	rjmp	UART_RXC	; UART RX Complete Handler
\$00c	rjmp	UART_DRE	; UDR Empty Handler
\$00d	rjmp	UART_TXC	; UART TX Complete Handler
\$00e	rjmp	ADC	; ADC Conversion Complete Interrupt
Handler			
\$00f	rjmp	EE_RDY	; EEPROM Ready Handler
\$010	rjmp	ANA_COMP	; Analog Comparator Handler
\$011 MAIN:	ldi	r16, high(R	AMEND); Main program start
\$012	out	SPH,r16	
\$013	ldi	r16, low(RA	MEND) ;
\$014	out	SPL,r16	
\$015	<instr> xx</instr>	x	

Reset Sources

The AT90S8535 has three sources of reset:

- Power-on Reset. The MCU is reset when the supply voltage is below the Power-on Reset threshold (V_{POT}).
- External Reset. The MCU is reset when a low level is present on the RESET pin for more than 50 ns.
- Watchdog Reset. The MCU is reset when the Watchdog timer period expires and the Watchdog is enabled.

During reset, all I/O registers are set to their initial values and the program starts execution from address \$000. The instruction placed in address \$000 must be an RJMP (relative jump) instruction to the reset handling routine. If the program never enables an interrupt source, the interrupt vectors are not used and regular program code can be





placed at these locations. The circuit diagram in Figure 23 shows the reset logic. Table 3 defines the timing and electrical parameters of the reset circuitry.

Figure 23. Reset Logic



Table 3. Reset Characteristics ($V_{CC} = 5.0V$)

Symbol	Parameter	Min	Тур	Max	Units
V (1)	Power-on Reset Threshold (rising)	1.0	1.4	1.8	V
V _{POT} `′	Power-on Reset Threshold (falling)	0.4	0.6	0.8	V
V _{RST}	RESET Pin Threshold Voltage		0.6 V _{CC}		V
t _{TOUT}	Reset Delay Time-out Period FSTRT Unprogrammed	11.0	16.0	21.0	ms
t _{TOUT}	Reset Delay Time-out Period FSTRT Programmed	1.0	1.1	1.2	ms

Note: 1. The Power-on Reset will not work unless the supply voltage has been below V_{POT} (falling).

Table 4. Number of Watchdog Oscillator Cycles

FSTRT	Time-out at V _{CC} = 5V	Number of WDT Cycles
Programmed	1.1 ms	1К
Unprogrammed	16.0 ms	16K

Power-on Reset

A Power-on Reset (POR) circuit ensures that the device is reset from power-on. As shown in Figure 23, an internal timer clocked from the Watchdog Timer oscillator prevents the MCU from starting until after a certain period after V_{CC} has reached the Power-on Threshold voltage (V_{POT}), regardless of the V_{CC} rise time (see Figure 24).

The user can select the start-up time according to typical oscillator start-up time. The number of WDT oscillator cycles is shown in Table 4. The frequency of the Watchdog oscillator is voltage-dependent as shown in "Typical Characteristics" on page 107.

If the built-in start-up delay is sufficient, $\overline{\text{RESET}}$ can be connected to V_{CC} directly or via an external pull-up resistor. By holding the pin low for a period after V_{CC} has been applied, the Power-on Reset period can be extended. Refer to Figure 25 for a timing example of this.

EXTRF	PORF	Reset Source
0	0	Watchdog Reset
0	1	Power-on Reset
1	0	External Reset
1	1	Power-on Reset

Table 6. Reset Source Identification

Interrupt Handling

The AT90S8535 has two 8-bit interrupt mask control registers: GIMSK (General Interrupt Mask register) and TIMSK (Timer/Counter Interrupt Mask register).

When an interrupt occurs, the Global Interrupt Enable I-bit is cleared (zero) and all interrupts are disabled. The user software can set (one) the I-bit to enable nested interrupts. The I-bit is set (one) when a Return from Interrupt instruction (RETI) is executed.

When the Program Counter is vectored to the actual interrupt vector in order to execute the interrupt handling routine, hardware clears the corresponding flag that generated the interrupt. Some of the interrupt flags can also be cleared by writing a logical "1" to the flag bit position(s) to be cleared. If an interrupt condition occurs when the corresponding interrupt enable bit is cleared (zero), the interrupt flag will be set and remembered until the interrupt is enabled or the flag is cleared by software.

If one or more interrupt conditions occur when the global interrupt enable bit is cleared (zero), the corresponding interrupt flag(s) will be set and remembered until the global interrupt enable bit is set (one) and will be executed by order of priority.

Note that external level interrupt does not have a flag and will only be remembered for as long as the interrupt condition is active.

Note that the Status Register is not automatically stored when entering an interrupt routine and restored when returning from an interrupt routine. This must be handled by software.

General Interrupt Mask Register – GIMSK



Bit 7 – INT1: External Interrupt Request 1 Enable

When the INT1 bit is set (one) and the I-bit in the Status Register (SREG) is set (one), the external pin interrupt is enabled. The Interrupt Sense Control1 bits 1/0 (ISC11 and ISC10) in the MCU general Control Register (MCUCR) define whether the external interrupt is activated on rising or falling edge of the INT1 pin or level sensed. Activity on the pin will cause an interrupt request even if INT1 is configured as an output. The corresponding interrupt of External Interrupt Request 1 is executed from program memory address \$002. See also "External Interrupts."

Bit 6 – INT0: External Interrupt Request 0 Enable

When the INT0 bit is set (one) and the I-bit in the Status Register (SREG) is set (one), the external pin interrupt is enabled. The Interrupt Sense Control0 bits 1/0 (ISC01 and ISC00) in the MCU general Control Register (MCUCR) define whether the external interrupt is activated on rising or falling edge of the INT0 pin or level sensed. Activity on the pin will cause an interrupt request even if INT0 is configured as an output. The corre-





sponding interrupt of External Interrupt Request 0 is executed from program memory address \$001. See also "External Interrupts."

• Bits 5.0 - Res: Reserved Bits

These bits are reserved bits in the AT90S8535 and always read as zero.

General Interrupt Flag Register – GIFR

Bit	7	6	5	4	3	2	1	0	
\$3A (\$5A)	INTF1	INTF0	-	-	-	-	-	-	GIFR
Read/Write	R/W	R/W	R	R	R	R	R	R	
Initial Value	0	0	0	0	0	0	0	0	

• Bit 7 – INTF1: External Interrupt Flag1

When an edge or logical change on the INT1 pin triggers an interrupt request, INTF1 becomes set (one). This flag is always cleared (0) when the pin is configured for low-level interrupts, as the state of a low-level interrupt can be determined by reading the PIN register.

If the I-bit in SREG and the INT1 bit in GIMSK are set (one), the MCU will jump to the interrupt address \$002. For edge and logic change interrupts, this flag is cleared when the interrupt routine is executed. Alternatively, the flag can be cleared by writing a logical "1" to it.

• Bit 6 – INTF0: External Interrupt Flag0

When an edge or logical change on the INT0 pin triggers an interrupt request, INTF0 becomes set (one). This flag is always cleared (0) when the pin is configured for low-level interrupts, as the state of a low-level interrupt can be determined by reading the PIN register.

If the I-bit in SREG and the INT0 bit in GIMSK are set (one), the MCU will jump to the interrupt address \$001. For edge and logic change interrupts, this flag is cleared when the interrupt routine is executed. Alternatively, the flag can be cleared by writing a logical "1" to it.

• Bits 5..0 - Res: Reserved Bits

These bits are reserved bits in the AT90S8535 and always read as zero.

Timer/Counter Interrupt Mask Register – TIMSK

Bit 7 6 5 4 2 0 3 TICIE1 OCIE1B \$39 (\$59) OCIE2 TOIE2 OCIE1A TOIE1 TOIE0 Read/Write R/W R/W R/W R/W R/W R/W R/W R Initial Value 0 0 0 0 0 0 0 0

• Bit 7 – OCIE2: Timer/Counter2 Output Compare Match Interrupt Enable

When the OCIE2 bit is set (one) and the I-bit in the Status Register is set (one), the Timer/Counter2 Compare Match interrupt is enabled. The corresponding interrupt (at vector \$003) is executed if a compare match in Timer/Counter2 occurs (i.e., when the OCF2 bit is set in the Timer/Counter Interrupt Flag Register [TIFR]).

Bit 6 – TOIE2: Timer/Counter2 Overflow Interrupt Enable

When the TOIE2 bit is set (one) and the I-bit in the Status Register is set (one), the Timer/Counter2 Overflow interrupt is enabled. The corresponding interrupt (at vector \$004) is executed if an overflow in Timer/Counter2 occurs (i.e., when the TOV2 bit is set in the Timer/Counter Interrupt Flag Register [TIFR]).

TIMSK



Timer/Counter0 Control Register – TCCR0



• Bits 7..3 – Res: Reserved Bits

These bits are reserved bits in the AT90S8535 and always read zero.

• Bits 2, 1, 0 – CS02, CS01, CS00: Clock Select0, Bits 2, 1 and 0

The Clock Select0 bits 2,1 and 0 define the prescaling source of Timer/Counter0.

Table 10.	Clock 0	Prescale	Select
-----------	---------	----------	--------

CS02	CS01	CS00	Description
0	0	0	Stop, Timer/Counter0 is stopped.
0	0	1	СК
0	1	0	СК/8
0	1	1	CK/64
1	0	0	CK/256
1	0	1	CK/1024
1	1	0	External Pin T0, falling edge
1	1	1	External Pin T0, rising edge

The Stop condition provides a Timer Enable/Disable function. The prescaled CK modes are scaled directly from the CK oscillator clock. If the external pin modes are used, the corresponding setup must be performed in the actual Data Direction Control Register (cleared to zero gives an input pin).

Timer Counter 0 – TCNT0



The Timer/Counter0 is realized as an up-counter with read and write access. If the Timer/Counter0 is written and a clock source is present, the Timer/Counter0 continues counting in the clock cycle following the write operation.



• Bit 3 – CTC1: Clear Timer/Counter1 on Compare Match

When the CTC1 control bit is set (one), the Timer/Counter1 is reset to \$0000 in the clock cycle after a compareA match. If the CTC1 control bit is cleared, Timer/Counter1 continues counting and is unaffected by a compare match. Since the compare match is detected in the CPU clock cycle following the match, this function will behave differently when a prescaling higher than 1 is used for the timer. When a prescaling of 1 is used and the compareA register is set to C, the timer will count as follows if CTC1 is set:

... | C-2 | C-1 | C | 0 | 1 |...

When the prescaler is set to divide by 8, the timer will count like this:

In PWM mode, this bit has no effect.

• Bits 2, 1, 0 – CS12, CS11, CS10: Clock Select1, Bits 2, 1 and 0

The Clock Select1 bits 2, 1 and 0 define the prescaling source of Timer/Counter1.

CS12	CS11	CS10	Description
0	0	0	Stop, the Timer/Counter1 is stopped.
0	0	1	СК
0	1	0	СК/8
0	1	1	СК/64
1	0	0	CK/256
1	0	1	CK/1024
1	1	0	External Pin T1, falling edge
1	1	1	External Pin T1, rising edge
-	1	1	

Table 13. Clock 1 Prescale Select

The Stop condition provides a Timer Enable/Disable function. The CK down divided modes are scaled directly from the CK oscillator clock. If the external pin modes are used, the corresponding setup must be performed in the actual Direction Control Register (cleared to zero gives an input pin).

Timer/Counter1 – TCNT1H AND TCNT1L



This 16-bit register contains the prescaled value of the 16-bit Timer/Counter1. To ensure that both the high and low bytes are read and written simultaneously when the CPU accesses these registers, the access is performed using an 8-bit temporary register (TEMP). This temporary register is also used when accessing OCR1A, OCR1B and ICR1. If the main program and also interrupt routines perform access to registers using

Watchdog Timer

The Watchdog Timer is clocked from a separate On-chip oscillator. By controlling the Watchdog Timer prescaler, the Watchdog reset interval can be adjusted as shown in Table 21. See characterization data for typical values at other V_{CC} levels. The WDR (Watchdog Reset) instruction resets the Watchdog Timer. Eight different clock cycle periods can be selected to determine the reset period. If the reset period expires without another Watchdog reset, the AT90S8535 resets and executes from the reset vector. For timing details on the Watchdog reset, refer to page 22.

To prevent unintentional disabling of the Watchdog, a special turn-off sequence must be followed when the Watchdog is disabled. Refer to the description of the Watchdog Timer Control Register for details.





Watchdog Timer Control Register – WDTCR

Bit	7	6	5	4	3	2	1	0	_
\$21 (\$41)	-	-	-	WDTOE	WDE	WDP2	WDP1	WDP0	WDTCR
Read/Write	R	R	R	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

• Bits 7..5 - Res: Reserved Bits

These bits are reserved bits in the AT90S8535 and will always read as zero.

• Bit 4 – WDTOE: Watchdog Turn-off Enable

This bit must be set (one) when the WDE bit is cleared. Otherwise, the Watchdog will not be disabled. Once set, hardware will clear this bit to zero after four clock cycles. Refer to the description of the WDE bit for a Watchdog disable procedure.

• Bit 3 – WDE: Watchdog Enable

When the WDE is set (one) the Watchdog Timer is enabled and if the WDE is cleared (zero) the Watchdog Timer function is disabled. WDE can only be cleared if the WDTOE bit is set (one). To disable an enabled Watchdog Timer, the following procedure must be followed:



Prevent EEPROM Corruption

During periods of low V_{CC}, the EEPROM data can be corrupted because the supply voltage is too low for the CPU and the EEPROM to operate properly. These issues are the same as for board level systems using the EEPROM and the same design solutions should be applied.

An EEPROM data corruption can be caused by two situations when the voltage is too low. First, a regular write sequence to the EEPROM requires a minimum voltage to operate correctly. Secondly, the CPU itself can execute instructions incorrectly, if the supply voltage for executing instructions is too low.

EEPROM data corruption can easily be avoided by following these design recommendations (one is sufficient):

- Keep the AVR RESET active (low) during periods of insufficient power supply voltage. This is best done by an external low V_{CC} Reset Protection circuit, often referred to as a Brown-out Detector (BOD). Please refer to application note AVR 180 for design considerations regarding power-on reset and low-voltage detection.
- Keep the AVR core in Power-down Sleep Mode during periods of low V_{CC}. This will prevent the CPU from attempting to decode and execute instructions, effectively protecting the EEPROM registers from unintentional writes.
- 3. Store constants in Flash memory if the ability to change memory contents from software is not required. Flash memory cannot be updated by the CPU and will not be subject to corruption.



1 denote the first zero-sample. Following the 1-to-0 transition, the receiver samples the RXD pin at samples 8, 9 and 10. If two or more of these three samples are found to be logical "1"s, the start bit is rejected as a noise spike and the receiver starts looking for the next 1-to-0 transition.

If however, a valid start bit is detected, sampling of the data bits following the start bit is performed. These bits are also sampled at samples 8, 9 and 10. The logical value found in at least two of the three samples is taken as the bit value. All bits are shifted into the Transmitter Shift register as they are sampled. Sampling of an incoming character is shown in Figure 43.

Figure 43. Sampling Received Data



When the stop bit enters the receiver, the majority of the three samples must be one to accept the stop bit. If two or more samples are logical "0"s, the Framing Error (FE) flag in the UART Status Register (USR) is set. Before reading the UDR register, the user should always check the FE bit to detect framing errors.

Whether or not a valid stop bit is detected at the end of a character reception cycle, the data is transferred to UDR and the RXC flag in USR is set. UDR is in fact two physically separate registers, one for transmitted data and one for received data. When UDR is read, the Receive Data register is accessed and when UDR is written, the Transmit Data register is accessed. If 9-bit data word is selected (the CHR9 bit in the UART Control Register, UCR is set), the RXB8 bit in UCR is loaded with bit 9 in the Transmit Shift register when data is transferred to UDR.

If, after having received a character, the UDR register has not been read since the last receive, the OverRun (OR) flag in UCR is set. This means that the last data byte shifted into the shift register could not be transferred to UDR and has been lost. The OR bit is buffered and is updated when the valid data byte in UDR is read. Thus, the user should always check the OR bit after reading the UDR register in order to detect any overruns if the baud rate is high or CPU load is high.

When the RXEN bit in the UCR register is cleared (zero), the receiver is disabled. This means that the PD0 pin can be used as a general I/O pin. When RXEN is set, the UART Receiver will be connected to PD0, which is forced to be an input pin regardless of the setting of the DDD0 bit in DDRD. When PD0 is forced to input by the UART, the PORTD0 bit can still be used to control the pull-up resistor on the pin.

When the CHR9 bit in the UCR register is set, transmitted and received characters are 9 bits long, plus start and stop bits. The ninth data bit to be transmitted is the TXB8 bit in UCR register. This bit must be set to the wanted value before a transmission is initiated by writing to the UDR register. The ninth data bit received is the RXB8 bit in the UCR register.





UART Control

UART I/O Data Register - UDR



The UDR register is actually two physically separate registers sharing the same I/O address. When writing to the register, the UART Transmit Data register is written. When reading from UDR, the UART Receive Data register is read.

UART Status Register – USR

Bit	7	6	5	4	3	2	1	0	_
\$0B (\$2B)	RXC	TXC	UDRE	FE	OR	-	-	-	USR
Read/Write	R	R/W	R	R	R	R	R	R	-
Initial Value	0	0	1	0	0	0	0	0	

The USR register is a read-only register providing information on the UART status.

Bit 7 – RXC: UART Receive Complete

This bit is set (one) when a received character is transferred from the Receiver Shift register to UDR. The bit is set regardless of any detected framing errors. When the RXCIE bit in UCR is set, the UART Receive Complete interrupt will be executed when RXC is set (one). RXC is cleared by reading UDR. When interrupt-driven data reception is used, the UART Receive Complete Interrupt routine must read UDR in order to clear RXC, otherwise a new interrupt will occur once the interrupt routine terminates.

Bit 6 – TXC: UART Transmit Complete

This bit is set (one) when the entire character (including the stop bit) in the Transmit Shift register has been shifted out and no new data has been written to UDR. This flag is especially useful in half-duplex communications interfaces, where a transmitting application must enter receive mode and free the communications bus immediately after completing the transmission.

When the TXCIE bit in UCR is set, setting of TXC causes the UART Transmit Complete interrupt to be executed. TXC is cleared by hardware when executing the corresponding interrupt handling vector. Alternatively, the TXC bit is cleared (zero) by writing a logical "1" to the bit.

• Bit 5 – UDRE: UART Data Register Empty

This bit is set (one) when a character written to UDR is transferred to the Transmit Shift register. Setting of this bit indicates that the transmitter is ready to receive a new character for transmission.

When the UDRIE bit in UCR is set, the UART Transmit Complete interrupt to be executed as long as UDRE is set. UDRE is cleared by writing UDR. When interrupt-driven data transmission is used, the UART Data Register Empty Interrupt routine must write UDR in order to clear UDRE, otherwise a new interrupt will occur once the interrupt routine terminates.

UDRE is set (one) during reset to indicate that the transmitter is ready.

• Bit 4 – FE: Framing Error

This bit is set if a Framing Error condition is detected, i.e., when the stop bit of an incoming character is zero.



Analog Comparator

The Analog Comparator compares the input values on the positive input PB2 (AIN0) and negative input PB3 (AIN1). When the voltage on the positive input PB2 (AIN0) is higher than the voltage on the negative input PB3 (AIN1), the Analog Comparator Output (ACO) is set (one). The comparator's output can be set to trigger the Timer/Counter1 Input Capture function. In addition, the comparator can trigger a separate interrupt, exclusive to the Analog Comparator. The user can select Interrupt triggering on comparator output rise, fall or toggle. A block diagram of the comparator and its surrounding logic is shown in Figure 44.





• Bit 7 – ACD: Analog Comparator Disable

When this bit is set (one), the power to the Analog Comparator is switched off. This bit can be set at any time to turn off the Analog Comparator. When changing the ACD bit, the Analog Comparator interrupt must be disabled by clearing the ACIE bit in ACSR. Otherwise an interrupt can occur when the bit is changed.

• Bit 6 - Res: Reserved Bit

This bit is a reserved bit in the AT90S8535 and will always read as zero.

• Bit 5 – ACO: Analog Comparator Output

ACO is directly connected to the comparator output.

• Bit 4 – ACI: Analog Comparator Interrupt Flag

This bit is set (one) when a comparator output event triggers the interrupt mode defined by ACI1 and ACI0. The Analog Comparator Interrupt routine is executed if the ACIE bit is set (one) and the I-bit in SREG is set (one). ACI is cleared by hardware when executing the corresponding interrupt handling vector. Alternatively, ACI is cleared by writing a logical "1" to the flag.

• Bit 3 – ACIE: Analog Comparator Interrupt Enable

When the ACIE bit is set (one) and the I-bit in the Status Register is set (one), the Analog Comparator interrupt is activated. When cleared (zero), the interrupt is disabled.

Alternate Functions of Port C When the AS2 bit in ASSR is set (one) to enable asynchronous clocking of Timer/Counter2, pins PC6 and PC7 are disconnected from the port. In this mode, a crystal oscillator is connected to the pins and the pins cannot be used as I/O pins.

Port C Schematics Note that all port pins are synchronized. The synchronization latch is, however, not shown in the figure.

Figure 58. Port C Schematic Diagram (Pins PC0 - PC5)











Table 37. Pin Name Mapping

Signal Name in Programming Mode	Pin Name	I/O	Function
RDY/BSY	PD1	0	0: Device is busy programming, 1: Device is ready for new command
ŌĒ	PD2	I	Output Enable (Active low)
WR	PD3	Ι	Write Pulse (Active low)
BS	PD4	I	Byte Select ("0" selects low byte, "1" selects high byte)
XA0	PD5	Ι	XTAL Action Bit 0
XA1	PD6	Ι	XTAL Action Bit 1
DATA	PB7 - 0	I/O	Bi-directional Data Bus (Output when \overline{OE} is low)

Table 38. XA1 and XA0 Coding

XA1	XA0	Action when XTAL1 is Pulsed
0	0	Load Flash or EEPROM Address (high or low address byte determined by BS)
0	1	Load Data (High or low data byte for Flash determined by BS)
1	0	Load Command
1	1	No Action, Idle

Table 39. Command Byte Bit Coding

Command Byte	Command Executed
1000 0000	Chip Erase
0100 0000	Write Fuse Bits
0010 0000	Write Lock Bits
0001 0000	Write Flash
0001 0001	Write EEPROM
0000 1000	Read Signature Bytes
0000 0100	Read Lock and Fuse Bits
0000 0010	Read Flash
0000 0011	Read EEPROM

Enter Programming Mode

The following algorithm puts the device in Parallel Programming Mode:

- 1. Apply supply voltage according to Table 36, between V_{CC} and GND.
- 2. Set the $\overline{\text{RESET}}$ and BS pin to "0" and wait at least 100 ns.
- 3. Apply 11.5 12.5V to RESET. Any activity on BS within 100 ns after +12V has been applied to RESET, will cause the device to fail entering programming mode.



- 1. Set BS to "1". This selects high data.
- 2. Give WR a negative pulse. This starts programming of the data byte. RDY/BSY goes low.
- 3. Wait until RDY/BSY goes high to program the next byte.

(See Figure 69 for signal waveforms.)

The loaded command and address are retained in the device during programming. For efficient programming, the following should be considered:

- The command needs only be loaded once when writing or reading multiple memory locations.
- Address high byte needs only be loaded before programming a new 256-word page in the Flash.
- Skip writing the data value \$FF, that is, the contents of the entire Flash and EEPROM after a Chip Erase.

These considerations also apply to EEPROM programming and Flash, EEPROM and signature byte reading.



Figure 68. Programming the Flash Waveforms

- If a Chip Erase is performed (must be done to erase the Flash), wait t_{WD_ERASE} after the instruction, give RESET a positive pulse and start over from step 2. See Table 44 for t_{WD_ERASE} value.
- 5. The Flash or EEPROM array is programmed one byte at a time by supplying the address and data together with the appropriate Write instruction. An EEPROM memory location is first automatically erased before new data is written. Use Data Polling to detect when the next byte in the Flash or EEPROM can be written. If polling is not used, wait t_{WD_PROG} before transmitting the next instruction. See Table 45 for t_{WD_PROG} value. In an erased device, no \$FFs in the data file(s) needs to be programmed.
- 6. Any memory location can be verified by using the Read instruction that returns the content at the selected address at the serial output MISO (PB6) pin.
- 7. At the end of the programming session, **RESET** can be set high to commence normal operation.
- 8. Power-off sequence (if needed):

Set XTAL1 to "0" (if a crystal is not used). Set $\overline{\text{RESET}}$ to "1".

Turn V_{CC} power off.

Data Polling EEPROMWhen a byte is being programmed into the EEPROM, reading the address location
being programmed will give the value P1 until the auto-erase is finished and then the
value P2. See Table 41 for P1 and P2 values.

At the time the device is ready for a new EEPROM byte, the programmed value will read correctly. This is used to determine when the next byte can be written. This will not work for the values P1 and P2, so when programming these values, the user will have to wait for at least the prescribed time t_{WD_PROG} before programming the next byte. See Table 45 for t_{WD_PROG} value. As a chip-erased device contains \$FF in all locations, programming of addresses that are meant to contain \$FF can be skipped. This does not apply if the EEPROM is reprogrammed without first chip-erasing the device.

Table 41. Read Back Value during EEPROM Polling

Par	t	P1	P2
AT9	00S/LS8535	\$00	\$FF

Data Polling Flash

When a byte is being programmed into the Flash, reading the address location being programmed will give the value FF. At the time the device is ready for a new byte, the programmed value will read correctly. This is used to determine when the next byte can be written. This will not work for the value FF, so when programming this value, the user will have to wait for at least t_{WD_PROG} before programming the next byte. As a chiperased device contains FF in all locations, programming of addresses that are meant to contain FF can be skipped.

Figure 72. Serial Programming Waveforms





AT90S/LS8535

Serial Programming Characteristics

Figure 73. Serial Programming Timing



Table 43. Serial Programming Characteristics, $T_A = -40^{\circ}C$ to $85^{\circ}C$, $V_{CC} = 2.7 - 6.0V$ (unless otherwise noted)

Symbol	Parameter	Min	Тур	Max	Units
1/t _{CLCL}	Oscillator Frequency ($V_{CC} = 2.7 - 6.0V$)	0		4.0	MHz
t _{CLCL}	Oscillator Period ($V_{CC} = 2.7 - 4.0V$)	250.0			ns
1/t _{CLCL}	Oscillator Frequency ($V_{CC} = 4.0 - 6.0V$)	0		8.0	MHz
t _{CLCL}	Oscillator Period ($V_{CC} = 4.0 - 6.0V$)	125.0			ns
t _{SHSL}	SCK Pulse Width High	2.0 t _{CLCL}			ns
t _{SLSH}	SCK Pulse Width Low	2.0 t _{CLCL}			ns
t _{ovsH}	MOSI Setup to SCK High	t _{CLCL}			ns
t _{SHOX}	MOSI Hold after SCK High	2.0 t _{CLCL}			ns
t _{SLIV}	SCK Low to MISO Valid	10.0	16.0	32.0	ns

Table 44. Minimum Wait Delay after the Chip Erase instruction

Symbol	3.2V	3.6V	4.0V	5.0V
t _{WD_ERASE}	18 ms	14 ms	12 ms	8 ms

Table 45.	Minimum	Wait Delay	after Writing	g a Flash o	or EEPROM Locatio	'n
-----------	---------	------------	---------------	-------------	-------------------	----

	,	•		
Symbol	3.2V	3.6V	4.0V	5.0V
t _{wd_prog}	9 ms	7 ms	6 ms	4 ms







Figure 84. Analog Comparator Offset Voltage vs. Common Mode Voltage







Figure 90. I/O Pin Source Current vs. Output Voltage













