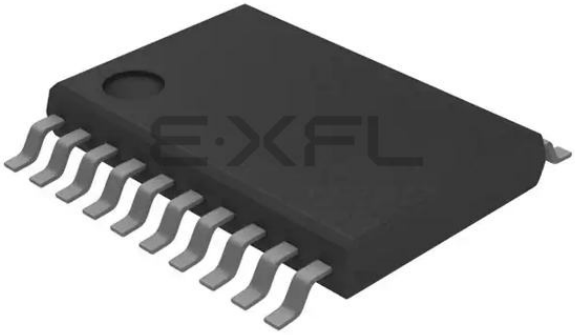

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	S08
Core Size	8-Bit
Speed	20MHz
Connectivity	LINbus, SCI, UART/USART
Peripherals	LVD, POR, PWM
Number of I/O	18
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 10x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-TSSOP (0.173", 4.40mm Width)
Supplier Device Package	20-TSSOP
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc9s08pl16ctj

1 Ordering information

The following table summarizes the part numbers of the devices covered by this document.

Table 1. Ordering information

Part Number	MC9S08PL16CLC	MC9S08PL16CTJ	MC9S08PL16CTG	MC9S08PL8CLC	MC9S08PL8CTJ	MC9S08PL8CTG
Max. frequency (MHz)	20	20	20	20	20	20
Flash memory (KB)	16	16	16	8	8	8
RAM (KB)	2	2	2	2	2	2
EEPROM (bytes)	256	256	256	256	256	256
10-bit ADC	12ch	10ch	6ch	12ch	10ch	6ch
16-bit FlexTimer	6ch + 2ch	6ch + 2ch	2ch + 2ch	6ch + 2ch	6ch + 2ch	2ch + 2ch
8-bit Modulo timer	1	1	1	1	1	1
RTC	Yes	Yes	Yes	Yes	Yes	Yes
SCI (LIN Capable)	2	1	1	2	1	1
Watchdog	Yes	Yes	Yes	Yes	Yes	Yes
CRC	Yes	Yes	Yes	Yes	Yes	Yes
KBI pins	8	8	8	8	8	8
GPIO	30	18	14	30	18	14
Package	32-LQFP	20-TSSOP	16-TSSOP	32-LQFP	20-TSSOP	16-TSSOP

2 Part identification

2.1 Description

Part numbers for the chip have fields that identify the specific part. You can use the values of these fields to determine the specific part you have received.

2.2 Format

Part numbers for this device have the following format:

MC 9 S08 PL AA B CC

2.3 Fields

This table lists the possible values for each field in the part number (not all combinations are valid):

Field	Description	Values
MC	Qualification status	• MC = fully qualified, general market flow
9	Memory	• 9 = flash based
S08	Core	• S08 = 8-bit CPU
PL	Device family	• PL
AA	Approximate flash size in KB	• 16 = 16 KB • 8 = 8 KB
B	Operating temperature range (°C)	• C = –40 to 85
CC	Package designator	• LC = 32-LQFP • TJ = 20-TSSOP • TG = 16-TSSOP

2.4 Example

This is an example part number:

MC9S08PL16CLC

3 Parameter Classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding, the following classification is used and the parameters are tagged accordingly in the tables where appropriate:

Table 2. Parameter Classifications

P	Those parameters are guaranteed during production testing on each individual device.
C	Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations.
T	Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category.
D	Those parameters are derived mainly from simulations.

NOTE

The classification is shown in the column labeled “C” in the parameter tables where appropriate.

4 Ratings

4.1 Thermal handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
T_{STG}	Storage temperature	–55	150	°C	1
T_{SDR}	Solder temperature, lead-free	—	260	°C	2

1. Determined according to JEDEC Standard JESD22-A103, *High Temperature Storage Life*.
2. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

4.2 Moisture handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
MSL	Moisture sensitivity level	—	3	—	1

1. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

4.3 ESD handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
V_{HBM}	Electrostatic discharge voltage, human body model	-6000	+6000	V	1
V_{CDM}	Electrostatic discharge voltage, charged-device model	-500	+500	V	2
I_{LAT}	Latch-up current at ambient temperature of 85°C	-100	+100	mA	

1. Determined according to JEDEC Standard JESD22-A114, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*.
2. Determined according to JEDEC Standard JESD22-C101, *Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components*.

4.4 Voltage and current operating ratings

Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the limits specified in below table may affect device reliability or cause permanent damage to the device. For functional operating conditions, refer to the remaining tables in this document.

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for instance, either V_{SS} or V_{DD}) or the programmable pullup resistor associated with the pin is enabled.

Symbol	Description	Min.	Max.	Unit
V_{DD}	Supply voltage	–0.3	6.0	V
I_{DD}	Maximum current into V_{DD}	—	120	mA
V_{DIO}	Digital input voltage (except $\overline{\text{RESET}}$, EXTAL, XTAL, or true open drain pin)	–0.3	V_{DD} + 0.3	V
	Digital input voltage (true open drain pin)	-0.3	6	V
V_{AIO}	Analog[1], $\overline{\text{RESET}}$, EXTAL, and XTAL input voltage	–0.3	V_{DD} + 0.3	V
I_D	Instantaneous maximum current single pin limit (applies to all port pins)	–25	25	mA
V_{DDA}	Analog supply voltage	V_{DD} – 0.3	V_{DD} + 0.3	V

1. All digital I/O pins, except open-drain pin , are internally clamped to V_{SS} and V_{DD}. is only clamped to V_{SS}.

5 General

5.1 Nonswitching electrical specifications

5.1.1 DC characteristics

This section includes information about power supply requirements and I/O pin characteristics.

Table 3. DC characteristics

Symbol	C	Descriptions			Min	Typical[1]	Max	Unit
—	—	Operating voltage		—	2.7	—	5.5	V
V_{OH}	C	Output high voltage	All I/O pins, standard-drive strength	5 V, I_{load} = -5 mA	V_{DD} - 0.8	—	—	V
	C			3 V, I_{load} = -2.5 mA	V_{DD} - 0.8	—	—	V
I_{OHT}	D	Output high current	Max total I_{OH} for all ports	5 V	—	—	-100	mA
				3 V	—	—	-50	
V_{OL}	C	Output low voltage	All I/O pins, standard-drive strength	5 V, I_{load} = 5 mA	—	—	0.8	V
	C			3 V, I_{load} = 2.5 mA	—	—	0.8	V
I_{OLT}	D	Output low current	Max total I_{OL} for all ports	5 V	—	—	100	mA
				3 V	—	—	50	
V_{IH}	P	Input high voltage	All digital inputs	V_{DD}>4.5V	0.70 × V_{DD}	—	—	V
	C			V_{DD}>2.7V	0.75 × V_{DD}	—	—	
V_{IL}	P	Input low voltage	All digital inputs	V_{DD}>4.5V	—	—	0.30 × V_{DD}	V
	C			V_{DD}>2.7V	—	—	0.35 × V_{DD}	
V_{hys}	C	Input hysteresis	All digital inputs	—	0.06 × V_{DD}	—	—	mV
$\lvert I_{In} \rvert$	P	Input leakage current	All input only pins (per pin)	V_{IN} = V_{DD} or V_{SS}	—	0.1	1	µA
$\lvert I_{OZ} \rvert$	P	Hi-Z (off-state) leakage current	All input/output (per pin)	V_{IN} = V_{DD} or V_{SS}	—	0.1	1	µA
$\lvert I_{OZTOT} \rvert$	C	Total leakage combined for all inputs and Hi-Z pins	All input only and I/O	V_{IN} = V_{DD} or V_{SS}	—	—	2	µA

Table continues on the next page...

Table 3. DC characteristics (continued)

Symbol	C	Descriptions			Min	Typical[1]	Max	Unit
R_{PU}	P	Pullup resistors	All digital inputs, when enabled (all I/O pins other than PTA2 and PTA3)	—	30.0	—	50.0	kΩ
R_{PU}[2]	P	Pullup resistors	PTA2 and PTA3 pin	—	30.0	—	60.0	kΩ
I_{IC}	D	DC injection current[3, 4, 5]	Single pin limit	$V_{IN} < V_{SS}$, $V_{IN} > V_{DD}$	-0.2	—	2	mA
			Total MCU limit, includes sum of all stressed pins		-5	—	25	
C_{In}	C	Input capacitance, all pins		—	—	—	7	pF
V_{RAM}	C	RAM retention voltage		—	2.0	—	—	V

1. Typical values are measured at 25 °C. Characterized, not tested.
2. The specified resistor value is the actual value internal to the device. The pullup value may appear higher when measured externally on the pin.
3. All functional non-supply pins, except for PTA2 and PTA3, are internally clamped to V_{SS} and V_{DD}.
4. Input must be current-limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the large one.
5. Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If the positive injection current ($V_{In} > V_{DD}$) is higher than I_{DD}, the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure that external V_{DD} load will shunt current higher than maximum injection current when the MCU is not consuming power, such as no system clock is present, or clock rate is very low (which would reduce overall power consumption).

Table 4. LVD and POR Specification

Symbol	C	Description		Min	Typ	Max	Unit
V_{POR}	D	POR re-arm voltage[1, 2]		1.5	1.75	2.0	V
V_{LVDH}	C	Falling low-voltage detect threshold - high range (LVDV = 1)[3]		4.2	4.3	4.4	V
V_{LVW1H}	C	Falling low-voltage warning threshold - high range	Level 1 falling (LVWV = 00)	4.3	4.4	4.5	V
V_{LVW2H}	C		Level 2 falling (LVWV = 01)	4.5	4.5	4.6	V
V_{LVW3H}	C		Level 3 falling (LVWV = 10)	4.6	4.6	4.7	V
V_{LVW4H}	C		Level 4 falling (LVWV = 11)	4.7	4.7	4.8	V
V_{HYSH}	C	High range low-voltage detect/warning hysteresis		—	100	—	mV
V_{LVDL}	C	Falling low-voltage detect threshold - low range (LVDV = 0)		2.56	2.61	2.66	V

Table continues on the next page...

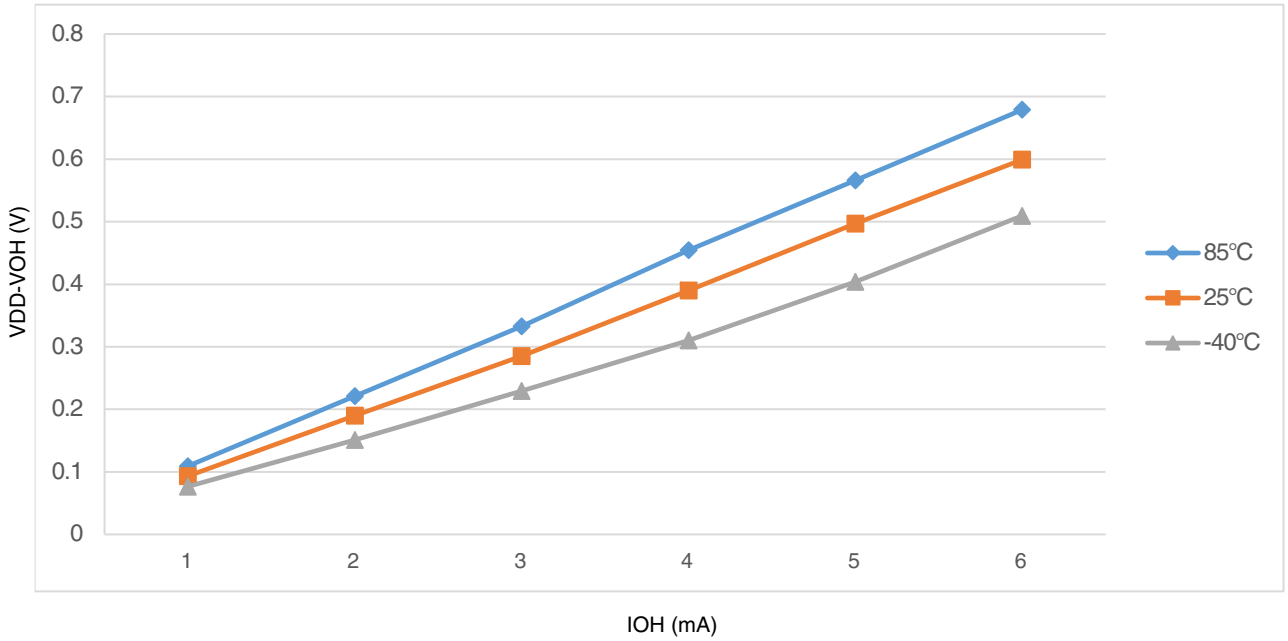


Figure 2. Typical I_{OH} Vs. V_{DD}-V_{OH} (standard drive strength) (V_{DD} = 3 V)

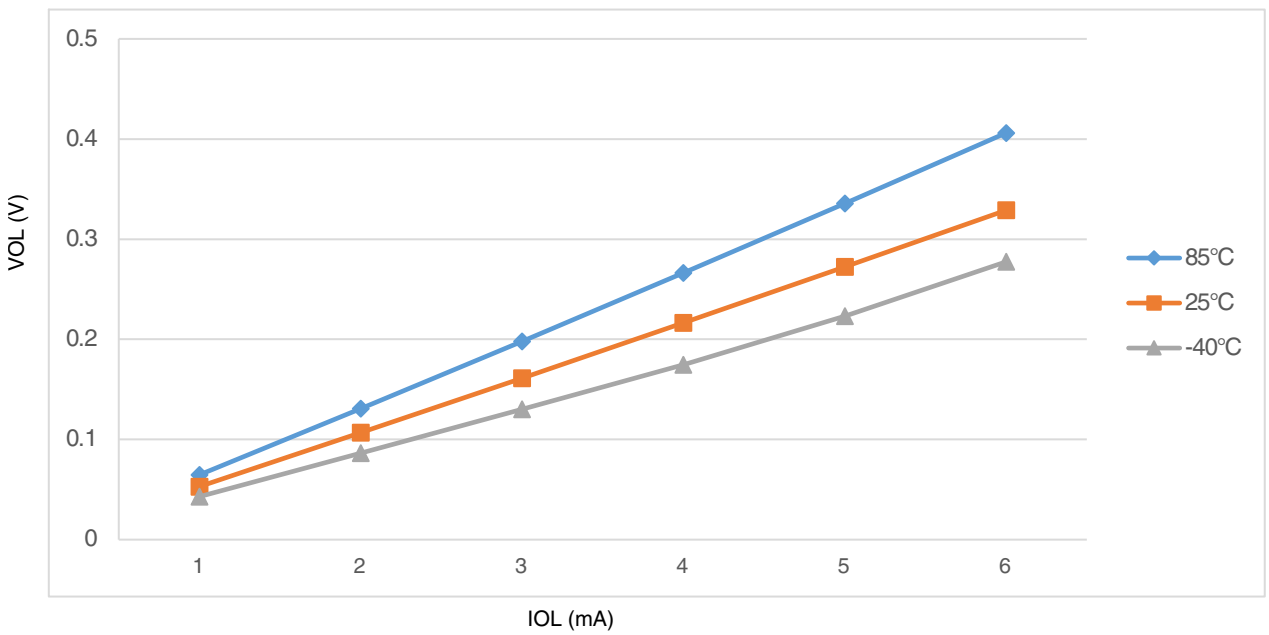


Figure 3. Typical I_{OL} Vs. V_{OL} (standard drive strength) (V_{DD} = 5 V)

5.2 Switching specifications

5.2.1 Control timing

Table 6. Control timing

Num	C	Rating		Symbol	Min	Typical[1]	Max	Unit
1	P	Bus frequency (t_{cyc} = 1/f_{Bus})		f_{Bus}	DC	—	20	MHz
2	C	Internal low power oscillator frequency		f_{LPO}	—	1.0	—	KHz
3	D	External reset pulse width[2]		t_{extrst}	1.5 × t_{cyc}	—	—	ns
4	D	Reset low drive		t_{rstdrv}	34 × t_{cyc}	—	—	ns
5	D	BKGD/MS setup time after issuing background debug force reset to enter user or BDM modes		t_{MSSU}	500	—	—	ns
6	D	BKGD/MS hold time after issuing background debug force reset to enter user or BDM modes[3]		t_{MSH}	100	—	—	ns
7	D	IRQ pulse width	Asynchronous path[2]	t_{ILIH}	100	—	—	ns
	D		Synchronous path[4]	t_{IHIL}	1.5 × t_{cyc}	—	—	ns
8	D	Keyboard interrupt pulse width	Asynchronous path[2]	t_{ILIH}	100	—	—	ns
	D		Synchronous path	t_{IHIL}	1.5 × t_{cyc}	—	—	ns
9	C	Port rise and fall time - standard drive strength (load = 50 pF)[5]	—	t_{Rise}	—	10.2	—	ns
	C			t_{Fall}	—	9.5	—	ns

1. Typical values are based on characterization data at V_{DD} = 5.0 V, 25 °C unless otherwise stated.
2. This is the shortest pulse that is guaranteed to be recognized as a reset pin request.
3. To enter BDM mode following a POR, BKGD/MS must be held low during the powerup and for a hold time of t_{MSH} after V_{DD} rises above V_{LVD}.
4. This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized. In stop mode, the synchronizer is bypassed so shorter pulses can be recognized.
5. Timing is shown with respect to 20% V_{DD} and 80% V_{DD} levels. Temperature range -40 °C to 85 °C.

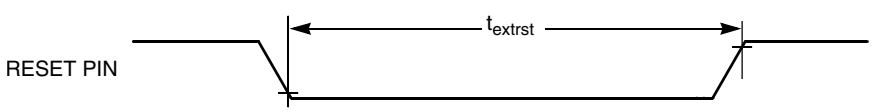


Figure 5. Reset timing

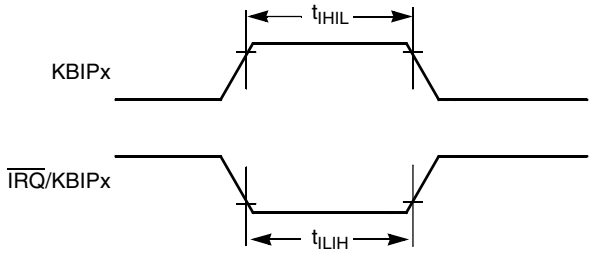


Figure 6. IRQ/KBIPx timing

5.2.2 Debug trace timing specifications

Table 7. Debug trace operating behaviors

Symbol	Description	Min.	Max.	Unit
t_{cyc}	Clock period	Frequency dependent		MHz
t_{wl}	Low pulse width	2	—	ns
t_{wh}	High pulse width	2	—	ns
t_r	Clock and data rise time	—	3	ns
t_f	Clock and data fall time	—	3	ns
t_s	Data setup	3	—	ns
t_h	Data hold	2	—	ns

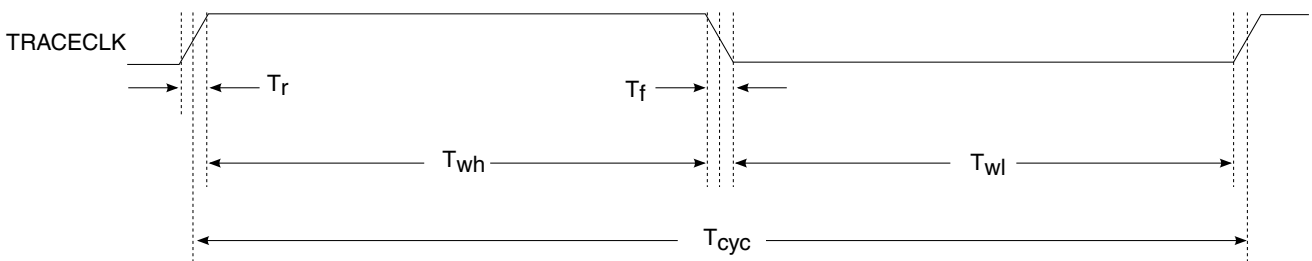


Figure 7. TRACE_CLKOUT specifications

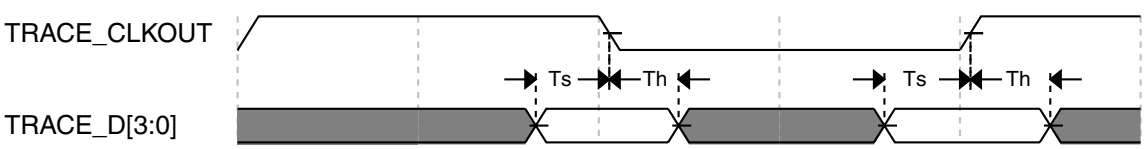


Figure 8. Trace data specifications

5.2.3 FTM module timing

Synchronizer circuits determine the shortest input pulses that can be recognized or the fastest clock that can be used as the optional external source to the timer counter. These synchronizers operate from the current bus rate clock.

Table 8. FTM input timing

No.	C	Function	Symbol	Min	Max	Unit
1	D	External clock frequency	f_{TCLK}	0	$f_{Bus}/4$	Hz
2	D	External clock period	t_{TCLK}	4	—	t_{cyc}
3	D	External clock high time	t_{clkh}	1.5	—	t_{cyc}
4	D	External clock low time	t_{clkl}	1.5	—	t_{cyc}
5	D	Input capture pulse width	t_{ICPW}	1.5	—	t_{cyc}

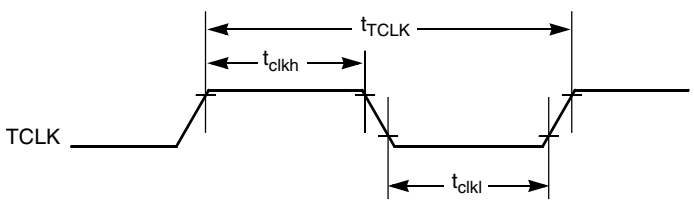


Figure 9. Timer external clock

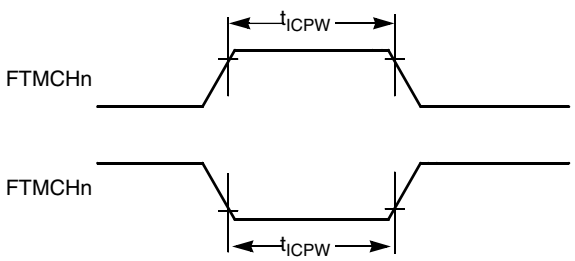


Figure 10. Timer input capture pulse

5.3 Thermal specifications

5.3.1 Thermal characteristics

This section provides information about operating temperature range, power dissipation, and package thermal resistance. Power dissipation on I/O pins is usually small compared to the power dissipation in on-chip logic and voltage regulator circuits, and it is user-determined rather than being controlled by the MCU design. To take $P_{I/O}$ into account in power calculations, determine the difference between actual pin voltage and V_{SS} or V_{DD} and multiply by the pin current for each I/O pin. Except in cases of unusually high pin current (heavy loads), the difference between pin voltage and V_{SS} or V_{DD} will be very small.

Table 9. Thermal characteristics

Rating	Symbol	Value	Unit
Operating temperature range (packaged)	T_A[1]	T_L to T_H -40 to 85	°C
Junction temperature range	T_J	-40 to 105	°C
Thermal resistance single-layer board			
32-pin LQFP	$R_{\theta JA}$	88	°C/W
20-pin TSSOP	$R_{\theta JA}$	116	°C/W
16-pin TSSOP	$R_{\theta JA}$	130	°C/W
Thermal resistance four-layer board			
32-pin LQFP	$R_{\theta JA}$	59	°C/W
20-pin TSSOP	$R_{\theta JA}$	76	°C/W
16-pin TSSOP	$R_{\theta JA}$	87	°C/W

1. Maximum T_A can be exceeded only if the user ensures that T_J does not exceed the maximum. The simplest method to determine T_J is: $T_J = T_A + R_{\theta JA}$ x chip power dissipation.

6 Peripheral operating requirements and behaviors

Table 10. XOSC and ICS specifications (temperature range = -40 to 85 °C ambient) (continued)

Num	C	Characteristic	Symbol	Min	Typical[1]	Max	Unit
13	C	Long term jitter of DCO output clock (averaged over 2 ms interval)[8]	C_{Jitter}	—	0.02	0.2	$\%f_{dco}$

1. Data in Typical column was characterized at 5.0 V, 25 °C or is typical recommended value.
2. When ICS is configured for FEE or FBE mode, input clock source must be divisible using RDIV to within the range of 31.25 kHz to 39.0625 kHz.
3. See crystal or resonator manufacturer's recommendation.
4. Load capacitors (C_1,C_2), feedback resistor (R_F) and series resistor (R_S) are incorporated internally when RANGE = HGO = 0.
5. This parameter is characterized and not tested on each device.
6. Proper PC board layout procedures must be followed to achieve specifications.
7. This specification applies to any time the FLL reference source or reference divider is changed, trim value changed, or changing from FLL disabled (FBELP, FBILP) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.
8. Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{Bus}. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the FLL circuitry via V_{DD} and V_{SS} and variation in crystal oscillator frequency increase the C_{Jitter} percentage for a given interval.

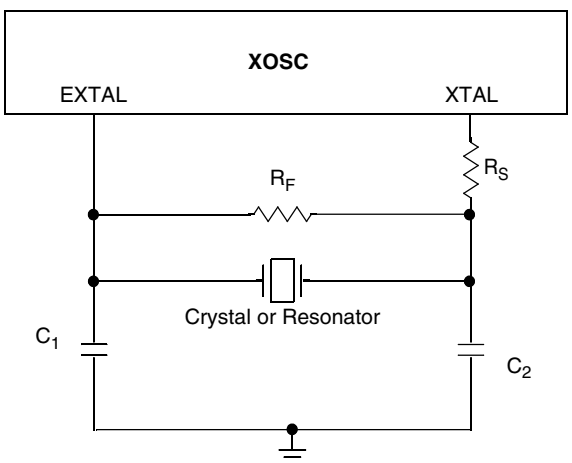


Figure 11. Typical crystal or resonator circuit

6.2 NVM specifications

This section provides details about program/erase times and program/erase endurance for the flash and EEPROM memories.

Table 11. Flash characteristics

C	Characteristic	Symbol	Min[1]	Typical[2]	Max[3]	Unit[4]
D	Supply voltage for program/erase -40 °C to 85 °C	$V_{prog/erase}$	2.7	—	5.5	V
D	Supply voltage for read operation	V_{Read}	2.7	—	5.5	V

Table continues on the next page...

Table 11. Flash characteristics (continued)

C	Characteristic	Symbol	Min[1]	Typical[2]	Max[3]	Unit[4]
D	NVM Bus frequency	f_{NVMBUS}	1	—	25	MHz
D	NVM Operating frequency	f_{NVMOP}	0.8	1	1.05	MHz
D	Erase Verify All Blocks	t_{VFYALL}	—	—	17338	t_{cyc}
D	Erase Verify Flash Block	t_{RD1BLK}	—	—	16913	t_{cyc}
D	Erase Verify EEPROM Block	t_{RD1BLK}	—	—	810	t_{cyc}
D	Erase Verify Flash Section	t_{RD1SEC}	—	—	484	t_{cyc}
D	Erase Verify EEPROM Section	$t_{DRD1SEC}$	—	—	555	t_{cyc}
D	Read Once	t_{RDONCE}	—	—	450	t_{cyc}
D	Program Flash (2 word)	t_{PGM2}	0.12	0.12	0.29	ms
D	Program Flash (4 word)	t_{PGM4}	0.20	0.21	0.46	ms
D	Program Once	$t_{PGMONCE}$	0.20	0.21	0.21	ms
D	Program EEPROM (1 Byte)	t_{DPGM1}	0.10	0.10	0.27	ms
D	Program EEPROM (2 Byte)	t_{DPGM2}	0.17	0.18	0.43	ms
D	Program EEPROM (3 Byte)	t_{DPGM3}	0.25	0.26	0.60	ms
D	Program EEPROM (4 Byte)	t_{DPGM4}	0.32	0.33	0.77	ms
D	Erase All Blocks	t_{ERSALL}	96.01	100.78	101.49	ms
D	Erase Flash Block	t_{ERSBLK}	95.98	100.75	101.44	ms
D	Erase Flash Sector	t_{ERSPG}	19.10	20.05	20.08	ms
D	Erase EEPROM Sector	t_{DERSPG}	4.81	5.05	20.57	ms
D	Unsecure Flash	t_{UNSECU}	96.01	100.78	101.48	ms
D	Verify Backdoor Access Key	t_{VFYKEY}	—	—	464	t_{cyc}
D	Set User Margin Level	t_{MLOADU}	—	—	407	t_{cyc}
C	FLASH Program/erase endurance T_L to T_H = -40 °C to 85 °C	n_{FLPE}	10 k	100 k	—	Cycles
C	EEPROM Program/erase endurance TL to TH = -40 °C to 85 °C	n_{FLPE}	50 k	500 k	—	Cycles
C	Data retention at an average junction temperature of T_{Javg} = 85°C after up to 10,000 program/erase cycles	t_{D_ret}	15	100	—	years

1. Minimum times are based on maximum f_{NVMOP} and maximum f_{NVMBUS}
2. Typical times are based on typical f_{NVMOP} and maximum f_{NVMBUS}
3. Maximum times are based on typical f_{NVMOP} and typical f_{NVMBUS} plus aging
4. $t_{cyc} = 1 / f_{NVMBUS}$

Program and erase operations do not require any special power sources other than the normal V_{DD} supply. For more detailed information about program/erase operations, see the Memory section.

6.3 Analog

6.3.1 ADC characteristics

Table 12. 5 V 10-bit ADC operating conditions

Characteristic	Conditions	Symb	Min	Typ[1]	Max	Unit	Comment
Supply voltage	Absolute	V_{DDA}	2.7	—	5.5	V	—
	Delta to V_{DD} (V_{DD}-V_{DDAD})	ΔV_{DDA}	-100	0	+100	mV	
Ground voltage	Delta to V_{SS} (V_{SS}-V_{SSA})[2]	ΔV_{SSA}	-100	0	+100	mV	
Input voltage		V_{ADIN}	V_{REFL}	—	V_{REFH}	V	
Input capacitance		C_{ADIN}	—	4.5	5.5	pF	
Input resistance		R_{ADIN}	—	3	5	kΩ	—
Analog source resistance	10-bit mode • f_{ADCK} > 4 MHz • f_{ADCK} < 4 MHz	R_{AS}	— —	— —	5 10	kΩ	External to MCU
	8-bit mode (all valid f_{ADCK})		—	—	10		
ADC conversion clock frequency	High speed (ADLPC=0)	f_{ADCK}	0.4	—	8.0	MHz	—
	Low power (ADLPC=1)		0.4	—	4.0		

1. Typical values assume V_{DDA} = 5.0 V, Temp = 25°C, f_{ADCK}=1.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.
2. DC potential difference.

Table 13. 10-bit ADC Characteristics (V_{REFH} = V_{DDA}, V_{REFL} = V_{SSA}) (continued)

Characteristic	Conditions	C	Symb	Min	Typ[1]	Max	Unit
	Low power (ADLPC = 1)			1.25	2	3.3	
Conversion time (including sample time)	Short sample (ADLSMP = 0)	T	t_{ADC}	—	20	—	ADCK cycles
	Long sample (ADLSMP = 1)			—	40	—	
Sample time	Short sample (ADLSMP = 0)	T	t_{ADS}	—	3.5	—	ADCK cycles
	Long sample (ADLSMP = 1)			—	23.5	—	
Total unadjusted Error[2]	10-bit mode	P	E_{TUE}	—	±1.5	±2.0	LSB[3]
	8-bit mode	P		—	±0.7	±1.0	
Differential Non-Linearity	10-bit mode[4]	P	DNL	—	±0.25	±0.5	LSB[3]
	8-bit mode[4]	P		—	±0.15	±0.25	
Integral Non-Linearity	10-bit mode	T	INL	—	±0.3	±0.5	LSB[3]
	8-bit mode	T		—	±0.15	±0.25	
Zero-scale error[5]	10-bit mode	P	E_{ZS}	—	±0.25	±1.0	LSB[3]
	8-bit mode	P		—	±0.65	±1.0	
Full-scale error[6]	10-bit mode	T	E_{FS}	—	±0.5	±1.0	LSB[3]
	8-bit mode	T		—	±0.5	±1.0	
Quantization error	≤10 bit modes	D	E_Q	—	—	±0.5	LSB[3]
Input leakage error[7]	all modes	D	E_{IL}	I_{In} * R_{AS}			mV
Temp sensor slope	-40°C– 25°C	D	m	—	3.266	—	mV/°C
	25°C– 85°C			—	3.638	—	
Temp sensor voltage	25°C	D	V_{TEMP25}	—	1.396	—	V

1. Typical values assume V_{DDA} = 5.0 V, Temp = 25°C, f_{ADCK}=1.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.
2. Includes quantization.
3. 1 LSB = (V_{REFH} - V_{REFL})/2^N
4. Monotonicity and no-missing-codes guaranteed in 10-bit and 8-bit modes
5. V_{ADIN} = V_{SSA}
6. V_{ADIN} = V_{DDA}
7. I_{In} = leakage current (refer to DC characteristics)

7 Dimensions

7.1 Obtaining package dimensions

Package dimensions are provided in package drawings.

To find a package drawing, go to nxp.com and perform a keyword search for the drawing's document number:

If you want the drawing for this package	Then use this document number
16-pin TSSOP	98ASH70247A
20-pin TSSOP	98ASH70169A
32-pin LQFP	98ASH70029A

8 Pinout

8.1 Signal multiplexing and pin assignments

The following table shows the signals available on each pin and the locations of these pins on the devices supported by this document. The Port Control Module is responsible for selecting which ALT functionality is available on each pin.

Table 14. Pin availability by package pin-count

Pin Number			Lowest Priority <-- --> Highest				
32-LQFP	20-TSSOP	16-TSSOP	Port Pin	Alt 1	Alt 2	Alt 3	Alt 4
1	—	—	PTD1	—	FTM2CH3	—	—
2	—	—	PTD0	—	FTM2CH2	—	—
3	—	—	PTE4	—	TCLK2	—	—
4	3	3	—	—	—	—	V_{DD}
5	4	4	—	—	—	—	V_{SS}
6	5	5	PTB7	—	—	—	EXTAL
7	6	6	PTB6	—	—	—	XTAL
8	7	7	PTB5	—	FTM2CH5	—	—
9	8	8	PTB4	—	FTM2CH4	—	—
10	9	—	PTC3	—	FTM2CH3	ADP11	—
11	10	—	PTC2	—	FTM2CH2	ADP10	—
12	—	—	PTD7	—	—	—	—
13	—	—	PTD6	—	—	—	—
14	11	—	PTC1	—	FTM2CH1	ADP9	—
15	12	—	PTC0	—	FTM2CH0	ADP8	—
16	13	9	PTB3	KBI0P7	—	ADP7	—
17	14	10	PTB2	KBI0P6	—	ADP6	—
18	15	11	PTB1	KBI0P5	TXD0	ADP5	—
19	16	12	PTB0	KBI0P4	RXD0	ADP4	—

Table continues on the next page...

Table 14. Pin availability by package pin-count (continued)

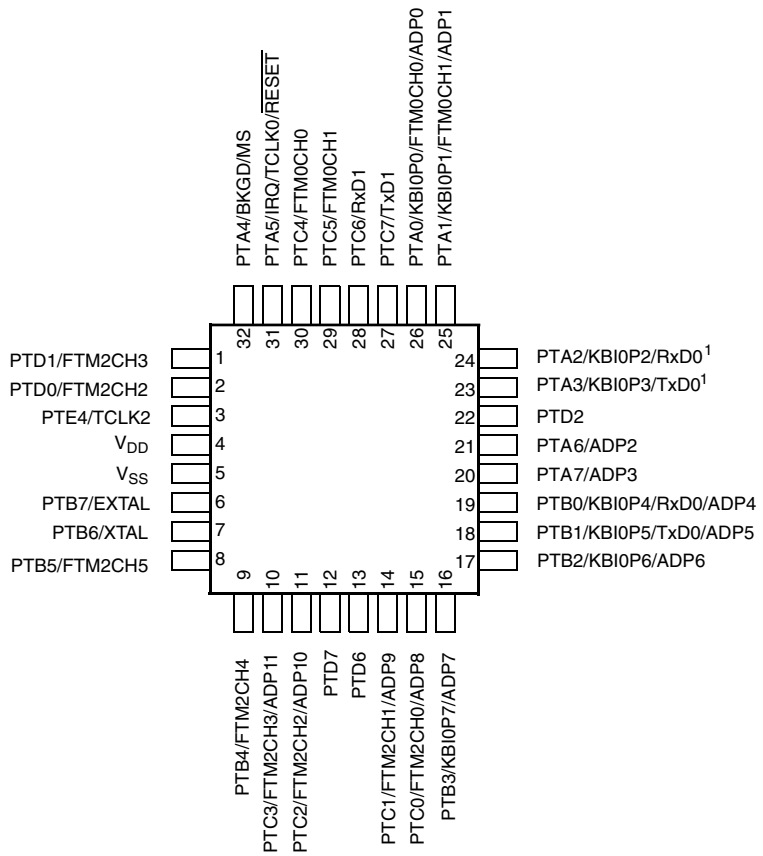
Pin Number			Lowest Priority <-- --> Highest				
32-LQFP	20-TSSOP	16-TSSOP	Port Pin	Alt 1	Alt 2	Alt 3	Alt 4
20	—	—	PTA7	—	—	ADP3	—
21	—	—	PTA6	—	—	ADP2	—
22	—	—	PTD2	—	—	—	—
23	17	13	PTA3[1]	KBI0P3	TXD0	—	—
24	18	14	PTA2[1]	KBI0P2	RXD0	—	—
25	19	15	PTA1	KBI0P1	FTM0CH1	—	ADP1
26	20	16	PTA0	KBI0P0	FTM0CH0	—	ADP0
27	—	—	PTC7	—	TxD1	—	—
28	—	—	PTC6	—	RxD1	—	—
29	—	—	PTC5	—	FTM0CH1	—	—
30	—	—	PTC4	—	FTM0CH0	—	—
31	1	1	PTA5	IRQ	TCLK0	—	$\overline{\text{RESET}}$
32	2	2	PTA4	—	—	BKGD	MS

1. This is a true open-drain pin when operated as output.

Note

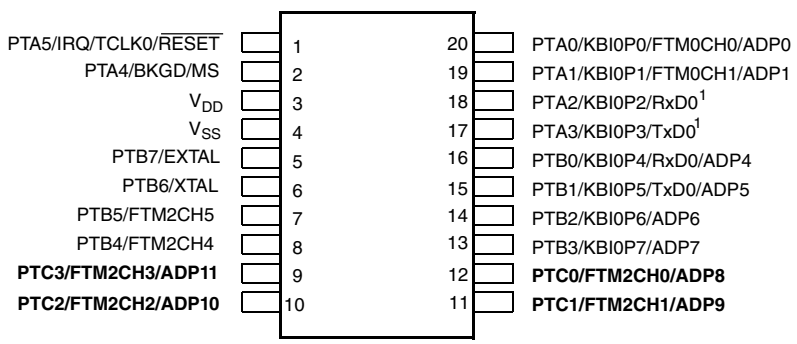
When an alternative function is first enabled, it is possible to get a spurious edge to the module. User software must clear any associated flags before interrupts are enabled. The table above illustrates the priority if multiple modules are enabled. The highest priority module will have control over the pin. Selecting a higher priority pin function with a lower priority function already enabled can cause spurious edges to the lower priority module. Disable all modules that share a pin before enabling another module.

8.2 Device pin assignment



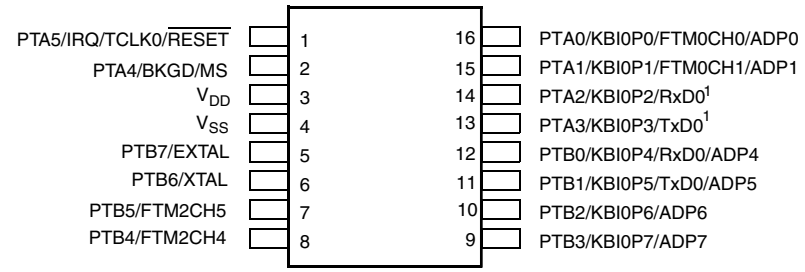
1. True open drain pins

Figure 13. 32-pin LQFP package



Pins in **bold** are not available on less pin-count packages.
1. True open drain pins

Figure 14. 20-pin TSSOP package



Pins in **bold** are not available on less pin-count packages.
1. True open drain pins

Figure 15. 16-pin TSSOP package

9 Revision history

The following table provides a revision history for this document.

Table 15. Revision history

Rev. No.	Date	Substantial Changes
0	03/2018	Initial Created
0.1	03/2018	Updated ordering information.
1	04/2018	Completed all the TBDs and added 20-pin TSSOP and 16-pin TSSOP packages.

How to Reach Us:

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Revision 1, 04/2018