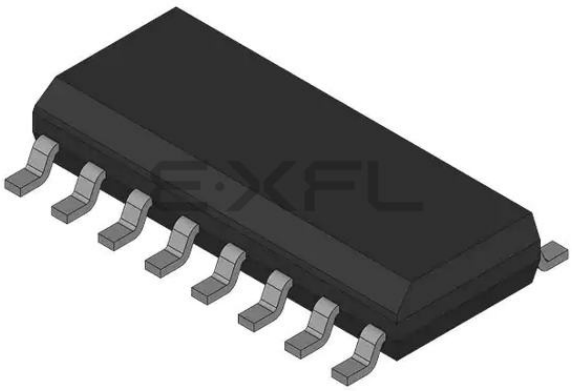

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	HC08
Core Size	8-Bit
Speed	8MHz
Connectivity	SCI
Peripherals	LVD, POR, PWM
Number of I/O	13
Program Memory Size	2KB (2K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	192 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 4x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	16-SOIC (0.295", 7.50mm Width)
Supplier Device Package	16-SOIC
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mc908kx2vdwe

MC68HC908KX8
MC68HC908KX2
MC68HC08KX8

Data Sheet

M68HC08
Microcontrollers

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1.4 Pin Assignments

Figure 1-2 shows the pin assignments for MC68HC908KX8.

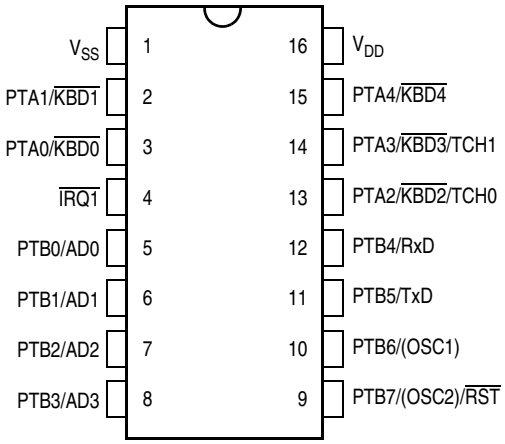
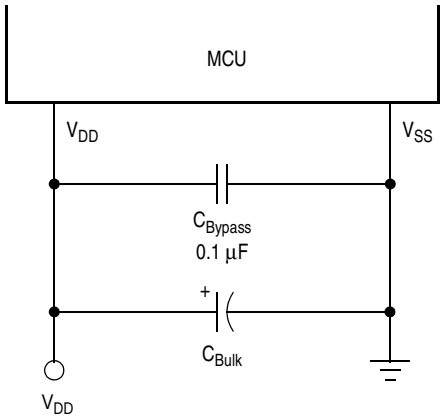


Figure 1-2. PDIP and SOIC Pin Assignments

1.4.1 Supply Pins (V_{DD} and V_{SS})

V_{DD} and V_{SS} are the power supply and ground pins. The MCU operates from a single power supply.

Fast signal transitions on MCU pins place high, short-duration current demands on the power supply. To prevent noise problems, take special care to provide power supply bypassing at the MCU as shown in Figure 1-3. Place the bypass capacitors as close to the MCU power pins as possible. Use high-frequency response ceramic capacitors for C_{Bypass}. C_{Bulk} are optional bulk current bypass capacitors for use in applications that require the port pins to source high-current levels.



Note: Component values shown represent typical applications.

Figure 1-3. Power Supply Bypassing

Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
$0038	ICG Trim Register (ICGTR) See page 89.	Read: Write:	TRIM7	TRIM6	TRIM5	TRIM4	TRIM3	TRIM2	TRIM1	TRIM0
		Reset:	1	0	0	0	0	0	0	0
$0039	ICG Divider Control Register (ICGDVR) See page 89.	Read: Write:					DDIV3	DDIV2	DDIV1	DDIV0
		Reset:	0	0	0	0	U	U	U	U
$003A	ICG DCO Stage Control Register (ICGDSR) See page 89.	Read:	DSTG7	DSTG6	DSTG5	DSTG4	DSTG3	DSTG2	DSTG1	DSTG0
		Write:	R	R	R	R	R	R	R	R
		Reset:	U	U	U	U	U	U	U	U
$003B	Reserved		R	R	R	R	R	R	R	R
$003C	Analog-to-Digital Status and Control Register (ADSCR) See page 43.	Read: Write:	COCO R	AIEN	ADCO	ADCH4	ADCH3	ADCH2	ADCH1	ADCH0
		Reset:	0	0	0	1	1	1	1	1
$003D	Analog-to-Digital Data Register (ADR) See page 45.	Read:	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
		Write:	R	R	R	R	R	R	R	R
		Reset:	Indeterminate after reset							
$003E	Analog-to-Digital Input Clock Register (ADCLK) See page 45.	Read: Write:	ADIV2	ADIV1	ADIV0	ADICLK	0	0	0	R
		Reset:	0	0	0	0	0	0	0	0
$003F	Unimplemented									
$FE00	SIM Break Status Register (SBSR)(1) See page 172.	Read:	0	0	0	1	0	0	BW	0
		Write:	R	R	R	R	R	R	NOTE	R
		Reset:	0	0	0	1	0	0	0	0
$FE01	SIM Reset Status Register (SRSR) See page 148.	Read: Write:	POR	0	COP	ILOP	ILAD	MENRST	LVI	0
		POR:	1	0	0	0	0	0	0	0
$FE02	Break Auxiliary Register (BRKAR) See page 173.	Read:	0	0	0	0	0	0	0	BDCOP
		Write:								
		Reset:	0	0	0	0	0	0	0	0
$FE03	SIM Break Flag Control Register (SBFCR) See page 173.	Read: Write:	BCFE	R	R	R	R	R	R	R
		Reset:	0							
$FE04	Interrupt Status Register 1 (INT1) See page 149.	Read:	IF6	IF5	IF4	IF3	IF2	IF1	0	0
		Write:	R	R	R	R	R	R	R	R
		Reset:	0	0	0	0	0	0	0	0

= Unimplemented R = Reserved U = Unaffected

1. Writing a 0 clears BW.

Figure 2-2. Control, Status, and Data Registers (Sheet 4 of 5)

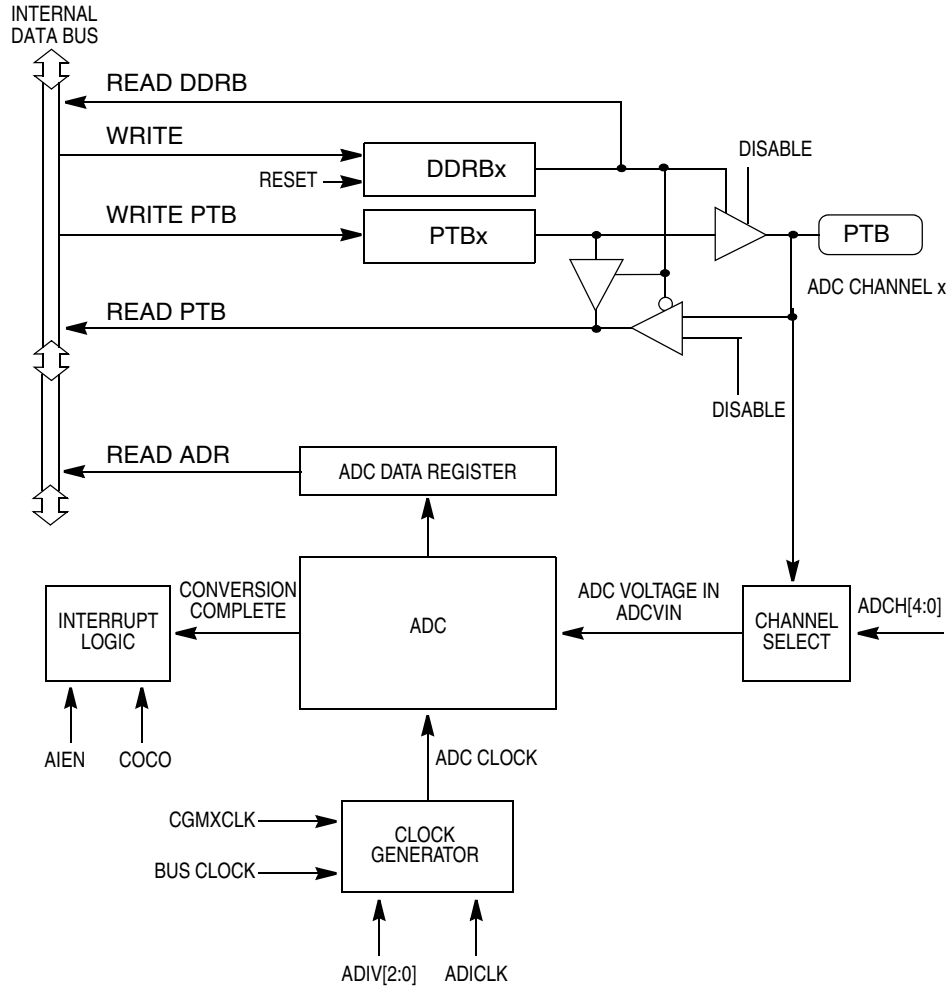


Figure 3-2. ADC Block Diagram

3.3.2 Voltage Conversion

When the input voltage to the ADC equals V_{REFH} (see 17.9 Trimmed Accuracy of the Internal Clock Generator), the ADC converts the signal to $FF (full scale). If the input voltage equals $V_{SS,}$ the ADC converts it to $00. Input voltages between V_{REFH} and V_{SS} are a straight-line linear conversion. All other input voltages will result in $FF if greater than V_{REFH} and $00 if less than V_{SS}.

NOTE

Input voltage should not exceed the high-voltage reference, which in turn should not exceed supply voltages.

3.3.3 Conversion Time

Conversion starts after a write to the ADSCR (ADC status control register, $003C) and requires between 16 and 17 ADC clock cycles to complete. Conversion time in terms of the number of bus cycles is a function of CGMXCLK frequency, bus frequency, the ADIV prescaler bits, and the ADICLK bit. For example, with a CGMXCLK frequency of 8 MHz, bus frequency of 2 MHz, and fixed ADC clock frequency of 1 MHz, one conversion will take between 16 and 17 µs and there will be 32 bus cycles between each conversion. Sample rate is approximately 60 kHz.

Address:	$001F							
	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	COPRS	LVISTOP	LVIRSTD	LVIPWRD	LVI5OR3(1)	SSREC	STOP	COPD
Reset:	0	0	0	0	0	0	0	0
Other Resets:	0	0	0	0	U	0	0	0

1. The LVI5OR3 bit is cleared only by a power-on reset (POR).

U = Unaffected

Figure 4-2. Configuration Register 1 (CONFIG1)

EXTCLKEN — External Clock Enable Bit

EXTCLKEN enables an external clock source or crystal/ceramic resonator to be used as a clock input. Setting this bit enables PTB6/(OSC1) pin to be a clock input pin. Clearing this bit (default setting) allows the PTB6/(OSC1) and PTB7/(OSC2)/$\overline{\text{RST}}$ pins to function as a general-purpose input/output (I/O) pin. Refer to Table 4-1 for configuration options for the external source. See Chapter 7 Internal Clock Generator Module (ICG) for a more detailed description of the external clock operation.

1 = Allows PTB6/(OSC1) to be an external clock connection

0 = PTB6/(OSC1) and PTB7/(OSC2)/$\overline{\text{RST}}$ function as I/O port pins (default).

Table 4-1. External Clock Option Settings

External Clock Configuration Bits		Pin Function		Description
EXTCLKEN	EXTXTALEN	PTB6/(OSC1)	PTB7/(OSC2)/$\overline{\text{RST}}$	
0	0	PTB6	PTB7	Default setting — external oscillator disabled
0	1	PTB6	PTB7	External oscillator disabled since EXTCLKEN not set
1	0	OSC1	PTB7	External oscillator configured for an external clock source input (square wave) on OSC1
1	1	OSC1	OSC2	External oscillator configured for an external crystal configuration on OSC1 and OSC2. System will also operate with square-wave clock source in OSC1.

EXTSLOW — Slow External Crystal Enable Bit

The EXTSLOW bit has two functions. It configures the ICG module for a fast (1 MHz to 8 MHz) or slow (30 kHz to 100 kHz) speed crystal. The option also configures the clock monitor operation in the ICG module to expect an external frequency higher (307.2 kHz to 32 MHz) or lower (60 Hz to 307.2 kHz) than the base frequency of the internal oscillator. See Chapter 7 Internal Clock Generator Module (ICG).

1 = ICG set for slow external crystal operation

0 = ICG set for fast external crystal operation

EXTXTALEN — External Crystal Enable Bit

EXTXTALEN enables the external oscillator circuits to be configured for a crystal configuration where the PTB6/(OSC1) and PTB7/(OSC2)/$\overline{\text{RST}}$ pins are the connections for an external crystal.

NOTE

This bit does not function without setting the EXTCLKEN bit also.

LVIPWRD — LVI Power Disable Bit

LVIPWRD disables the LVI module. See Chapter 10 Low-Voltage Inhibit (LVI).

1 = LVI module power disabled
0 = LVI module power enabled

LVI5OR3 — LVI 5-V or 3-V Operating Mode Bit

LVI5OR3 selects the voltage operating mode of the LVI module (see See Chapter 10 Low-Voltage Inhibit (LVI).). The voltage mode selected for the LVI should match the operating V_{DD}. See Chapter 17 Electrical Specifications for the LVI's voltage trip points for each of the modes.

1 = LVI operates in 5-V mode.
0 = LVI operates in 3-V mode.

NOTE

The LVI5OR3 bit is cleared by a power-on reset (POR) only. Other resets will leave this bit unaffected.

SSREC — Short Stop Recovery Bit

SSREC enables the CPU to exit stop mode with a delay of 32 CGMXCLK cycles instead of a 4096-CGMXCLK cycle delay.

1 = Stop mode recovery after 32 CGMXCLK cycles
0 = Stop mode recovery after 4096 CGMXCLCK cycles

NOTE

Exiting stop mode by an LVI reset will result in the long stop recovery.

If the system clock source selected is the internal oscillator or the external crystal and the OSCENINSTOP configuration bit is not set, the oscillator will be disabled during stop mode. The short stop recovery does not provide enough time for oscillator stabilization and thus the SSREC bit should not be set.

When using the LVI during normal operation but disabling during stop mode, the LVI will have an enable time of t_{EN}. The system stabilization time for power-on reset and long stop recovery (both 4096 CGMXCLK cycles) gives a delay longer than the LVI enable time for these startup scenarios. There is no period where the MCU is not protected from a low-power condition. However, when using the short stop recovery configuration option, the 32-CGMXCLK delay must be greater than the LVI's turn on time to avoid a period in startup where the LVI is not protecting the MCU.

STOP — STOP Instruction Enable Bit

STOP enables the STOP instruction.

1 = STOP instruction enabled
0 = STOP instruction treated as illegal opcode

COPD — COP Disable Bit

COPD disables the COP module. See Chapter 5 Computer Operating Properly Module (COP).

1 = COP module disabled
0 = COP module enabled

Z — Zero Flag

The CPU sets the zero flag when an arithmetic operation, logic operation, or data manipulation produces a result of $00.

1 = Zero result
0 = Non-zero result

C — Carry/Borrow Flag

The CPU sets the carry/borrow flag when an addition operation produces a carry out of bit 7 of the accumulator or when a subtraction operation requires a borrow. Some instructions — such as bit test and branch, shift, and rotate — also clear or set the carry/borrow flag.

1 = Carry out of bit 7
0 = No carry out of bit 7

6.4 Arithmetic/Logic Unit (ALU)

The ALU performs the arithmetic and logic operations defined by the instruction set.

Refer to the *CPU08 Reference Manual* (document order number CPU08RM/AD) for a description of the instructions and addressing modes and more detail about the architecture of the CPU.

6.5 Low-Power Modes

The WAIT and STOP instructions put the MCU in low power-consumption standby modes.

6.5.1 Wait Mode

The WAIT instruction:

- Clears the interrupt mask (I bit) in the condition code register, enabling interrupts. After exit from wait mode by interrupt, the I bit remains clear. After exit by reset, the I bit is set.
- Disables the CPU clock

6.5.2 Stop Mode

The STOP instruction:

- Clears the interrupt mask (I bit) in the condition code register, enabling external interrupts. After exit from stop mode by external interrupt, the I bit remains clear. After exit by reset, the I bit is set.
- Disables the CPU clock

After exiting stop mode, the CPU clock begins running after the oscillator stabilization delay.

6.6 CPU During Break Interrupts

If a break module is present on the MCU, the CPU starts a break interrupt by:

- Loading the instruction register with the SWI instruction
- Loading the program counter with $FFFC:$FFFD or with $FEFC:$FEFD in monitor mode

The break interrupt begins after completion of the CPU instruction in progress. If the break address register match occurs on the last cycle of a CPU instruction, the break interrupt begins immediately.

A return-from-interrupt instruction (RTI) in the break routine ends the break interrupt and returns the MCU to normal operation if the break interrupt has been deasserted.

```
                                ;Clock Monitor Enabling Code Example
                                ;This code turns on both clocks, selects the desired
                                ; one, then turns on the Clock Monitor and Interrupts
start   lda     #$AF            ;Mask for CMIE, CMON, ICGON, ICGS, ECGON, ECGS
                                ; If Internal Clock desired, mask is $AF
                                ; If External Clock desired, mask is $BF
                                ; If interrupts not desired mask is $2F int; $3F ext
loop    **      **              ;Other code here, such as writing the COP, since ECGS
                                ; and ICGS may take some time to set.
        sta     icgcr           ;Try to set CMIE. CMIE wont set until CMON set; CMON
                                ; won't set until ICGON, ICGS, ECGON, ECGS set.
        brset   6,ICGCR,error   ;Verify CMF is not set
        cmpa    icgcr           ;Check if ECGS set, then CMON set, then CMIE set
        bne     loop            ;Keep looping until CMIE is set.
```

Figure 7-9. Code Example for Enabling the Clock Monitor

7.4.3 Using Clock Monitor Interrupts

The clock monitor circuit can be used to recover from perilous situations such as crystal loss. To use the clock monitor effectively, the following notes should be observed:

- Enable the clock monitor and clock monitor interrupts.
- The first statement in the clock monitor interrupt service routine (CMISR) should be a read to the ICG control register (ICGCR) to verify the clock monitor flag (CMF) is set. This is also the first step in clearing the CMF bit.
- The second statement in the CMISR should be a write to the ICGCR to clear the CMF bit (write the bit low). Writing the bit high will not affect it. This statement does not need to immediately follow the first, but must be contained in the CMISR.
- The third statement in the CMISR should be to clear the CMON bit. This is required to ensure proper reconfiguration of the reference dividers. This statement must also be contained in the CMISR.
- Although the clock monitor can only be enabled when both clocks are stable (ICGS is set or ECGS is set), it will remain set if one of the clocks goes unstable.
- The clock monitor only works if the external slow (EXTSLOW) bit in the CONFIG (or MOR) register is set to the correct value.
- The internal and external clocks must both be enabled and running in order to use the clock monitor.
- When the clock monitor detects inactivity, the inactive clock is automatically deselected and the active clock selected as the source for CGMXCLK and TBMCLK. The CMISR can use the state of the CS bit to check which clock is inactive.
- When the clock monitor detects inactivity, the application may have been subjected to extreme conditions which may have affected other circuits. The CMISR should take any appropriate precautions.

Chapter 9
Keyboard Interrupt Module (KBI)

9.1 Introduction

The keyboard interrupt module (KBI) provides five independently maskable external interrupt pins.

9.2 Features

KBI features include:

- Five keyboard interrupt pins, on the MC68HC08KX8, are with separate keyboard interrupt enable bits and one keyboard interrupt mask
- Hysteresis buffers
- Programmable edge-only or edge- and level-interrupt sensitivity
- Automatic interrupt acknowledge
- Exit from low-power modes

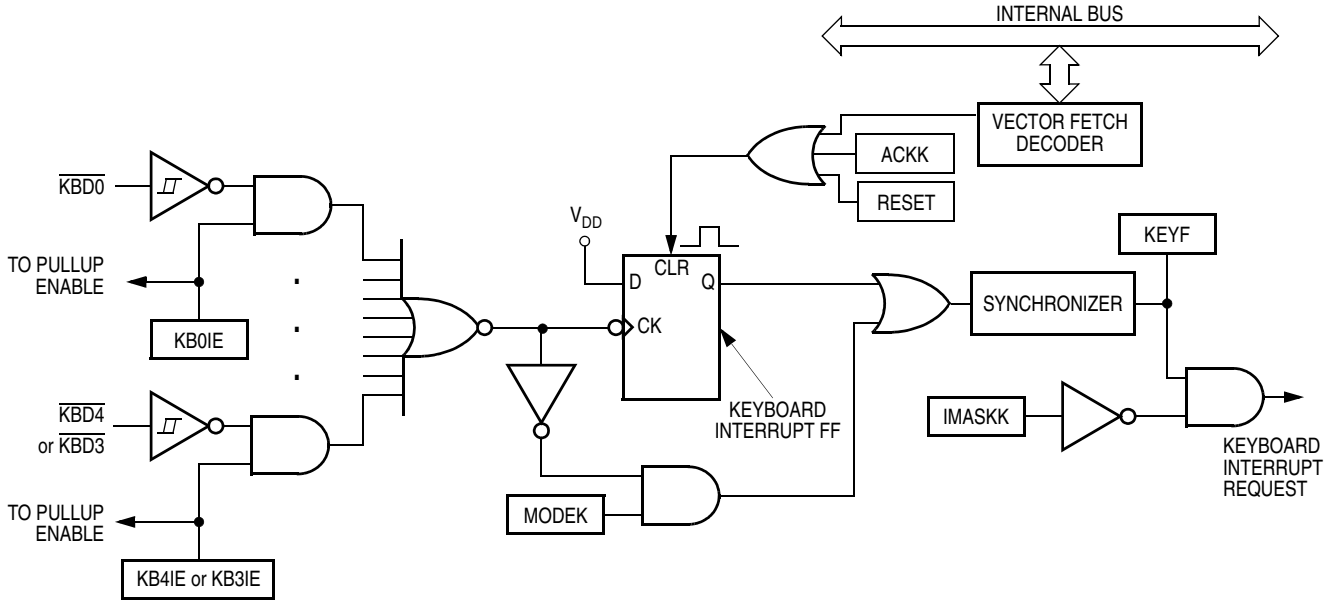


Figure 9-1. Keyboard Module Block Diagram

Chapter 11
Input/Output (I/O) Ports (PORTS)

11.1 Introduction

Thirteen bidirectional input/output (I/O) pins form two parallel ports in the 16-pin plastic dual in-line package (PDIP) and small outline integrated circuit (SOIC) package in the MC68HC908KX8 part. All I/O pins are programmable as inputs or outputs. Port A has software selectable pullup resistors if the port is used as a general-function input port.

NOTE

Connect any unused I/O pins to an appropriate logic level, either V_{DD} or V_{SS}. Although the I/O ports do not require termination for proper operation, termination reduces excess current consumption and the possibility of electrostatic damage.

See Figure 11-1 for a summary of the I/O port registers.

Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
$0000	Port A Data Register (PTA) See page 106.	Read:	0	0	0	PTA4	PTA3	PTA2	PTA1	PTA0
		Write:								
		Reset:	Unaffected by reset							
$0001	Port B Data Register (PTB) See page 108.	Read:	PTB7	PTB6	PTB5	PTB4	PTB3	PTB2	PTB1	PTB0
		Write:								
		Reset:	Unaffected by reset							
$0004	Data Direction Register A (DDRA) See page 106.	Read:	0	0	0	DDRA4	DDRA3	DDRA2	DDRA1	DDRA0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
$0005	Data Direction Register B (DDRB) See page 109.	Read:	DDRB7	DDRB6	DDRB5	DDRB4	DDRB3	DDRB2	DDRB1	DDRB0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
$000D	Port A Input Pullup Enable Register (PTAPUE) See page 108.	Read:	0	0	0	PTAPUE4	PTAPUE3	PTAPUE2	PTAPUE1	PTAPUE0
		Write:								
		Reset:	0	0	0	0	0	0	0	0

= Unimplemented

Figure 11-1. I/O Port Register Summary

11.2 Port A

Port A is a 5-bit special function port on the MC68HC908KX8 that shares all of its pins with the keyboard interrupt module (KBI) and the 2-channel timer. Port A contains software programmable pullup resistors enabled when a port pin is used as a general-function input. Port A pins are also high-current port pins with 15-mA source/15-mA sink capabilities.

11.2.1 Port A Data Register

The port A data register (PTA) contains a data latch for each of the five port A pins.

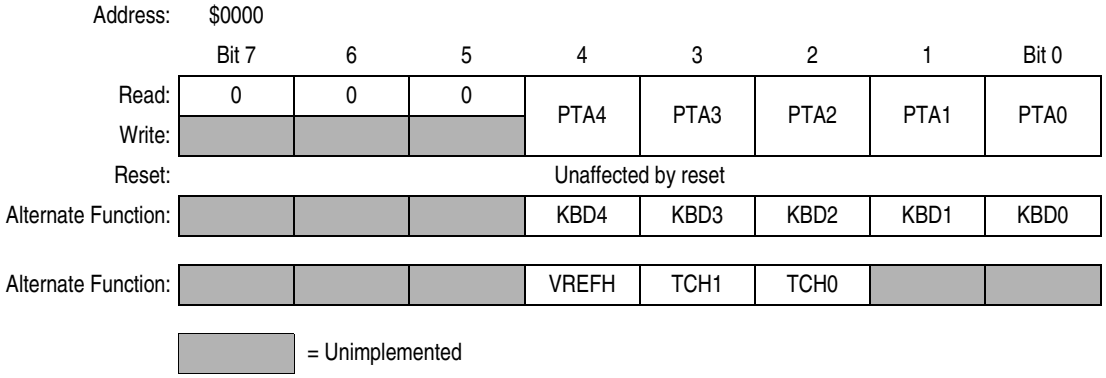


Figure 11-2. Port A Data Register (PTA)

PTA4–PTA0 — Port A Data Bits

These read/write bits are software programmable. Data direction of each port A pin is under the control of the corresponding bit in data direction register A. Reset has no effect on port A data.

KBD4–KBD0 — Keyboard Wakeup Bits

The keyboard interrupt enable bits, KBIE4–KBIE0, in the keyboard interrupt control register, enable the port A pins as external interrupt pins. See Chapter 9 Keyboard Interrupt Module (KBI).

TCH1 and TCH0 — Timer Channel I/O Bits

The PTA3/$\overline{\text{KBD3}}$/TCH1 and PTA2/$\overline{\text{KBD2}}$/TCH0 pins are the TIM input capture/output compare pins. The edge/level select bits, ELSxB and ELSxA, determine whether the pins are timer channel I/O pins or general-purpose I/O pins. See Chapter 9 Keyboard Interrupt Module (KBI).

11.2.2 Data Direction Register A

Data direction register A (DDRA) determines whether each port A pin is an input or an output. Writing a 1 to a DDRA bit enables the output buffer for the corresponding port A pin; a 0 disables the output buffer.

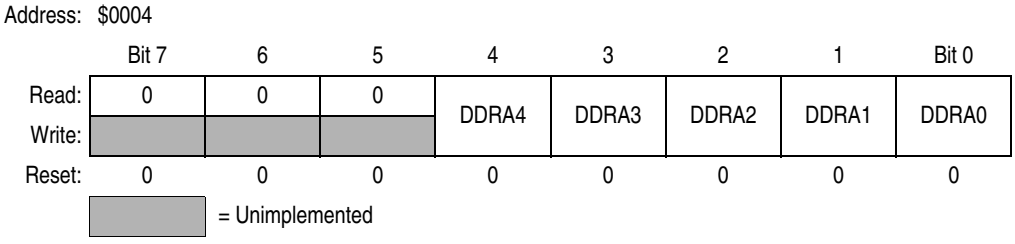


Figure 11-3. Data Direction Register A (DDRA)

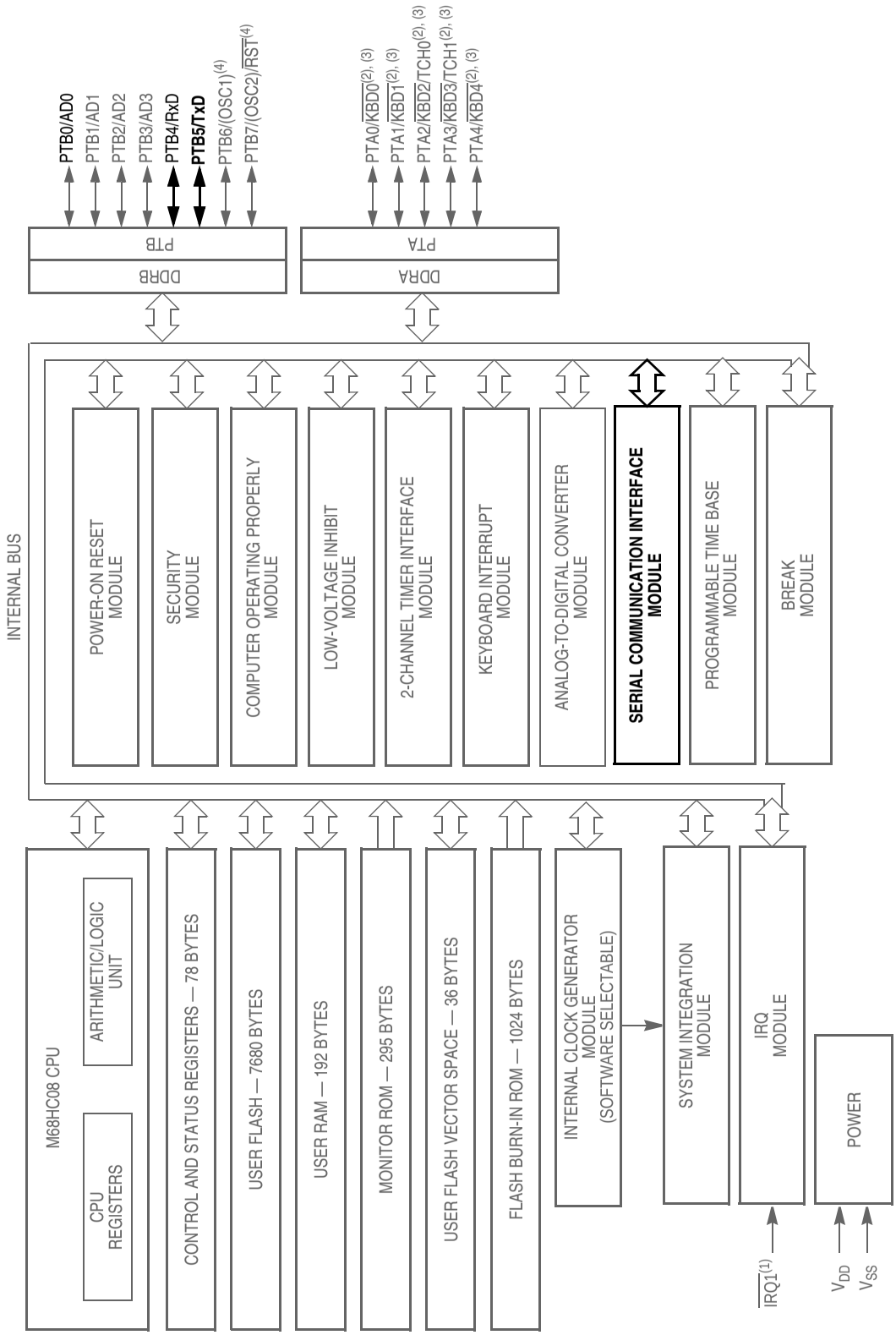


Figure 12-1. Block Diagram Highlighting SCI Block and Pins

Notes:
1. Pin contains integrated pullup resistor
2. High-current source/sink pin
3. Pin contains software selectable pullup resistor if general function I/O pin is configured as input.

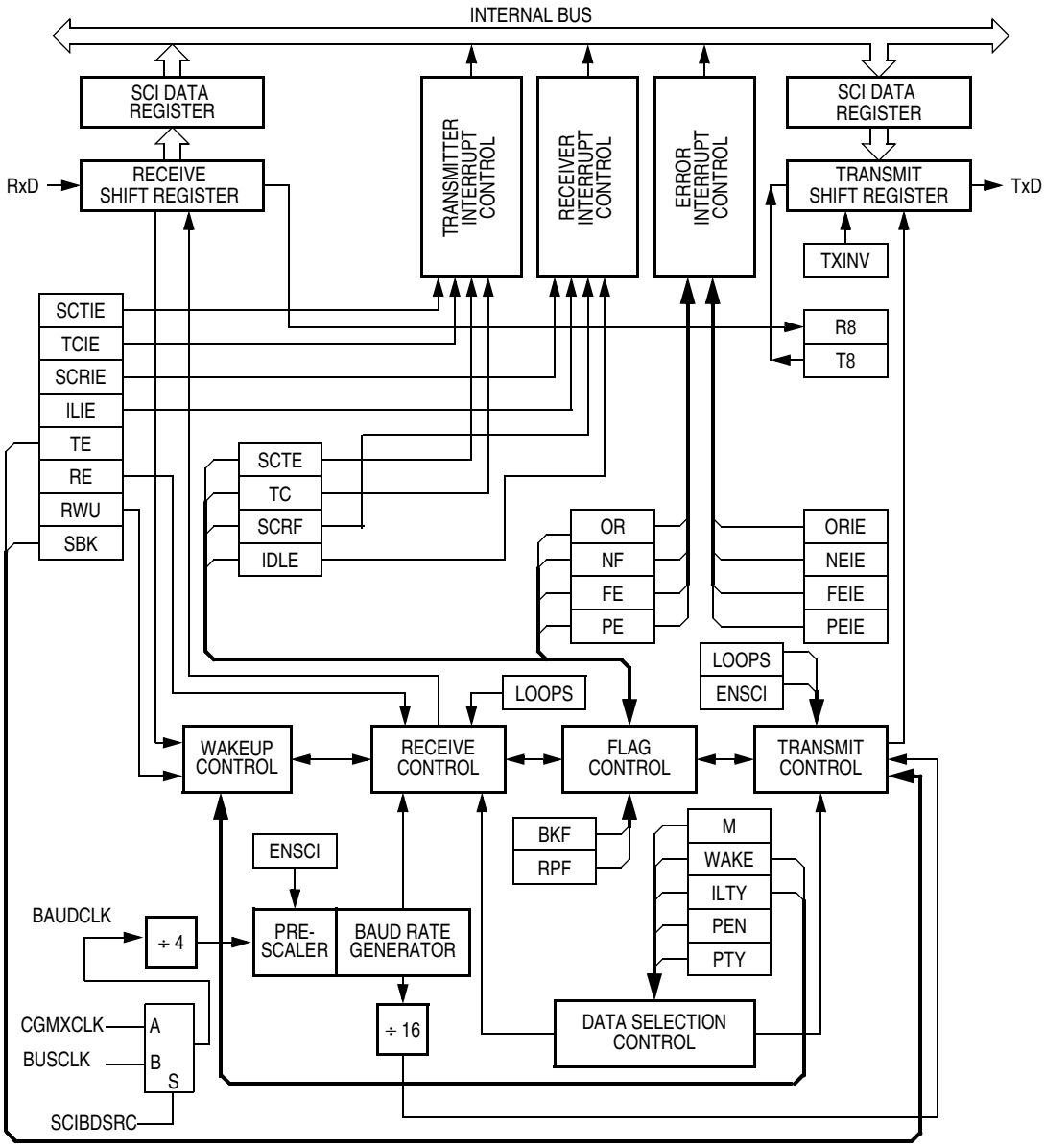


Figure 12-3. SCI Module Block Diagram

break character and then transmits at least one 1. The automatic 1 at the end of a break character guarantees the recognition of the start bit of the next character.

12.4.2.3 Break Characters

The SCI recognizes a break character when a start bit is followed by eight or nine 0 data bits and a 0 where the stop bit should be. Receiving a break character has these effects on SCI registers:

- Sets the framing error bit (FE) in SCS1
- Sets the SCI receiver full bit (SCRF) in SCS1
- Clears the SCI data register (SCDR)
- Clears the R8 bit in SCC3
- Sets the break flag bit (BKF) in SCS2
- May set the overrun (OR), noise flag (NF), parity error (PE), or reception-in-progress flag (RPF) bits

12.4.2.4 Idle Characters

An idle character contains all 1s and has no start, stop, or parity bit. Idle character length depends on the M bit in SCC1. The preamble is a synchronizing idle character that begins every transmission.

If the TE bit is cleared during a transmission, the TxD pin becomes idle after completion of the transmission in progress. Clearing and then setting the TE bit during a transmission queues an idle character to be sent after the character currently being transmitted.

NOTE

When queueing an idle character, return the TE bit to 1 before the stop bit of the current character shifts out to the TxD pin. Setting TE after the stop bit appears on TxD causes data previously written to the SCDR to be lost.

A good time to toggle the TE bit for a queued idle character is when the SCTE bit becomes set and just before writing the next byte to the SCDR.

12.4.2.5 Inversion of Transmitted Output

The transmit inversion bit (TXINV) in SCI control register 1 (SCC1) reverses the polarity of transmitted data. All transmitted values, including idle, break, start, and stop bits, are inverted when TXINV is at 1. See 12.7.1 SCI Control Register 1.

12.4.2.6 Transmitter Interrupts

These conditions can generate CPU interrupt requests from the SCI transmitter:

- SCI transmitter empty (SCTE) — The SCTE bit in SCS1 indicates that the SCDR has transferred a character to the transmit shift register. SCTE can generate a transmitter CPU interrupt request. Setting the SCI transmit interrupt enable bit, SCTIE, in SCC2 enables the SCTE bit to generate transmitter CPU interrupt requests.
- Transmission complete (TC) — The TC bit in SCS1 indicates that the transmit shift register and the SCDR are empty and that no break or idle character has been generated. The transmission complete interrupt enable bit, TCIE, in SCC2 enables the TC bit to generate transmitter CPU interrupt requests.

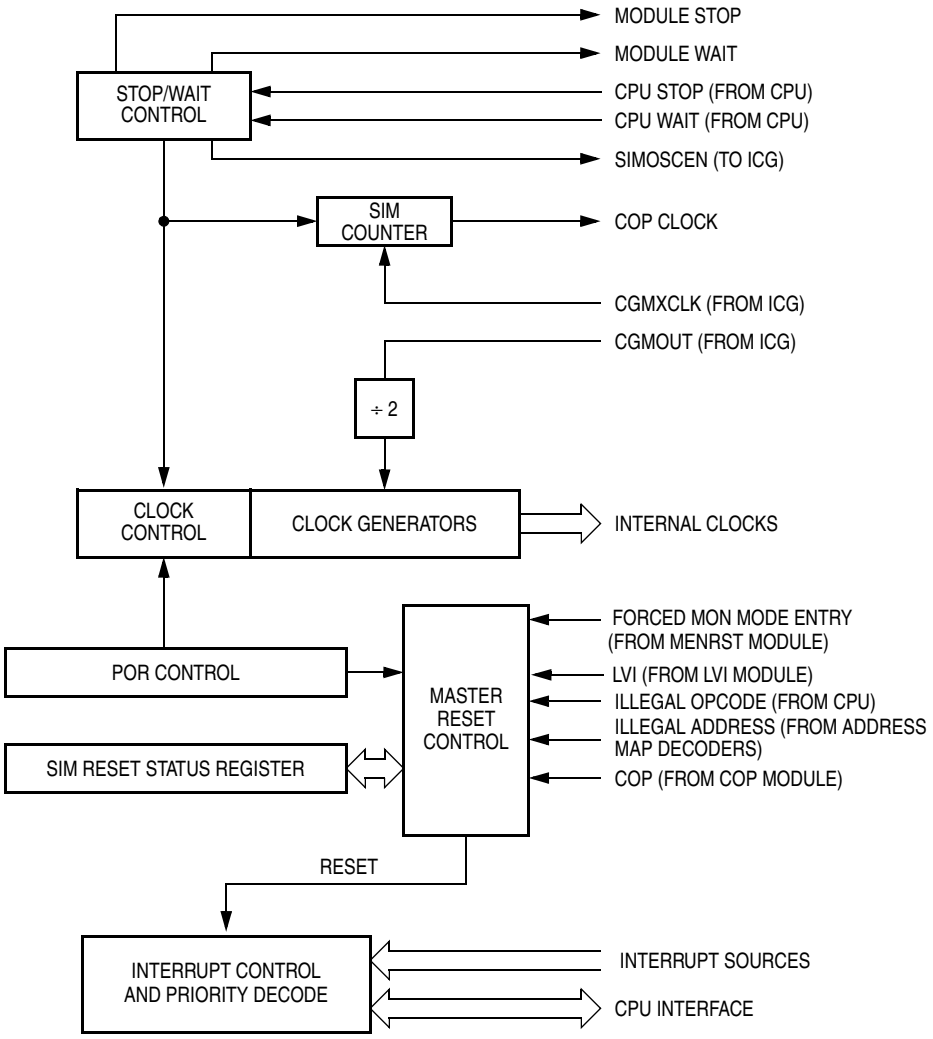


Figure 13-2. SIM Block Diagram

Table 13-1 shows the internal signal names used in this section.

Table 13-1. Signal Name Conventions

Signal Name	Description
CGMXCLK	Selected clock source from internal clock generator module (ICG)
CGMOUT	Clock output from ICG module (bus clock = CGMOUT divided by two)
IAB	Internal address bus
IDB	Internal data bus
PORRST	Signal from the power-on reset (POR) module to the SIM
IRST	Internal reset signal
R/$\overline{W}$	Read/write signal

If the stop enable bit, STOP, in the configuration register (CONFIG1) is 0, the SIM treats the STOP instruction as an illegal opcode and causes an illegal opcode reset.

13.3.1.4 Illegal Address Reset

An opcode fetch from an unmapped address generates an illegal address reset. The SIM verifies that the CPU is fetching an opcode prior to asserting the ILAD bit in the SIM reset status register (SRSR) and resetting the MCU. A data fetch from an unmapped address does not generate a reset.

13.3.1.5 Forced Monitor Mode Entry Reset (MENRST)

The MENRST module is monitoring the reset vector fetches and will assert an internal reset if it detects that the reset vectors are erased ($FF). When the MCU comes out of reset, it is forced into monitor mode. See 16.3 Monitor ROM (MON).

13.3.1.6 Low-Voltage Inhibit (LVI) Reset

The low-voltage inhibit module (LVI) asserts its output to the SIM when the V_{DD} voltage falls to the V_{TRIPF} voltage. The LVI bit in the SIM reset status register (SRSR) is set and a chip reset is asserted if the LVIPWRD and LVIRSTD bits in the CONFIG register are at 0. The MCU is held in reset until V_{DD} rises above V_{TRIPR}. The MCU remains in reset until the SIM counts 4096 CGMXCLK to begin a reset recovery. Another 64 CGMXCLK cycles later, the CPU is released from reset to allow the reset vector sequence to occur. See Chapter 10 Low-Voltage Inhibit (LVI).

13.4 SIM Counter

The SIM counter is used by the power-on reset module (POR) and in stop mode recovery to allow the oscillator time to stabilize before enabling the internal bus (IBUS) clocks. The SIM counter also serves as a prescaler for the computer operating properly module (COP). The SIM counter overflow supplies the clock for the COP module. The SIM counter is 12 bits long and is clocked by the falling edge of CGMXCLK.

13.4.1 SIM Counter During Power-On Reset

The power-on reset module (POR) detects power applied to the MCU. At power-on, the POR circuit asserts the signal PORRST. Once the SIM is initialized, it enables the internal clock generator to drive the bus clock state machine.

13.4.2 SIM Counter During Stop Mode Recovery

The SIM counter also is used for stop mode recovery. The STOP instruction clears the SIM counter. After an interrupt or reset, the SIM senses the state of the short stop recovery bit, SSREC, in the configuration register. If the SSREC bit is a 1, then the stop recovery is reduced from the normal delay of 4096 CGMXCLK cycles down to 32 CGMXCLK cycles.

13.4.3 SIM Counter and Reset States

The SIM counter is free-running after all reset states. See 13.3.1 Active Resets from Internal Sources for counter control and internal reset recovery sequences.

5. In the TIM status control register (TSC), clear the TIM stop bit, TSTOP.

Setting MS0B links channels 0 and 1 and configures them for buffered PWM operation. The TIM channel 0 registers (TCH0H and TCH0L) initially control the buffered PWM output. TIM status control register 0 (TSCR0) controls and monitors the PWM signal from the linked channels.

Clearing the toggle-on-overflow bit, TOVx, inhibits output toggles on TIM overflows. Subsequent output compares try to force the output to a state it is already in and have no effect. The result is a 0 percent duty cycle output.

Setting the channel x maximum duty cycle bit (CHxMAX) and setting the TOVx bit generates a 100 percent duty cycle output. See 15.8.4 TIM Channel Status and Control Registers.

15.5 Interrupts

These TIM sources can generate interrupt requests:

- TIM overflow flag (TOF) — The timer overflow flag (TOF) bit is set when the TIM counter reaches the modulo value programmed in the TIM counter modulo registers. The TIM overflow interrupt enable bit, TOIE, enables TIM overflow interrupt requests. TOF and TOIE are in the TIM status and control registers.
- TIM channel flags (CH1F and CH0F) — The CHxF bit is set when an input capture or output compare occurs on channel x. Channel x TIM CPU interrupt requests are controlled by the channel x interrupt enable bit, CHxIE. Channel x TIM CPU interrupt requests are enabled when CHxIE = 1. CHxF and CHxIE are in the TIM channel x status and control register.

15.6 Low-Power Modes

The WAIT and STOP instructions put the MCU in low power-consumption standby modes.

15.6.1 Wait Mode

The TIM remains active after the execution of a WAIT instruction. In wait mode the TIM registers are not accessible by the CPU. Any enabled CPU interrupt request from the TIM can bring the MCU out of wait mode.

If TIM functions are not required during wait mode, reduce power consumption by stopping the TIM before executing the WAIT instruction.

15.6.2 Stop Mode

The TIM is inactive after the execution of a STOP instruction. The STOP instruction does not affect register conditions or the state of the TIM counter. TIM operation resumes when the MCU exits stop mode after an external interrupt.

15.7 I/O Signals

Port A shares two of its pins with the TIM, PTA3/$\overline{\text{KBD3}}$/TCH1 and PTA2/$\overline{\text{KBD2}}$/TCH0. Each channel input/output (I/O) pin is programmable independently as an input capture pin or an output compare pin. TCH0 can be configured as buffered output compare or buffered PWM pins.

17.10 Analog-to-Digital Converter (ADC) Characteristics

Characteristic	Symbol	Min	Max	Unit	Notes
Supply voltage	V_{DD}	2.7	5.5	V	
Input voltages	V_{ADIN}	0	V_{DD}	V	
Resolution	B_{AD}	8	8	Bits	
Absolute accuracy(1), (2)	A_{AD}	–2.5	+2.5	Counts	8 bits = 256 counts
ADC clock rate	f_{ADIC}	500 k	1.048 M	Hz	$t_{AIC} = 1/f_{ADIC}$, Tested only at 1 MHz
Conversion range	R_{AD}	V_{SS}	V_{DD}	V	
Power-up time	t_{ADPU}	16	—	t_{AIC} cycles	
Conversion time	t_{ADC}	16	17	t_{AIC} cycles	
Sample time	t_{ADS}	5	—	t_{AIC} cycles	
Monotocity	M_{AD}	Guaranteed			
Zero input reading	Z_{ADI}	00	—	Hex	$V_{In} = V_{SS}$
Full-scale reading	F_{ADI}	—	FF	Hex	$V_{In} = V_{DD}$
Input capacitance	C_{ADI}	—	20	pF	Not tested

1. One count is 1/256 of V_{DD}.
2. V_{REFH} is shared with V_{DD}. V_{REFL} is shared with V_{SS}.

B.4.8 Trimmed Accuracy of the Internal Clock Generator

The unadjusted frequency of the low-frequency base clock (IBASE), when the comparators in the frequency comparator indicate zero error, can vary as much as ±25% due to process, temperature, and voltage. The trimming capability exists to compensate for process affects. The remaining variation in frequency is due to temperature, voltage, and change in target frequency (multiply register setting). These affects are designed to be minimal, however variation does occur. Better performance is seen at 3 V and lower settings of N.

B.4.8.1 2.7-Volt to 3.3-Volt Trimmed Internal Clock Generator Characteristics

Characteristic[1]	Symbol	Min	Typ	Max	Unit
Absolute trimmed internal oscillator tolerance[2], [3] –40°C to 85°C	F_{abs_tol}	—	1.5	5.0	%
Variation over temperature[3], [4]	V_{ar_temp}	—	0.03	0.05	%/C
Variation over voltage[3], [5] 25°C –40°C to 85°C	V_{ar_volt}	— —	0.5 0.7	2.0 2.0	%/V

1. These specifications concern long-term frequency variation. Each measurement is taken over a 1-ms period.
2. Absolute value of variation in ICG output frequency, trimmed at nominal V_{DD} and temperature, as temperature and V_{DD} are allowed to vary for a single given setting of N.
3. Specification is characterized but not tested.
4. Variation in ICG output frequency for a fixed N and voltage
5. Variation in ICG output frequency for a fixed N

B.4.8.2 4.5-Volt to 5.5-Volt Trimmed Internal Clock Generator Characteristics

Characteristic[1]	Symbol	Min	Typ	Max	Unit
Absolute trimmed internal oscillator tolerance[2], [3] –40°C to 85°C	F_{abs_tol}	—	4.0	7.0	%
Variation over temperature[3], [4]	V_{ar_temp}	—	0.05	0.08	%/C
Variation over voltage[3], [5] 25°C –40°C to 85°C	V_{ar_volt}	— —	1.0 1.0	2.0 2.0	%/V

1. These specifications concern long-term frequency variation. Each measurement is taken over a 1-ms period.
2. Absolute value of variation in ICG output frequency, trimmed at nominal V_{DD} and temperature, as temperature and V_{DD} are allowed to vary for a single given setting of N.
3. Specification is characterized but not tested.
4. Variation in ICG output frequency for a fixed N and voltage
5. Variation in ICG output frequency for a fixed N