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Details	
Product Status	Not For New Designs
Core Processor	HC08
Core Size	8-Bit
Speed	8MHz
Connectivity	SCI
Peripherals	LVD, POR, PWM
Number of I/O	13
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	192 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 4x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	16-SOIC (0.295", 7.50mm Width)
Supplier Device Package	16-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc908kx8cdwe

Chapter 11
Input/Output (I/O) Ports (PORTS)

Chapter 12
Serial Communications Interface Module (SCI)

MC68HC908KX8 • MC68HC908KX2 • MC68HC08KX8 Data Sheet, Rev. 2.1

3.7.2 ADC Data Register

One 8-bit result register is provided. This register is updated each time an ADC conversion completes.

Address: $003D

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
Write:	R	R	R	R	R	R	R	R
Reset:				Indeterminate after reset				

R	= Reserved

Figure 3-4. ADC Data Register (ADR)

3.7.3 ADC Input Clock Register

This register selects the clock frequency for the ADC.

Address: $003E

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	ADIV2	ADIV1	ADIV0	ADICLK	0	0	0	R
Write:								
Reset:	0	0	0	0	0	0	0	0

	= Unimplemented		R	= Reserved

Figure 3-5. ADC Input Clock Register (ADICLK)

ADIV2–ADIV0 — ADC Clock Prescaler Bits
　　ADIV2, ADIV1, and ADIV0 form a 3-bit field which selects the divide ratio used by the ADC to generate the internal ADC clock. Table 3-2 shows the available clock configurations. The ADC clock should be set to approximately 1 MHz.

Table 3-2. ADC Clock Divide Ratio

ADIV2	ADIV1	ADIV0	ADC Clock Rate
0	0	0	ADC input clock ÷ 1
0	0	1	ADC input clock ÷ 2
0	1	0	ADC input clock ÷ 4
0	1	1	ADC input clock ÷ 8
1	X	X	ADC input clock ÷ 16

X = don't care

ADICLK — ADC Input Clock Select Bit
　　ADICLK selects either bus clock or the oscillator output clock (CGMXCLK) as the input clock source to generate the internal ADC rate clock. Reset selects CGMXCLK as the ADC clock source.
　　　1 = Internal bus clock
　　　0 = Oscillator output clock (CGMXCLK)

LVIPWRD — LVI Power Disable Bit

LVIPWRD disables the LVI module. See Chapter 10 Low-Voltage Inhibit (LVI).

 1 = LVI module power disabled

 0 = LVI module power enabled

LVI5OR3 — LVI 5-V or 3-V Operating Mode Bit

LVI5OR3 selects the voltage operating mode of the LVI module (see See Chapter 10 Low-Voltage Inhibit (LVI).). The voltage mode selected for the LVI should match the operating V_{DD}. See Chapter 17 Electrical Specifications for the LVI's voltage trip points for each of the modes.

 1 = LVI operates in 5-V mode.

 0 = LVI operates in 3-V mode.

> *NOTE*
>
> *The LVI5OR3 bit is cleared by a power-on reset (POR) only. Other resets will leave this bit unaffected.*

SSREC — Short Stop Recovery Bit

SSREC enables the CPU to exit stop mode with a delay of 32 CGMXCLK cycles instead of a 4096-CGMXCLK cycle delay.

 1 = Stop mode recovery after 32 CGMXCLK cycles

 0 = Stop mode recovery after 4096 CGMXCLCK cycles

> *NOTE*
>
> *Exiting stop mode by an LVI reset will result in the long stop recovery.*

If the system clock source selected is the internal oscillator or the external crystal and the OSCENINSTOP configuration bit is not set, the oscillator will be disabled during stop mode. The short stop recovery does not provide enough time for oscillator stabilization and thus the SSREC bit should not be set.

When using the LVI during normal operation but disabling during stop mode, the LVI will have an enable time of t_{EN}. The system stabilization time for power-on reset and long stop recovery (both 4096 CGMXCLK cycles) gives a delay longer than the LVI enable time for these startup scenarios. There is no period where the MCU is not protected from a low-power condition. However, when using the short stop recovery configuration option, the 32-CGMXCLK delay must be greater than the LVI's turn on time to avoid a period in startup where the LVI is not protecting the MCU.

STOP — STOP Instruction Enable Bit

STOP enables the STOP instruction.

 1 = STOP instruction enabled

 0 = STOP instruction treated as illegal opcode

COPD — COP Disable Bit

COPD disables the COP module. See Chapter 5 Computer Operating Properly Module (COP).

 1 = COP module disabled

 0 = COP module enabled

Table 6-1. Instruction Set Summary (Sheet 2 of 6)

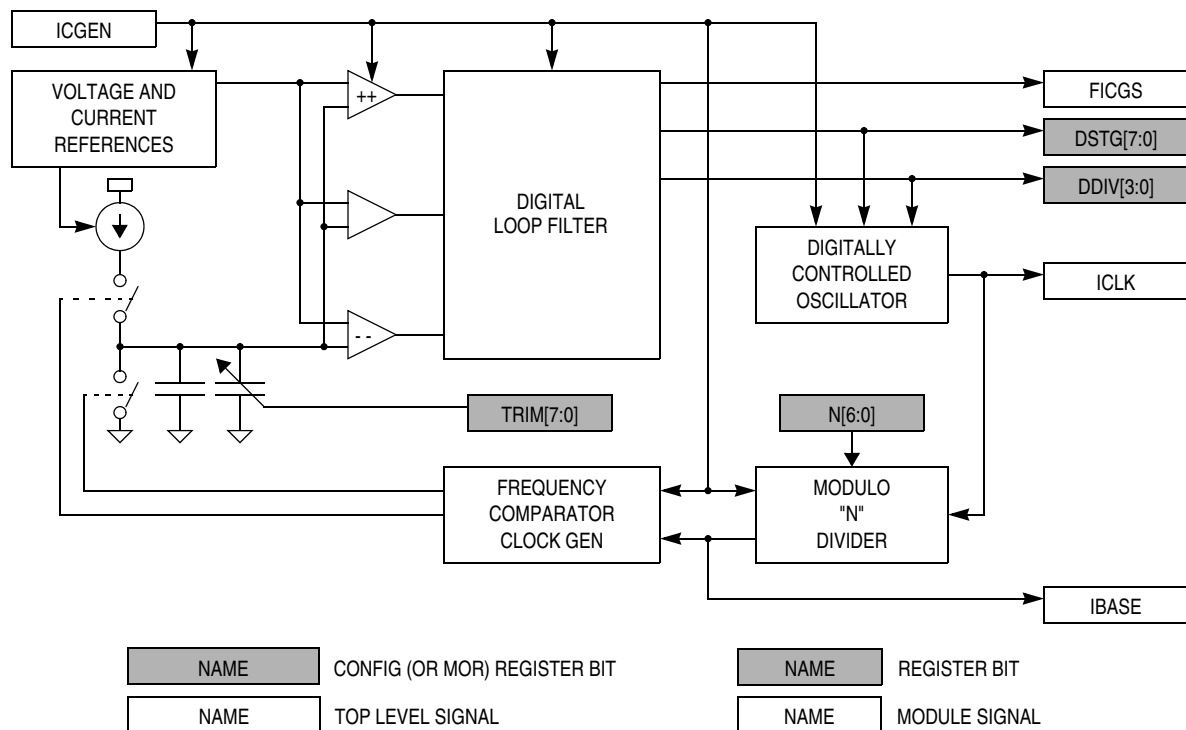| Source Form	Operation	Description	V	H	I	N	Z	C	Address Mode	Opcode	Operand	Cycles
BHS rel	Branch if Higher or Same (Same as BCC)	PC ← (PC) + 2 + rel ? (C) = 0	–	–	–	–	–	–	REL	24	rr	3
BIH rel	Branch if $\overline{IRQ}$ Pin High	PC ← (PC) + 2 + rel ? $\overline{IRQ}$ = 1	–	–	–	–	–	–	REL	2F	rr	3
BIL rel	Branch if $\overline{IRQ}$ Pin Low	PC ← (PC) + 2 + rel ? $\overline{IRQ}$ = 0	–	–	–	–	–	–	REL	2E	rr	3
BIT #opr BIT opr BIT opr BIT opr,X BIT opr,X BIT ,X BIT opr,SP BIT opr,SP	Bit Test	(A) & (M)	0	–	–	↕	↕	–	IMM DIR EXT IX2 IX1 IX SP1 SP2	A5 B5 C5 D5 E5 F5 9EE5 9ED5	ii dd hh ll ee ff ff ff ee ff	2 3 4 4 3 2 4 5
BLE opr	Branch if Less Than or Equal To (Signed Operands)	PC ← (PC) + 2 + rel ? (Z) | (N ⊕ V) = 1	–	–	–	–	–	–	REL	93	rr	3
BLO rel	Branch if Lower (Same as BCS)	PC ← (PC) + 2 + rel ? (C) = 1	–	–	–	–	–	–	REL	25	rr	3
BLS rel	Branch if Lower or Same	PC ← (PC) + 2 + rel ? (C) | (Z) = 1	–	–	–	–	–	–	REL	23	rr	3
BLT opr	Branch if Less Than (Signed Operands)	PC ← (PC) + 2 + rel ? (N ⊕ V) =1	–	–	–	–	–	–	REL	91	rr	3
BMC rel	Branch if Interrupt Mask Clear	PC ← (PC) + 2 + rel ? (I) = 0	–	–	–	–	–	–	REL	2C	rr	3
BMI rel	Branch if Minus	PC ← (PC) + 2 + rel ? (N) = 1	–	–	–	–	–	–	REL	2B	rr	3
BMS rel	Branch if Interrupt Mask Set	PC ← (PC) + 2 + rel ? (I) = 1	–	–	–	–	–	–	REL	2D	rr	3
BNE rel	Branch if Not Equal	PC ← (PC) + 2 + rel ? (Z) = 0	–	–	–	–	–	–	REL	26	rr	3
BPL rel	Branch if Plus	PC ← (PC) + 2 + rel ? (N) = 0	–	–	–	–	–	–	REL	2A	rr	3
BRA rel	Branch Always	PC ← (PC) + 2 + rel	–	–	–	–	–	–	REL	20	rr	3
BRCLR n,opr,rel	Branch if Bit n in M Clear	PC ← (PC) + 3 + rel ? (Mn) = 0	–	–	–	–	–	↕	DIR (b0) DIR (b1) DIR (b2) DIR (b3) DIR (b4) DIR (b5) DIR (b6) DIR (b7)	01 03 05 07 09 0B 0D 0F	dd rr dd rr dd rr dd rr dd rr dd rr dd rr dd rr	5 5 5 5 5 5 5 5
BRN rel	Branch Never	PC ← (PC) + 2	–	–	–	–	–	–	REL	21	rr	3
BRSET n,opr,rel	Branch if Bit n in M Set	PC ← (PC) + 3 + rel ? (Mn) = 1	–	–	–	–	–	↕	DIR (b0) DIR (b1) DIR (b2) DIR (b3) DIR (b4) DIR (b5) DIR (b6) DIR (b7)	00 02 04 06 08 0A 0C 0E	dd rr dd rr dd rr dd rr dd rr dd rr dd rr dd rr	5 5 5 5 5 5 5 5
BSET n,opr	Set Bit n in M	Mn ← 1	–	–	–	–	–	–	DIR (b0) DIR (b1) DIR (b2) DIR (b3) DIR (b4) DIR (b5) DIR (b6) DIR (b7)	10 12 14 16 18 1A 1C 1E	dd dd dd dd dd dd dd dd	4 4 4 4 4 4 4 4
BSR rel	Branch to Subroutine	PC ← (PC) + 2; push (PCL) SP ← (SP) − 1; push (PCH) SP ← (SP) − 1 PC ← (PC) + rel	–	–	–	–	–	–	REL	AD	rr	4
CBEQ opr,rel CBEQA #opr,rel CBEQX #opr,rel CBEQ opr,X+,rel CBEQ X+,rel CBEQ opr,SP,rel	Compare and Branch if Equal	PC ← (PC) + 3 + rel ? (A) − (M) = $00 PC ← (PC) + 3 + rel ? (A) − (M) = $00 PC ← (PC) + 3 + rel ? (X) − (M) = $00 PC ← (PC) + 3 + rel ? (A) − (M) = $00 PC ← (PC) + 2 + rel ? (A) − (M) = $00 PC ← (PC) + 4 + rel ? (A) − (M) = $00	–	–	–	–	–	–	DIR IMM IMM IX1+ IX+ SP1	31 41 51 61 71 9E61	dd rr ii rr ii rr ff rr rr ff rr	5 4 4 5 4 6
CLC	Clear Carry Bit	C ← 0	–	–	–	–	–	0	INH	98		1
CLI	Clear Interrupt Mask	I ← 0	–	–	0	–	–	–	INH	9A		2

Figure 7-2. Internal Clock Generator Block Diagram

7.3.2.1 Digitally Controlled Oscillator

The digitally controlled oscillator (DCO) is an inaccurate oscillator which generates the internal clock (ICLK). The clock period of ICLK is dependent on the digital loop filter outputs (DSTG[7:0] and DDIV[3:0]). Because there is only a limited number of bits in DDIV and DSTG, the precision of the output (ICLK) is restricted to a precision of approximately ±0.202% to ±0.368% when measured over several cycles (of the desired frequency). Additionally, since the propagation delays of the devices used in the DCO ring oscillator are a measurable fraction of the bus clock period, reaching the long-term precision may require alternately running faster and slower than desired, making the worst case cycle-to-cycle frequency variation ±6.45% to ±11.8% (of the desired frequency). The valid values of DDIV:DSTG range from $000 to $9FF. For more information on the quantization error in the DCO, see 7.4.4 Quantization Error in DCO Output.

7.3.2.2 Modulo "N" Divider

The modulo "N" divider creates the low frequency base clock (IBASE) by dividing the internal clock (ICLK) by the ICG multiplier factor (N), contained in the ICG multiplier register (ICGMR). When N is programmed to a $01 or $00, the divider is disabled and ICLK is passed through to IBASE undivided. When the ICG is stable, the frequency of IBASE will be equal to the nominal frequency (f_{NOM}) of 307.2 kHz ± 25%.

7.3.2.3 Frequency Comparator

The frequency comparator effectively compares the low frequency base clock (IBASE) to a nominal frequency, f_{NOM}. First, the frequency comparator converts IBASE to a voltage by charging a known capacitor with a current reference for a period dependent on IBASE. This voltage is compared to a voltage

near 307.2 kHz. For proper operation, EREF must be at least twice as slow as IBASE and IREF must be at least twice as slow as ECLK.

To guarantee that IREF is slower than ECLK and EREF is slower than IBASE, one of the signals is divided down. Which signal is divided and by how much is determined by the external slow (EXTSLOW) and external crystal enable (EXTXTALEN) bits in the CONFIG (or MOR) register, according to the rules in Table 7-2.

NOTE
Each signal (IBASE and ECLK) is always divided by four. A longer divider is used on either IBASE or ECLK based on the EXTSLOW bit.

Table 7-2. Clock Monitor Reference Divider Ratios

ICGON	ECGON	ECGS	EXTSLOW	EXTXTALEN	External Frequency		EREF Divider Ratio	EREF Frequency	ESTBCLK Divider Ratio	ESTBCLK Frequency	IREF Divider Ratio[1]	IREF Frequency
0	x	x	x	x	U		U	U	U	U	Off	0
x	0	0	x	x	0		Off	0	Off	0	U	U
1	1	0	x	0	Minimum	60 Hz	Off	0	16 (ECLK)	3.75 Hz	1*4	76.8 kHz ± 25%
					Maximum	32 MHz				2.0 MHz		
1	1	0	x	1	Minimum	30 kHz	Off	0	4096 (ECLK)	7.324 kHz	1*4	76.8 kHz ± 25%
					Maximum	8 MHz				1.953 kHz		
1	1	1	0	0	Minimum	307.2 kHz	128*4	600 Hz	16 (ECLK)	19.2 kHz	1*4	76.8 kHz ± 25%
					Maximum	32 MHz		62.5 kHz		2.0 MHz		
1	1	1	0	1	Minimum	1 MHz	128*4	1.953 kHz	4096 (ECLK)	244 Hz	1*4	76.8 kHz ± 25%
					Maximum	8 MHz		15.63 kHz		1.953 kHz		
1	1	1	1	0	Minimum	60 Hz	1*4	15 Hz	16 (IBASE)[2]	19.2 kHz ± 25%	4096*4	18.75 Hz ± 125%
					Maximum	307.2 kHz		76.8 kHz				
1	1	1	1	1	Minimum	30 kHz	1*4	7.5 kHz	4096 (IBASE)[2]	75 Hz ± 25%	16*4	4.8 kHz ± 25%
					Maximum	100 kHz		25.0 kHz				

1. U = Unaffected; refer to section of table where ICGON or ECGON is set to 1.
2. IBASE is always used as the internal frequency (307.2 kHz).

To conserve size, the long divider (divide by 4096) is also used as an external crystal stabilization divider. The divider is reset when the external clock generator is turned off or in STOP (ECGEN is clear). When the external clock generator is first turned on, the external clock generator stable bit (ECGS) will be clear. This condition automatically selects ECLK as the input to the long divider. The external stabilization clock (ESTBCLK) will be ECLK divided by 16 when EXTXTALEN is low or 4096 when EXTXTALEN is high. This time-out allows the crystal to stabilize. The falling edge of ESTBCLK is used to set ECGS (ECGS will set after a full 16 or 4096 cycles). When ECGS is set, the divider returns to its normal function. ESTBCLK may be generated by either IBASE or ECLK, but any clocking will only reinforce the set condition. If ECGS is cleared because the clock monitor determined that ECLK was inactive, the divider will revert to a stabilization divider. Since this will change the EREF and IREF divide ratios, it is important to turn the clock monitor off (CMON = 0) after inactivity is detected to ensure valid recovery.

Chapter 10
Low-Voltage Inhibit (LVI)

10.1 Introduction

This section describes the low-voltage inhibit (LVI) module, which monitors the voltage on the V_{DD} pin and can force a reset when the V_{DD} voltage falls below the LVI trip falling voltage, V_{TRIPF}.

10.2 Features

Features of the LVI module include:
- Programmable LVI reset
- Programmable power consumption
- Selectable LVI trip voltage
- Programmable stop mode operation

10.3 Functional Description

Figure 10-1 shows the structure of the LVI module. LVISTOP, LVIPWRD, LVI5OR3, and LVIRSTD are user selectable options found in the configuration register (CONFIG1). See Chapter 4 Configuration Register (CONFIG).
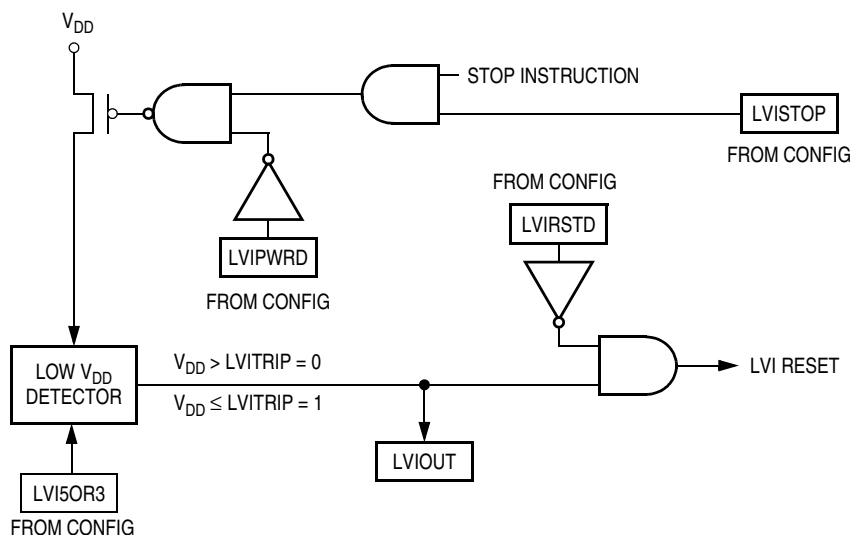
Figure 10-1. LVI Module Block Diagram

The LVI is enabled out of reset. The LVI module contains a bandgap reference circuit and comparator. Clearing the LVI power disable bit, LVIPWRD, enables the LVI to monitor V_{DD} voltage. Clearing the LVI reset disable bit, LVIRSTD, enables the LVI module to generate a reset when V_{DD} falls below a voltage, V_{TRIPF}. Setting the LVI enable in stop mode bit, LVISTOP, enables the LVI to operate in stop mode.

Chapter 11
Input/Output (I/O) Ports (PORTS)

11.1 Introduction

Thirteen bidirectional input/output (I/O) pins form two parallel ports in the 16-pin plastic dual in-line package (PDIP) and small outline integrated circuit (SOIC) package in the MC68HC908KX8 part. All I/O pins are programmable as inputs or outputs. Port A has software selectable pullup resistors if the port is used as a general-function input port.

NOTE
Connect any unused I/O pins to an appropriate logic level, either V_{DD} or V_{SS}. Although the I/O ports do not require termination for proper operation, termination reduces excess current consumption and the possibility of electrostatic damage.

See Figure 11-1 for a summary of the I/O port registers.

Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
$0000	Port A Data Register (PTA) See page 106.	Read:	0	0	0	PTA4	PTA3	PTA2	PTA1	PTA0
		Write:				PTA4	PTA3	PTA2	PTA1	PTA0
		Reset:				Unaffected by reset				
$0001	Port B Data Register (PTB) See page 108.	Read:	PTB7	PTB6	PTB5	PTB4	PTB3	PTB2	PTB1	PTB0
		Write:	PTB7	PTB6	PTB5	PTB4	PTB3	PTB2	PTB1	PTB0
		Reset:				Unaffected by reset				
$0004	Data Direction Register A (DDRA) See page 106.	Read:	0	0	0	DDRA4	DDRA3	DDRA2	DDRA1	DDRA0
		Write:				DDRA4	DDRA3	DDRA2	DDRA1	DDRA0
		Reset:	0	0	0	0	0	0	0	0
$0005	Data Direction Register B (DDRB) See page 109.	Read:	DDRB7	DDRB6	DDRB5	DDRB4	DDRB3	DDRB2	DDRB1	DDRB0
		Write:	DDRB7	DDRB6	DDRB5	DDRB4	DDRB3	DDRB2	DDRB1	DDRB0
		Reset:	0	0	0	0	0	0	0	0
$000D	Port A Input Pullup Enable Register (PTAPUE) See page 108.	Read:	0	0	0	PTAPUE4	PTAPUE3	PTAPUE2	PTAPUE1	PTAPUE0
		Write:				PTAPUE4	PTAPUE3	PTAPUE2	PTAPUE1	PTAPUE0
		Reset:	0	0	0	0	0	0	0	0

☐ = Unimplemented

Figure 11-1. I/O Port Register Summary

12.7 I/O Registers

These I/O registers control and monitor SCI operation:

- SCI control register 1 (SCC1)
- SCI control register 2 (SCC2)
- SCI control register 3 (SCC3)
- SCI status register 1 (SCS1)
- SCI status register 2 (SCS2)
- SCI data register (SCDR)
- SCI baud rate register (SCBR)

12.7.1 SCI Control Register 1

SCI control register 1 (SCC1):

- Enables loop mode operation
- Enables the SCI
- Controls output polarity
- Controls character length
- Controls SCI wakeup method
- Controls idle character detection
- Enables parity function
- Controls parity type

Address: $0013

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	LOOPS	ENSCI	TXINV	M	WAKE	ILTY	PEN	PTY
Reset:	0	0	0	0	0	0	0	0

Figure 12-10. SCI Control Register 1 (SCC1)

LOOPS — Loop Mode Select Bit
This read/write bit enables loop mode operation. In loop mode the RxD pin is disconnected from the SCI, and the transmitter output goes into the receiver input. Both the transmitter and the receiver must be enabled to use loop mode. Reset clears the LOOPS bit.
  1 = Loop mode enabled
  0 = Normal operation enabled

ENSCI — Enable SCI Bit
This read/write bit enables the SCI and the SCI baud rate generator. Clearing ENSCI sets the SCTE and TC bits in SCI status register 1 and disables transmitter interrupts. Reset clears the ENSCI bit.
  1 = SCI enabled
  0 = SCI disabled

SCRF — SCI Receiver Full Bit

This clearable, read-only bit is set when the data in the receive shift register transfers to the SCI data register. SCRF can generate an SCI receiver CPU interrupt request. When the SCRIE bit in SCC2 is set the SCRF generates a CPU interrupt request. In normal operation, clear the SCRF bit by reading SCS1 with SCRF set and then reading the SCDR. Reset clears SCRF.

    1 = Received data available in SCDR
    0 = Data not available in SCDR

IDLE — Receiver Idle Bit

This clearable, read-only bit is set when 10 or 11 consecutive 1s appear on the receiver input. IDLE generates an SCI error CPU interrupt request if the ILIE bit in SCC2 is also set. Clear the IDLE bit by reading SCS1 with IDLE set and then reading the SCDR. After the receiver is enabled, it must receive a valid character that sets the SCRF bit before an idle condition can set the IDLE bit. Also, after the IDLE bit has been cleared, a valid character must again set the SCRF bit before an idle condition can set the IDLE bit. Reset clears the IDLE bit.

    1 = Receiver input idle
    0 = Receiver input active (or idle since the IDLE bit was cleared)

OR — Receiver Overrun Bit

This clearable, read-only bit is set when software fails to read the SCDR before the receive shift register receives the next character. The OR bit generates an SCI error CPU interrupt request if the ORIE bit in SCC3 is also set. The data in the shift register is lost, but the data already in the SCDR is not affected. Clear the OR bit by reading SCS1 with OR set and then reading the SCDR. Reset clears the OR bit.

    1 = Receive shift register full and SCRF = 1
    0 = No receiver overrun

Software latency may allow an overrun to occur between reads of SCS1 and SCDR in the flag-clearing sequence. Figure 12-14 shows the normal flag-clearing sequence and an example of an overrun caused by a delayed flag-clearing sequence. The delayed read of SCDR does not clear the OR bit because OR was not set when SCS1 was read. Byte 2 caused the overrun and is lost. The next flag-clearing sequence reads byte 3 in the SCDR instead of byte 2.

In applications that are subject to software latency or in which it is important to know which byte is lost due to an overrun, the flag-clearing routine can check the OR bit in a second read of SCS1 after reading the data register.

NF — Receiver Noise Flag Bit

This clearable, read-only bit is set when the SCI detects noise on the RxD pin. NF generates an NF CPU interrupt request if the NEIE bit in SCC3 is also set. Clear the NF bit by reading SCS1 and then reading the SCDR. Reset clears the NF bit.

    1 = Noise detected
    0 = No noise detected

FE — Receiver Framing Error Bit

This clearable, read-only bit is set when a 0 is accepted as the stop bit. FE generates an SCI error CPU interrupt request if the FEIE bit in SCC3 also is set. Clear the FE bit by reading SCS1 with FE set and then reading the SCDR. Reset clears the FE bit.

    1 = Framing error detected
    0 = No framing error detected

SCP1 and SCP0 — SCI Baud Rate Prescaler Bits
These read/write bits select the baud rate prescaler divisor as shown in Table 12-6. Reset clears SCP1 and SCP0.

Table 12-6. SCI Baud Rate Prescaling

SCP[1:0]	Prescaler Divisor (PD)
00	1
01	3
10	4
11	13

SCR2–SCR0 — SCI Baud Rate Select Bits
These read/write bits select the SCI baud rate divisor as shown in Table 12-7. Reset clears SCR2–SCR0.

Table 12-7. SCI Baud Rate Selection

SCR[2:1:0]	Baud Rate Divisor (BD)
000	1
001	2
010	4
011	8
100	16
101	32
110	64
111	128

Use this formula to calculate the SCI baud rate:

$$\text{Baud rate} = \frac{f_{BAUDCLK}}{64 \times PD \times BD}$$

where:
$f_{BAUDCLK}$ = baud clock frequency
PD = prescaler divisor
BD = baud rate divisor

Table 12-8 shows the SCI baud rates that can be generated with a 4.9152-MHz CGMXCLK frequency.

15.8 I/O Registers

These I/O registers control and monitor operation of the TIM:
- TIM status and control register (TSC)
- TIM control registers (TCNTH and TCNTL)
- TIM counter modulo registers (TMODH and TMODL)
- TIM channel status and control registers (TSC0 and TSC1)
- TIM channel registers (TCH0H and TCH0L, TCH1H and TCH1L)

15.8.1 TIM Status and Control Register

The TIM status and control register (TSC):
- Enables TIM overflow interrupts
- Flags TIM overflows
- Stops the TIM counter
- Resets the TIM counter
- Prescales the TIM counter clock

Address: $0020

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	TOF	TOIE	TSTOP	0	0	PS2	PS1	PS0
Write:	0			TRST				
Reset:	0	0	1	0	0	0	0	0

= Unimplemented

Figure 15-5. TIM Status and Control Register (TSC)

TOF — TIM Overflow Flag Bit
This read/write flag is set when the TIM counter reaches the modulo value programmed in the TIM counter modulo registers. Clear TOF by reading the TIM status and control register when TOF is set and then writing a 0 to TOF. If another TIM overflow occurs before the clearing sequence is complete, then writing 0 to TOF has no effect. Therefore, a TOF interrupt request cannot be lost due to inadvertent clearing of TOF. Reset clears the TOF bit. Writing a 1 to TOF has no effect.
   1 = TIM counter has reached modulo value.
   0 = TIM counter has not reached modulo value.

TOIE — TIM Overflow Interrupt Enable Bit
This read/write bit enables TIM overflow interrupts when the TOF bit becomes set. Reset clears the TOIE bit.
   1 = TIM overflow interrupts enabled
   0 = TIM overflow interrupts disabled

TSTOP — TIM Stop Bit
This read/write bit stops the TIM counter. Counting resumes when TSTOP is cleared. Reset sets the TSTOP bit, stopping the TIM counter until software clears the TSTOP bit.
   1 = TIM counter stopped
   0 = TIM counter active

NOTE
Do not set the TSTOP bit before entering wait mode if the TIM is required to exit wait mode.

Table 15-3. Mode, Edge, and Level Selection

MSxB	MSxA	ELSxB	ELSxA	Mode	Configuration
X	0	0	0	Output preset	Pin under port control; initial output level high
X	1	0	0		Pin under port control; initial output level low
0	0	0	1	Input capture	Capture on rising edge only
0	0	1	0		Capture on falling edge only
0	0	1	1		Capture on rising or falling edge
0	1	0	0	Output compare or PWM	Software compare only
0	1	0	1		Toggle output on compare
0	1	1	0		Clear output on compare
0	1	1	1		Set output on compare
1	X	0	1	Buffered output compare or buffered PWM	Toggle output on compare
1	X	1	0		Clear output on compare
1	X	1	1		Set output on compare

> **NOTE**
> *Before enabling a TIM channel register for input capture operation, make sure that the PTAx/TCHx pin is stable for at least two bus clocks.*

TOVx — Toggle On Overflow Bit

When channel x is an output compare channel, this read/write bit controls the behavior of the channel x output when the TIM counter overflows. When channel x is an input capture channel, TOVx has no effect. Reset clears the TOVx bit.

    1 = Channel x pin toggles on TIM counter overflow.
    0 = Channel x pin does not toggle on TIM counter overflow.

> **NOTE**
> *When TOVx is set, a TIM counter overflow takes precedence over a channel x output compare if both occur at the same time.*

CHxMAX — Channel x Maximum Duty Cycle Bit

When the TOVx bit is at 1 and clear output on compare is selected, setting the CHxMAX bit forces the duty cycle of buffered and unbuffered PWM signals to 100 percent. As Figure 15-9 shows, the CHxMAX bit takes effect in the cycle after it is set or cleared. The output stays at 100 percent duty cycle level until the cycle after CHxMAX is cleared.

> **NOTE**
> *The PWM 0 percent duty cycle is defined as output low all of the time. To generate the 0 percent duty cycle, select clear output on compare and then clear the TOVx bit (CHxMAX = 0). The PWM 100 percent duty cycle is defined as output high all of the time. To generate the 100 percent duty cycle, use the CHxMAX bit in the TSCx register.*
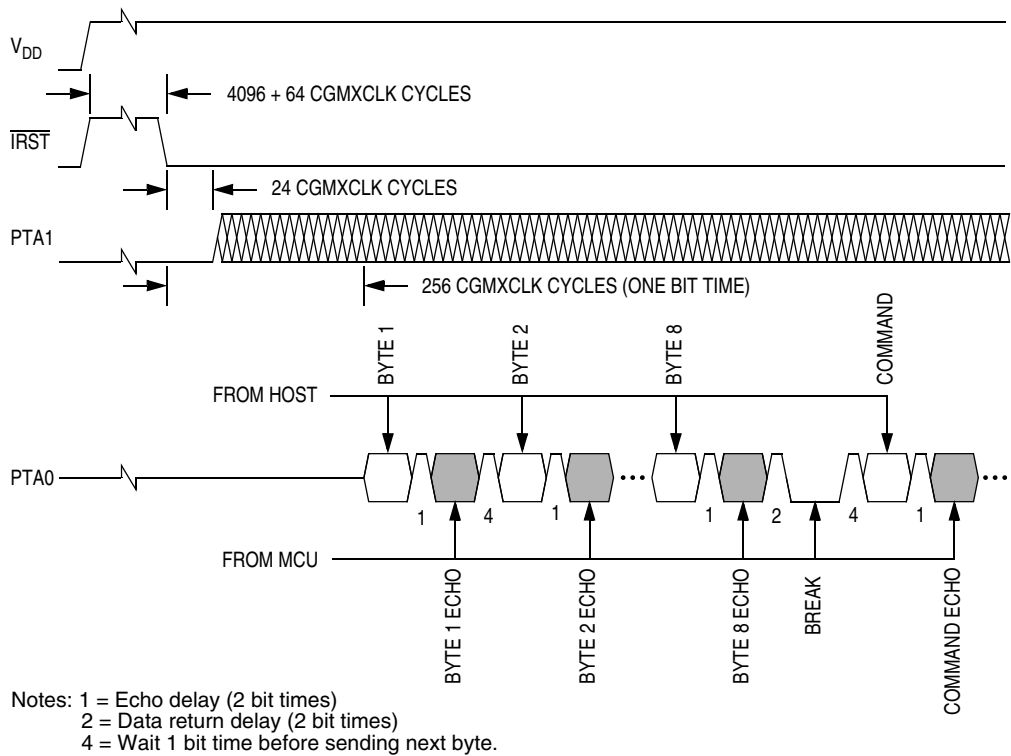
Figure 16-15. Monitor Mode Entry Timing

After receiving the eight security bytes from the host, the MCU transmits a break character signalling that it is ready to receive a command.

> **NOTE**
> *The MCU does not transmit a break character until after the host sends the eight security bytes.*

Chapter 17
Electrical Specifications

17.1 Introduction

This section contains electrical and timing specifications.

17.2 Absolute Maximum Ratings

Maximum ratings are the extreme limits to which the microcontroller unit (MCU) can be exposed without permanently damaging it.

> **NOTE**
> *This device is not guaranteed to operate properly at the maximum ratings. Refer to 17.5 5.0-Vdc DC Electrical Characteristics, and   for guaranteed operating conditions.*

Characteristic[1]	Symbol	Value	Unit
Supply voltage	V_{DD}	−0.3 to +6.0	V
Input voltage	V_{In}	V_{SS} −0.3 to V_{DD} +0.3	V
Maximum current per pin Excluding V_{DD}, V_{SS}, and PTA0–PTA4	I	±15	mA
Maximum current for pins PTA0–PTA4	I_{PTA0}–I_{PTA4}	±25	mA
Maximum current out of V_{SS}	I_{MVSS}	100	mA
Maximum current into V_{DD}	I_{MVDD}	100	mA
Storage temperature	T_{STG}	−55 to +150	°C

1. Voltages referenced to V_{SS}

> **NOTE**
> *This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum-rated voltages to this high-impedance circuit. For proper operation, it is recommended that V_{In} and V_{Out} be constrained to the range $V_{SS} \leq (V_{In}$ or $V_{Out}) \leq V_{DD}$. Reliability of operation is enhanced if unused inputs are connected to an appropriate logic voltage level (for example, either V_{SS} or V_{DD}).*

17.5 5.0-Vdc DC Electrical Characteristics

Characteristic[1]	Symbol	Min	Typ[2]	Max	Unit
Output high voltage I_{Load} = −2.0 mA, all I/O pins I_{Load} = −10.0 mA, all I/O pins I_{Load} = −15.0 mA, PTA0–PTA4 only	V_{OH}	V_{DD} −0.4 V_{DD} −1.5 V_{DD} −0.8	— — —	— — —	V
Output low voltage I_{Load} = 1.6 mA, all I/O pins I_{Load} = 10.0 mA, all I/O pins I_{Load} = 15.0 mA, PTA0–PTA4 only	V_{OL}	— — —	— — —	0.4 1.5 0.8	V
Input high voltage — all ports, $\overline{IRQ1}$	V_{IH}	0.7 x V_{DD}	—	V_{DD} + 0.3	V
Input low voltage — all ports, $\overline{IRQ1}$	V_{IL}	V_{SS}	—	0.3 x V_{DD}	V
V_{DD} supply current Run[3], [4] Wait[4], [5] Stop, 25°C[6]	I_{DD}	— — —	15 2.2 0.8	25 5 1.75	mA mA µA
I/O ports Hi-Z leakage current[7]	I_{IL}	−10	—	+10	µA
Input current	I_{In}	−10	—	+10	µA
Capacitance Ports (as input or output)	C_{Out} C_{In}	— —	— —	12 8	pF
POR rearm voltage[8]	V_{POR}	0	—	100	mV
POR reset voltage[9]	V_{POR}	0	700	800	mV
POR rise time ramp rate	R_{POR}	0.035	—	—	V/ms
Monitor mode entry voltage	V_{TST}	V_{DD}+ 2.5		V_{DD}+ 4.0	V
Low-voltage inhibit reset, trip falling voltage	V_{TRIPF}	3.90	4.25	4.50	V
Low-voltage inhibit reset, trip rising voltage	V_{TRIPR}	4.20	4.35	4.60	V
Low-voltage inhibit reset/recover hysteresis	V_{HYS}	—	100	—	mV
Pullup resistor PTA0–PTA4, $\overline{IRQ1}$	R_{PU}	24	—	48	kΩ

1. V_{DD} = 5.5 Vdc to 4.5 Vdc, V_{SS} = 0 Vdc, T_A = −40°C to +125°C, unless otherwise noted
2. Typical values reflect average measurements at midpoint of voltage range, 25°C only.
3. Run (operating) I_{DD} measured using internal oscillator at its 32-MHz rate. V_{DD} = 5.5 Vdc. All inputs 0.2 V from rail. No dc loads. Less than 100 pF on all outputs. All ports configured as inputs. Measured with all modules enabled.
4. All measurements taken with LVI enabled.
5. Wait I_{DD} measured using internal oscillator at its 1-MHz rate. All inputs 0.2 V from rail; no dc loads; less than 100 pF on all outputs. All ports configured as inputs.
6. Stop I_{DD} is measured with no port pin sourcing current; all modules are disabled. OSCSTOPEN option is not selected.
7. Pullups and pulldowns are disabled.
8. Maximum is highest voltage that POR is guaranteed.
9. Maximum is highest voltage that POR is possible.

17.11 Memory Characteristics

Characteristic	Symbol	Min	Typ	Max	Unit
RAM data retention voltage	V_{RDR}	1.3	—	—	V
FLASH program bus clock frequency	—	1	—	—	MHz
FLASH read bus clock frequency	f_{Read}[1]	0	—	8 M	Hz
FLASH page erase time <1 K cycles >1 K cycles	t_{Erase}	0.9 3.6	1 4	1.1 5.5	ms
FLASH mass erase time	t_{MErase}	4	—	—	ms
FLASH PGM/ERASE to HVEN setup time	t_{NVS}	10	—	—	μs
FLASH high-voltage hold time	t_{NVH}	5	—	—	μs
FLASH high-voltage hold time (mass erase)	t_{NVHL}	100	—	—	μs
FLASH program hold time	t_{PGS}	5	—	—	μs
FLASH program time	t_{PROG}	30	—	40	μs
FLASH return to read time	t_{RCV}[2]	1	—	—	μs
FLASH cumulative program HV period	t_{HV}[3]	—	—	4	ms
FLASH endurance[4]	—	10 k	100 k	—	Cycles
FLASH data retention time[5]	—	15	100	—	Years

1. f_{Read} is defined as the frequency range for which the FLASH memory can be read.
2. t_{RCV} is defined as the time it needs before the FLASH can be read after turning off the high voltage charge pump, by clearing HVEN to 0.
3. t_{HV} is defined as the cumulative high voltage programming time to the same row before next erase.
   t_{HV} must satisfy this condition: $t_{NVS} + t_{NVH} + t_{PGS} + (t_{PROG}$ x 64$) \leq t_{HV}$ maximum.
4. Typical endurance was evaluated for this product family. For additional information on how Freescale defines *Typical Endurance*, please refer to Engineering Bulletin EB619.
5. Typical data retention values are based on intrinsic capability of the technology measured at high temperature and de-rated to 25°C using the Arrhenius equation. For additional information on how Freescale defines *Typical Data Retention*, please refer to Engineering Bulletin EB618.

Chapter 18
Ordering Information and Mechanical Specifications

18.1 Introduction

This section contains ordering numbers for MC68HC908KX8 and MC68HC908KX2. Refer to Figure 18-1 for an example of the device numbering system.

In addition, this section gives the package dimensions for:

- 16-pin plastic dual in-line package (case number 648D)
- 16-pin small outline package (case number 751G)

18.2 MC Order Numbers

Table 18-1. MC Order Numbers

MC Order Number[1]	Operating Temperature Range
MC68HC908KX8CP MC68HC908KX8CDW	−40°C to +85°C
MC68HC908KX8VP MC68HC908KX8VDW	−40°C to +105°C
MC68HC908KX8MP MC68HC908KX8MDW	−40°C to +125°C
MC68HC908KX2CP MC68HC908KX2CDW	−40°C to +85°C
MC68HC908KX2VP MC68HC908KX2VDW	−40°C to +105°C
MC68HC908KX2MP MC68HC908KX2MDW	−40°C to +125°C

1. P = Plastic dual in-line package
   DW = Small outline package

M C 6 8 H C 9 0 8 K X 8 X X X

FAMILY ← → PACKAGE DESIGNATOR
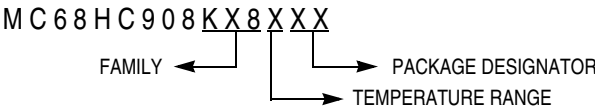→ TEMPERATURE RANGE

Figure 18-1. Device Numbering System

B.4.8 Trimmed Accuracy of the Internal Clock Generator

The unadjusted frequency of the low-frequency base clock (IBASE), when the comparators in the frequency comparator indicate zero error, can vary as much as ±25% due to process, temperature, and voltage. The trimming capability exists to compensate for process affects. The remaining variation in frequency is due to temperature, voltage, and change in target frequency (multiply register setting). These affects are designed to be minimal, however variation does occur. Better performance is seen at 3 V and lower settings of N.

B.4.8.1 2.7-Volt to 3.3-Volt Trimmed Internal Clock Generator Characteristics

Characteristic[1]	Symbol	Min	Typ	Max	Unit
Absolute trimmed internal oscillator tolerance[2], [3] −40°C to 85°C	F_{abs_tol}	—	1.5	5.0	%
Variation over temperature[3], [4]	V_{ar_temp}	—	0.03	0.05	%/C
Variation over voltage[3], [5] 25°C −40°C to 85°C	V_{ar_volt}	— —	0.5 0.7	2.0 2.0	%/V

1. These specifications concern long-term frequency variation. Each measurement is taken over a 1-ms period.
2. Absolute value of variation in ICG output frequency, trimmed at nominal V_{DD} and temperature, as temperature and V_{DD} are allowed to vary for a single given setting of N.
3. Specification is characterized but not tested.
4. Variation in ICG output frequency for a fixed N and voltage
5. Variation in ICG output frequency for a fixed N

B.4.8.2 4.5-Volt to 5.5-Volt Trimmed Internal Clock Generator Characteristics

Characteristic[1]	Symbol	Min	Typ	Max	Unit
Absolute trimmed internal oscillator tolerance[2], [3] −40°C to 85°C	F_{abs_tol}	—	4.0	7.0	%
Variation over temperature[3], [4]	V_{ar_temp}	—	0.05	0.08	%/C
Variation over voltage[3], [5] 25°C −40°C to 85°C	V_{ar_volt}	— —	1.0 1.0	2.0 2.0	%/V

1. These specifications concern long-term frequency variation. Each measurement is taken over a 1-ms period.
2. Absolute value of variation in ICG output frequency, trimmed at nominal V_{DD} and temperature, as temperature and V_{DD} are allowed to vary for a single given setting of N.
3. Specification is characterized but not tested.
4. Variation in ICG output frequency for a fixed N and voltage
5. Variation in ICG output frequency for a fixed N