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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | HC08 |
| Core Size | 8-Bit |
| Speed | 8MHz |
| Connectivity | SCI |
| Peripherals | LVD, POR, PWM |
| Number of I/O | 13 |
| Program Memory Size | 8KB (8K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 192 x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.7V ~ 5.5V |
| Data Converters | A/D 4x8b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 125°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 16-SOIC (0.295", 7.50mm Width) |
| Supplier Device Package | 16-SOIC |
| Purchase URL | https://www.e-xfl.com/product-detail/nxp-semiconductors/mc908kx8mdwer2 |

## Chapter 13
## System Integration Module (SIM)

## Chapter 14
## Timebase Module (TBM)



## Chapter 15
## Timer Interface Module (TIM)



## Chapter 16
## Development Support

## Chapter 17
## Electrical Specifications

### 1.4.2 Oscillator Pins (OSC1 and OSC2)

The OSC1 and OSC2 pins are available through programming options in the configuration register. These pins then become the connections to an external clock source or crystal/ceramic resonator. PTB7 and PTB6 are not available for the crystal/ceramic resonator option and PTB6 is unavailable for the external clock source option.

### 1.4.3 External Interrupt Pin ($\overline{\text{IRQ1}}$)

$\overline{\text{IRQ1}}$ is an asynchronous external interrupt pin with an internal pullup resistor. See Chapter 8 External Interrupt (IRQ).

### 1.4.4 Port A Input/Output (I/O) Pins (PTA4/$\overline{\text{KBD4}}$–PTA0/$\overline{\text{KBD0}}$)

PTA4/$\overline{\text{KBD4}}$–PTA0/$\overline{\text{KBD0}}$ is a 5-bit special-function port that shares its pins with the keyboard interrupt (KBI) module and the 2-channel timer module (TIM).

- Any or all of the port A pins can be programmed to serve as keyboard interrupt pins. The respective pin utilizes an internal pullup resistor when enabled. See Chapter 9 Keyboard Interrupt Module (KBI).
- Each port A pin contains a software selectable internal pullup resistor when the general-function I/O port is configured as an input. See Chapter 11 Input/Output (I/O) Ports (PORTS). The pullup resistor is automatically disabled once a TIM special function is enabled for that pin.
- All port A pins are high-current source/sink pins.

***NOTE***

*Any unused inputs and I/O ports should be tied to an appropriate logic level (either $V_{DD}$ or $V_{SS}$). Although the I/O ports of the MC68HC908KX8 do not require termination, termination is recommended to reduce the possibility of static damage.*

### 1.4.5 Analog Reference Pin ($V_{REFH}$)

The $V_{REFH}$ pin is the analog reference voltage for the analog-to-digital converter (ADC) module. The voltage is supplied through a double-bond to the $V_{DD}$ pin. See Chapter 17 Electrical Specifications for ADC parameters.

### 1.4.6 Port B Input/Output (I/O) Pins (PTB7/(OSC2)/$\overline{\text{RST}}$–PTB0/AD0)

PTB7/(OSC2)/$\overline{\text{RST}}$–PTB0/AD0 are general-purpose bidirectional I/O port pins, all sharing special functions.

- PTB7 and PTB6 share with the on-chip oscillator circuit through configuration options. See 7.3.3 External Clock Generator.
- PTB5 and PTB4 share with the SCI module. See Chapter 12 Serial Communications Interface Module (SCI).
- PTB3–PTB0 share with the ADC module. See Chapter 3 Analog-to-Digital Converter (ADC).

### 7.3.1 Clock Enable Circuit

The clock enable circuit is used to enable the internal clock (ICLK) or external clock (ECLK) and the port logic which is shared with the oscillator pins (OSC1 and OSC2). The clock enable circuit generates an ICG stop (ICGSTOP) signal which stops all clocks (ICLK, ECLK, and the low-frequency base clock, IBASE). ICGSTOP is set and the ICG is disabled in stop mode if the oscillator enable in stop (OSCENINSTOP) bit in the CONFIG (or MOR) register is clear. The ICG clocks will be enabled in stop mode if OSCENINSTOP is high.

The internal clock enable signal (ICGEN) turns on the ICG which generates ICLK. ICGEN is set (active) whenever the ICGON bit is set and the ICGSTOP signal is clear. When ICGEN is clear, ICLK and IBASE are both low.

The external clock enable signal (ECGEN) turns on the external clock generator which generates ECLK. ECGEN is set (active) whenever the ECGON bit is set and the ICGSTOP signal is clear. ECGON cannot be set unless the external clock enable (EXTCLKEN) bit in the CONFIG (or MOR) register is set. When ECGEN is clear, ECLK is low.

The port B6 enable signal (PB6EN) turns on the port B6 logic. Since port B6 is on the same pin as OSC1, this signal is only active (set) when the external clock function is not desired. Therefore, PB6EN is clear when ECGON is set. PB6EN is not gated with ICGSTOP, which means that if the ECGON bit is set, the port B6 logic will remain disabled in stop mode.

The port B7 enable signal (PB7EN) turns on the port B7 logic. Since port B7 is on the same pin as OSC2, this signal is only active (set) when two-pin oscillator function is not desired. Therefore, PB7EN is clear when ECGON and the external crystal enable (EXTXTALEN) bit in the CONFIG (or MOR) register are both set. PB6EN is not gated with ICGSTOP, which means that if ECGON and EXTXTALEN are set, the port B7 logic will remain disabled in stop mode.

### 7.3.2 Internal Clock Generator

The ICG, shown in Figure 7-2, creates a low frequency base clock (IBASE), which operates at a nominal frequency ($f_{NOM}$) of 307.2 kHz $\pm$ 25%, and an internal clock (ICLK) which is an integer multiple of IBASE. This multiple is the ICG multiplier factor (N), which is programmed in the ICG multiplier register (ICGMR). The ICG is turned off and the output clocks (IBASE and ICLK) are held low when the ICG enable signal (ICGEN) is clear.

The ICG contains:

- A digitally controlled oscillator
- A modulo "N" divider
- A frequency comparator, which contains voltage and current references, a frequency to voltage converter, and comparators
- A digital loop filter

near 307.2 kHz. For proper operation, EREF must be at least twice as slow as IBASE and IREF must be at least twice as slow as ECLK.

To guarantee that IREF is slower than ECLK and EREF is slower than IBASE, one of the signals is divided down. Which signal is divided and by how much is determined by the external slow (EXTSLOW) and external crystal enable (EXTXTALEN) bits in the CONFIG (or MOR) register, according to the rules in Table 7-2.

***NOTE***

*Each signal (IBASE and ECLK) is always divided by four. A longer divider is used on either IBASE or ECLK based on the EXTSLOW bit.*

**Table 7-2. Clock Monitor Reference Divider Ratios**

| ICGON | ECGON | ECGS | EXTSLOW | EXTXTALEN | External Frequency | | EREF Divider Ratio | EREF Frequency | ESTBCLK Divider Ratio | ESTBCLK Frequency | IREF Divider Ratio[1] | IREF Frequency |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | x | x | x | x | U | | U | U | U | U | Off | 0 |
| x | 0 | 0 | x | x | 0 | | Off | 0 | Off | 0 | U | U |
| 1 | 1 | 0 | x | 0 | Minimum | 60 Hz | Off | 0 | 16 (ECLK) | 3.75 Hz | 1*4 | 76.8 kHz ± 25% |
| | | | | | Maximum | 32 MHz | | | | 2.0 MHz | | |
| 1 | 1 | 0 | x | 1 | Minimum | 30 kHz | Off | 0 | 4096 (ECLK) | 7.324 kHz | 1*4 | 76.8 kHz ± 25% |
| | | | | | Maximum | 8 MHz | | | | 1.953 kHz | | |
| 1 | 1 | 1 | 0 | 0 | Minimum | 307.2 kHz | 128*4 | 600 Hz | 16 (ECLK) | 19.2 kHz | 1*4 | 76.8 kHz ± 25% |
| | | | | | Maximum | 32 MHz | | 62.5 kHz | | 2.0 MHz | | |
| 1 | 1 | 1 | 0 | 1 | Minimum | 1 MHz | 128*4 | 1.953 kHz | 4096 (ECLK) | 244 Hz | 1*4 | 76.8 kHz ± 25% |
| | | | | | Maximum | 8 MHz | | 15.63 kHz | | 1.953 kHz | | |
| 1 | 1 | 1 | 1 | 0 | Minimum | 60 Hz | 1*4 | 15 Hz | 16 (IBASE)[2] | 19.2 kHz ± 25% | 4096*4 | 18.75 Hz ± 125% |
| | | | | | Maximum | 307.2 kHz | | 76.8 kHz | | | | |
| 1 | 1 | 1 | 1 | 1 | Minimum | 30 kHz | 1*4 | 7.5 kHz | 4096 (IBASE)[2] | 75 Hz ± 25% | 16*4 | 4.8 kHz ± 25% |
| | | | | | Maximum | 100 kHz | | 25.0 kHz | | | | |

1. U = Unaffected; refer to section of table where ICGON or ECGON is set to 1.
2. IBASE is always used as the internal frequency (307.2 kHz).

To conserve size, the long divider (divide by 4096) is also used as an external crystal stabilization divider. The divider is reset when the external clock generator is turned off or in STOP (ECGEN is clear). When the external clock generator is first turned on, the external clock generator stable bit (ECGS) will be clear. This condition automatically selects ECLK as the input to the long divider. The external stabilization clock (ESTBCLK) will be ECLK divided by 16 when EXTXTALEN is low or 4096 when EXTXTALEN is high. This time-out allows the crystal to stabilize. The falling edge of ESTBCLK is used to set ECGS (ECGS will set after a full 16 or 4096 cycles). When ECGS is set, the divider returns to its normal function. ESTBCLK may be generated by either IBASE or ECLK, but any clocking will only reinforce the set condition. If ECGS is cleared because the clock monitor determined that ECLK was inactive, the divider will revert to a stabilization divider. Since this will change the EREF and IREF divide ratios, it is important to turn the clock monitor off (CMON = 0) after inactivity is detected to ensure valid recovery.

### 7.4.1 Switching Clock Sources

Switching from one clock source to another requires both clock sources to be enabled and stable. A simple flow requires:

1. Enable desired clock source
2. Wait for it to become stable
3. Switch clocks
4. Disable previous clock source

The key point to remember in this flow is that the clock source cannot be switched (CS cannot be written) unless the desired clock is on and stable. A short assembly code example of how to employ this flow is shown in Figure 7-8. This code is for illustrative purposes only and does not represent valid syntax for any particular assembler.

```
                        ;Clock Switching Code Example
                        ;This code switches from Internal to External clock
                        ;Clock Monitor and interrupts are not enabled
start   lda     #$13    ;Mask for CS, ECGON, ECGS
                        ; If switching from External to Internal, mask is $0C.
loop    **      **      ;Other code here, such as writing the COP, since ECGS may
                        ; take some time to set
        sta     icgcr   ;Try to set CS, ECGON and clear ICGON. ICGON will not
                        ; clear until CS is set, and CS will not set until
                        ; ECGON and ECGS are set.
        cmpa    icgcr   ;Check to see if ECGS set, then CS set, then ICGON clear
        bne     loop    ;Keep looping until ICGON is clear.
```

**Figure 7-8. Code Example for Switching Clock Sources**

### 7.4.2 Enabling the Clock Monitor

Many applications require the clock monitor to determine if one of the clock sources has become inactive, so the other can be used to recover from a potentially dangerous situation. Using the clock monitor requires both clocks to be active (ECGON and ICGON both set). To enable the clock monitor, both clocks must also be stable (ECGS and ICGS both set). This is to prevent the use of the clock monitor when a clock is first turned on and potentially unstable.

Enabling the clock monitor and clock monitor interrupts requires a flow similar to the one below:

1. Enable the alternate clock source
2. Wait for both clock sources to be stable
3. Switch to the desired clock source if necessary
4. Enable the clock monitor
5. Enable clock monitor interrupts

These events must happen in sequence. A short assembly code example of how to employ this flow is shown in Figure 7-9. This code is for illustrative purposes only and does not represent valid syntax for any particular assembler.

### 7.5.2 Stop Mode

The value of the oscillator enable in stop (OSCENINSTOP) bit in the CONFIG (or MOR) register determines the behavior of the ICG in stop mode. If OSCENINSTOP is low, the ICG is disabled in stop and, upon execution of the STOP instruction, all ICG activity will cease and the output clocks (CGMXCLK, CGMOUT, and TBMCLK) will be held low. Power consumption will be minimal.

If OSCENINSTOP is high, the ICG is enabled in stop and activity will continue. This is useful if the timebase module (TBM) is required to bring the MCU out of stop mode. ICG interrupts will not bring the MCU out of stop mode in this case.

During STOP, if OSCENINSTOP is low, several functions in the ICG are affected. The stable bits (ECGS and ICGS) are cleared, which will enable the external clock stabilization divider upon recovery. The clock monitor is disabled (CMON = 0) which will also clear the clock monitor interrupt enable (CMIE) and clock monitor flag (CMF) bits. The CS, ICGON, ECGON, N, TRIM, DDIV, and DSTG bits are unaffected.

## 7.6 CONFIG (or MOR) Register Options

There are four CONFIG (or MOR) register options that affect the functionality of the ICG. These options are:

- EXTCLKEN (external clock enable)
- EXTXTALEN (external crystal enable)
- EXTSLOW (slow external clock)
- OSCENINSTOP (oscillator enable in stop)

All CONFIG (or MOR) register options will have a default setting.

### 7.6.1 External Clock Enable (EXTCLKEN)

External clock enable (EXTCLKEN), when set, enables the ECGON bit to be set. ECGON turns on the external clock input path through the PTB6/(OSC1) pin. When EXTCLKEN is clear, ECGON cannot be set and PTB6/(OSC1) will always perform the PTB6 function.

The default state for this option is clear.

### 7.6.2 External Crystal Enable (EXTXTALEN)

External crystal enable (EXTXTALEN), when set, will enable an amplifier to drive the PTB7/(OSC2)/$\overline{\text{RST}}$ pin from the PTB6/(OSC1) pin. The amplifier will only drive if the external clock enable (EXTCLKEN) bit and the ECGON bit are also set. If EXTCLKEN or ECGON are clear, PTB7/(OSC2)/$\overline{\text{RST}}$ will perform the PTB7 function. When EXTXTALEN is clear, PTB7/(OSC2)/$\overline{\text{RST}}$ will always perform the PTB7 function.

EXTXTALEN, when set, also configures the clock monitor to expect an external clock source in the valid range of crystals (30 kHz to 100 kHz or 1 MHz to 8 MHz). When EXTXTALEN is clear, the clock monitor will expect an external clock source in the valid range for externally generated clocks when using the clock monitor (60 Hz to 32 MHz).

EXTXTALEN, when set, also configures the external clock stabilization divider in the clock monitor for a 4096 cycle time-out to allow the proper stabilization time for a crystal. When EXTXTALEN is clear, the stabilization divider is configured to 16 cycles since an external clock source does not need a start-up time.

The default state for this option is clear.

| Addr. | Register Name | | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|---|
| $0039 | ICG DCO Divider Control Register (ICGDVR) See page 89. | Read: | | | | | DDIV3 | DDIV2 | DDIV1 | DDIV0 |
| | | Write: | | | | | | | | |
| | | Reset: | 0 | 0 | 0 | 0 | U | U | U | U |
| $003A | ICG DCO Stage Control Register (ICGDSR) See page 89. | Read: | DSTG7 | DSTG6 | DSTG5 | DSTG4 | DSTG3 | DSTG2 | DSTG1 | DSTG0 |
| | | Write: | R | R | R | R | R | R | R | R |
| | | Reset: | U | U | U | U | U | U | U | U |

= Unimplemented R = Reserved U = Unaffected

**Figure 7-10. ICG Module I/O Register Summary (Continued)**

**Table 7-5. ICG Module Register Bit Interaction Summary**

| Condition | Register Bit Results for Given Condition | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | CMIE | CMF | CMON | CS | ICGON | ICGS | ECGON | ECGS | N[6:0] | TRIM[7:0] | DDIV[3:0] | DSTB[7:0] |
| Reset | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | $15 | $80 | — | — |
| OSCENINSTOP = 0, STOP = 1 | 0 | 0 | 0 | — | — | 0 | — | 0 | — | — | — | — |
| EXTCLKEN = 0 | 0 | 0 | 0 | 0 | 1 | — | 0 | 0 | — | — | uw | uw |
| CMF = 1 | — | (1) | 1 | — | 1 | — | 1 | — | uw | uw | uw | uw |
| CMON = 0 | 0 | 0 | (0) | — | — | — | — | — | — | — | — | — |
| CMON = 1 | — | — | (1) | — | 1 | — | 1 | — | uw | uw | uw | uw |
| CS = 0 | — | — | — | (0) | 1 | — | — | — | — | — | uw | uw |
| CS = 1 | — | — | — | (1) | — | — | 1 | — | — | — | — | — |
| ICGON = 0 | 0 | 0 | 0 | 1 | (0) | 0 | 1 | — | — | — | — | — |
| ICGON = 1 | — | — | — | — | (1) | — | — | — | — | — | uw | uw |
| ICGS = 0 | us | — | us | uc | — | (0) | — | — | — | — | — | — |
| ECGON = 0 | 0 | 0 | 0 | 0 | 1 | — | (0) | 0 | — | — | uw | uw |
| ECGS = 0 | us | — | us | us | — | — | — | (0) | — | — | — | — |
| IOFF = 1 | — | 1* | (1) | 1 | (1) | 0 | (1) | — | uw | uw | uw | uw |
| EOFF = 1 | — | 1* | (1) | 0 | (1) | — | (1) | 0 | uw | uw | uw | uw |
| N = written | (0) | (0) | (0) | — | — | 0* | — | — | — | — | — | — |
| TRIM = written | (0) | (0) | (0) | — | — | 0* | — | — | — | — | — | — |

—Register bit is unaffected by the given condition.
0, 1Register bit is forced clear or set (respectively) in the given condition.
0*, 1*Register bit is temporarily forced clear or set (respectively) in the given condition.
(0), (1)Register bit must be clear or set (respectively) for the given condition to occur.
us, uc, uwRegister bit cannot be set, cleared, or written (respectively) in the given condition.

Setting the LVI 5-V or 3-V trip point bit, LVI5OR3, enables the trip point voltage, $V_{TRIPF}$, to be configured for 5-V operation. Clearing the LVI5OR3 bit enables the trip point voltage, $V_{TRIPF}$, to be configured for 3-V operation. The actual trip thresholds are specified in 17.5 5.0-Vdc DC Electrical Characteristics and .

**NOTE**

*After a power-on reset, the LVI's default mode of operation is 3 volts. If a 5-V system is used, the user must set the LVI5OR3 bit to raise the trip point to 5-V operation.*

*If the user requires 5-V mode and sets the LVI5OR3 bit after power-on reset while the $V_{DD}$ supply is not above the $V_{TRIPR}$ for 5-V mode, the MCU will immediately go into reset. The next time the LVI releases the reset, the supply will be above the $V_{TRIPR}$ for 5-V mode.*

Once an LVI reset occurs, the MCU remains in reset until $V_{DD}$ rises above a voltage, $V_{TRIPR}$, which causes the MCU to exit reset. See Chapter 13 System Integration Module (SIM) for the reset recovery sequence.

The output of the comparator controls the state of the LVIOUT flag in the LVI status register (LVISR) and can be used for polling LVI operation when the LVI reset is disabled.

### 10.3.1 Polled LVI Operation

In applications that can operate at $V_{DD}$ levels below the $V_{TRIPF}$ level, software can monitor $V_{DD}$ by polling the LVIOUT bit. In the configuration register, the LVIPWRD bit must be at 0 to enable the LVI module, and the LVIRSTD bit must be at 1 to disable LVI resets.

### 10.3.2 Forced Reset Operation

In applications that require $V_{DD}$ to remain above the $V_{TRIPF}$ level, enabling LVI resets allows the LVI module to reset the MCU when $V_{DD}$ falls below the $V_{TRIPF}$ level. In the configuration register, the LVIPWRD and LVIRSTD bits must be at 0 to enable the LVI module and to enable LVI resets.

### 10.3.3 Voltage Hysteresis Protection

Once the LVI has triggered (by having $V_{DD}$ fall below $V_{TRIPF}$), the LVI will maintain a reset condition until $V_{DD}$ rises above the rising trip point voltage, $V_{TRIPR}$. This prevents a condition in which the MCU is continually entering and exiting reset if $V_{DD}$ is approximately equal to $V_{TRIPF}$. $V_{TRIPR}$ is greater than $V_{TRIPF}$ by the hysteresis voltage, $V_{HYS}$.

### 10.3.4 LVI Trip Selection

The LVI5OR3 bit in the configuration register selects whether the LVI is configured for 5-V or 3-V protection.

**NOTE**

*The microcontroller is guaranteed to operate at a minimum supply voltage. The trip point ($V_{TRIPF}$ [5 V] or $V_{TRIPF}$ [3 V]) may be lower than this. See 17.5 5.0-Vdc DC Electrical Characteristics and  for the actual trip point voltages.*

**TxD — SCI Transmit Data Output Bit**

The PTB0/TxD pin is the transmit data output for the SCI module. When the enable SCI bit, ENSCI, is clear, the SCI module is disabled, and the PTB0/TxD pin is available for general-purpose I/O. See Chapter 12 Serial Communications Interface Module (SCI).

**AD3–AD0 — Analog-to-Digital Input Bits**

AD3–AD0 are pins used for the input channels to the analog-to-digital converter (ADC) module. The channel select bits in the ADC status and control register define which port B pin will be used as an ADC input and overrides any control from the port I/O logic by forcing that pin as the input to the analog circuitry. See Chapter 3 Analog-to-Digital Converter (ADC).

## 11.3.2 Data Direction Register B

Data direction register B (DDRB) determines whether each port B pin is an input or an output. Writing a 1 to a DDRB bit enables the output buffer for the corresponding port B pin; a 0 disables the output buffer.

Address: $0005

| | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|
| Read:<br>Write: | DDRB7 | DDRB6 | DDRB5 | DDRB4 | DDRB3 | DDRB2 | DDRB1 | DDRB0 |
| Reset: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Figure 11-7. Data Direction Register B (DDRB)**

**DDRB7–DDRB0 — Data Direction Register B Bits**

These read/write bits control port B data direction. Reset clears DDRB7–DDRB0, configuring all port B pins as inputs.

1 = Corresponding port B pin configured as output
0 = Corresponding port B pin configured as input

***NOTE***

*Avoid glitches on port B pins by writing to the port B data register before changing data direction register B bits from 0 to 1.*

Figure 11-8 shows the port B I/O logic.

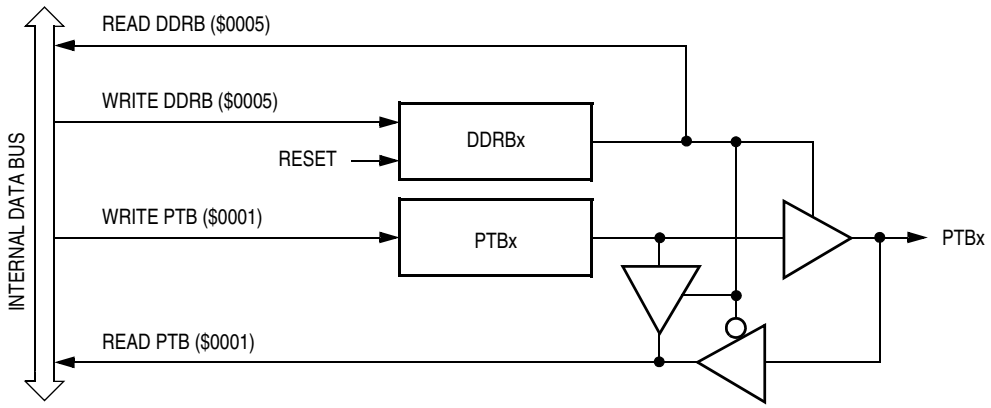



**Figure 11-8. Port B I/O Circuit**

## 12.3 Pin Name Conventions

The generic names of the SCI input/output (I/O) pins are:

- RxD, receive data
- TxD, transmit data

SCI I/O lines are implemented by sharing parallel I/O port pins. The full name of an SCI input or output reflects the name of the shared port pin. Table 12-1 shows the full names and the generic names of the SCI I/O pins.The generic pin names appear in the text of this section.

**Table 12-1. Pin Name Conventions**

| Generic Pin Names | RxD | TxD |
|---|---|---|
| Full Pin Names | PTB4/RxD | PTB5/TxD |

## 12.4 Functional Description

Figure 12-3 shows the structure of the SCI module. The SCI allows full-duplex, asynchronous, NRZ serial communication between the MCU and remote devices, including other MCUs. The transmitter and receiver of the SCI operate independently, although they use the same baud rate generator.

The source of the baud rate clock is determined by the configuration register 2 bit, SCIBDSRC. If SCIBDSRC is set then the source of the SCI is the internal data bus clock. If SCIBDSRC is cleared, the source of the SCI is oscillator output CGMXCLK.

During normal operation, the CPU monitors the status of the SCI, writes the data to be transmitted, and processes received data.

### 12.4.1 Data Format

The SCI uses the standard non-return-to-zero mark/space data format illustrated in Figure 12-2.

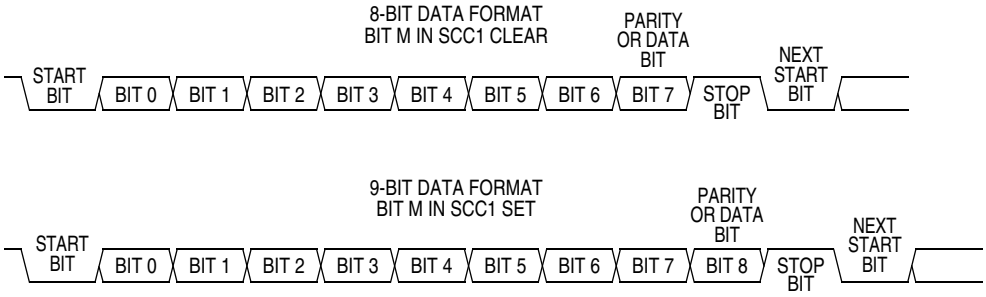



**Figure 12-2. SCI Data Formats**

#### 12.4.3.1 Character Length

The receiver can accommodate either 8-bit or 9-bit data. The state of the M bit in SCI control register 1 (SCC1) determines character length. When receiving 9-bit data, bit R8 in SCI control register 2 (SCC2) is the ninth bit (bit 8). When receiving 8-bit data, bit R8 is a copy of the eighth bit (bit 7).

#### 12.4.3.2 Character Reception

During an SCI reception, the receive shift register shifts characters in from the RxD pin. The SCI data register (SCDR) is the read-only buffer between the internal data bus and the receive shift register.

After a complete character shifts into the receive shift register, the data portion of the character transfers to the SCDR. The SCI receiver full bit, SCRF, in SCI status register 1 (SCS1) becomes set, indicating that the received byte can be read. If the SCI receive interrupt enable bit, SCRIE, in SCC2 is also set, the SCRF bit generates a receiver CPU interrupt request.

#### 12.4.3.3 Data Sampling

The receiver samples the RxD pin at the RT clock rate. The RT clock is an internal signal with a frequency 16 times the baud rate. To adjust for baud rate mismatch, the RT clock is resynchronized at these times (see Figure 12-7):

- After every start bit
- After the receiver detects a data bit change from 1 to 0 (after the majority of data bit samples at RT8, RT9, and RT10 returns a valid 1 and the majority of the next RT8, RT9, and RT10 samples returns a valid 0)

To locate the start bit, data recovery logic does an asynchronous search for a 0 preceded by three 1s. When the falling edge of a possible start bit occurs, the RT clock begins to count to 16.

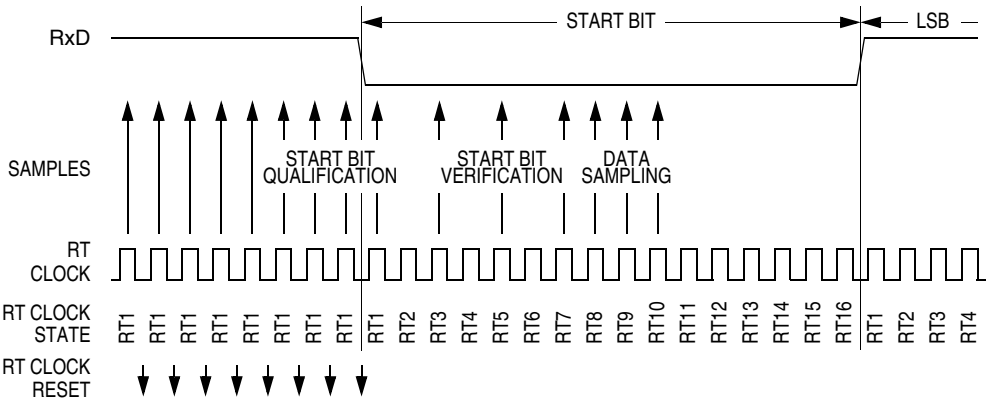



**Figure 12-7. Receiver Data Sampling**

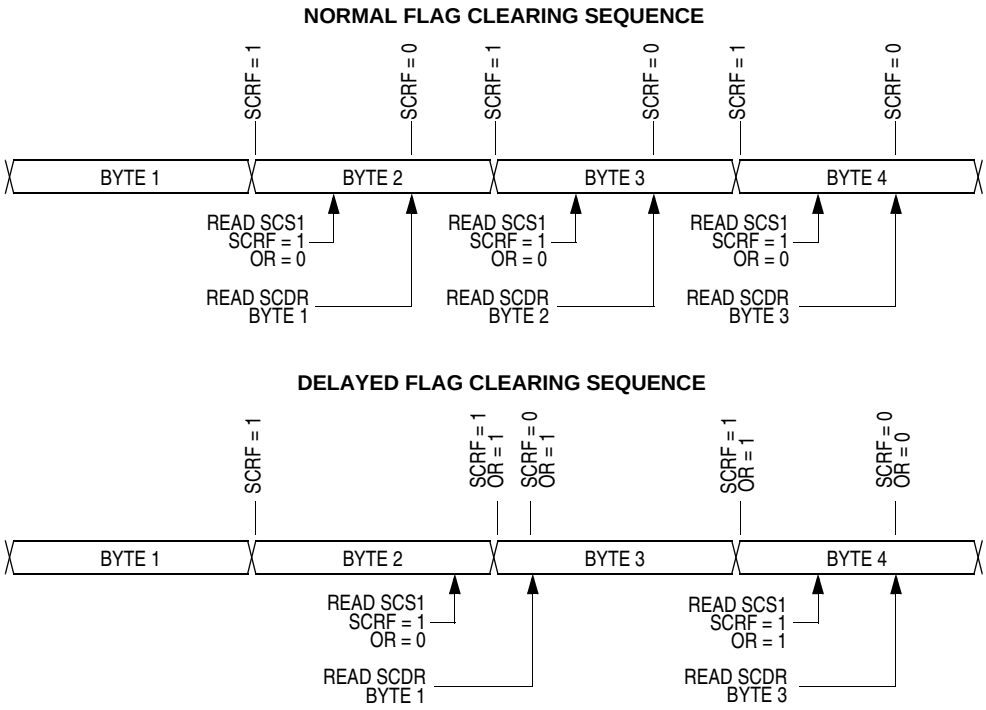



**Figure 12-14. Flag Clearing Sequence**

**PE — Receiver Parity Error Bit**

This clearable, read-only bit is set when the SCI detects a parity error in incoming data. PE generates a PE CPU interrupt request if the PEIE bit in SCC3 is also set. Clear the PE bit by reading SCS1 with PE set and then reading the SCDR. Reset clears the PE bit.

1 = Parity error detected
0 = No parity error detected

### 12.7.5 SCI Status Register 2

SCI status register 2 (SCS2) contains flags to signal these conditions:

- Break character detected
- Incoming data

Address: $0017

| | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|
| Read: | 0 | 0 | 0 | 0 | 0 | 0 | BKF | RPF |
| Write: | | | | | | | | |
| Reset: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

= Unimplemented

**Figure 12-15. SCI Status Register 2 (SCS2)**

**BKF — Break Flag Bit**

This clearable, read-only bit is set when the SCI detects a break character on the RxD pin. In SCS1, the FE and SCRF bits are also set. In 9-bit character transmissions, the R8 bit in SCC3 is cleared. BKF does not generate a CPU interrupt request. Clear BKF by reading SCS2 with BKF set and then reading

*in the event of software error or noise. Toggling on output compare also can cause incorrect PWM signal generation when changing the PWM pulse width to a new, much larger value.*

### 15.4.8 Buffered PWM Signal Generation

Channels 0 and 1 can be linked to form a buffered PWM channel whose output appears on the TCH0 pin. The TIM channel registers of the linked pair alternately control the pulse width of the output.

Setting the MS0B bit in TIM channel 0 status and control register (TSC0) links channel 0 and channel 1. The TIM channel 0 registers initially control the pulse width on the TCH0 pin. Writing to the TIM channel 1 registers enables the TIM channel 1 registers to synchronously control the pulse width at the beginning of the next PWM period. At each subsequent overflow, the TIM channel registers (0 or 1) that control the pulse width are the 1s written to last. TSC0 controls and monitors the buffered PWM function, and TIM channel 1 status and control register (TSC1) is unused. While the MS0B bit is set, the channel 1 pin, TCH1, is available as a general-purpose I/O pin.

***NOTE***

*In buffered PWM signal generation, do not write new pulse width values to the currently active channel registers. User software should track the currently active channel to prevent writing a new value to the active channel. Writing to the active channel registers is the same as generating unbuffered PWM signals.*

### 15.4.9 PWM Initialization

To ensure correct operation when generating unbuffered or buffered PWM signals, use this initialization procedure:

1. In the TIM status and control register (TSC):
   a. Stop the TIM counter by setting the TIM stop bit, TSTOP.
   b. Reset the TIM counter and prescaler by setting the TIM reset bit, TRST.
2. In the TIM counter modulo registers (TMODH and TMODL), write the value for the required PWM period.
3. In the TIM channel x registers (TCHxH and TCHxL), write the value for the required pulse width.
4. In TIM channel x status and control register (TSCx):
   a. Write 0:1 (for unbuffered output compare or PWM signals) or 1:0 (for buffered output compare or PWM signals) to the mode select bits, MSxB and MSxA. See Table 15-2.
   b. Write 1 to the toggle-on-overflow bit, TOVx.
   c. Write 1:0 (to clear output on compare) or 1:1 (to set output on compare) to the edge/level select bits, ELSxB and ELSxA. The output action on compare must force the output to the complement of the pulse width level. See Table 15-2.

***NOTE***

*In PWM signal generation, do not program the PWM channel to toggle on output compare. Toggling on output compare prevents reliable 0 percent duty cycle generation and removes the ability of the channel to self-correct in the event of software error or noise. Toggling on output compare can also cause incorrect PWM signal generation when changing the PWM pulse width to a new, much larger value.*

### CHxF — Channel x Flag Bit

When channel x is an input capture channel, this read/write bit is set when an active edge occurs on the channel x pin. When channel x is an output compare channel, CHxF is set when the value in the TIM counter registers matches the value in the TIM channel x registers.

When TIM CPU interrupt requests are enabled (CHxIE = 1), clear CHxF by reading TIM channel x status and control register with CHxF set and then writing a 0 to CHxF. If another interrupt request occurs before the clearing sequence is complete, then writing 0 to CHxF has no effect. Therefore, an interrupt request cannot be lost due to inadvertent clearing of CHxF.

Reset clears the CHxF bit. Writing a 1 to CHxF has no effect.

1 = Input capture or output compare on channel x
0 = No input capture or output compare on channel x

### CHxIE — Channel x Interrupt Enable Bit

This read/write bit enables TIM CPU interrupts on channel x. Reset clears the CHxIE bit.

1 = Channel x CPU interrupt requests
0 = Channel x CPU interrupt requests disabled

### MS0B — Mode Select Bit B

This read/write bit selects buffered output compare/PWM operation. MS0B exists only in the TIM channel 0 status and control register.

Setting MS0B disables the channel 1 status and control register and reverts TCH1 to general-purpose I/O. Reset clears the MSxB bit.

1 = Buffered output compare/PWM operation enabled
0 = Buffered output compare/PWM operation disabled

### MSxA — Mode Select Bit A

When ELSxB:A ≠ 00, this read/write bit selects either input capture operation or unbuffered output compare/PWM operation. See Table 15-3.

1 = Unbuffered output compare/PWM operation
0 = Input capture operation

When ELSxB:A = 00, this read/write bit selects the initial output level of the TCHx pin. See Table 15-3. Reset clears the MSxA bit.

1 = Initial output level low
0 = Initial output level high

***NOTE***

*Before changing a channel function by writing to the MS0B or MSxA bit, set the TSTOP and TRST bits in the TIM status and control register (TSC).*

### ELSxB and ELSxA — Edge/Level Select Bits

When channel x is an input capture channel, these read/write bits control the active edge-sensing logic on channel x.

When channel x is an output compare channel, ELSxB and ELSxA control the channel x output behavior when an output compare occurs.

When ELSxB and ELSxA are both clear, channel x is not connected to port A, and pin PTAx/TCHx is available as a general-purpose I/O pin. Table 15-3 shows how ELSxB and ELSxA work. Reset clears the ELSxB and ELSxA bits.

#### 16.2.1.3 TIM1 and TIM2 During Break Interrupts

A break interrupt stops the timer counters.

#### 16.2.1.4 COP During Break Interrupts

The COP is disabled during a break interrupt when BDCOP bit is set in break auxiliary register (BRKAR).

### 16.2.2 Break Module Registers

These registers control and monitor operation of the break module:

- Break status and control register (BRKSCR)
- Break address register high (BRKH)
- Break address register low (BRKL)
- SIM break status register (SBSR)
- SIM break flag control register (SBFCR)

#### 16.2.2.1 Break Status and Control Register

The break status and control register (BRKSCR) contains break module enable and status bits.

Address: $FE0B

| | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|
| Read: | BRKE | BRKA | 0 | 0 | 0 | 0 | 0 | 0 |
| Write: | | | | | | | | |
| Reset: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

= Unimplemented

**Figure 16-3. Break Status and Control Register (BRKSCR)**

**BRKE — Break Enable Bit**

This read/write bit enables breaks on break address register matches. Clear BRKE by writing a 0 to bit 7. Reset clears the BRKE bit.

1 = Breaks enabled on 16-bit address match
0 = Breaks disabled on 16-bit address match

**BRKA — Break Active Bit**

This read/write status and control bit is set when a break address match occurs. Writing a 1 to BRKA generates a break interrupt. Clear BRKA by writing a 0 to it before exiting the break routine. Reset clears the BRKA bit.

1 = When read, break address match
0 = When read, no break address match

A brief description of each monitor mode command is given in Table 16-4 through Table 16-9.

**Table 16-4. READ (Read Memory) Command**

| | |
|---|---|
| **Description** | Read byte from memory |
| **Operand** | 2-byte address in high-byte:low-byte order |
| **Data Returned** | Returns contents of specified address |
| **Opcode** | $4A |

**Command Sequence**

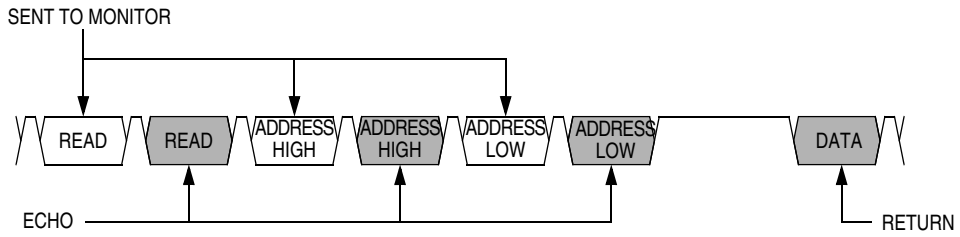



**Table 16-5. WRITE (Write Memory) Command**

| | |
|---|---|
| **Description** | Write byte to memory |
| **Operand** | 2-byte address in high-byte:low-byte order; low byte followed by data byte |
| **Data Returned** | None |
| **Opcode** | $49 |

**Command Sequence**

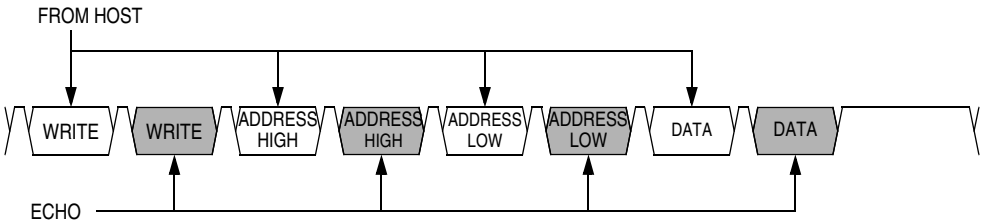
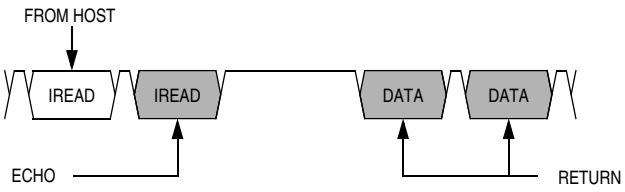



**Table 16-6. IREAD (Indexed Read) Command**

| | |
|---|---|
| **Description** | Read next 2 bytes in memory from last address accessed |
| **Operand** | 2-byte address in high byte:low byte order |
| **Data Returned** | Returns contents of next two addresses |
| **Opcode** | $1A |

**Command Sequence**



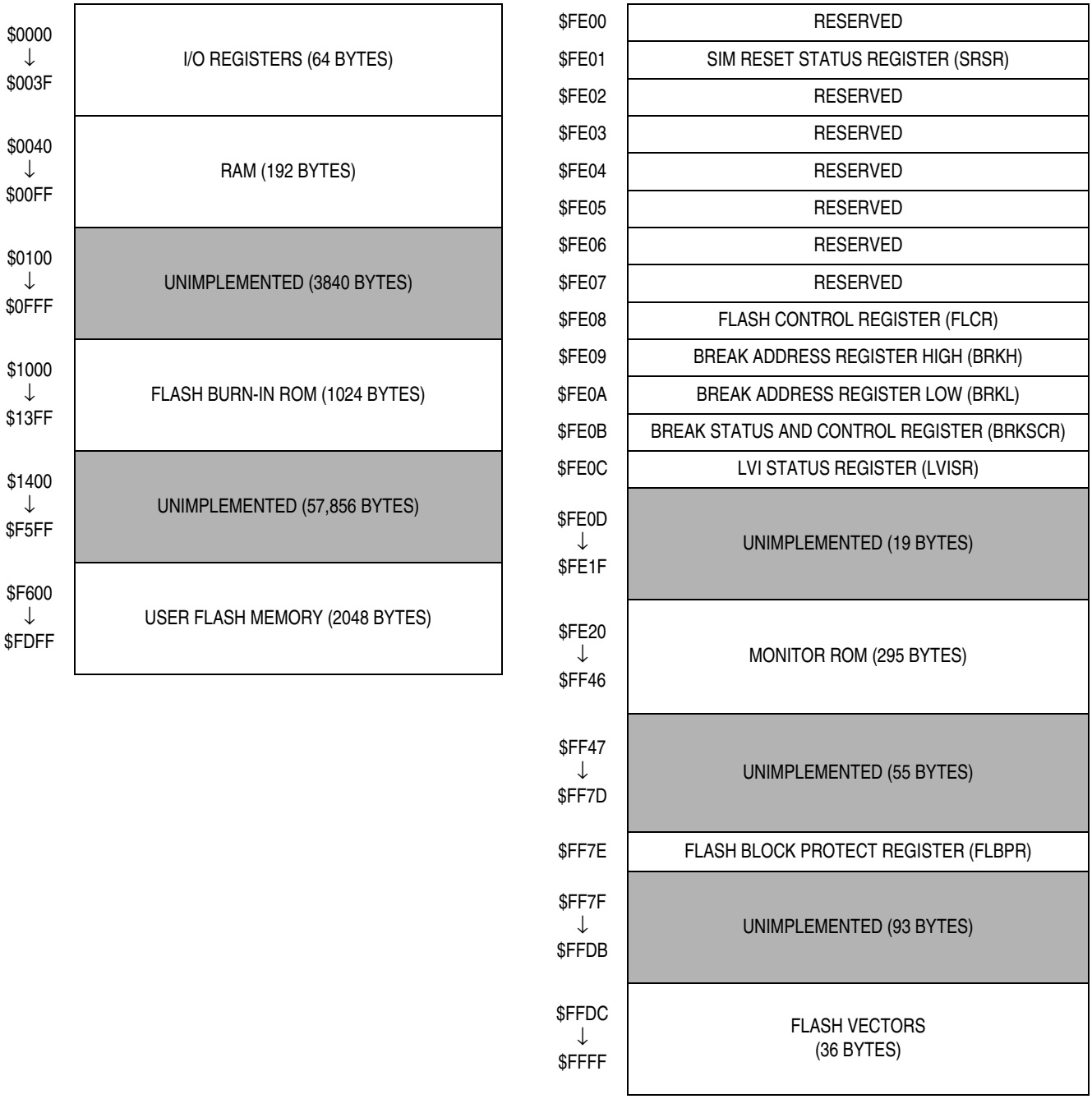



**Figure A-1. MC68HC908KX2 Memory Map**

## B.4.8 Trimmed Accuracy of the Internal Clock Generator

The unadjusted frequency of the low-frequency base clock (IBASE), when the comparators in the frequency comparator indicate zero error, can vary as much as ±25% due to process, temperature, and voltage. The trimming capability exists to compensate for process affects. The remaining variation in frequency is due to temperature, voltage, and change in target frequency (multiply register setting). These affects are designed to be minimal, however variation does occur. Better performance is seen at 3 V and lower settings of N.

### *B.4.8.1 2.7-Volt to 3.3-Volt Trimmed Internal Clock Generator Characteristics*

| Characteristic[1] | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Absolute trimmed internal oscillator tolerance[2], [3]<br>–40°C to 85°C | $F_{abs\_tol}$ | — | 1.5 | 5.0 | % |
| Variation over temperature[3], [4] | $V_{ar\_temp}$ | — | 0.03 | 0.05 | %/C |
| Variation over voltage[3], [5]<br>25°C<br>–40°C to 85°C | $V_{ar\_volt}$ | —<br>— | 0.5<br>0.7 | 2.0<br>2.0 | %/V |

1. These specifications concern long-term frequency variation. Each measurement is taken over a 1-ms period.
2. Absolute value of variation in ICG output frequency, trimmed at nominal $V_{DD}$ and temperature, as temperature and $V_{DD}$ are allowed to vary for a single given setting of N.
3. Specification is characterized but not tested.
4. Variation in ICG output frequency for a fixed N and voltage
5. Variation in ICG output frequency for a fixed N

### *B.4.8.2 4.5-Volt to 5.5-Volt Trimmed Internal Clock Generator Characteristics*

| Characteristic[1] | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Absolute trimmed internal oscillator tolerance[2], [3]<br>–40°C to 85°C | $F_{abs\_tol}$ | — | 4.0 | 7.0 | % |
| Variation over temperature[3], [4] | $V_{ar\_temp}$ | — | 0.05 | 0.08 | %/C |
| Variation over voltage[3], [5]<br>25°C<br>–40°C to 85°C | $V_{ar\_volt}$ | —<br>— | 1.0<br>1.0 | 2.0<br>2.0 | %/V |

1. These specifications concern long-term frequency variation. Each measurement is taken over a 1-ms period.
2. Absolute value of variation in ICG output frequency, trimmed at nominal $V_{DD}$ and temperature, as temperature and $V_{DD}$ are allowed to vary for a single given setting of N.
3. Specification is characterized but not tested.
4. Variation in ICG output frequency for a fixed N and voltage
5. Variation in ICG output frequency for a fixed N