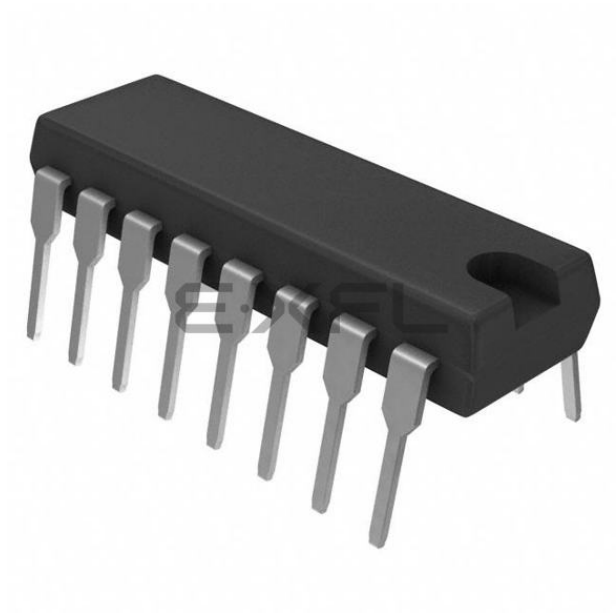

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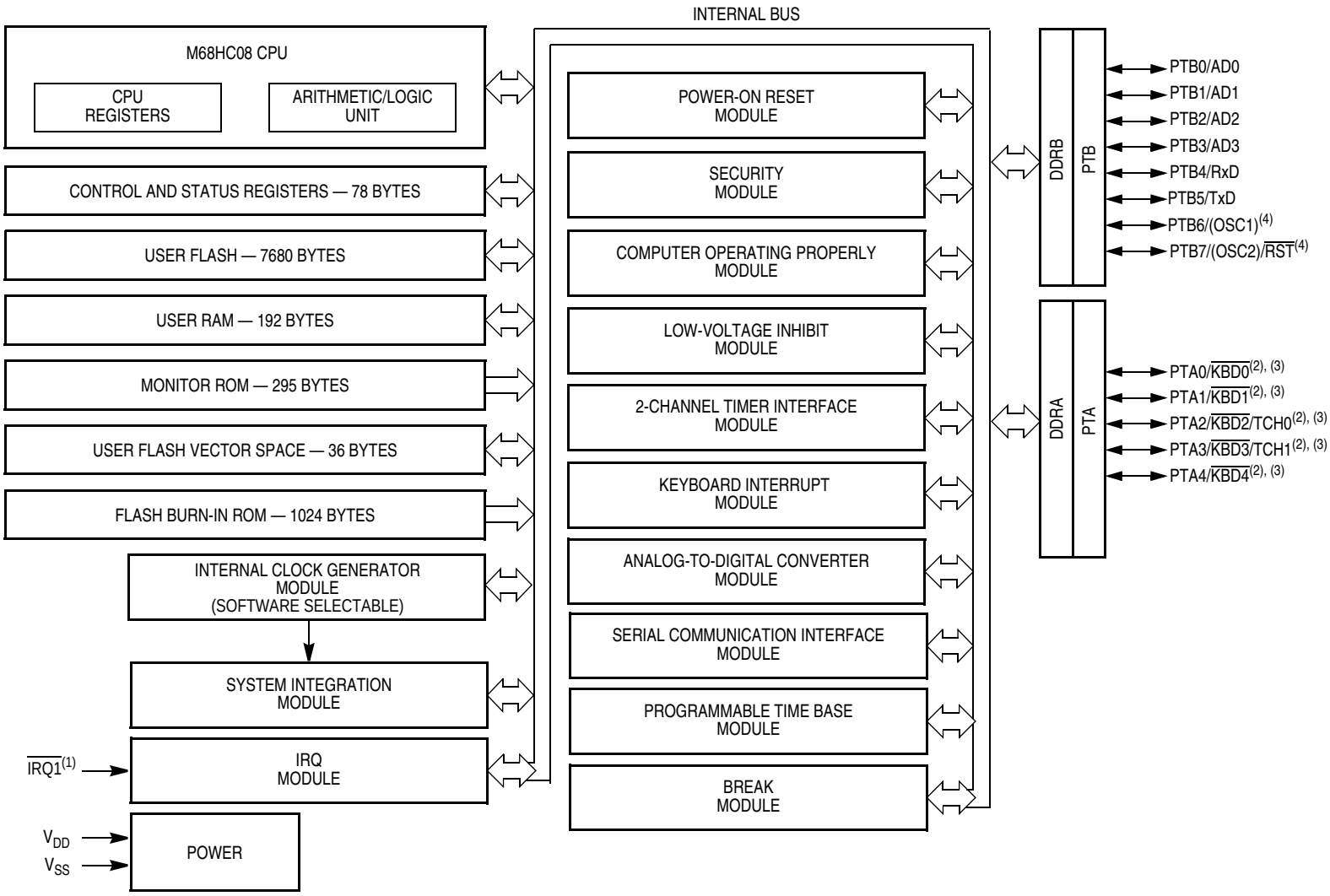
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	HC08
Core Size	8-Bit
Speed	8MHz
Connectivity	SCI
Peripherals	LVD, POR, PWM
Number of I/O	13
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	192 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 4x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Through Hole
Package / Case	16-DIP (0.300", 7.62mm)
Supplier Device Package	16-PDIP
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc908kx8mpe



Notes:
1. Pin contains integrated pullup resistor
2. High-current source/sink pin
3. Pin contains software selectable pullup resistor if general function I/O pin is configured as input.

Figure 1-1. MC68HC908KX8 MCU Block Diagram

Chapter 2
Memory

2.1 Introduction

The central processor unit (CPU08) can address 64 Kbytes of memory space.

The memory map, shown in Figure 2-1, includes:

- 7680 bytes of FLASH memory
- 192 bytes of random-access memory (RAM)
- 36 bytes of user-defined vectors
- 295 bytes of monitor read-only memory (ROM)

2.2 I/O Registers

Most of the control, status, and data registers are in the zero-page area of $0000–$003F. Additional input/output (I/O) registers have the following addresses:

- $FE01 — SIM reset status register, SRSR
- $FE04 — Interrupt status register 1, INT1
- $FE05 — Interrupt status register 2, INT2
- $FE06 — Interrupt status register 3, INT3
- $FE08 — FLASH control register, FLCR
- $FE09 — Break address register high, BRKH
- $FE0A — Break address register low, BRKL
- $FE0B — Break status and control register, BRKSCR
- $FE0C — LVI status register, LVISR
- $FF7E — FLASH block protect register, FLBPR
  in non-volatile FLASH memory
- $FFFF — COP control register, COPCTL

A summary of the available registers is provided in Figure 2-2. Table 2-1 is a list of vector locations.

2.3 Monitor ROM

The 295 bytes at addresses $FE20–$FF46 are reserved ROM addresses that contain the instructions for the monitor functions.

2.8 FLASH Mass Erase Operation

Use the following procedure to erase the entire FLASH memory to read as a 1:

1. Set both the ERASE bit and the MASS bit in the FLASH control register.
2. Read the FLASH block protect register.
3. Write any data to any FLASH address[1] within the FLASH memory address range.
4. Wait for a time, t_{NVS} (minimum 10 µs).
5. Set the HVEN bit.
6. Wait for a time, t_{MErase} (minimum 4 ms).
7. Clear the ERASE and MASS bits.

NOTE

Mass erase is disabled whenever any block is protected (FLBPR does not equal $FF).

8. Wait for a time, t_{NVHL} (minimum 100 µs).
9. Clear the HVEN bit.
10. After time, t_{RCV} (typical 1 µs), the memory can be accessed in read mode again.

NOTE

Programming and erasing of FLASH locations cannot be performed by code being executed from the FLASH memory. While these operations must be performed in the order shown, other unrelated operations may occur between the steps.

1. When in monitor mode, with security sequence failed (see 16.3.2 Security), write to the FLASH block protect register instead of any FLASH address.

Chapter 3
Analog-to-Digital Converter (ADC)

3.1 Introduction

This section describes the 8-bit analog-to-digital converter (ADC).

3.2 Features

Features of the ADC module include:

- Four channels with multiplexed input
- Linear successive approximation
- 8-bit resolution
- Single or continuous conversion
- Conversion complete flag or conversion complete interrupt
- Selectable ADC clock

3.3 Functional Description

The ADC provides four pins for sampling external sources at pins PTB3–PTB0. An analog multiplexer allows the single ADC converter to select one of four ADC channels as ADC voltage in (ADCVIN). ADCVIN is converted by the successive approximation register-based counters. When the conversion is completed, ADC places the result in the ADC data register and sets a flag or generates an interrupt. See Figure 3-2.

The MC68HC908KX8 uses V_{DD} as the high voltage reference.

3.3.1 ADC Port I/O Pins

PTB3–PTB0 are general-purpose input/output (I/O) pins that are shared with the ADC channels.

The channel select bits define which ADC channel/port pin will be used as the input signal. The ADC overrides the port I/O logic by forcing that pin as input to the ADC. The remaining ADC channels/port pins are controlled by the port I/O logic and can be used as general-purpose I/O. Writes to the port register or DDR will not have any effect on the port pin that is selected by the ADC. Read of a port pin which is in use by the ADC will return a logic 0 if the corresponding DDR bit is at 0. If the DDR bit is at 1, the value in the port data latch is read.

Refer to 17.9 Trimmed Accuracy of the Internal Clock Generator.

$$\text{Conversion time} = \frac{\text{16 to 17 ADC clock cycles}}{\text{ADC clock frequency}}$$

Number of bus cycles = conversion time x bus frequency

3.3.4 Continuous Conversion

In continuous conversion mode, the ADC data register will be filled with new data after each conversion. Data from the previous conversion will be overwritten whether that data has been read or not. Conversions will continue until the ADCO bit (ADC status control register, $003C) is cleared. The COCO bit is set after the first conversion and will stay set until the next write of the ADC status and control register or the next read of the ADC data register.

3.3.5 Accuracy and Precision

The conversion process is monotonic and has no missing codes. See 17.9 Trimmed Accuracy of the Internal Clock Generator for accuracy information.

3.4 Interrupts

When the AIEN bit is set, the ADC module is capable of generating a CPU interrupt after each ADC conversion. A CPU interrupt is generated if the COCO bit (ADC status control register, $003C) is at 0. If the COCO bit is set, a direct-memory access (DMA) interrupt is generated.

NOTE

Because the MC68HC908KX8 *does not have a DMA module, the COCO bit should not be set while interrupts are enabled (AIEN = 1).*

The COCO bit is not used as a conversion complete flag when interrupts are enabled.

3.5 Low-Power Modes

The following subsections describe the low-power modes.

3.5.1 Wait Mode

The ADC continues normal operation during wait mode. Any enabled CPU interrupt request from the ADC can bring the MCU out of wait mode. If the ADC is not required to bring the MCU out of wait mode, power down the ADC by setting the ADCH[4:0] bits in the ADC status and control register before executing the WAIT instruction.

3.5.2 Stop Mode

The ADC module is inactive after the execution of a STOP instruction. Any pending conversion is aborted. ADC conversions resume when the MCU exits stop mode. Allow one conversion cycle to stabilize the analog circuitry before attempting a new ADC conversion after exiting stop mode.

The ADC requires a clock rate of approximately 1 MHz for correct operation. If the selected clock source is not fast enough, the ADC will generate incorrect conversions. See 17.9 Trimmed Accuracy of the Internal Clock Generator.

$$f_{ADIC} = \frac{f_{CGMXCLK} \text{ or bus frequency}}{ADIV[2:0]} \cong 1 \text{ MHz}$$

NOTE

During the conversion process, changing the ADC clock will result in an incorrect conversion.

5.4.6 Reset Vector Fetch

A reset vector fetch occurs when the vector address appears on the data bus. A reset vector fetch clears the COP prescaler.

5.4.7 COPD (COP Disable)

The COPD signal reflects the state of the COP disable bit (COPD) in the configuration register. See Chapter 4 Configuration Register (CONFIG).

5.4.8 COPRS (COP Rate Select)

The COPRS signal reflects the state of the COP rate select bit (COPRS) in the configuration register. See Chapter 4 Configuration Register (CONFIG).

5.5 COP Control Register

The COP control register (COPCTL) is located at address $FFFF and overlaps the reset vector. Writing any value to $FFFF clears the COP counter and stages 12–5 of the COP prescaler and starts a new timeout period. Reading location $FFFF returns the low byte of the reset vector.

Address: $FFFF

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	Low byte of reset vector							
Write:	Clear COP counter							
Reset:	Unaffected by reset							

Figure 5-2. COP Control Register (COPCTL)

5.6 Interrupts

The COP does not generate CPU interrupt requests.

5.7 Monitor Mode

The COP is disabled in monitor mode when V_{TST} is present on the $\overline{IRQ1}$ pin.

5.8 Low-Power Modes

The WAIT and STOP instructions put the MCU in low power-consumption standby modes.

5.8.1 Wait Mode

The COP remains active in wait mode. To prevent a COP reset during wait mode, periodically clear the COP counter in a CPU interrupt routine.

Chapter 7
Internal Clock Generator Module (ICG)

7.1 Introduction

The internal clock generator module (ICG) is used to create a stable clock source for the microcontroller without using any external components. The ICG generates the oscillator output clock (CGMXCLK), which is used by the computer operating properly (COP), low-voltage inhibit (LVI), and other modules. The ICG also generates the clock generator output (CGMOUT), which is fed to the system integration module (SIM) to create the bus clocks. The bus frequency will be one-fourth the frequency of CGMXCLK and one-half the frequency of CGMOUT. Finally, the ICG generates the timebase clock (TBMCLK), which is used in the timebase module (TBM).

7.2 Features

Features of the ICG include:

- Selectable external clock generator, either one pin external source or two pin crystal, multiplexed with port pins
- Internal clock generator with programmable frequency output in integer multiples of a nominal frequency (307.2 kHz ± 25%)
- Frequency adjust (trim) register to improve variability to ± 2%
- Bus clock software selectable from either internal or external clock (bus frequency range from 76.8 kHz ± 25% to 9.75 MHz ± 25% in 76.8 kHz increments — note that for the MC68HC908KX8, MC68HC908KX2, and MC68HC08KX8, do not exceed the maximum bus frequency of 8 MHz at 5.0 V and 4 MHz at 3.0 V
- Timebase clock automatically selected externally, if external clock is available
- Clock monitor for both internal and external clocks

7.3 Functional Description

As shown in Figure 7-1, the ICG contains these major submodules:

- Clock enable circuit
- Internal clock generator
- External clock generator
- Clock monitor circuit
- Clock selection circuit

7.4.1 Switching Clock Sources

Switching from one clock source to another requires both clock sources to be enabled and stable. A simple flow requires:

1. Enable desired clock source
2. Wait for it to become stable
3. Switch clocks
4. Disable previous clock source

The key point to remember in this flow is that the clock source cannot be switched (CS cannot be written) unless the desired clock is on and stable. A short assembly code example of how to employ this flow is shown in Figure 7-8. This code is for illustrative purposes only and does not represent valid syntax for any particular assembler.

```
                        ;Clock Switching Code Example
                        ;This code switches from Internal to External clock
                        ;Clock Monitor and interrupts are not enabled
start   lda     #$13    ;Mask for CS, ECGON, ECGS
                        ; If switching from External to Internal, mask is $0C.
loop    **      **      ;Other code here, such as writing the COP, since ECGS may
                        ; take some time to set
        sta     icgcr   ;Try to set CS, ECGON and clear ICGON. ICGON will not
                        ; clear until CS is set, and CS will not set until
                        ; ECGON and ECGS are set.
        cmpa    icgcr   ;Check to see if ECGS set, then CS set, then ICGON clear
        bne     loop    ;Keep looping until ICGON is clear.
```

Figure 7-8. Code Example for Switching Clock Sources

7.4.2 Enabling the Clock Monitor

Many applications require the clock monitor to determine if one of the clock sources has become inactive, so the other can be used to recover from a potentially dangerous situation. Using the clock monitor requires both clocks to be active (ECGON and ICGON both set). To enable the clock monitor, both clocks must also be stable (ECGS and ICGS both set). This is to prevent the use of the clock monitor when a clock is first turned on and potentially unstable.

Enabling the clock monitor and clock monitor interrupts requires a flow similar to the one below:

1. Enable the alternate clock source
2. Wait for both clock sources to be stable
3. Switch to the desired clock source if necessary
4. Enable the clock monitor
5. Enable clock monitor interrupts

These events must happen in sequence. A short assembly code example of how to employ this flow is shown in Figure 7-9. This code is for illustrative purposes only and does not represent valid syntax for any particular assembler.

```
                                ;Clock Monitor Enabling Code Example
                                ;This code turns on both clocks, selects the desired
                                ; one, then turns on the Clock Monitor and Interrupts
start   lda     #$AF            ;Mask for CMIE, CMON, ICGON, ICGS, ECGON, ECGS
                                ; If Internal Clock desired, mask is $AF
                                ; If External Clock desired, mask is $BF
                                ; If interrupts not desired mask is $2F int; $3F ext
loop    **      **              ;Other code here, such as writing the COP, since ECGS
                                ; and ICGS may take some time to set.
        sta     icgcr           ;Try to set CMIE. CMIE wont set until CMON set; CMON
                                ; won't set until ICGON, ICGS, ECGON, ECGS set.
        brset   6,ICGCR,error   ;Verify CMF is not set
        cmpa    icgcr           ;Check if ECGS set, then CMON set, then CMIE set
        bne     loop            ;Keep looping until CMIE is set.
```

Figure 7-9. Code Example for Enabling the Clock Monitor

7.4.3 Using Clock Monitor Interrupts

The clock monitor circuit can be used to recover from perilous situations such as crystal loss. To use the clock monitor effectively, the following notes should be observed:

- Enable the clock monitor and clock monitor interrupts.
- The first statement in the clock monitor interrupt service routine (CMISR) should be a read to the ICG control register (ICGCR) to verify the clock monitor flag (CMF) is set. This is also the first step in clearing the CMF bit.
- The second statement in the CMISR should be a write to the ICGCR to clear the CMF bit (write the bit low). Writing the bit high will not affect it. This statement does not need to immediately follow the first, but must be contained in the CMISR.
- The third statement in the CMISR should be to clear the CMON bit. This is required to ensure proper reconfiguration of the reference dividers. This statement must also be contained in the CMISR.
- Although the clock monitor can only be enabled when both clocks are stable (ICGS is set or ECGS is set), it will remain set if one of the clocks goes unstable.
- The clock monitor only works if the external slow (EXTSLOW) bit in the CONFIG (or MOR) register is set to the correct value.
- The internal and external clocks must both be enabled and running in order to use the clock monitor.
- When the clock monitor detects inactivity, the inactive clock is automatically deselected and the active clock selected as the source for CGMXCLK and TBMCLK. The CMISR can use the state of the CS bit to check which clock is inactive.
- When the clock monitor detects inactivity, the application may have been subjected to extreme conditions which may have affected other circuits. The CMISR should take any appropriate precautions.

10.4 LVI Status Register

The LVI status register (LVISR) indicates if the V_{DD} voltage was detected below the V_{TRIPF} level while LVI resets have been disabled.

Address: $FE0C

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	LVIOUT	0	0	0	0	0	0	R
Write:								
Reset:	0	0	0	0	0	0	0	0

= Unimplemented R = Reserved

Figure 10-2. LVI Status Register (LVISR)

LVIOUT — LVI Output Bit

This read-only flag becomes set when the V_{DD} voltage falls below the V_{TRIPF} trip voltage and is cleared when V_{DD} voltage rises above V_{TRIPR}. The difference in these threshold levels results in a hysteresis that prevents oscillation into and out of reset. (See Table 10-1.) Reset clears the LVIOUT bit.

Table 10-1. LVIOUT Bit Indication

V_{DD}	LVIOUT
$V_{DD} > V_{TRIPR}$	0
$V_{DD} < V_{TRIPF}$	1
$V_{TRIPF} < V_{DD} < V_{TRIPR}$	Previous value

10.5 LVI Interrupts

The LVI module does not generate interrupt requests.

10.6 Low-Power Modes

The STOP and WAIT instructions put the MCU in low power-consumption standby modes.

10.6.1 Wait Mode

If enabled, the LVI module remains active in wait mode. If enabled to generate resets, the LVI module can generate a reset and bring the MCU out of wait mode.

10.6.2 Stop Mode

When the LVIPWRD bit in the configuration register is cleared and the LVISTOP bit in the configuration register is set, the LVI module remains active in stop mode. If enabled to generate resets, the LVI module can generate a reset and bring the MCU out of stop mode.

12.4.3 Receiver

Figure 12-6 shows the structure of the SCI receiver.

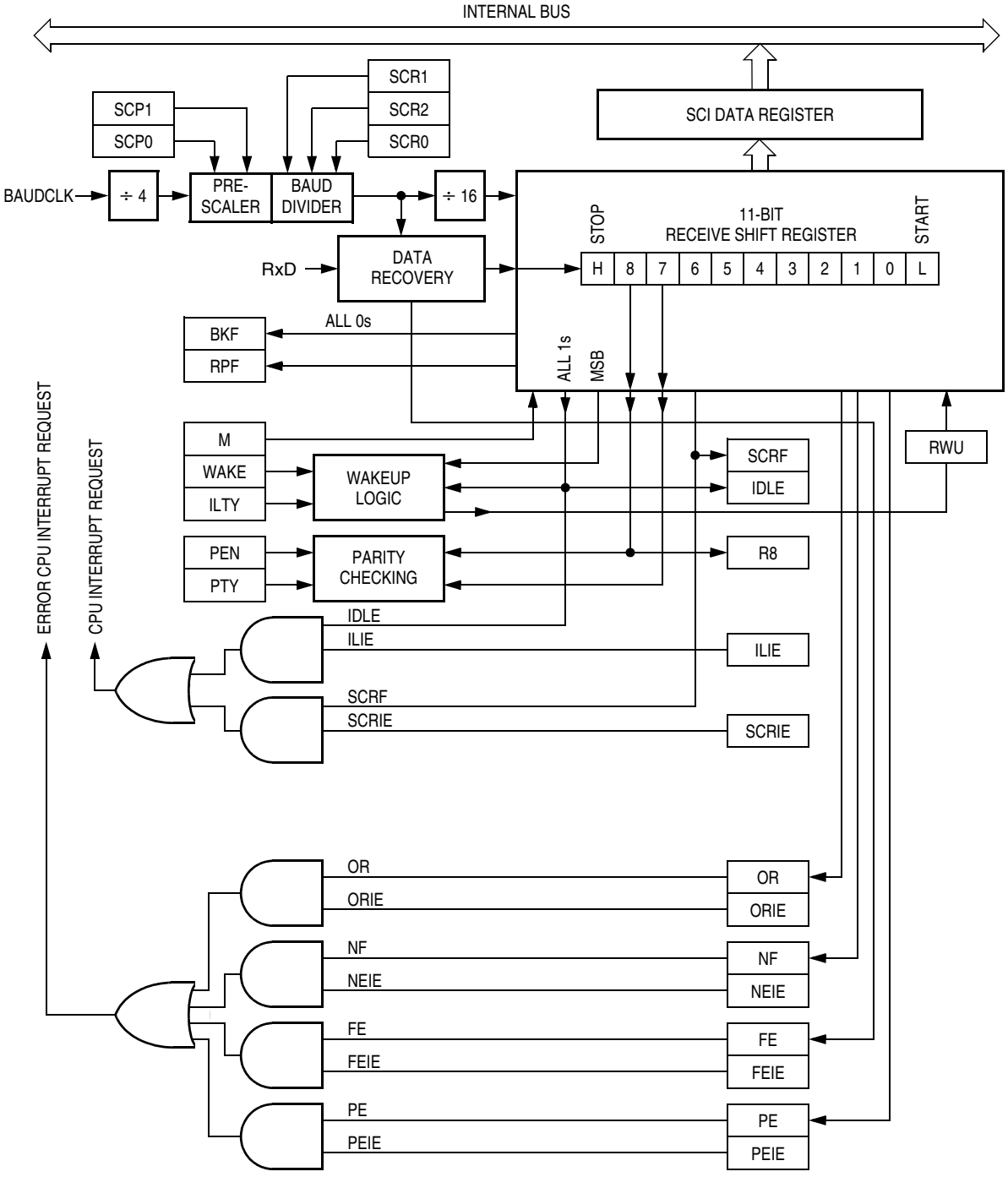


Figure 12-6. SCI Receiver Block Diagram

To verify the start bit and to detect noise, data recovery logic takes samples at RT3, RT5, and RT7.

Table 12-2 summarizes the results of the start bit verification samples.

Table 12-2. Start Bit Verification

RT3, RT5, and RT7 Samples	Start Bit Verification	Noise Flag
000	Yes	0
001	Yes	1
010	Yes	1
011	No	0
100	Yes	1
101	No	0
110	No	0
111	No	0

If start bit verification is not successful, the RT clock is reset and a new search for a start bit begins.

To determine the value of a data bit and to detect noise, recovery logic takes samples at RT8, RT9, and RT10. Table 12-3 summarizes the results of the data bit samples.

Table 12-3. Data Bit Recovery

RT8, RT9, and RT10 Samples	Data Bit Determination	Noise Flag
000	0	0
001	0	1
010	0	1
011	1	1
100	0	1
101	1	1
110	1	1
111	1	0

NOTE

The RT8, RT9, and RT10 samples do not affect start bit verification. If any or all of the RT8, RT9, and RT10 start bit samples are 1s following a successful start bit verification, the noise flag (NF) is set and the receiver assumes that the bit is a start bit.

15.8 I/O Registers

These I/O registers control and monitor operation of the TIM:

- TIM status and control register (TSC)
- TIM control registers (TCNTH and TCNTL)
- TIM counter modulo registers (TMODH and TMODL)
- TIM channel status and control registers (TSC0 and TSC1)
- TIM channel registers (TCH0H and TCH0L, TCH1H and TCH1L)

15.8.1 TIM Status and Control Register

The TIM status and control register (TSC):

- Enables TIM overflow interrupts
- Flags TIM overflows
- Stops the TIM counter
- Resets the TIM counter
- Prescales the TIM counter clock

Address: $0020

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	TOF	TOIE	TSTOP	0	0	PS2	PS1	PS0
Write:	0			TRST				
Reset:	0	0	1	0	0	0	0	0

= Unimplemented

Figure 15-5. TIM Status and Control Register (TSC)

TOF — TIM Overflow Flag Bit

This read/write flag is set when the TIM counter reaches the modulo value programmed in the TIM counter modulo registers. Clear TOF by reading the TIM status and control register when TOF is set and then writing a 0 to TOF. If another TIM overflow occurs before the clearing sequence is complete, then writing 0 to TOF has no effect. Therefore, a TOF interrupt request cannot be lost due to inadvertent clearing of TOF. Reset clears the TOF bit. Writing a 1 to TOF has no effect.

1 = TIM counter has reached modulo value.
0 = TIM counter has not reached modulo value.

TOIE — TIM Overflow Interrupt Enable Bit

This read/write bit enables TIM overflow interrupts when the TOF bit becomes set. Reset clears the TOIE bit.

1 = TIM overflow interrupts enabled
0 = TIM overflow interrupts disabled

TSTOP — TIM Stop Bit

This read/write bit stops the TIM counter. Counting resumes when TSTOP is cleared. Reset sets the TSTOP bit, stopping the TIM counter until software clears the TSTOP bit.

1 = TIM counter stopped
0 = TIM counter active

NOTE

Do not set the TSTOP bit before entering wait mode if the TIM is required to exit wait mode.

The MCU executes the SWI and PSHH instructions when it enters monitor mode. The RUN command tells the MCU to execute the PULH and RTI instructions. Before sending the RUN command, the host can modify the stacked CPU registers to prepare to run the host program. The READSP command returns the incremented stack pointer value, SP + 1. The high and low bytes of the program counter are at addresses SP + 5 and SP + 6.

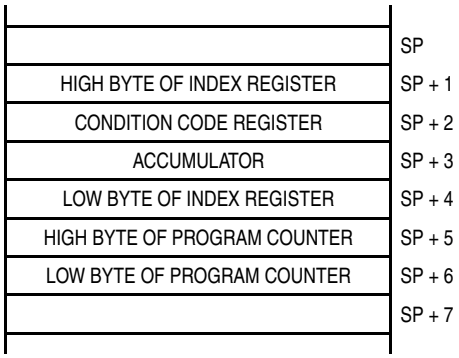


Figure 16-14. Stack Pointer at Monitor Mode Entry

16.3.2 Security

A security feature discourages unauthorized reading of FLASH locations while in monitor mode. The host can bypass the security feature at monitor mode entry by sending eight security bytes that match the bytes at locations $FFF6–$FFFD. Locations $FFF6–$FFFD contain user-defined data.

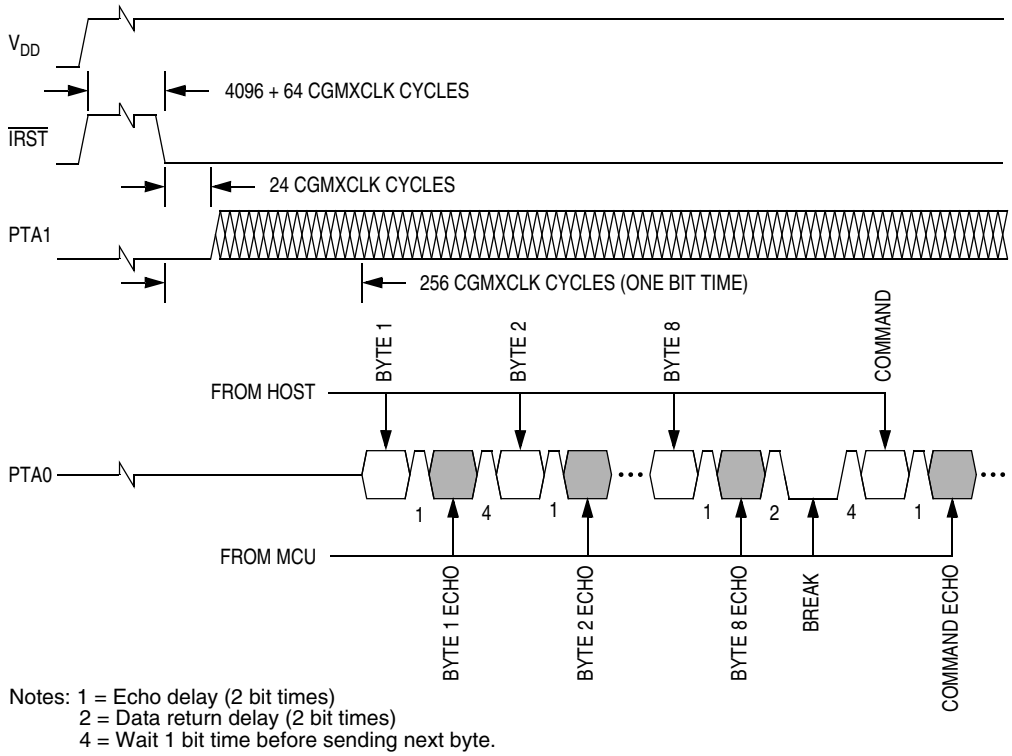
NOTE

Do not leave locations $FFF6–$FFFD blank. For security reasons, program locations $FFF6–$FFFD even if they are not used for vectors. If FLASH is erased, the eight security byte values to be sent to the MCU are $FF, the unprogrammed state of the FLASH.

During monitor mode entry, a reset must be asserted. PTA1 must be held low during the reset and 24 CGMXCLK cycles after the end of the reset. Then the MCU will wait for eight security bytes on PTA0. Each byte will be echoed back to the host. See Figure 16-15.

If the received bytes match those at locations $FFF6–$FFFD, the host bypasses the security feature and can read all FLASH locations and execute code from FLASH. Security remains bypassed until a reset occurs. After any reset, security will be locked. To bypass security again, the host must resend the eight security bytes on PTA0.

If the received bytes do not match the data at locations $FFF6–$FFFD, the host fails to bypass the security feature. The MCU remains in monitor mode, but reading FLASH locations returns undefined data, and trying to execute code from FLASH causes an illegal address reset.



Notes: 1 = Echo delay (2 bit times)
2 = Data return delay (2 bit times)
4 = Wait 1 bit time before sending next byte.

Figure 16-15. Monitor Mode Entry Timing

After receiving the eight security bytes from the host, the MCU transmits a break character signalling that it is ready to receive a command.

NOTE

The MCU does not transmit a break character until after the host sends the eight security bytes.

17.7 Internal Oscillator Characteristics

Characteristic[1]	Symbol	Min	Typ	Max	Unit
Internal oscillator base frequency[2], [3]	f_{INTOSC}	230.4	307.2	384	kHz
Internal oscillator tolerance	f_{OSC_TOL}	–25	—	+25	%
Internal oscillator multiplier[4]	N	1	—	127	—

1. V_{DD} = 5.5 Vdc to 2.7 Vdc, V_{SS} = 0 Vdc, T_A = –40°C to +125°C, unless otherwise noted
2. Internal oscillator is selectable through software for a maximum frequency. Actual frequency will be multiplier (N) x base frequency.
3. $f_{Bus} = (f_{INTOSC} / 4) \times N$ when internal clock source selected
4. Multiplier must be chosen to limit the maximum bus frequency of 4 MHz for 2.7-V operation and 8 MHz for 4.5-V operation.

17.8 External Oscillator Characteristics

Characteristic[1]	Symbol	Min	Typ	Max	Unit
External clock option[2], [3] With ICG clock disabled With ICG clock enabled EXTSLOW = 1[4] EXTSLOW = 0[4]	f_{EXTOSC}	 dc[5] 60 307.2 k	 — — —	 32 M[6] 307.2 k 32 M[6]	Hz
External crystal options[7], [8] EXTSLOW = 1[4] EXTSLOW = 0[4]	f_{EXTOSC}	 30 k 1 M	 — —	 100 k 8 M	Hz
Crystal load capacitance[9]	C_L	—	—	—	pF
Crystal fixed capacitance[9]	C_1	—	2 x C_L	—	pF
Crystal tuning capacitance[9]	C_2	—	2 x C_L	—	pF
Feedback bias resistor[9]	R_B	—	10	—	MΩ
Series resistor [9], [10]	R_S	—	—	—	MΩ

1. V_{DD} = 5.5 to 2.7 Vdc, V_{SS} = 0 Vdc, T_A = –40°C to +125°C, unless otherwise noted
2. Setting EXTCLKEN configuration option enables OSC1 pin for external clock square-wave input.
3. No more than 10% duty cycle deviation from 50%
4. EXTSLOW configuration option configures external oscillator for a slow speed crystal and sets the clock monitor circuits of the ICG module to expect an external clock frequency that is higher/lower than the internal oscillator base frequency, f_{INTOSC}.
5. Some modules may require a minimum frequency greater than dc for proper operation. See appropriate table for this information.
6. MCU speed derates from 32 MHz at V_{DD} = 4.5 Vdc to 16 MHz at V_{DD} = 2.7 Vdc.
7. Setting EXTCLKEN and EXTXTALEN configuration options enables OSC1 and OSC2 pins for external crystal option.
8. $f_{Bus} = (f_{EXTOSC} / 4)$ when external clock source is selected.
9. Consult crystal vendor data sheet, see Figure 7-3. External Clock Generator Block Diagram.
10. Not required for high-frequency crystals

17.11 Memory Characteristics

Characteristic	Symbol	Min	Typ	Max	Unit
RAM data retention voltage	V_{RDR}	1.3	—	—	V
FLASH program bus clock frequency	—	1	—	—	MHz
FLASH read bus clock frequency	f_{Read}[1]	0	—	8 M	Hz
FLASH page erase time <1 K cycles >1 K cycles	t_{Erase}	 0.9 3.6	 1 4	 1.1 5.5	ms
FLASH mass erase time	t_{MErase}	4	—	—	ms
FLASH PGM/ERASE to HVEN setup time	t_{NVS}	10	—	—	µs
FLASH high-voltage hold time	t_{NVH}	5	—	—	µs
FLASH high-voltage hold time (mass erase)	t_{NVHL}	100	—	—	µs
FLASH program hold time	t_{PGS}	5	—	—	µs
FLASH program time	t_{PROG}	30	—	40	µs
FLASH return to read time	t_{RCV}[2]	1	—	—	µs
FLASH cumulative program HV period	t_{HV}[3]	—	—	4	ms
FLASH endurance[4]	—	10 k	100 k	—	Cycles
FLASH data retention time[5]	—	15	100	—	Years

1. f_{Read} is defined as the frequency range for which the FLASH memory can be read.
2. t_{RCV} is defined as the time it needs before the FLASH can be read after turning off the high voltage charge pump, by clearing HVEN to 0.
3. t_{HV} is defined as the cumulative high voltage programming time to the same row before next erase. t_{HV} must satisfy this condition: $t_{NVS} + t_{NVH} + t_{PGS} + (t_{PROG} \times 64) \leq t_{HV}$ maximum.
4. Typical endurance was evaluated for this product family. For additional information on how Freescale defines *Typical Endurance*, please refer to Engineering Bulletin EB619.
5. Typical data retention values are based on intrinsic capability of the technology measured at high temperature and de-rated to 25°C using the Arrhenius equation. For additional information on how Freescale defines *Typical Data Retention*, please refer to Engineering Bulletin EB618.

B.4.2 Functional Operating Range

Characteristic	Symbol	Value	Unit
Operating temperature range	T_A	–40 to 105	°C
Operating voltage range	V_{DD}	3.0 ± 10% 5.0 ± 10%	V

B.4.3 Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal resistance PDIP (16 pins) SOIC (16 pins)	θ_{JA}	 66 95	°C/W
I/O pin power dissipation	$P_{I/O}$	User determined	W
Power dissipation(1)	P_D	$P_D = (I_{DD} \times V_{DD}) + P_{I/O} = K/(T_J + 273°C)$	W
Constant(2)	K	$P_D \times (T_A + 273°C) + P_D^2 \times \theta_{JA}$	W/°C
Average junction temperature	T_J	$T_A + (P_D \times \theta_{JA})$	°C
Maximum junction temperature	T_{JM}	125	°C

1. Power dissipation is a function of temperature.
2. K is a constant unique to the device. K can be determined for a known T_A and measured P_D. With this value of K, P_D and T_J can be determined for any value of T_A.

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