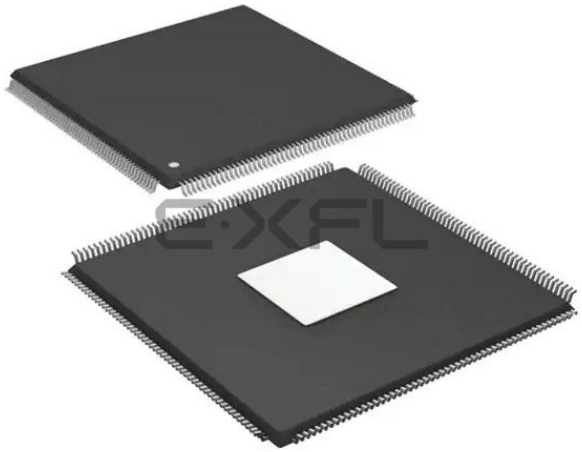


Welcome to E-XFL.COM

Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Active
Type	Floating Point
Interface	DAI, DPI
Clock Rate	266MHz
Non-Volatile Memory	ROM (512kB)
On-Chip RAM	128kB
Voltage - I/O	3.30V
Voltage - Core	1.20V
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	208-LQFP Exposed Pad
Supplier Device Package	208-LQFP-EP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-21371kswz-2b

TABLE OF CONTENTS

REVISION HISTORY

4/13—Rev. C to Rev. D

Corrected Extended Precision Normal or Instruction Word (48 bits) ADSP-21375 Internal Memory Space 7

Updated Development Tools 11

Added section Related Signal Chains 12

Revised $\overline{MS}_{1-0}$ pin description in Pin Function Descriptions 13

Corrected $\overline{EMU}$ pin Type from O/T (pu) to O (O/D) (pu) in Pin Function Descriptions 13

Corrected $T_{JUNCTION}$ specifications in Operating Conditions 16

Added footnote 3 to Table 25 in Memory Read—Bus Master 29

Updated Serial Ports timing parameter data in Serial Ports—External Clock 33

Updated Serial Ports timing parameter data in Serial Ports—Internal Clock 34

Changed Max values in Table 33 in Pulse-Width Modulation Generators (PWM) 40

Updated timing parameters in Table 37 and in Figure 31 in SPI Interface—Master 44

Added 1.0 V, 200 MHz specifications to the following timing specifications.

Clock Input 21

Precision Clock Generator (Direct Pin Routing) 26

SDRAM Interface Timing 28

Memory Read—Bus Master 29

Memory Write—Bus Master 31

Serial Ports 33

Input Data Port (IDP) 38

S/PDIF Transmitter Input Data Timing 42

S/PDIF Receiver 43

SPI Interface—Slave 45

Serial ports operate in five modes:

- Standard DSP serial mode
- Multichannel (TDM) mode with support for packed I²S mode
- I²S mode
- Packed I²S mode
- Left-justified sample pair mode

Left-justified sample pair mode is a mode where in each frame sync cycle two samples of data are transmitted/received—one sample on the high segment of the frame sync, the other on the low segment of the frame sync. Programs have control over various attributes of this mode.

Each of the serial ports supports the left-justified sample pair and I²S protocols (I²S is an industry-standard interface commonly used by audio codecs, ADCs, and DACs such as the Analog Devices AD183x family), with two data pins, allowing four left-justified sample pair or I²S channels (using two stereo devices) per serial port, with a maximum of up to 32 I²S channels. The serial ports permit little-endian or big-endian transmission formats and word lengths selectable from 3 bits to 32 bits. For the left-justified sample pair and I²S modes, data-word lengths are selectable between 8 bits and 32 bits. Serial ports offer selectable synchronization and transmit modes as well as optional μ-law or A-law companding selection on a per channel basis. Serial port clocks and frame syncs can be internally or externally generated.

The serial ports also contain frame sync error detection logic where the serial ports detect frame syncs that arrive early (for example frame syncs that arrive while the transmission/reception of the previous word is occurring). All the serial ports also share one dedicated error interrupt.

S/PDIF-Compatible Digital Audio Receiver/Transmitter

The ADSP-21371 S/PDIF receiver/transmitter has no separate DMA channels. It receives audio data in serial format and converts it into a biphase encoded signal. The serial data input to the receiver/transmitter can be formatted as left justified, I²S or right justified with word widths of 16, 18, 20, or 24 bits.

The serial data, clock, and frame sync inputs to the S/PDIF receiver/transmitter are routed through the signal routing unit (SRU). They can come from a variety of sources such as the SPORTs, external pins, the precision clock generators (PCGs), and are controlled by the SRU control registers.

The ADSP-21375 does not have an S/PDIF-compatible digital receiver/transmitter.

Input Data Port (IDP)

The IDP provides up to eight serial input channels—each with its own clock, frame sync, and data inputs. The eight channels are automatically multiplexed into a single 32-bit by eight-deep FIFO. Data is always formatted as a 64-bit frame and divided into two 32-bit words. The serial protocol is designed to receive audio channels in I²S, left-justified sample pair, or right-justified mode. One frame sync cycle indicates one 64-bit left/right pair, but data is sent to the FIFO as 32-bit words (that is, one-half of a frame at a time). The processor supports 24- and 32-bit I²S, 24- and 32-bit left-justified, and 24-, 20-, 18- and 16-bit right-justified formats.

Precision Clock Generator (PCG)

The precision clock generators (PCG) consist of four units, each of which generates a pair of signals (clock and frame sync) derived from a clock input signal. The units, A B, C, and D, are identical in functionality and operate independently of each other. The two signals generated by each unit are normally used as a serial bit clock/frame sync pair.

Digital Peripheral Interface (DPI)

The digital peripheral interface provides connections to two serial peripheral interface (SPI) ports, one universal asynchronous receiver-transmitter (UART), 12 flags, a 2-wire interface (TWI), and two general-purpose timers.

Serial Peripheral (Compatible) Interface

The ADSP-21371/ADSP-21375 SHARC processors contain two serial peripheral interface ports (SPIs). The SPI is an industry-standard synchronous serial link, enabling the SPI-compatible ports of the processors to communicate with other SPI compatible devices. The SPI consists of two data pins, one device select pin, and one clock pin. It is a full-duplex synchronous serial interface, supporting both master and slave modes. The SPI port can operate in a multimaster environment by interfacing with up to four other SPI-compatible devices, either acting as a master or slave device.

The SPI-compatible peripheral implementation also features programmable baud rates and clock phases and polarities. The SPI-compatible port uses open drain drivers to support a multimaster configuration and to avoid data contention.

UART Port

The processors provide a full-duplex Universal Asynchronous Receiver/Transmitter (UART) port, which is fully compatible with PC-standard UARTs. The UART port provides a simplified UART interface to other peripherals or hosts, supporting full-duplex, DMA-supported, asynchronous transfers of serial data. The UART also has multiprocessor communication capability using 9-bit address detection. This allows it to be used in multidrop networks through the RS-485 data interface standard. The UART port also includes support for 5 to 8 data bits, 1 or 2 stop bits, and none, even, or odd parity. The UART port supports two modes of operation:

- PIO (programmed I/O) – The processor sends or receives data by writing or reading I/O-mapped UART registers. The data is double-buffered on both transmit and receive.
- DMA (direct memory access) – The DMA controller transfers both transmit and receive data. This reduces the number and frequency of interrupts required to transfer data to and from memory. The UART has two dedicated

Table 9. Pin Descriptions (Continued)

Name	Type	State During and After Reset	Description
SDCKE	O/T (pu)	Pulled high/ driven high	**SDRAM Clock Enable.** Connect to SDRAM's CKE pin. Enables and disables the CLK signal. For details, see the data sheet supplied with the SDRAM device.
SDA10	O/T (pu)	Pulled high/ driven low	**SDRAM A10 Pin.** Enables applications to refresh an SDRAM in parallel with a non-SDRAM accesses. This pin replaces the DSP's A10 pin only during SDRAM accesses.
SDCLK	O/T	High-Z/driving	**SDRAM Clock.**
$\overline{MS}_{0-1}$	O/T (pu)	Pulled high/ driven high	**Memory Select Lines 0–1.** These lines are asserted (low) as chip selects for the corresponding banks of external memory. The $\overline{MS}_{1-0}$ lines are decoded memory address lines that change at the same time as the other address lines. The $\overline{MS1}$ pin can be used in EPORT/FLASH boot mode. For more information, see the *ADSP-2137x SHARC Processor Hardware Reference*.
FLAG[0]/$\overline{IRQ0}$	I/O	FLAG[0] INPUT	**FLAG0/Interrupt Request0.**
FLAG[1]/$\overline{IRQ1}$	I/O	FLAG[1] INPUT	**FLAG1/Interrupt Request1.**
FLAG[2]/$\overline{IRQ2}$/ $\overline{MS2}$	I/O with programmable pu (for MS mode)	FLAG[2] INPUT	**FLAG2/Interrupt Request/Memory Select2.**
FLAG[3]/ TMREXP/ $\overline{MS3}$	I/O with programmable pu (for MS mode)	FLAG[3] INPUT	**FLAG3/Timer Expired/Memory Select3.**
TDI	I (pu)		**Test Data Input (JTAG).** Provides serial data for the boundary scan logic. TDI has a 22.5 kΩ internal pull-up resistor.
TDO	O/T		**Test Data Output (JTAG).** Serial scan output of the boundary scan path.
TMS	I (pu)		**Test Mode Select (JTAG).** Used to control the test state machine. TMS has a 22.5 kΩ internal pull-up resistor.
TCK	I		**Test Clock (JTAG).** Provides a clock for JTAG boundary scan. TCK must be asserted (pulsed low) after power-up or held low for proper operation of the processor.
$\overline{TRST}$	I (pu)		**Test Reset (JTAG).** Resets the test state machine. $\overline{TRST}$ must be asserted (pulsed low) after power-up or held low for proper operation of the processor. $\overline{TRST}$ has a 22.5 kΩ internal pull-up resistor.
$\overline{EMU}$	O (O/D) (pu)		**Emulation Status.** Must be connected to the processor. Analog Devices DSP Tools product line of JTAG emulators target board connector only. $\overline{EMU}$ has a 22.5 kΩ internal pull-up resistor.
CLK_CFG_{1-0}	I		**Core to CLKIN Ratio Control.** These pins set the start up clock frequency. See the *ADSP-2137x SHARC Processor Hardware Reference* for a description of the clock configuration modes. Note that the operating frequency can be changed by programming the PLL multiplier and divider in the PMCTL register at any time after the core comes out of reset.
$BOOT\_CFG_{1-0}$	I		**Boot Configuration Select.** These pins select the boot mode for the processor. The BOOT_CFG pins must be valid before reset is asserted. See the *ADSP-2137x SHARC Processor Hardware Reference* for information about boot modes.

ADSP-21371/ADSP-21375 SPECIFICATIONS

OPERATING CONDITIONS

Parameter[1]	Description	1.0 V, 200 MHz Min	1.0 V, 200 MHz Max	1.2 V, 266 MHz Min	1.2 V, 266 MHz Max	Unit
V_{DDINT}	Internal (Core) Supply Voltage	0.95	1.05	1.14	1.26	V
V_{DDEXT}	External (I/O) Supply Voltage	3.13	3.47	3.13	3.47	V
V_{IH}[2]	High Level Input Voltage @ V_{DDEXT} = Max	2.0	V_{DDEXT} + 0.5	2.0	V_{DDEXT} + 0.5	V
V_{IL}[2]	Low Level Input Voltage @ V_{DDEXT} = Min	–0.5	+0.8	–0.5	+0.8	V
V_{IH_CLKIN}[3]	High Level Input Voltage @ V_{DDEXT} = Max	1.74	V_{DDEXT} + 0.5	1.74	V_{DDEXT} + 0.5	V
V_{IL_CLKIN}[3]	Low Level Input Voltage @ V_{DDEXT} = Min	–0.5	+1.10	–0.5	+1.10	V
$T_{JUNCTION}$	Junction Temperature 208-Lead LQFP_EP @ $T_{AMBIENT}$ 0°C to +70°C	N/A	N/A	0	95	°C
$T_{JUNCTION}$	Junction Temperature 208-Lead LQFP_EP @ $T_{AMBIENT}$ –40°C to +85°C	N/A	N/A	–40	+110	°C
$T_{JUNCTION}$	Junction Temperature 208-Lead LQFP_EP @ $T_{AMBIENT}$ –40°C to +105°C	–40	+120	N/A	N/A	°C

[1] Specifications subject to change without notice.

[2] Applies to input and bidirectional pins: ADDR23–0, DATA31–0 (DATA15–0 on ADSP-21375), FLAG3–0, DAI_Px, DPI_Px, $\overline{SPIDS}$, BOOT_CFGx, CLK_CFGx, $\overline{RUNRSTIN}$, $\overline{RESET}$, TCK, TMS, TDI, $\overline{TRST}$.

[3] Applies to input pin CLKIN.

PACKAGE INFORMATION

The information presented in Figure 3 provides details about the package branding for the ADSP-21371/ADSP-21375 processor. For a complete listing of product availability, see Ordering Guide on Page 56.

Figure 3. Typical Package Brand

Table 10. Package Brand Information

Brand Key	Field Description
t	Temperature Range
pp	Package Type
Z	RoHS Compliant Part
cc	See Ordering Guide
vvvvvv.x	Assembly Lot Code
n.n	Silicon Revision
yyww	Date Code

MAXIMUM POWER DISSIPATION

See Engineer-to-Engineer Note *"Estimating Power Dissipation for ADSP-2137x SHARC Processors"* (EE-318) for detailed thermal and power information regarding maximum power dissipation. For information on package thermal specifications, see Thermal Characteristics on Page 50.

ABSOLUTE MAXIMUM RATINGS

Stresses greater than those listed in Table 11 may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 11. Absolute Maximum Ratings

Parameter	Rating
Internal (Core) Supply Voltage (V_{DDINT})	–0.3 V to +1.5 V
External (I/O) Supply Voltage (V_{DDEXT})	–0.3 V to +4.6 V
Input Voltage –0.5 V to V_{DDEXT}	+0.5 V
Output Voltage Swing –0.5 V to V_{DDEXT}	+0.5 V

Table 11. Absolute Maximum Ratings (Continued)

Parameter	Rating
Load Capacitance	200 pF
Storage Temperature Range	–65°C to +150°C
Junction Temperature under Bias	125°C

ESD SENSITIVITY

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

TIMING SPECIFICATIONS

Use the exact timing information given. Do not attempt to derive parameters from the addition or subtraction of others. While addition or subtraction would yield meaningful results for an individual device, the values given in this data sheet reflect statistical variations and worst cases. Consequently, it is not meaningful to add parameters to derive longer times. See Figure 38 on Page 49 under Test Conditions for voltage reference levels.

Switching Characteristics specify how the processor changes its signals. Circuitry external to the processor must be designed for compatibility with these signal characteristics. Switching characteristics describe what the processor will do in a given circumstance. Use switching characteristics to ensure that any timing requirement of a device connected to the processor (such as memory) is satisfied.

Timing Requirements apply to signals that are controlled by circuitry external to the processor, such as the data input for a read operation. Timing requirements guarantee that the processor operates correctly with other devices.

Core Clock Requirements

The processor's internal clock (a multiple of CLKIN) provides the clock signal for timing internal memory, processor core, and serial ports. During reset, program the ratio between the processor's internal clock frequency and external (CLKIN) clock frequency with the CLK_CFG1–0 pins.

The processor's internal clock switches at higher frequencies than the system input clock (CLKIN). To generate the internal clock, the processor uses an internal phase-locked loop (PLL, see Figure 4). This PLL-based clocking minimizes the skew between the system clock (CLKIN) signal and the processor's internal clock.

Power-Up Sequencing

The timing requirements for processor startup are given in Table 13.

Note that during power-up, a leakage current of approximately 200 µA may be observed on the $\overline{\text{RESET}}$ pin. This leakage current results from the weak internal pull-up resistor on this pin being enabled during power-up.

Table 13. Power Up Sequencing Timing Requirements (Processor Startup)

Parameter		Min	Max	Unit
Timing Requirements				
t_{RSTVDD}	$\overline{\text{RESET}}$ Low Before V_{DDINT}/V_{DDEXT} On	0		ns
$t_{IVDDEVDD}$	V_{DDINT} on Before V_{DDEXT}	–50	+200	ms
t_{CLKVDD} [1]	CLKIN Valid After V_{DDINT}/V_{DDEXT} Valid	0	200	ms
t_{CLKRST}	CLKIN Valid Before $\overline{\text{RESET}}$ Deasserted	10 [2]		µs
t_{PLLRST}	PLL Control Setup Before $\overline{\text{RESET}}$ Deasserted	20 [3]		µs
Switching Characteristic				
$t_{CORERST}$	Core Reset Deasserted After $\overline{\text{RESET}}$ Deasserted	$4096 \times t_{CK} + 2 \times t_{CCLK}$ [4, 5]		

[1] Valid V_{DDINT}/V_{DDEXT} assumes that the supplies are fully ramped to their 1.2 and 3.3 volt rails. Voltage ramp rates can vary from microseconds to hundreds of milliseconds depending on the design of the power supply subsystem.

[2] Assumes a stable CLKIN signal, after meeting worst-case startup timing of crystal oscillators. Refer to your crystal oscillator manufacturer's datasheet for startup time. Assume a 25 ms maximum oscillator startup time if using the XTAL pin and internal oscillator circuit in conjunction with an external crystal.

[3] Based on CLKIN cycles.

[4] Applies after the power-up sequence is complete. Subsequent resets require a minimum of four CLKIN cycles for $\overline{\text{RESET}}$ to be held low in order to properly initialize and propagate default states at all I/O pins.

[5] The 4096 cycle count depends on t_{SRST} specification in Table 15. If setup time is not met, one additional CLKIN cycle may be added to the core reset time, resulting in 4097 cycles maximum.

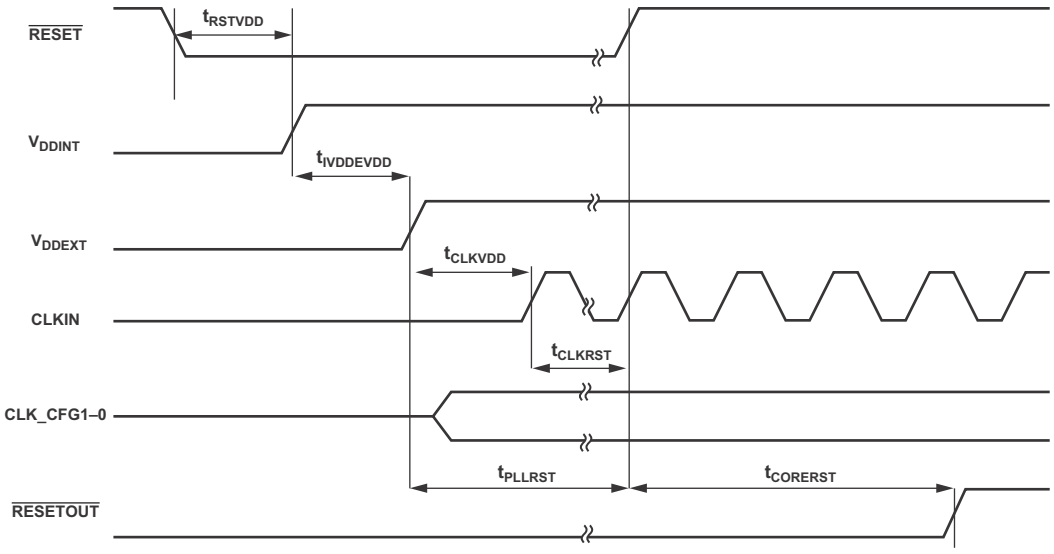


Figure 5. Power-Up Sequencing

Clock Input

Table 14. Clock Input

Parameter		200 MHz Min	200 MHz Max	266 MHz Min	266 MHz Max	Unit
Timing Requirements						
t_{CK}	CLKIN Period	30[1]	100	22.5[1]	100	ns
t_{CKL}	CLKIN Width Low	15[1]	45	11.25[1]	45	ns
t_{CKH}	CLKIN Width High	15[1]	45	11.25[1]	45	ns
t_{CKRF}	CLKIN Rise/Fall (0.4 V to 2.0 V)		6		6	ns
t_{CCLK}[2]	CCLK Period	5	10	3.75	10	ns
f_{VCO}	VCO Frequency	200	800	200	800	MHz

[1] Applies only for CLKCFG1–0 = 00 and default values for PLL control bits in the PMCTL register.
[2] Any changes to PLL control bits in the PMCTL register must meet core clock timing specification t_{CCLK}.

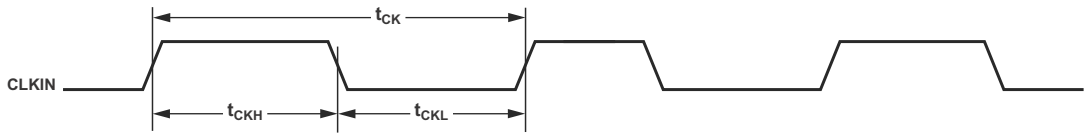


Figure 6. Clock Input

Clock Signals

The processor can use an external clock or a crystal. See the CLKIN pin description in Table 9. Programs can configure the processor to use its internal clock generator by connecting the necessary components to CLKIN and XTAL. Figure 7 shows the component connections used for a crystal operating in fundamental mode. Note that the clock rate is achieved using a 16.67 MHz crystal and a PLL multiplier ratio 16:1 (CCLK:CLKIN achieves a clock speed of 266 MHz). To achieve the full core clock rate, programs need to configure the multiplier bits in the PMCTL register.

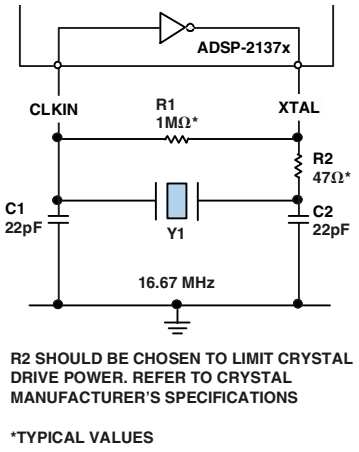


Figure 7. 266 MHz Operation (Fundamental Mode Crystal)

Reset

Table 15. Reset

Parameter		Min	Max	Unit
Timing Requirements				
t_{WRST}[1]	$\overline{\text{RESET}}$ Pulse Width Low	$4 \times t_{CK}$		ns
t_{SRST}	$\overline{\text{RESET}}$ Setup Before CLKIN Low	8		ns

[1] Applies after the power-up sequence is complete. At power-up, the processor's internal phase-locked loop requires no more than 100 µs while $\overline{\text{RESET}}$ is low, assuming stable V_{DD} and CLKIN (not including start-up time of external clock oscillator).

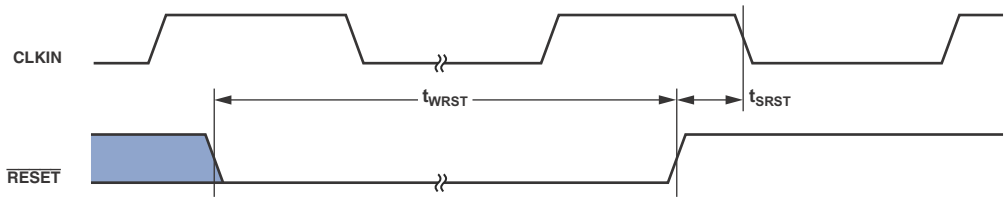


Figure 8. Reset

Running Reset

The following timing specification applies to the $\overline{\text{RESETOUT}}$/$\overline{\text{RUNRSTIN}}$ pin when it is configured as $\overline{\text{RUNRSTIN}}$.

Table 16. Running Reset

Parameter		Min	Max	Unit
Timing Requirements				
$t_{WRUNRST}$	Running $\overline{\text{RESET}}$ Pulse Width Low	$4 \times t_{CK}$		ns
$t_{SRUNRST}$	Running $\overline{\text{RESET}}$ Setup Before CLKIN High	8		ns

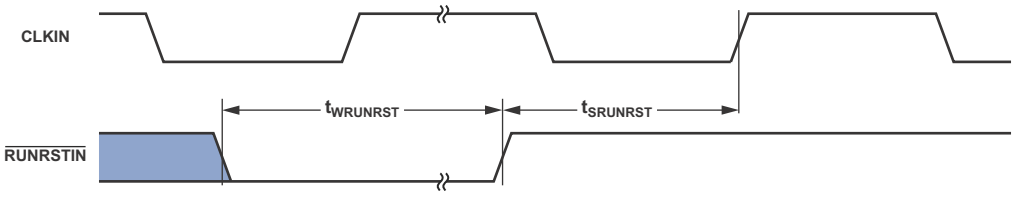


Figure 9. Running Reset

Precision Clock Generator (Direct Pin Routing)

This timing is only valid when the SRU is configured such that the precision clock generator (PCG) takes its inputs directly from the DAI pins (via pin buffers) and sends its outputs directly to the DAI pins. For the other cases, where the PCG's inputs and outputs are not directly routed to/from DAI pins (via pin buffers) there is no timing data available. All timing parameters and switching characteristics apply to external DAI pins (DAI_P01 through DAI_P20).

Table 22. Precision Clock Generator (Direct Pin Routing)

Parameter		1.0 V, 200 MHz Min	1.0 V, 200 MHz Max	1.2 V, 266 MHz Min	1.2 V, 266 MHz Max	Unit
Timing Requirements						
t_{PCGIP}	Input Clock Period	$t_{PCLK} \times 4$		$t_{PCLK} \times 4$		ns
t_{STRIG}	PCG Trigger Setup Before Falling Edge of PCG Input Clock	4.5		4.5		ns
t_{HTRIG}	PCG Trigger Hold After Falling Edge of PCG Input Clock	3		3		ns
Switching Characteristics						
t_{DPCGIO}	PCG Output Clock and Frame Sync Active Edge Delay After PCG Input Clock	2.5	12.8	2.5	10	ns
$t_{DTRIGCLK}$	PCG Output Clock Delay After PCG Trigger	$2.5 + ((2.5) \times t_{PCGIW})$	$12.8 + ((2.5) \times t_{PCGIW})$	$2.5 + ((2.5) \times t_{PCGIW})$	$10 + ((2.5) \times t_{PCGIW})$	ns
$t_{DTRIGFS}$	PCG Frame Sync Delay After PCG Trigger	$2.5 + ((2.5 + D - PH) \times t_{PCGIW})$	$12.8 + ((2.5 + D - PH) \times t_{PCGIW})$	$2.5 + ((2.5 + D - PH) \times t_{PCGIW})$	$10 + ((2.5 + D - PH) \times t_{PCGIW})$	ns
t_{PCGOW}[1]	Output Clock Period	$2 \times t_{PCGIW} - 1$		$2 \times t_{PCGIW} - 1$		ns

D = FSxDIV, PH = FSxPHASE. For more information, see the *ADSP-2137x SHARC Processor Hardware Reference*, "Precision Clock Generators" chapter.

[1] Normal mode of operation.

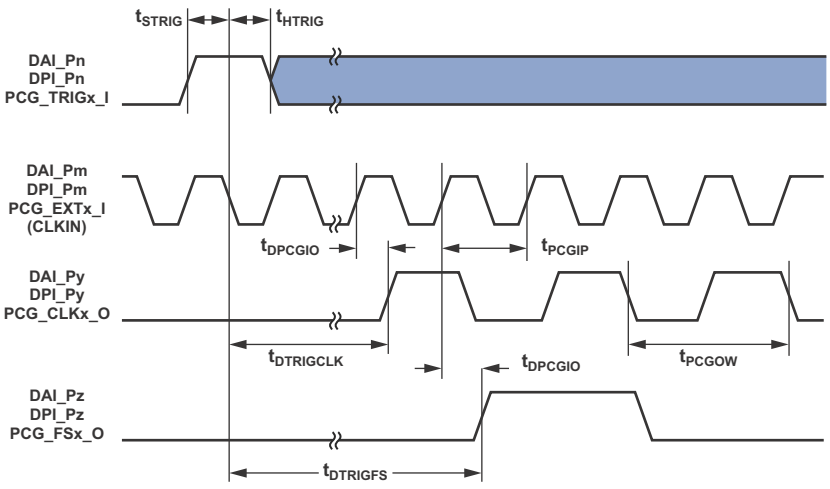


Figure 15. Precision Clock Generator (Direct Pin Routing)

Memory Read—Bus Master

Use these specifications for asynchronous interfacing to memories. Note that timing for ACK, DATA, $\overline{RD}$, $\overline{WR}$, and strobe timing parameters only apply to asynchronous access mode.

Table 25. Memory Read—Bus Master

Parameter		1.0 V, 200 MHz Min	1.0 V, 200 MHz Max	1.2 V, 266 MHz Min	1.2 V, 266 MHz Max	Unit
Timing Requirements						
t_{DAD}	Address, Selects Delay to Data Valid[1, 2, 3]		W + t_{SDCLK} – 5.12		W + t_{SDCLK} – 5.12	ns
t_{DRLD}	$\overline{RD}$ Low to Data Valid[1, 3]		W – 3		W – 3	ns
t_{SDS}	Data Setup to $\overline{RD}$ High	2.2		2.2		ns
t_{HDRH}	Data Hold from $\overline{RD}$ High[4, 5]	0		0		ns
t_{DAAK}	ACK Delay from Address, Selects[2, 6]		t_{SCDCLK} – 11.4 + W		t_{SCDCLK} – 10.1 + W	ns
t_{DSAK}	ACK Delay from $\overline{RD}$ Low[5]		W – 7.25		W – 7.0	ns
Switching Characteristics						
t_{DRHA}	Address Selects Hold After $\overline{RD}$ High	RHC + 0.38		RHC + 0.38		ns
t_{DARL}	Address Selects to $\overline{RD}$ Low[2]	t_{SDCLK} – 3.8		t_{SDCLK} – 3.3		ns
t_{RW}	$\overline{RD}$ Pulse Width	W – 1.4		W – 1.4		ns
t_{RWR}	$\overline{RD}$ High to $\overline{WR}$, $\overline{RD}$, Low	HI + t_{SDCLK} – 0.8		HI + t_{SDCLK} – 0.8		ns

W = (number of wait states specified in AMICTLx register) × t_{SDCLK}
HI = RHC + IC (RHC = (number of Read Hold Cycles specified in AMICTLx register) × t_{SDCLK}
IC = (number of idle cycles specified in AMICTLx register) × t_{SDCLK})
H = (number of hold cycles specified in AMICTLx register) × t_{SDCLK}

[1] Data delay/setup: System must meet t_{DAD}, t_{DRLD}, or t_{SDS}.
[2] The falling edge of $\overline{MS}$x, is referenced.
[3] The maximum limit of timing requirement values for t_{DAD} and t_{DRLD} parameters are applicable for the case where AMI_ACK is always high and when the ACK feature is not used.
[4] Note that timing for ACK, DATA, $\overline{RD}$, $\overline{WR}$, and strobe timing parameters only apply to asynchronous access mode.
[5] Data hold: User must meet t_{HDRH} in asynchronous access mode. See Test Conditions on Page 49 for the calculation of hold times given capacitive and dc loads.
[6] ACK delay/setup: User must meet t_{DAAK}, or t_{DSAK}, for deassertion of ACK (low). For asynchronous assertion of ACK (high) user must meet t_{DAAK} or t_{DSAK}.

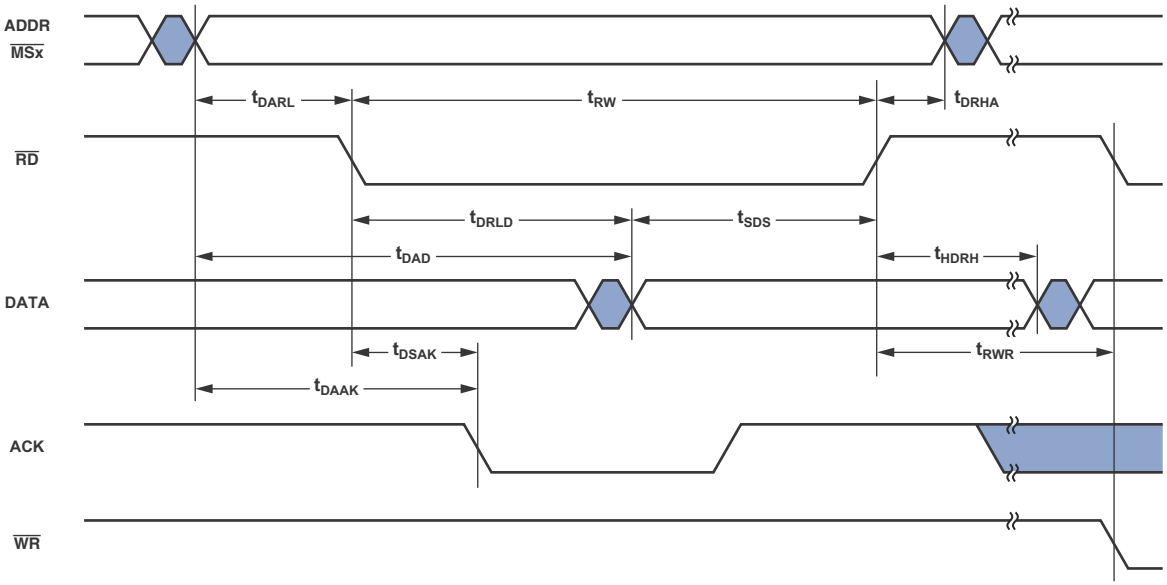


Figure 18. Memory Read—Bus Master

Input Data Port (IDP)

The timing requirements for the IDP are given in Table 31. IDP signals are routed to the DAI_P20–1 pins using the SRU. Therefore, the timing specifications provided below are valid at the DAI_P20–1 pins.

Table 31. Input Data Port (IDP)

Parameter		1.0 V, 200 MHz Min	1.0 V, 200 MHz Max	1.2 V, 266 MHz Min	1.2 V, 266 MHz Max	Unit
Timing Requirements						
t_{SISFS}[1]	Frame Sync Setup Before Serial Clock Rising Edge	4.95		3.8		ns
t_{SIHFS}[1]	Frame Sync Hold After Serial Clock Rising Edge	2.5		2.5		ns
t_{SISD}[1]	Data Setup Before Serial Clock Rising Edge	3.35		2.5		ns
t_{SIHD}[1]	Data Hold After Serial Clock Rising Edge	2.5		2.5		ns
$t_{IDPCLKW}$	Clock Width	$(t_{PCLK} \times 4) \div 2 - 1$		$(t_{PCLK} \times 4) \div 2 - 1$		ns
t_{IDPCLK}	Clock Period	$t_{PCLK} \times 4$		$t_{PCLK} \times 4$		ns

[1] The data, serial clock, and frame sync signals can come from any of the DAI pins. Serial clock and frame sync can also come via PCG or SPORTs. PCG's input can be either CLKIN or any of the DAI pins.

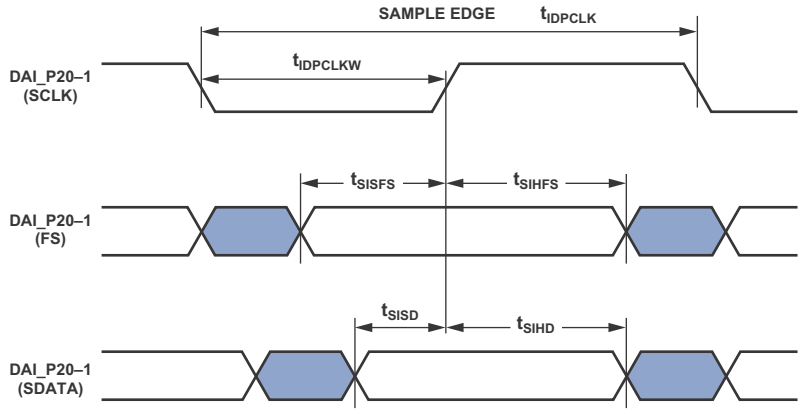


Figure 23. IDP Master Timing

Pulse-Width Modulation Generators (PWM)

For the ADSP-21371, the following timing specifications apply when the DATA31–16 pins are configured as PWM.

Pulse-width modulation generator information does not apply to the ADSP-21375.

Table 33. Pulse-Width Modulation (PWM) Timing

Parameter		Min	Max	Unit
Switching Characteristics				
t_{PWMW}	PWM Output Pulse Width	$t_{PCLK} - 2.5$	$(2^{16} - 2) \times t_{PCLK}$	ns
t_{PWMP}	PWM Output Period	$2 \times t_{PCLK} - 2.5$	$(2^{16} - 1) \times t_{PCLK}$	ns

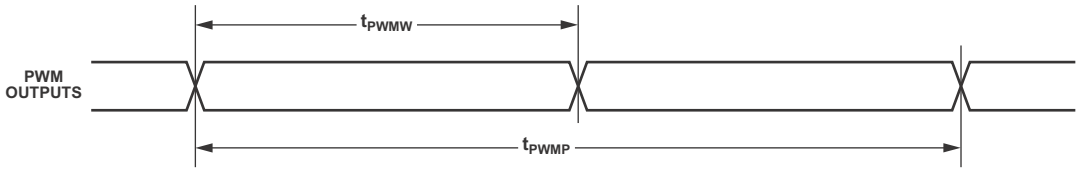


Figure 25. PWM Timing

JTAG Test Access Port and Emulation

Table 41. JTAG Test Access Port and Emulation

Parameter		Min	Max	Unit
Timing Requirements				
t_{TCK}	TCK Period	t_{CK}		ns
t_{STAP}	TDI, TMS Setup Before TCK High	5		ns
t_{HTAP}	TDI, TMS Hold After TCK High	6		ns
t_{SSYS}[1]	System Inputs Setup Before TCK High	7		ns
t_{HSYS}[1]	System Inputs Hold After TCK High	18		ns
t_{TRSTW}	$\overline{\text{TRST}}$ Pulse Width	$4 \times t_{CK}$		ns
Switching Characteristics				
t_{DTDO}	TDO Delay from TCK Low		7	ns
t_{DSYS}[2]	System Outputs Delay After TCK Low		$t_{CK} \div 2 + 7$	ns

[1] System Inputs = ADDR15–0, CLKCFG1–0, $\overline{\text{RESET}}$, BOOT_CFG1–0, DAI_Px, and FLAG3–0.
[2] System Outputs = DAI_Px, ADDR15–0, $\overline{\text{RD}}$, $\overline{\text{WR}}$, FLAG3–0, $\overline{\text{EMU}}$, and ALE.

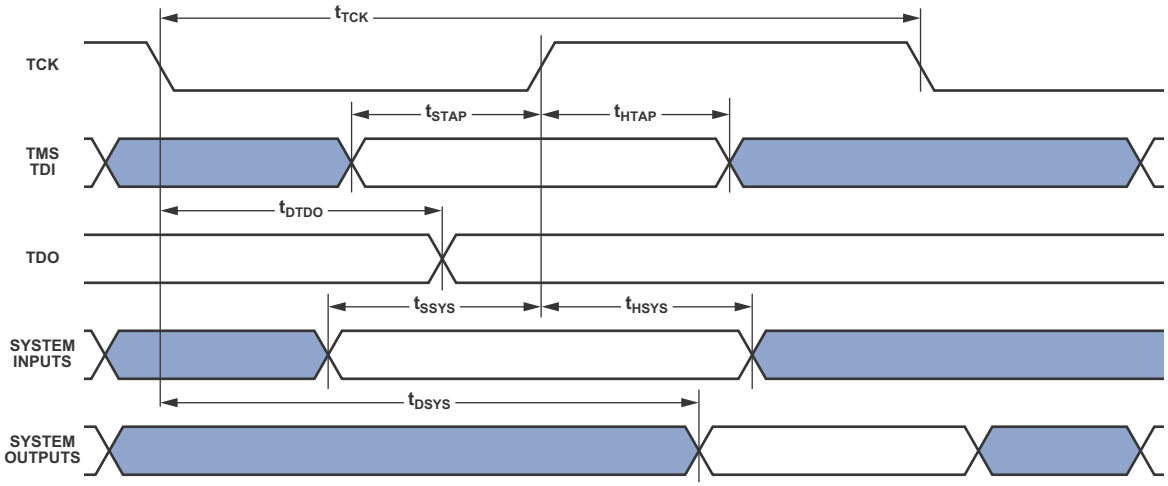


Figure 35. IEEE 1149.1 JTAG Test Access Port

OUTPUT DRIVE CURRENTS

Figure 36 shows typical I-V characteristics for the output drivers of the processors. The curves represent the current drive capability of the output drivers as a function of output voltage.

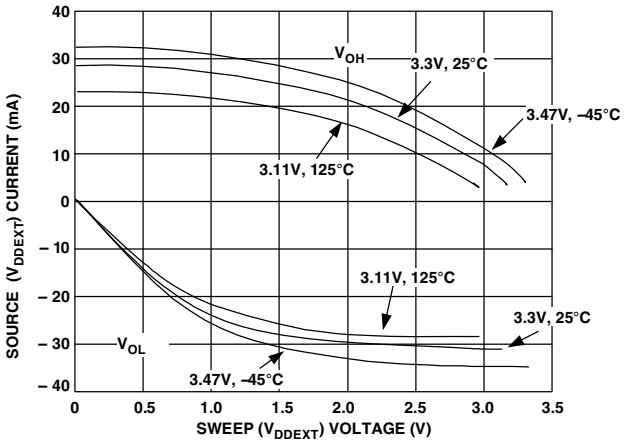


Figure 36. Typical Drive at Junction Temperature

TEST CONDITIONS

The ac signal specifications (timing parameters) appear in Table 15 on Page 22 through Table 41 on Page 48. These include output disable time, output enable time, and capacitive loading. The timing specifications for the SHARC apply for the voltage reference levels in Figure 37.

Timing is measured on signals when they cross the 1.5 V level as described in Figure 38. All delays (in nanoseconds) are measured between the point that the first signal reaches 1.5 V and the point that the second signal reaches 1.5 V.

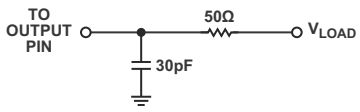


Figure 37. Equivalent Device Loading for AC Measurements (Includes All Fixtures)

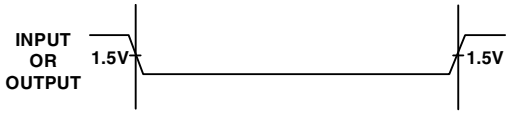


Figure 38. Voltage Reference Levels for AC Measurements

CAPACITIVE LOADING

Output delays and holds are based on standard capacitive loads: 30 pF on all pins (see Figure 37). Figure 41 shows graphically how output delays and holds vary with load capacitance. The graphs of Figure 39, Figure 40, and Figure 41 may not be linear outside the ranges shown for Typical Output Delay vs. Load Capacitance and Typical Output Rise Time (20% to 80%, V = Min) vs. Load Capacitance.

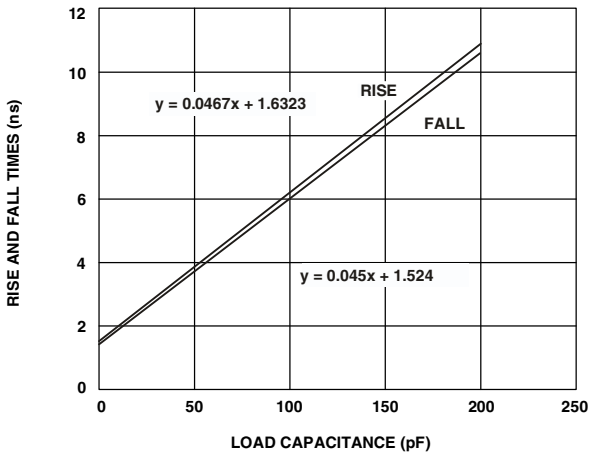


Figure 39. Typical Output Rise/Fall Time (20% to 80%, V_{DDEXT} = Max)

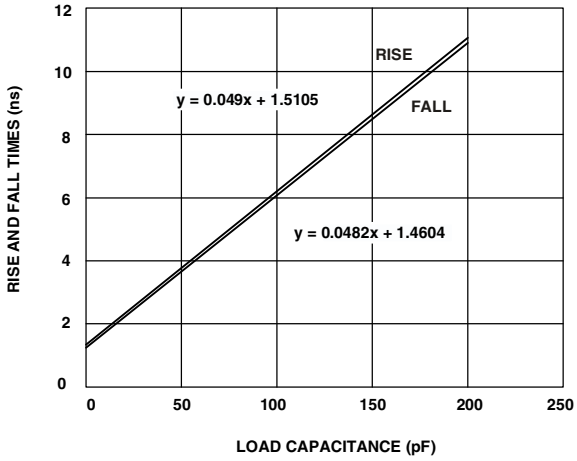


Figure 40. Typical Output Rise/Fall Time (20% to 80%, V_{DDEXT} = Min)

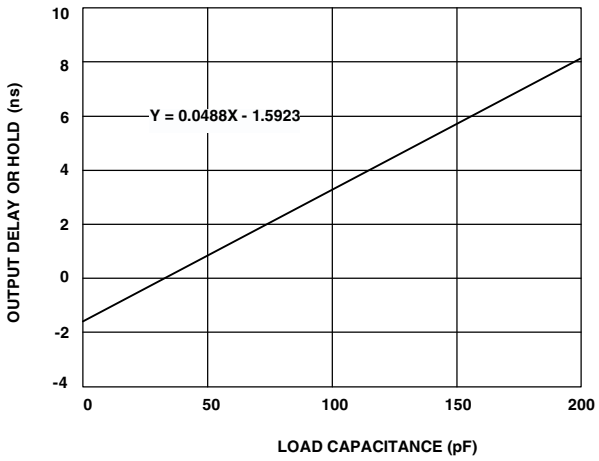


Figure 41. Typical Output Delay or Hold vs. Load Capacitance (at Ambient Temperature)

THERMAL CHARACTERISTICS

The processor is rated for performance over the temperature range specified in Operating Conditions on Page 16.

Table 42 airflow measurements comply with JEDEC standards JESD51-2 and JESD51-6 and the junction-to-board measurement complies with JESD51-8. Test board design complies with JEDEC standard JESD51-7 (LQFP_EP). The junction-to-case measurement complies with MIL- STD-883. All measurements use a 2S2P JEDEC test board.

To determine the junction temperature of the device while on the application PCB, use

$$T_J = T_{CASE} + (\Psi_{JT} \times P_D)$$

where:

T_J = junction temperature °C

T_{CASE} = case temperature (°C) measured at the top center of the package

Ψ_{JT} = junction-to-top (of package) characterization parameter is the Typical value from Table 42.

P_D = power dissipation

Values of θ_{JA} are provided for package comparison and PCB design considerations. θ_{JA} can be used for a first order approximation of T_J by the equation

$$T_J = T_A + (\theta_{JA} \times P_D)$$

where:

T_A = ambient temperature °C

Values of θ_{JC} are provided for package comparison and PCB design considerations when an external heatsink is required.

Values of θ_{JB} are provided for package comparison and PCB design considerations. Note that the thermal characteristics values provided in Table 42 are modeled values.

Table 42. Thermal Characteristics for 208-Lead LQFP E_PAD (With Exposed Pad Soldered to PCB)

Parameter	Condition	Typical	Unit
θ_{JA}	Airflow = 0 m/s	17.1	°C/W
θ_{JMA}	Airflow = 1 m/s	14.7	°C/W
θ_{JMA}	Airflow = 2 m/s	14.0	°C/W
θ_{JC}		9.6	°C/W
Ψ_{JT}	Airflow = 0 m/s	0.23	°C/W
Ψ_{JMT}	Airflow = 1 m/s	0.39	°C/W
Ψ_{JMT}	Airflow = 2 m/s	0.45	°C/W
Ψ_{JB}	Airflow = 0 m/s	11.5	°C/W
Ψ_{JMB}	Airflow = 1 m/s	11.2	°C/W
Ψ_{JMB}	Airflow = 2 m/s	11.0	°C/W

Table 43. ADSP-21371, 208-Lead LQFP_EP Pin Assignment (Numerical by Lead Number) (Continued)

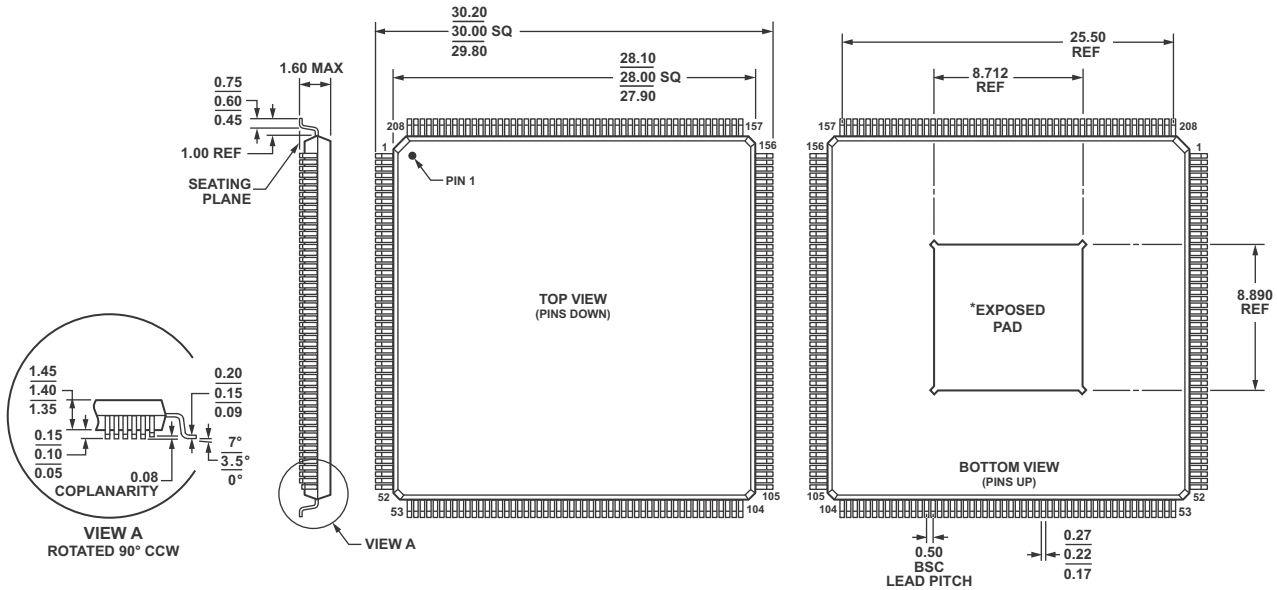
Pin No.	Signal	Pin No.	Signal	Pin No.	Signal	Pin No.	Signal
45	DATA5	97	ADDR19	149	DAI_P5 (SD1A)	201	$\overline{\text{RESETOUT}}$/ $\overline{\text{RUNRSTIN}}$
46	DATA2	98	ADDR20	150	V_{DDEXT}	202	$\overline{\text{RESET}}$
47	DATA3	99	ADDR21	151	GND	203	V_{DDEXT}
48	DATA0	100	ADDR23	152	V_{DDINT}	204	GND
49	DATA1	101	ADDR22	153	GND	205	DATA30
50	V_{DDEXT}	102	$\overline{\text{MS1}}$	154	V_{DDINT}	206	DATA31
51	GND	103	$\overline{\text{MS0}}$	155	GND	207	DATA29
52	V_{DDINT}	104	V_{DDINT}	156	V_{DDINT}	208	V_{DDINT}

Table 44. ADSP-21375, 208-Lead LQFP_EP Pin Assignment (Numerical by Lead Number) (Continued)

Pin No.	Signal	Pin No.	Signal	Pin No.	Signal	Pin No.	Signal
45	DATA5	97	ADDR19	149	DAI_P5 (SD1A)	201	$\overline{\text{RESETOUT}}$/ $\overline{\text{RUNRSTIN}}$
46	DATA2	98	ADDR20	150	V_{DDEXT}	202	$\overline{\text{RESET}}$
47	DATA3	99	ADDR21	151	GND	203	V_{DDEXT}
48	DATA0	100	ADDR23	152	V_{DDINT}	204	GND
49	DATA1	101	ADDR22	153	GND	205	DATA30
50	V_{DDEXT}	102	$\overline{\text{MS1}}$	154	V_{DDINT}	206	DATA31
51	GND	103	$\overline{\text{MS0}}$	155	GND	207	DATA29
52	V_{DDINT}	104	V_{DDINT}	156	V_{DDINT}	208	V_{DDINT}

PACKAGE DIMENSIONS

The processors are available in a 208-lead RoHS compliant LQFP_EP package.



COMPLIANT TO JEDEC STANDARDS MS-026-BJB-HD

*NOTE:
THE EXPOSED PAD IS REQUIRED TO BE ELECTRICALLY AND THERMALLY CONNECTED TO GND. THIS SHOULD BE IMPLEMENTED BY SOLDERING THE EXPOSED PAD TO A GND PCB LAND THAT IS THE SAME SIZE AS THE EXPOSED PAD. THE GND PCB LAND SHOULD BE ROBUSTLY CONNECTED TO THE GND PLANE IN THE PCB WITH AN ARRAY OF THERMAL VIAS FOR BEST PERFORMANCE.

Figure 42. 208-Lead Low Profile Quad Flat Package, Exposed Pad [LQFP_EP]
(SW-208-1)
Dimensions shown in millimeters

AUTOMOTIVE PRODUCTS

Some ADSP-21371/ADSP-21375 models are available for automotive applications with controlled manufacturing. Note that this special model may have specifications that differ from the general release models.

The automotive grade products shown in Table 45 are available for use in automotive applications. Contact your local ADI account representative or authorized ADI product distributor for specific product ordering information. Note that all automotive products are RoHS compliant.

Table 45. Automotive Products

Model	Temperature Range[1]	Instruction Rate	On-Chip SRAM	ROM	Package Description	Package Option
AD21371WBSWZ2xx	–40°C to 85°C	266 MHz	1M bit	4M bit	208-Lead LQFP_EP	SW-208-1
AD21371WYSWZ1xx	–40°C to 105°C	200 MHz	1M bit	4M bit	208-Lead LQFP_EP	SW-208-1
AD21375WBSWZ2xx	–40°C to 85°C	266 MHz	0.5M bit	2M bit	208-Lead LQFP_EP	SW-208-1
AD21375WYSWZ1xx	–40°C to 105°C	200 MHz	0.5M bit	2M bit	208-Lead LQFP_EP	SW-208-1

[1] Referenced temperature is ambient temperature.

ORDERING GUIDE

Model	Notes	Temperature Range[1]	Instruction Rate	On-Chip SRAM	ROM	Package Description	Package Option
ADSP-21371KSWZ-2A	[2]	0°C to +70°C	266 MHz	1M bit	4M bit	208-Lead LQFP_EP	SW-208-1
ADSP-21371KSWZ-2B	[2]	0°C to +70°C	266 MHz	1M bit	4M bit	208-Lead LQFP_EP	SW-208-1
ADSP-21371BSWZ-2B	[2, 3]	–40°C to +85°C	266 MHz	1M bit	4M bit	208-Lead LQFP_EP	SW-208-1
ADSP-21375KSWZ-2B	[2]	0°C to +70°C	266 MHz	0.5M bit	2M bit	208-Lead LQFP_EP	SW-208-1
ADSP-21375BSWZ-2B	[2, 3]	–40°C to +85°C	266 MHz	0.5M bit	2M bit	208-Lead LQFP_EP	SW-208-1

[1] Referenced temperature is ambient temperature.
[2] Z = RoHS Compliant Part.
[3] Available with a wide variety of audio algorithm combinations sold as part of a chipset and bundled with necessary software. For a complete list, visit our website at www.analog.com/SHARC.

D07170-0-4/13(D)