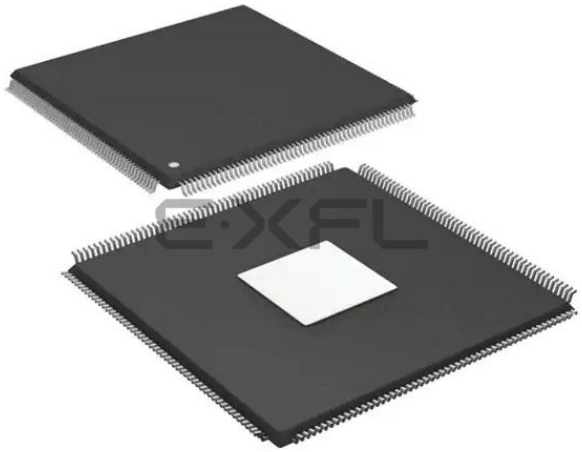

Welcome to E-XFL.COM

Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Active
Type	Floating Point
Interface	DAI, DPI
Clock Rate	266MHz
Non-Volatile Memory	ROM (256kB)
On-Chip RAM	64kB
Voltage - I/O	3.30V
Voltage - Core	1.20V
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	208-LQFP Exposed Pad
Supplier Device Package	208-LQFP-EP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-21375bswz-2b

SHARC FAMILY CORE ARCHITECTURE

The ADSP-21371/ADSP-21375 processors are code compatible at the assembly level with the ADSP-2136x, ADSP-2126x, ADSP-21160x, and ADSP-21161N, and with the first generation ADSP-2106x SHARC processors. The ADSP-21371/ADSP-21375 processors share architectural features with the ADSP-2126x, ADSP-2136x, and ADSP-2116x SIMD SHARC processors, as shown in Figure 2 and detailed in the following sections.

SIMD Computational Engine

The processors contain two computational processing elements that operate as a single-instruction, multiple-data (SIMD) engine. The processing elements are referred to as PEX and PEY, and each contains an ALU, multiplier, shifter, and register file. PEX is always active, and PEY may be enabled by setting the PEYEN mode bit in the MODE1 register. When this mode is enabled, the same instruction is executed in both processing elements, but each processing element operates on different data. This architecture is efficient at executing math intensive DSP algorithms.

Entering SIMD mode also has an effect on the way data is transferred between memory and the processing elements. When in SIMD mode, twice the data bandwidth is required to sustain computational operation in the processing elements. Because of this requirement, entering SIMD mode also doubles the bandwidth between memory and the processing elements. When using the DAGs to transfer data in SIMD mode, two data values are transferred with each access of memory or the register file.

Independent, Parallel Computation Units

Within each processing element is a set of computational units. The computational units consist of an arithmetic/logic unit (ALU), multiplier, and shifter. These units perform all operations in a single cycle. The three units within each processing element are arranged in parallel, maximizing computational throughput. Single multifunction instructions execute parallel ALU and multiplier operations. In SIMD mode, the parallel ALU and multiplier operations occur in both processing elements. These computation units support IEEE 32-bit single-precision floating-point, 40-bit extended precision floating-point, and 32-bit fixed-point data formats.

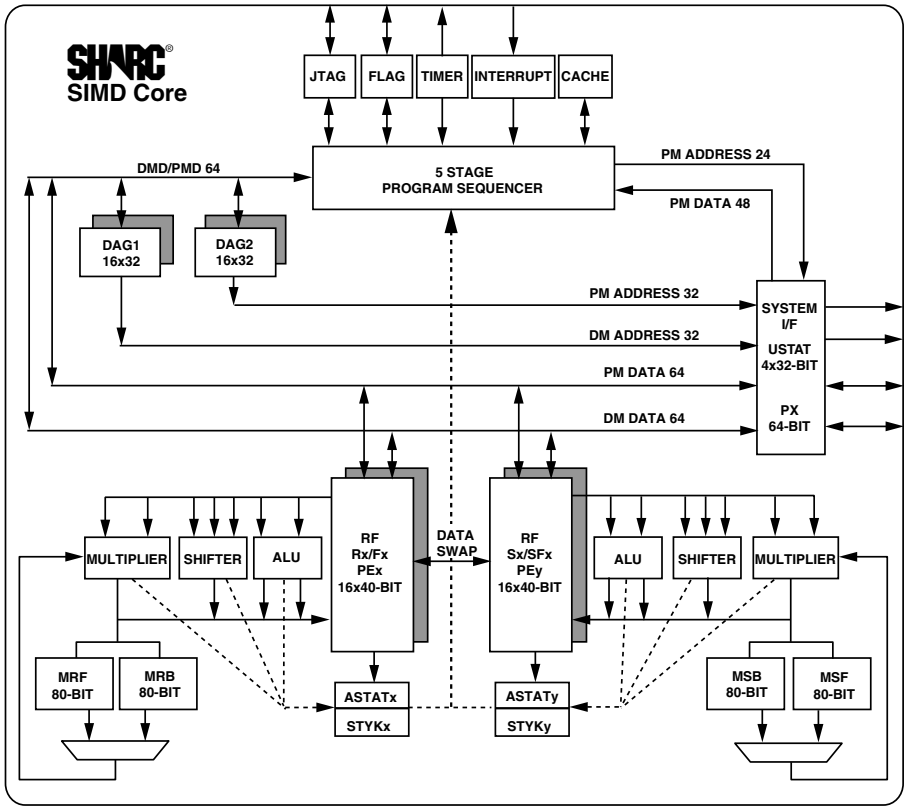

Figure 2. SHARC Core Block Diagram

Table 4. ADSP-21375 Internal Memory Space

IOP Registers 0x0000 0000–0x0003 FFFF			
Long Word (64 bits)	**Extended Precision Normal or Instruction Word (48 bits)**	**Normal Word (32 bits)**	**Short Word (16 bits)**
BLOCK 0 ROM 0x0004 0000–0x0004 3FFF	BLOCK 0 ROM 0x0008 0000–0x0008 5554	BLOCK 0 ROM 0x0008 0000–0x0008 7FFF	BLOCK 0 ROM 0x0010 0000–0x0010 FFFF
Reserved 0x0004 4000–0x0004 BFFF	Reserved 0x0008 5555–0x0008 FFFF	Reserved 0x0008 8000–0x0009 7FFF	Reserved 0x0011 0000–0x0012 FFFF
BLOCK 0 RAM 0x0004 C000–0x0004 C7FF	BLOCK 0 RAM 0x0009 0000–0x0009 0AA9	BLOCK 0 RAM 0x0009 8000–0x0009 8FFF	BLOCK 0 RAM 0x0013 0000–0x0013 1FFF
Reserved 0x0004 C800–0x0004 FFFF	Reserved 0x0009 0AAA–0x0009 FFFF	Reserved 0x0009 9000–0x0009 FFFF	Reserved 0x0013 2000–0x0013 FFFF
BLOCK 1 ROM 0x0005 0000–0x0005 3FFF	BLOCK 1 ROM 0x000A 0000–0x000A 5554	BLOCK 1 ROM 0x000A 0000–0x000A 7FFF	BLOCK 1 ROM 0x0014 0000–0x0014 FFFF
Reserved 0x0005 4000–0x0005 BFFF	Reserved 0x000A 5555–0x000A FFFF	Reserved 0x000A 8000–0x000B 7FFF	Reserved 0x0015 0000–0x0016 FFFF
BLOCK 1 RAM 0x0005 C000–0x0005 C7FF	BLOCK 1 RAM 0x000B 0000–0x000B 0AA9	BLOCK 1 RAM 0x000B 8000–0x000B 8FFF	BLOCK 1 RAM 0x0017 0000–0x0017 1FFF
Reserved 0x0005 C800–0x0005 FFFF	Reserved 0x000B 0AAA–0x000B FFFF	Reserved 0x000B 9000–0x000B FFFF	Reserved 0x0017 2000–0x0017 FFFF
BLOCK 2 RAM 0x0006 0000–0x0006 07FF	BLOCK 2 RAM 0x000C 0000–0x000C 0AA9	BLOCK 2 RAM 0x000C 0000–0x000C 0FFF	BLOCK 2 RAM 0x0018 0000–0x0018 1FFF
Reserved 0x0006 0800–0x0006 FFFF	Reserved 0x000C 0AAA–0x000D FFFF	Reserved 0x000C 1000–0x000D FFFF	Reserved 0x0018 2000–0x001B FFFF
BLOCK 3 RAM 0x0007 0000–0x0007 07FF	BLOCK 3 RAM 0x000E 0000–0x000E 0AA9	BLOCK 3 RAM 0x000E 0000–0x000E 0FFF	BLOCK 3 RAM 0x001C 0000–0x001C 1FFF
Reserved 0x0007 0800–0x0007 FFFF	Reserved 0x000E 0AAA–0x000F FFFF	Reserved 0x000E 1000–0x000F FFFF	Reserved 0x001C 2000–0x001F FFFF

SDRAM Controller

The SDRAM controller provides an interface to up to four separate banks of industry-standard SDRAM devices or DIMMs. Fully compliant with the SDRAM standard, each bank has its own memory select line ($\overline{MS0}$–$\overline{MS3}$), and can be configured to contain between 16M bytes and 256M bytes of memory. SDRAM external memory address space is shown in Table 5.

The controller maintains all of the banks as a contiguous address space so that the processor sees this as a single address space, even if different size devices are used in the different banks.

A set of programmable timing parameters is available to configure the SDRAM banks to support slower memory devices. The memory banks can be configured as 16 bits wide or as 32 bits wide. The SDRAM controller address, data, clock, and command pins can drive loads up to 30 pF. For larger memory systems, the SDRAM controller external buffer timing should be selected and external buffering should be provided so that the load on the SDRAM controller pins does not exceed 30 pF.

Table 5. External Memory for SDRAM Addresses

Bank	Size in Words	Address Range
Bank 0	62M	0x0020 0000–0x03FF FFFF
Bank 1	64M	0x0400 0000–0x07FF FFFF
Bank 2	64M	0x0800 0000–0x0BFF FFFF
Bank 3	64M	0x0C00 0000–0x0FFF FFFF

Note that the external memory bank addresses shown in Table 5 are for normal word accesses. If 48-bit instructions are placed in any such bank (with two instructions packed into three 32-bit locations), then care must be taken to map data buffers in the same bank. For example, if 2k instructions are placed starting at the bank 0 base address (0x0020 0000), then the data buffers can be placed starting at an address that is offset by 3k words (0x0020 0C00).

External Memory Code Execution

The program sequencer can execute code directly from external memory bank 0 (SRAM, SDRAM) over the 48-bit external port data bus (EPD). This allows a reduction in internal memory size, thereby reducing the die area. Because instructions on the

Serial ports operate in five modes:

- Standard DSP serial mode
- Multichannel (TDM) mode with support for packed I²S mode
- I²S mode
- Packed I²S mode
- Left-justified sample pair mode

Left-justified sample pair mode is a mode where in each frame sync cycle two samples of data are transmitted/received—one sample on the high segment of the frame sync, the other on the low segment of the frame sync. Programs have control over various attributes of this mode.

Each of the serial ports supports the left-justified sample pair and I²S protocols (I²S is an industry-standard interface commonly used by audio codecs, ADCs, and DACs such as the Analog Devices AD183x family), with two data pins, allowing four left-justified sample pair or I²S channels (using two stereo devices) per serial port, with a maximum of up to 32 I²S channels. The serial ports permit little-endian or big-endian transmission formats and word lengths selectable from 3 bits to 32 bits. For the left-justified sample pair and I²S modes, data-word lengths are selectable between 8 bits and 32 bits. Serial ports offer selectable synchronization and transmit modes as well as optional μ-law or A-law companding selection on a per channel basis. Serial port clocks and frame syncs can be internally or externally generated.

The serial ports also contain frame sync error detection logic where the serial ports detect frame syncs that arrive early (for example frame syncs that arrive while the transmission/reception of the previous word is occurring). All the serial ports also share one dedicated error interrupt.

S/PDIF-Compatible Digital Audio Receiver/Transmitter

The ADSP-21371 S/PDIF receiver/transmitter has no separate DMA channels. It receives audio data in serial format and converts it into a biphase encoded signal. The serial data input to the receiver/transmitter can be formatted as left justified, I²S or right justified with word widths of 16, 18, 20, or 24 bits.

The serial data, clock, and frame sync inputs to the S/PDIF receiver/transmitter are routed through the signal routing unit (SRU). They can come from a variety of sources such as the SPORTs, external pins, the precision clock generators (PCGs), and are controlled by the SRU control registers.

The ADSP-21375 does not have an S/PDIF-compatible digital receiver/transmitter.

Input Data Port (IDP)

The IDP provides up to eight serial input channels—each with its own clock, frame sync, and data inputs. The eight channels are automatically multiplexed into a single 32-bit by eight-deep FIFO. Data is always formatted as a 64-bit frame and divided into two 32-bit words. The serial protocol is designed to receive audio channels in I²S, left-justified sample pair, or right-justified mode. One frame sync cycle indicates one 64-bit left/right pair, but data is sent to the FIFO as 32-bit words (that is, one-half of a frame at a time). The processor supports 24- and 32-bit I²S, 24- and 32-bit left-justified, and 24-, 20-, 18- and 16-bit right-justified formats.

Precision Clock Generator (PCG)

The precision clock generators (PCG) consist of four units, each of which generates a pair of signals (clock and frame sync) derived from a clock input signal. The units, A B, C, and D, are identical in functionality and operate independently of each other. The two signals generated by each unit are normally used as a serial bit clock/frame sync pair.

Digital Peripheral Interface (DPI)

The digital peripheral interface provides connections to two serial peripheral interface (SPI) ports, one universal asynchronous receiver-transmitter (UART), 12 flags, a 2-wire interface (TWI), and two general-purpose timers.

Serial Peripheral (Compatible) Interface

The ADSP-21371/ADSP-21375 SHARC processors contain two serial peripheral interface ports (SPIs). The SPI is an industry-standard synchronous serial link, enabling the SPI-compatible ports of the processors to communicate with other SPI compatible devices. The SPI consists of two data pins, one device select pin, and one clock pin. It is a full-duplex synchronous serial interface, supporting both master and slave modes. The SPI port can operate in a multimaster environment by interfacing with up to four other SPI-compatible devices, either acting as a master or slave device.

The SPI-compatible peripheral implementation also features programmable baud rates and clock phases and polarities. The SPI-compatible port uses open drain drivers to support a multimaster configuration and to avoid data contention.

UART Port

The processors provide a full-duplex Universal Asynchronous Receiver/Transmitter (UART) port, which is fully compatible with PC-standard UARTs. The UART port provides a simplified UART interface to other peripherals or hosts, supporting full-duplex, DMA-supported, asynchronous transfers of serial data. The UART also has multiprocessor communication capability using 9-bit address detection. This allows it to be used in multidrop networks through the RS-485 data interface standard. The UART port also includes support for 5 to 8 data bits, 1 or 2 stop bits, and none, even, or odd parity. The UART port supports two modes of operation:

- PIO (programmed I/O) – The processor sends or receives data by writing or reading I/O-mapped UART registers. The data is double-buffered on both transmit and receive.
- DMA (direct memory access) – The DMA controller transfers both transmit and receive data. This reduces the number and frequency of interrupts required to transfer data to and from memory. The UART has two dedicated

Power Supplies

The processors have separate power supply connections for the internal (V_{DDINT}), and external (V_{DDEXT}) power supplies. The internal supplies must meet the 1.2 V requirement. The external supply must meet the 3.3 V requirement. All external supply pins must be connected to the same power supply.

Target Board JTAG Emulator Connector

Analog Devices DSP Tools product line of JTAG emulators uses the IEEE 1149.1 JTAG test access port of the processor to monitor and control the target board processor during emulation. Analog Devices DSP Tools product line of JTAG emulators provides emulation at full processor speed, allowing inspection and modification of memory, registers, and processor stacks. The processor's JTAG interface ensures that the emulator will not affect target system loading
or timing.

For complete information on Analog Devices' SHARC DSP Tools product line of JTAG emulator operation, see the appropriate "Emulator Hardware User's Guide".

DEVELOPMENT TOOLS

Analog Devices supports its processors with a complete line of software and hardware development tools, including integrated development environments (which include CrossCore® Embedded Studio and/or VisualDSP++®), evaluation products, emulators, and a wide variety of software add-ins.

Integrated Development Environments (IDEs)

For C/C++ software writing and editing, code generation, and debug support, Analog Devices offers two IDEs.

The newest IDE, CrossCore Embedded Studio, is based on the Eclipse™ framework. Supporting most Analog Devices processor families, it is the IDE of choice for future processors, including multicore devices. CrossCore Embedded Studio seamlessly integrates available software add-ins to support real time operating systems, file systems, TCP/IP stacks, USB stacks, algorithmic software modules, and evaluation hardware board support packages. For more information visit www.analog.com/cces.

The other Analog Devices IDE, VisualDSP++, supports processor families introduced prior to the release of CrossCore Embedded Studio. This IDE includes the Analog Devices VDK real time operating system and an open source TCP/IP stack. For more information visit www.analog.com/visualdsp. Note that VisualDSP++ will not support future Analog Devices processors.

EZ-KIT Lite Evaluation Board

For processor evaluation, Analog Devices provides wide range of EZ-KIT Lite® evaluation boards. Including the processor and key peripherals, the evaluation board also supports on-chip emulation capabilities and other evaluation and development features. Also available are various EZ-Extenders®, which are daughter cards delivering additional specialized functionality, including audio and video processing. For more information visit www.analog.com and search on "ezkit" or "ezextender".

EZ-KIT Lite Evaluation Kits

For a cost-effective way to learn more about developing with Analog Devices processors, Analog Devices offer a range of EZ-KIT Lite evaluation kits. Each evaluation kit includes an EZ-KIT Lite evaluation board, directions for downloading an evaluation version of the available IDE(s), a USB cable, and a power supply. The USB controller on the EZ-KIT Lite board connects to the USB port of the user's PC, enabling the chosen IDE evaluation suite to emulate the on-board processor in-circuit. This permits the customer to download, execute, and debug programs for the EZ-KIT Lite system. It also supports in-circuit programming of the on-board Flash device to store user-specific boot code, enabling standalone operation. With the full version of CrossCore Embedded Studio or VisualDSP++ installed (sold separately), engineers can develop software for supported EZ-KITs or any custom system utilizing supported Analog Devices processors.

Software Add-Ins for CrossCore Embedded Studio

Analog Devices offers software add-ins which seamlessly integrate with CrossCore Embedded Studio to extend its capabilities and reduce development time. Add-ins include board support packages for evaluation hardware, various middleware packages, and algorithmic modules. Documentation, help, configuration dialogs, and coding examples present in these add-ins are viewable through the CrossCore Embedded Studio IDE once the add-in is installed.

Board Support Packages for Evaluation Hardware

Software support for the EZ-KIT Lite evaluation boards and EZ-Extender daughter cards is provided by software add-ins called Board Support Packages (BSPs). The BSPs contain the required drivers, pertinent release notes, and select example code for the given evaluation hardware. A download link for a specific BSP is located on the web page for the associated EZ-KIT or EZ-Extender product. The link is found in the *Product Download* area of the product web page.

Middleware Packages

Analog Devices separately offers middleware add-ins such as real time operating systems, file systems, USB stacks, and TCP/IP stacks. For more information see the following web pages:

- www.analog.com/ucos3
- www.analog.com/ucfs
- www.analog.com/ucusbd
- www.analog.com/lwip

Algorithmic Modules

To speed development, Analog Devices offers add-ins that perform popular audio and video processing algorithms. These are available for use with both CrossCore Embedded Studio and VisualDSP++. For more information visit www.analog.com and search on "Blackfin software modules" or "SHARC software modules".

PIN FUNCTION DESCRIPTIONS

The following symbols appear in the Type column of Table 9:
A = asynchronous, I = input, O = output, S = synchronous,
(A/D) = active drive, (O/D) = open drain, and T = three-state,
(pd) = pull-down resistor, (pu) = pull-up resistor.

Table 9. Pin Descriptions

Name	Type	State During and After Reset	Description
$ADDR_{23-0}$	O/T (pu)	Pulled high/ driven low	**External Address.** The processor outputs addresses for external memory and peripherals on these pins.
$DATA_{31-0}$	I/O (pu)	Pulled high/ pulled high	**External Data.** The data pins can be multiplexed to support the external memory interface data (I/O), the PDAP (I) (PDAP for ADSP-21371), FLAGS (I/O) and PWM (O). After reset, all DATA pins are in EMIF mode and FLAG(0–3) pins are in FLAGS mode (default). When configured in the IDP_PDAP_CTL register, IDP channel 0 scans the external port data pins for parallel input data. PDAP over 16-bit external port DATA is not supported on the ADSP-21375 processor.
DAI $_P_{20-1}$	I/O with programmable (pu)[1]	Pulled high/ pulled high	**Digital Applications Interface Pins**. These pins provide the physical interface to the DAI SRU. The DAI SRU configuration registers define the combination of on-chip audio-centric peripheral inputs or outputs connected to the pin and to the pin's output enable. The configuration registers of these peripherals then determine the exact behavior of the pin. Any input or output signal present in the DAI SRU may be routed to any of these pins. The DAI SRU provides the connection from the serial ports, the S/PDIF module (ADSP-21371), IDP (2), and the PCGs (4), to the DAI_P20–1 pins. Pullups can be disabled via the DAI_PIN_PULLUP register.
DPI $_P_{14-1}$	I/O with programmable (pu)[1]	Pulled high/ pulled high	**Digital Peripheral Interface.** These pins provide the physical interface to the DPI SRU. The DPI SRU configuration registers define the combination of on-chip peripheral inputs or outputs connected to the pin and to the pin's output enable. The configuration registers of these peripherals then determines the exact behavior of the pin. Any input or output signal present in the DPI SRU may be routed to any of these pins. The DPI SRU provides the connection from the timers (2), SPIs (2), UART (1), flags (12), and general-purpose I/O (9) to the DPI_P14–1 pins. Pull-ups can be disabled via the DPI_PIN_PULLUP register.
ACK	I (pu)		**Memory Acknowledge.** External devices can deassert ACK (low) to add wait states to an external memory access. ACK is used by I/O devices, memory controllers, or other peripherals to hold off completion of an external memory access.
$\overline{RD}$	O/T (pu)	Pulled high/ driven high	**External Port Read Enable.** $\overline{RD}$ is asserted whenever the processor reads a word from external memory. $\overline{RD}$ has a 22.5 kΩ internal pull-up resistor.
$\overline{WR}$	O/T (pu)	Pulled high/ driven high	**External Port Write Enable.** $\overline{WR}$ is asserted when the processor writes a word to external memory. $\overline{WR}$ has a 22.5 kΩ internal pull-up resistor.
$\overline{SDRAS}$	O/T (pu)	Pulled high/ driven high	**SDRAM Row Address Strobe.** Connect to SDRAM's RAS pin. In conjunction with other SDRAM command pins, defines the operation for the SDRAM to perform.
$\overline{SDCAS}$	O/T (pu)	Pulled high/ driven high	**SDRAM Column Address Select.** Connect to SDRAM's CAS pin. In conjunction with other SDRAM command pins, defines the operation for the SDRAM to perform.
$\overline{SDWE}$	O/T (pu)	Pulled high/ driven high	**SDRAM Write Enable.** Connect to SDRAM's WE or W buffer pin.

PACKAGE INFORMATION

The information presented in Figure 3 provides details about the package branding for the ADSP-21371/ADSP-21375 processor. For a complete listing of product availability, see Ordering Guide on Page 56.

Figure 3. Typical Package Brand

Table 10. Package Brand Information

Brand Key	Field Description
t	Temperature Range
pp	Package Type
Z	RoHS Compliant Part
cc	See Ordering Guide
vvvvvv.x	Assembly Lot Code
n.n	Silicon Revision
yyww	Date Code

MAXIMUM POWER DISSIPATION

See Engineer-to-Engineer Note *"Estimating Power Dissipation for ADSP-2137x SHARC Processors"* (EE-318) for detailed thermal and power information regarding maximum power dissipation. For information on package thermal specifications, see Thermal Characteristics on Page 50.

ABSOLUTE MAXIMUM RATINGS

Stresses greater than those listed in Table 11 may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 11. Absolute Maximum Ratings

Parameter	Rating
Internal (Core) Supply Voltage (V_{DDINT})	–0.3 V to +1.5 V
External (I/O) Supply Voltage (V_{DDEXT})	–0.3 V to +4.6 V
Input Voltage –0.5 V to V_{DDEXT}	+0.5 V
Output Voltage Swing –0.5 V to V_{DDEXT}	+0.5 V

Table 11. Absolute Maximum Ratings (Continued)

Parameter	Rating
Load Capacitance	200 pF
Storage Temperature Range	–65°C to +150°C
Junction Temperature under Bias	125°C

ESD SENSITIVITY

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

TIMING SPECIFICATIONS

Use the exact timing information given. Do not attempt to derive parameters from the addition or subtraction of others. While addition or subtraction would yield meaningful results for an individual device, the values given in this data sheet reflect statistical variations and worst cases. Consequently, it is not meaningful to add parameters to derive longer times. See Figure 38 on Page 49 under Test Conditions for voltage reference levels.

Switching Characteristics specify how the processor changes its signals. Circuitry external to the processor must be designed for compatibility with these signal characteristics. Switching characteristics describe what the processor will do in a given circumstance. Use switching characteristics to ensure that any timing requirement of a device connected to the processor (such as memory) is satisfied.

Timing Requirements apply to signals that are controlled by circuitry external to the processor, such as the data input for a read operation. Timing requirements guarantee that the processor operates correctly with other devices.

Core Clock Requirements

The processor's internal clock (a multiple of CLKIN) provides the clock signal for timing internal memory, processor core, and serial ports. During reset, program the ratio between the processor's internal clock frequency and external (CLKIN) clock frequency with the CLK_CFG1–0 pins.

The processor's internal clock switches at higher frequencies than the system input clock (CLKIN). To generate the internal clock, the processor uses an internal phase-locked loop (PLL, see Figure 4). This PLL-based clocking minimizes the skew between the system clock (CLKIN) signal and the processor's internal clock.

Timer PWM_OUT Cycle Timing

The following timing specification applies to Timer0 and Timer1 in PWM_OUT (pulse-width modulation) mode. Timer signals are routed to the DPI_P14–1 pins through the DPI SRU. Therefore, the specifications provided below are valid at the DPI_P14–1 pins.

Table 19. Timer PWM_OUT Timing

Parameter		Min	Max	Unit
Switching Characteristic				
t_{PWMO}	Timer Pulse Width Output	$2 \times t_{PCLK} - 2$	$2 \times (2^{31} - 1) \times t_{PCLK}$	ns

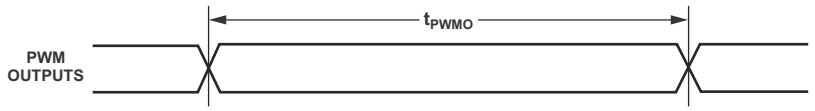

Figure 12. Timer PWM_OUT Timing

Timer WDTH_CAP Timing

The following timing specification applies to Timer0 and Timer1 in WDTH_CAP (pulse width count and capture) mode. Timer signals are routed to the DPI_P14–1 pins through the SRU. Therefore, the specifications provided below are valid at the DPI_P14–1 pins.

Table 20. Timer Width Capture Timing

Parameter		Min	Max	Unit
Timing Requirement				
t_{PWI}	Timer Pulse Width	$2 \times t_{PCLK}$	$2 \times (2^{31} - 1) \times t_{PCLK}$	ns

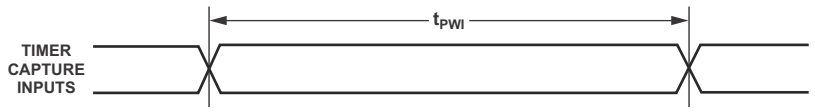

Figure 13. Timer Width Capture Timing

Precision Clock Generator (Direct Pin Routing)

This timing is only valid when the SRU is configured such that the precision clock generator (PCG) takes its inputs directly from the DAI pins (via pin buffers) and sends its outputs directly to the DAI pins. For the other cases, where the PCG's inputs and outputs are not directly routed to/from DAI pins (via pin buffers) there is no timing data available. All timing parameters and switching characteristics apply to external DAI pins (DAI_P01 through DAI_P20).

Table 22. Precision Clock Generator (Direct Pin Routing)

Parameter		1.0 V, 200 MHz Min	1.0 V, 200 MHz Max	1.2 V, 266 MHz Min	1.2 V, 266 MHz Max	Unit
Timing Requirements						
t_{PCGIP}	Input Clock Period	$t_{PCLK} \times 4$		$t_{PCLK} \times 4$		ns
t_{STRIG}	PCG Trigger Setup Before Falling Edge of PCG Input Clock	4.5		4.5		ns
t_{HTRIG}	PCG Trigger Hold After Falling Edge of PCG Input Clock	3		3		ns
Switching Characteristics						
t_{DPCGIO}	PCG Output Clock and Frame Sync Active Edge Delay After PCG Input Clock	2.5	12.8	2.5	10	ns
$t_{DTRIGCLK}$	PCG Output Clock Delay After PCG Trigger	$2.5 + ((2.5) \times t_{PCGIW})$	$12.8 + ((2.5) \times t_{PCGIW})$	$2.5 + ((2.5) \times t_{PCGIW})$	$10 + ((2.5) \times t_{PCGIW})$	ns
$t_{DTRIGFS}$	PCG Frame Sync Delay After PCG Trigger	$2.5 + ((2.5 + D - PH) \times t_{PCGIW})$	$12.8 + ((2.5 + D - PH) \times t_{PCGIW})$	$2.5 + ((2.5 + D - PH) \times t_{PCGIW})$	$10 + ((2.5 + D - PH) \times t_{PCGIW})$	ns
t_{PCGOW}[1]	Output Clock Period	$2 \times t_{PCGIW} - 1$		$2 \times t_{PCGIW} - 1$		ns

D = FSxDIV, PH = FSxPHASE. For more information, see the *ADSP-2137x SHARC Processor Hardware Reference*, "Precision Clock Generators" chapter.

[1] Normal mode of operation.

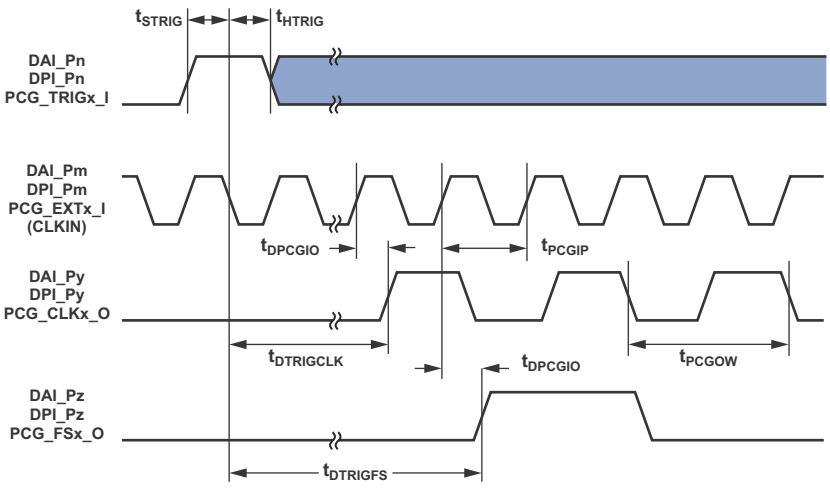

Figure 15. Precision Clock Generator (Direct Pin Routing)

Memory Write—Bus Master

Use these specifications for asynchronous interfacing to memories. Note that timing for ACK, DATA, $\overline{RD}$, $\overline{WR}$, and strobe timing parameters only apply to asynchronous access mode.

Table 26. Memory Write—Bus Master

Parameter		1.0 V, 200 MHz Min	1.0 V, 200 MHz Max	1.2 V, 266 MHz Min	1.2 V, 266 MHz Max	Unit
Timing Requirements						
t_{DAAK}	ACK Delay from Address, Selects[1, 2]		t_{SDCLK} – 11 + W		t_{SDCLK} – 10.1 + W	ns
t_{DSAK}	ACK Delay from $\overline{WR}$ Low [1, 3]		W – 7.35		W – 7.1	ns
Switching Characteristics						
t_{DAWH}	Address, Selects to $\overline{WR}$ Deasserted[2]	t_{SDCLK} – 4.3 + W		t_{SDCLK} – 3.6 + W		ns
t_{DAWL}	Address, Selects to $\overline{WR}$ Low[2]	t_{SDCLK} – 2.7		t_{SDCLK} – 2.7		ns
t_{WW}	$\overline{WR}$ Pulse Width	W – 1.3		W – 1.3		ns
t_{DDWH}	Data Setup Before $\overline{WR}$ High	t_{SDCLK} – 3.0 + W		t_{SDCLK} – 3.0 + W		ns
t_{DWHA}	Address Hold After $\overline{WR}$ Deasserted	H + 0.15		H + 0.15		ns
t_{DWHD}	Data Hold After $\overline{WR}$ Deasserted	H + 0.02		H + 0.02		ns
t_{DATRWH}	Data Disable After $\overline{WR}$ Deasserted[4]	t_{SDCLK} – 1.37 + H	t_{SDCLK} + 10.7+ H	t_{SDCLK} – 1.37 + H	t_{SDCLK} + 4.9+ H	ns
t_{WWR}	$\overline{WR}$ High to $\overline{WR}$, $\overline{RD}$ Low	t_{SDCLK} – 1.5+ H		t_{SDCLK} – 1.5+ H		ns
t_{DDWR}	Data Disable Before $\overline{RD}$ Low	$2t_{SDCLK}$ – 12		$2t_{SDCLK}$ – 5.1		ns
t_{WDE}	$\overline{WR}$ Low to Data Enabled	t_{SDCLK} – 4.1		t_{SDCLK} – 4.1		ns

W = (number of wait states specified in AMICTLx register) × t_{SDCLK}, H = (number of hold cycles specified in AMICTLx register) × t_{SDCLK}

[1] ACK delay/setup: System must meet t_{DAAK}, or t_{DSAK}, for deassertion of ACK (low). For asynchronous assertion of ACK (high) user must meet t_{DAAK} or t_{DSAK}.
[2] The falling edge of $\overline{MSx}$ is referenced.
[3] Note that timing for ACK, DATA, $\overline{RD}$, $\overline{WR}$, and strobe timing parameters only applies to asynchronous access mode.
[4] See Test Conditions on Page 49 for calculation of hold times given capacitive and dc loads.

Serial Ports

To determine whether communication is possible between two devices at clock speed n, the following specifications must be confirmed: 1) frame sync delay and frame sync setup and hold, 2) data delay and data setup and hold, and 3) serial clock (SCLK) width.

Serial port signals are routed to the DAI_P20–1 pins using the SRU. Therefore, the timing specifications provided below are valid at the DAI_P20–1 pins.

Table 27. Serial Ports—External Clock

Parameter		1.0 V, 200 MHz Min	1.0 V, 200 MHz Max	1.2 V, 266 MHz Min	1.2 V, 266 MHz Max	Unit
Timing Requirements						
t_{SFSE}[1]	Frame Sync Setup Before SCLK (Externally Generated Frame Sync in either Transmit or Receive Mode)	2.8		2.5		ns
t_{HFSE}[1]	Frame Sync Hold After SCLK (Externally Generated Frame Sync in either Transmit or Receive Mode)	2.5		2.5		ns
t_{SDRE}[1]	Receive Data Setup Before Receive SCLK	3.1		2.5		ns
t_{HDRE}[1]	Receive Data Hold After SCLK	2.5		2.5		ns
t_{SCLKW}	SCLK Width	$(t_{PCLK} \times 4) \div 2 - 1.5$		$(t_{PCLK} \times 4) \div 2 - 1.5$		ns
t_{SCLK}	SCLK Period	$t_{PCLK} \times 4$		$t_{PCLK} \times 4$		ns
Switching Characteristics						
t_{DFSE}[2]	Frame Sync Delay After SCLK (Internally Generated Frame Sync in either Transmit or Receive Mode)		13.5		10.5	ns
t_{HOFSE}[2]	Frame Sync Hold After SCLK (Internally Generated Frame Sync in either Transmit or Receive Mode)	2		2		ns
t_{DDTE}[2]	Transmit Data Delay After Transmit SCLK		13.9		11	ns
t_{HDTE}[2]	Transmit Data Hold After Transmit SCLK	2		2		ns

[1] Referenced to sample edge.
[2] Referenced to drive edge.

Parallel Data Acquisition Port (PDAP)

The timing requirements for the PDAP are provided in Table 32. PDAP is the parallel mode operation of Channel 0 of the IDP. For details on the operation of the PDAP, see the PDAP chapter of the *ADSP-2137x SHARC Processor Hardware Reference*.

Note that the 20-bits of external PDAP data can be provided through the external port DATA31–12 pins. On the ADSP-21375 processors, PDAP can not be multiplexed on the external port (since only DATA15–0). Use the SRU DAI instead.

Table 32. Parallel Data Acquisition Port (PDAP)

Parameter		Min	Max	Unit
Timing Requirements				
$t_{SPCLKEN}$[1]	PDAP_CLKEN Setup Before PDAP_CLK Sample Edge	2.5		ns
$t_{HPCLKEN}$[1]	PDAP_CLKEN Hold After PDAP_CLK Sample Edge	2.5		ns
t_{PDSD}[1]	PDAP_DAT Setup Before Serial Clock PDAP_CLK Sample Edge	3.85		ns
t_{PDHD}[1]	PDAP_DAT Hold After Serial Clock PDAP_CLK Sample Edge	2.5		ns
t_{PDCLKW}	Clock Width	$(t_{PCLK} \times 4) \div 2 - 3$		ns
t_{PDCLK}	Clock Period	$t_{PCLK} \times 4$		ns
Switching Characteristics				
t_{PDHLDD}	Delay of PDAP Strobe After Last PDAP_CLK Capture Edge for a Word	$2 \times t_{PCLK} + 3$		ns
t_{PDSTRB}	PDAP Strobe Pulse Width	$2 \times t_{PCLK} - 1$		ns

[1] Data source pins are DATA31–12 or DAI pins. Source pins for serial clock and frame sync are: 1) DATA11–10 pins, 2) DAI pins.

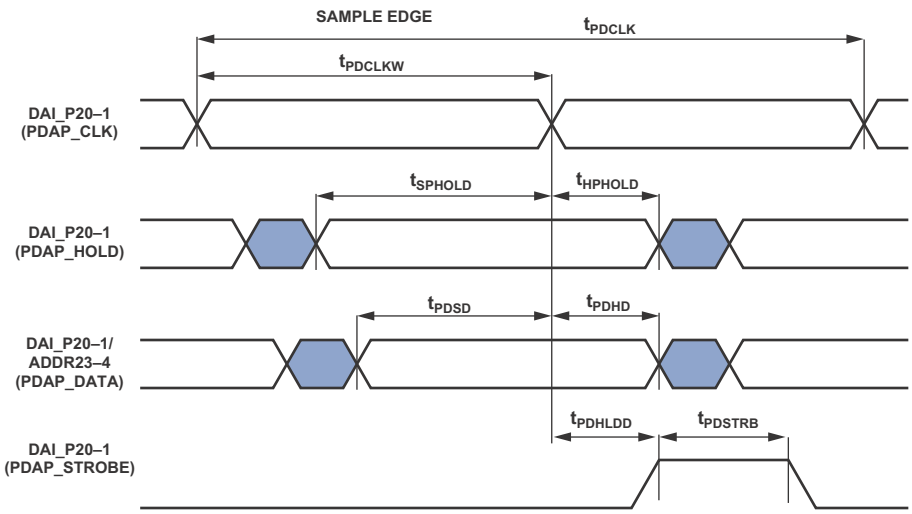

Figure 24. PDAP Timing

Pulse-Width Modulation Generators (PWM)

For the ADSP-21371, the following timing specifications apply when the DATA31–16 pins are configured as PWM.

Pulse-width modulation generator information does not apply to the ADSP-21375.

Table 33. Pulse-Width Modulation (PWM) Timing

Parameter		Min	Max	Unit
Switching Characteristics				
t_{PWMW}	PWM Output Pulse Width	$t_{PCLK} - 2.5$	$(2^{16} - 2) \times t_{PCLK}$	ns
t_{PWMP}	PWM Output Period	$2 \times t_{PCLK} - 2.5$	$(2^{16} - 1) \times t_{PCLK}$	ns

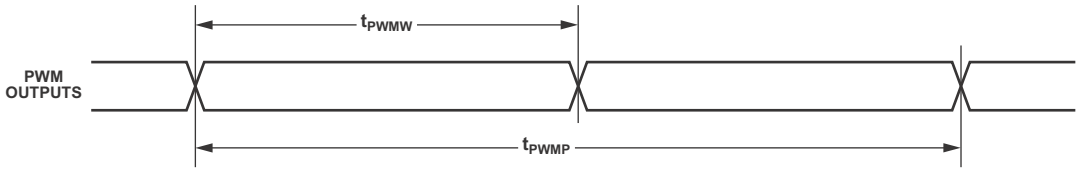

Figure 25. PWM Timing

S/PDIF Transmitter

For the ADSP-21371, serial data input to the S/PDIF transmitter can be formatted as left-justified, I²S, or right-justified with word widths of 16-, 18-, 20-, or 24-bits. The following sections provide timing for the transmitter.

S/PDIF Transmitter-Serial Input Waveforms

Figure 26 shows the right-justified mode. LRCLK is high for the left channel and low for the right channel. Data is valid on the rising edge of serial clock. The MSB is delayed 12-bit clock periods (in 20-bit output mode) or 16-bit clock periods (in 16-bit output mode) from an LRCLK transition, so that when there are 64 serial clock periods per LRCLK period, the LSB of the data will be right-justified to the next LRCLK transition.

S/PDIF transmitter information does not apply to the ADSP-21375.

Figure 27 shows the default I²S-justified mode. LRCLK is low for the left channel and high for the right channel. Data is valid on the rising edge of serial clock. The MSB is left-justified to an LRCLK transition but with a single serial clock period delay.

Figure 28 shows the left-justified mode. LRCLK is high for the left channel and low for the right channel. Data is valid on the rising edge of serial clock. The MSB is left-justified to an LRCLK transition with no MSB delay.

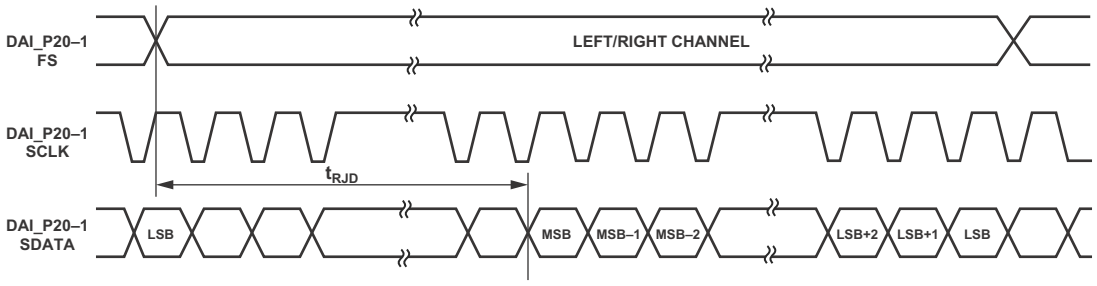

Figure 26. Right-Justified Mode

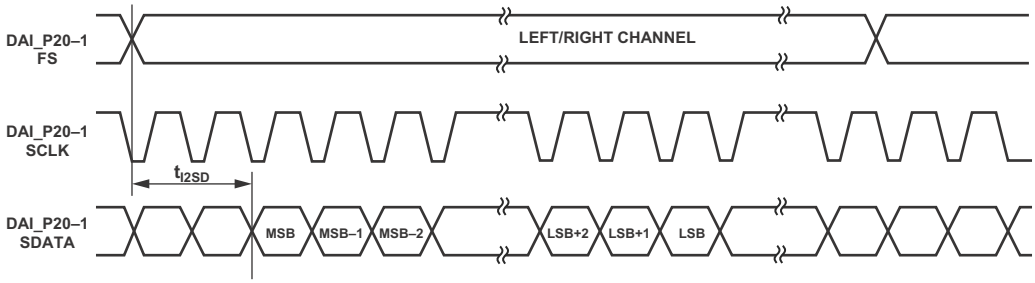

Figure 27. I²S-Justified Mode

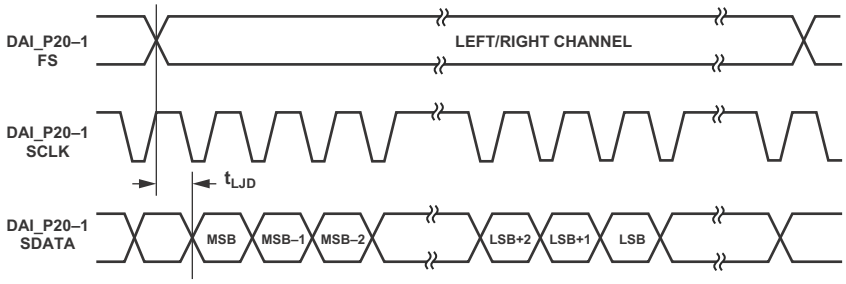

Figure 28. Left-Justified Mode

SPI Interface—Master

The processor contains two SPI ports. Both primary and secondary are available through DPI only. The timing provided in Table 37 and Table 38 applies to both.

Table 37. SPI Interface Protocol—Master Switching and Timing Specifications

Parameter		Min	Max	Unit
Timing Requirements				
t_{SSPIDM}	Data Input Valid To SPICLK Edge (Data Input Setup Time)	8.2		ns
t_{HSPIDM}	SPICLK Last Sampling Edge To Data Input Not Valid	2		ns
Switching Characteristics				
$t_{SPICLKM}$	Serial Clock Cycle	$8 \times t_{PCLK} - 2$		ns
t_{SPICHM}	Serial Clock High Period	$4 \times t_{PCLK} - 2$		ns
t_{SPICLM}	Serial Clock Low Period	$4 \times t_{PCLK} - 2$		ns
$t_{DDSPIDM}$	SPICLK Edge to Data Out Valid (Data Out Delay Time)		2.5	ns
$t_{HDSPIDM}$	SPICLK Edge to Data Out Not Valid (Data Out Hold Time)	$4 \times t_{PCLK} - 2$		ns
t_{SDSCIM}	DPI Pin (SPI Device Select) Low to First SPICLK Edge	$4 \times t_{PCLK} - 2$		ns
t_{HDSM}	Last SPICLK Edge to DPI Pin (SPI Device Select) High	$4 \times t_{PCLK} - 2$		ns
t_{SPITDM}	Sequential Transfer Delay	$4 \times t_{PCLK} - 1$		ns

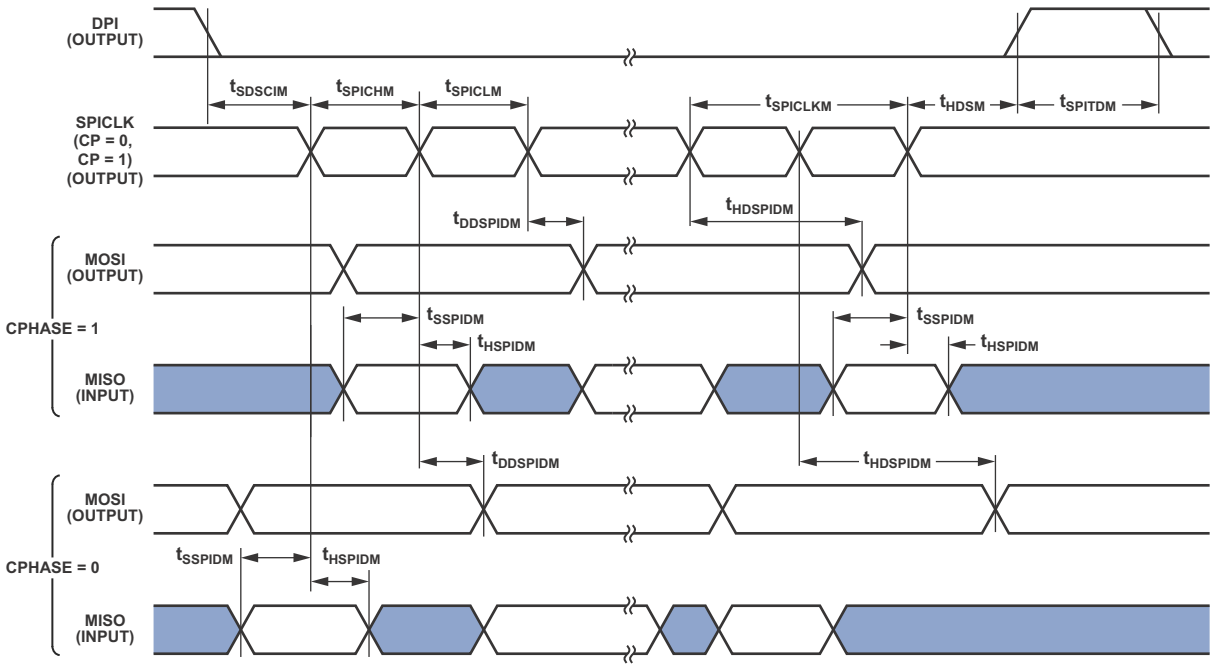

Figure 31. SPI Master Timing

TWI Controller Timing

Table 40 and Figure 34 provide timing information for the TWI interface. Input signals (SCL, SDA) are routed to the DPI_P14–1 pins using the SRU. Therefore, the timing specifications provided below are valid at the DPI_P14–1 pins.

Table 40. Characteristics of the SDA and SCL Bus Lines for F/S-Mode TWI Bus Devices[1]

Parameter		Standard Mode		Fast Mode		Unit
		Min	Max	Min	Max	
f_{SCL}	SCL Clock Frequency	0	100	0	400	kHz
t_{HDSTA}	Hold Time (repeated) Start Condition. After This Period, the First Clock Pulse is Generated.	4.0		0.6		µs
t_{LOW}	Low Period of the SCL Clock	4.7		1.3		µs
t_{HIGH}	High Period of the SCL Clock	4.0		0.6		µs
t_{SUSTA}	Setup Time for a Repeated Start Condition	4.7		0.6		µs
t_{HDDAT}	Data Hold Time for TWI-Bus Devices	0		0		µs
t_{SUDAT}	Data Setup Time	250		100		ns
t_{SUSTO}	Setup Time for Stop Condition	4.0		0.6		µs
t_{BUF}	Bus Free Time Between a Stop and Start Condition	4.7		1.3		µs
t_{SP}	Pulse Width of Spikes Suppressed By the Input Filter	N/A	N/A	0	50	ns

[1] All values referred to V_{IHmin} and V_{ILmax} levels. For more information, see Electrical Characteristics on page 17.

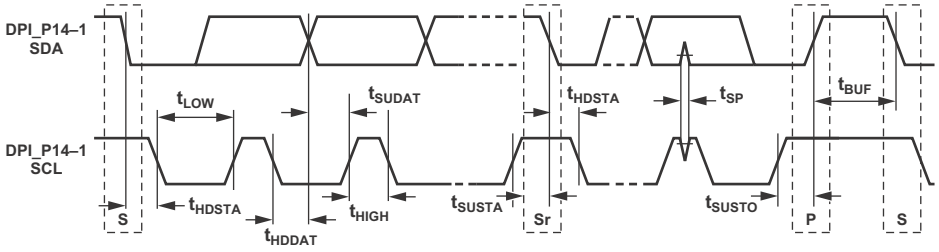

Figure 34. Fast and Standard Mode Timing on the TWI Bus

JTAG Test Access Port and Emulation

Table 41. JTAG Test Access Port and Emulation

Parameter		Min	Max	Unit
Timing Requirements				
t_{TCK}	TCK Period	t_{CK}		ns
t_{STAP}	TDI, TMS Setup Before TCK High	5		ns
t_{HTAP}	TDI, TMS Hold After TCK High	6		ns
t_{SSYS}[1]	System Inputs Setup Before TCK High	7		ns
t_{HSYS}[1]	System Inputs Hold After TCK High	18		ns
t_{TRSTW}	$\overline{\text{TRST}}$ Pulse Width	$4 \times t_{CK}$		ns
Switching Characteristics				
t_{DTDO}	TDO Delay from TCK Low		7	ns
t_{DSYS}[2]	System Outputs Delay After TCK Low		$t_{CK} \div 2 + 7$	ns

[1] System Inputs = ADDR15–0, CLKCFG1–0, $\overline{\text{RESET}}$, BOOT_CFG1–0, DAI_Px, and FLAG3–0.
[2] System Outputs = DAI_Px, ADDR15–0, $\overline{\text{RD}}$, $\overline{\text{WR}}$, FLAG3–0, $\overline{\text{EMU}}$, and ALE.

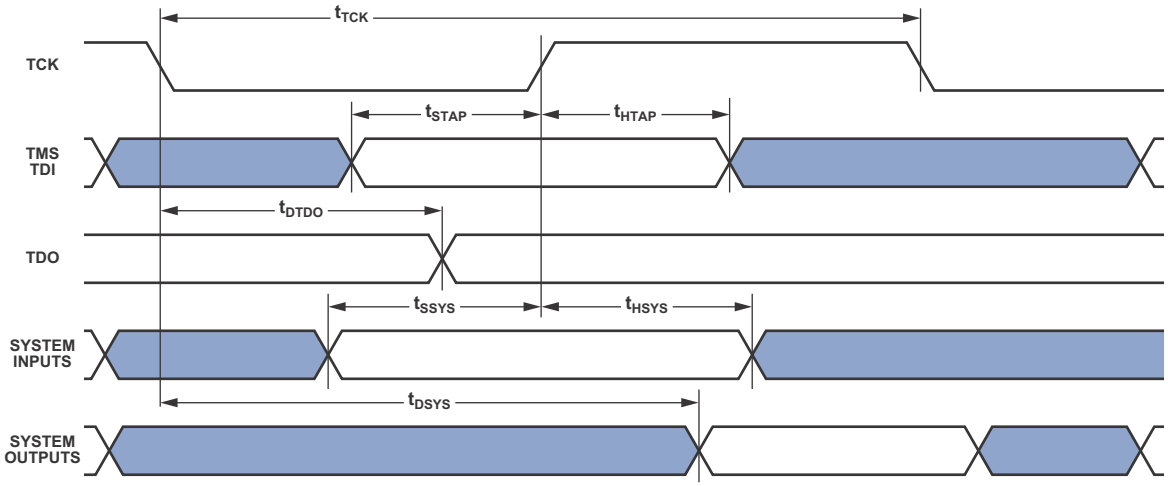

Figure 35. IEEE 1149.1 JTAG Test Access Port

OUTPUT DRIVE CURRENTS

Figure 36 shows typical I-V characteristics for the output drivers of the processors. The curves represent the current drive capability of the output drivers as a function of output voltage.

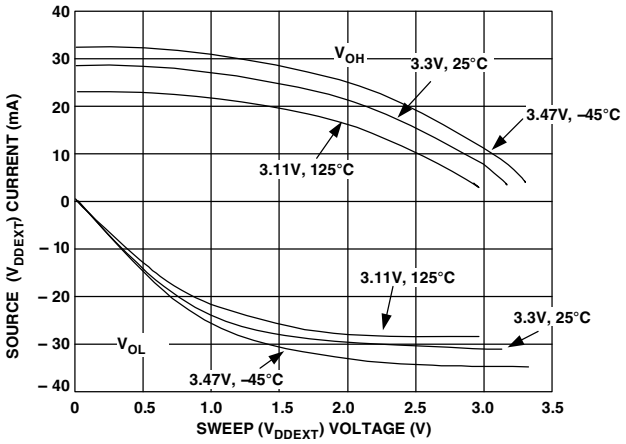

Figure 36. Typical Drive at Junction Temperature

TEST CONDITIONS

The ac signal specifications (timing parameters) appear in Table 15 on Page 22 through Table 41 on Page 48. These include output disable time, output enable time, and capacitive loading. The timing specifications for the SHARC apply for the voltage reference levels in Figure 37.

Timing is measured on signals when they cross the 1.5 V level as described in Figure 38. All delays (in nanoseconds) are measured between the point that the first signal reaches 1.5 V and the point that the second signal reaches 1.5 V.

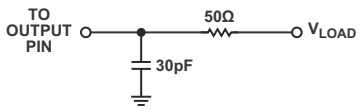

Figure 37. Equivalent Device Loading for AC Measurements (Includes All Fixtures)

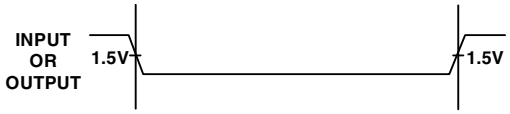

Figure 38. Voltage Reference Levels for AC Measurements

CAPACITIVE LOADING

Output delays and holds are based on standard capacitive loads: 30 pF on all pins (see Figure 37). Figure 41 shows graphically how output delays and holds vary with load capacitance. The graphs of Figure 39, Figure 40, and Figure 41 may not be linear outside the ranges shown for Typical Output Delay vs. Load Capacitance and Typical Output Rise Time (20% to 80%, V = Min) vs. Load Capacitance.

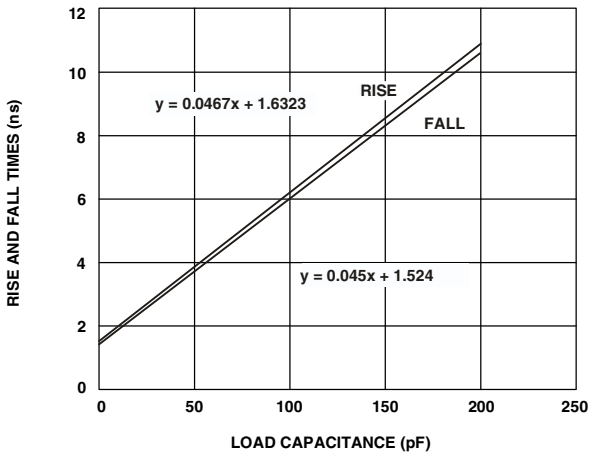

Figure 39. Typical Output Rise/Fall Time (20% to 80%, V_{DDEXT} = Max)

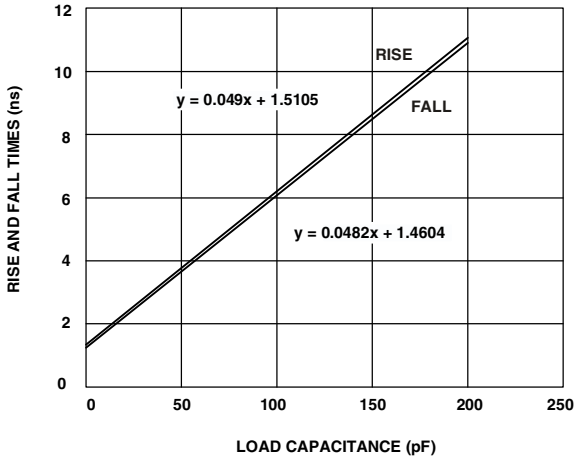

Figure 40. Typical Output Rise/Fall Time (20% to 80%, V_{DDEXT} = Min)

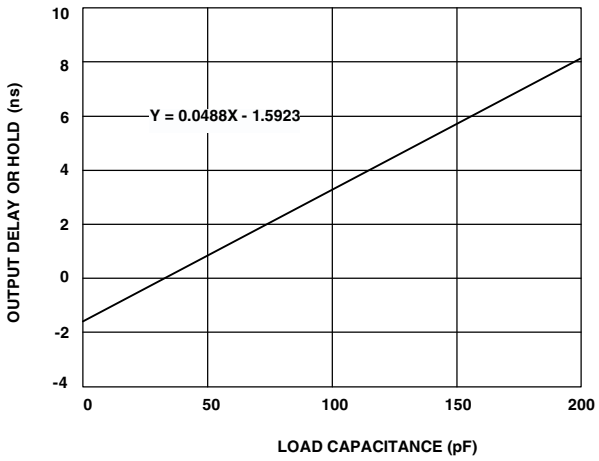

Figure 41. Typical Output Delay or Hold vs. Load Capacitance (at Ambient Temperature)

THERMAL CHARACTERISTICS

The processor is rated for performance over the temperature range specified in Operating Conditions on Page 16.

Table 42 airflow measurements comply with JEDEC standards JESD51-2 and JESD51-6 and the junction-to-board measurement complies with JESD51-8. Test board design complies with JEDEC standard JESD51-7 (LQFP_EP). The junction-to-case measurement complies with MIL- STD-883. All measurements use a 2S2P JEDEC test board.

To determine the junction temperature of the device while on the application PCB, use

$$T_J = T_{CASE} + (\Psi_{JT} \times P_D)$$

where:

T_J = junction temperature °C

T_{CASE} = case temperature (°C) measured at the top center of the package

Ψ_{JT} = junction-to-top (of package) characterization parameter is the Typical value from Table 42.

P_D = power dissipation

Values of θ_{JA} are provided for package comparison and PCB design considerations. θ_{JA} can be used for a first order approximation of T_J by the equation

$$T_J = T_A + (\theta_{JA} \times P_D)$$

where:

T_A = ambient temperature °C

Values of θ_{JC} are provided for package comparison and PCB design considerations when an external heatsink is required.

Values of θ_{JB} are provided for package comparison and PCB design considerations. Note that the thermal characteristics values provided in Table 42 are modeled values.

Table 42. Thermal Characteristics for 208-Lead LQFP E_PAD (With Exposed Pad Soldered to PCB)

Parameter	Condition	Typical	Unit
θ_{JA}	Airflow = 0 m/s	17.1	°C/W
θ_{JMA}	Airflow = 1 m/s	14.7	°C/W
θ_{JMA}	Airflow = 2 m/s	14.0	°C/W
θ_{JC}		9.6	°C/W
Ψ_{JT}	Airflow = 0 m/s	0.23	°C/W
Ψ_{JMT}	Airflow = 1 m/s	0.39	°C/W
Ψ_{JMT}	Airflow = 2 m/s	0.45	°C/W
Ψ_{JB}	Airflow = 0 m/s	11.5	°C/W
Ψ_{JMB}	Airflow = 1 m/s	11.2	°C/W
Ψ_{JMB}	Airflow = 2 m/s	11.0	°C/W

Table 43. ADSP-21371, 208-Lead LQFP_EP Pin Assignment (Numerical by Lead Number) (Continued)

Pin No.	Signal	Pin No.	Signal	Pin No.	Signal	Pin No.	Signal
45	DATA5	97	ADDR19	149	DAI_P5 (SD1A)	201	$\overline{\text{RESETOUT}}$/ $\overline{\text{RUNRSTIN}}$
46	DATA2	98	ADDR20	150	V_{DDEXT}	202	$\overline{\text{RESET}}$
47	DATA3	99	ADDR21	151	GND	203	V_{DDEXT}
48	DATA0	100	ADDR23	152	V_{DDINT}	204	GND
49	DATA1	101	ADDR22	153	GND	205	DATA30
50	V_{DDEXT}	102	$\overline{\text{MS1}}$	154	V_{DDINT}	206	DATA31
51	GND	103	$\overline{\text{MS0}}$	155	GND	207	DATA29
52	V_{DDINT}	104	V_{DDINT}	156	V_{DDINT}	208	V_{DDINT}

Table 44. ADSP-21375, 208-Lead LQFP_EP Pin Assignment (Numerical by Lead Number) (Continued)

Pin No.	Signal	Pin No.	Signal	Pin No.	Signal	Pin No.	Signal
45	DATA5	97	ADDR19	149	DAI_P5 (SD1A)	201	$\overline{\text{RESETOUT}}$/ $\overline{\text{RUNRSTIN}}$
46	DATA2	98	ADDR20	150	V_{DDEXT}	202	$\overline{\text{RESET}}$
47	DATA3	99	ADDR21	151	GND	203	V_{DDEXT}
48	DATA0	100	ADDR23	152	V_{DDINT}	204	GND
49	DATA1	101	ADDR22	153	GND	205	DATA30
50	V_{DDEXT}	102	$\overline{\text{MS1}}$	154	V_{DDINT}	206	DATA31
51	GND	103	$\overline{\text{MS0}}$	155	GND	207	DATA29
52	V_{DDINT}	104	V_{DDINT}	156	V_{DDINT}	208	V_{DDINT}