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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I²C, FlexIO, SPI, UART/USART
Peripherals	DMA, I²S, PWM, WDT
Number of I/O	32
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 15x16b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	36-XFBGA
Supplier Device Package	36-XFBGA (3.5x3.5)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mkl17z64vda4r

The system oscillator supports low frequency crystals (32 kHz to 40 kHz), high frequency crystals (1 MHz to 32 MHz), and ceramic resonators (1 MHz to 32 MHz). An external clock source, DC to 48 MHz, can be used as the system clock through the EXTAL0 pin. The external oscillator also supports a low speed external clock (32.768 kHz) on the RTC_CLKIN pin for use with the RTC.

For more details on the clock operations and configurations, see Reference Manual.

The following figure is a high level block diagram of the clock generation.

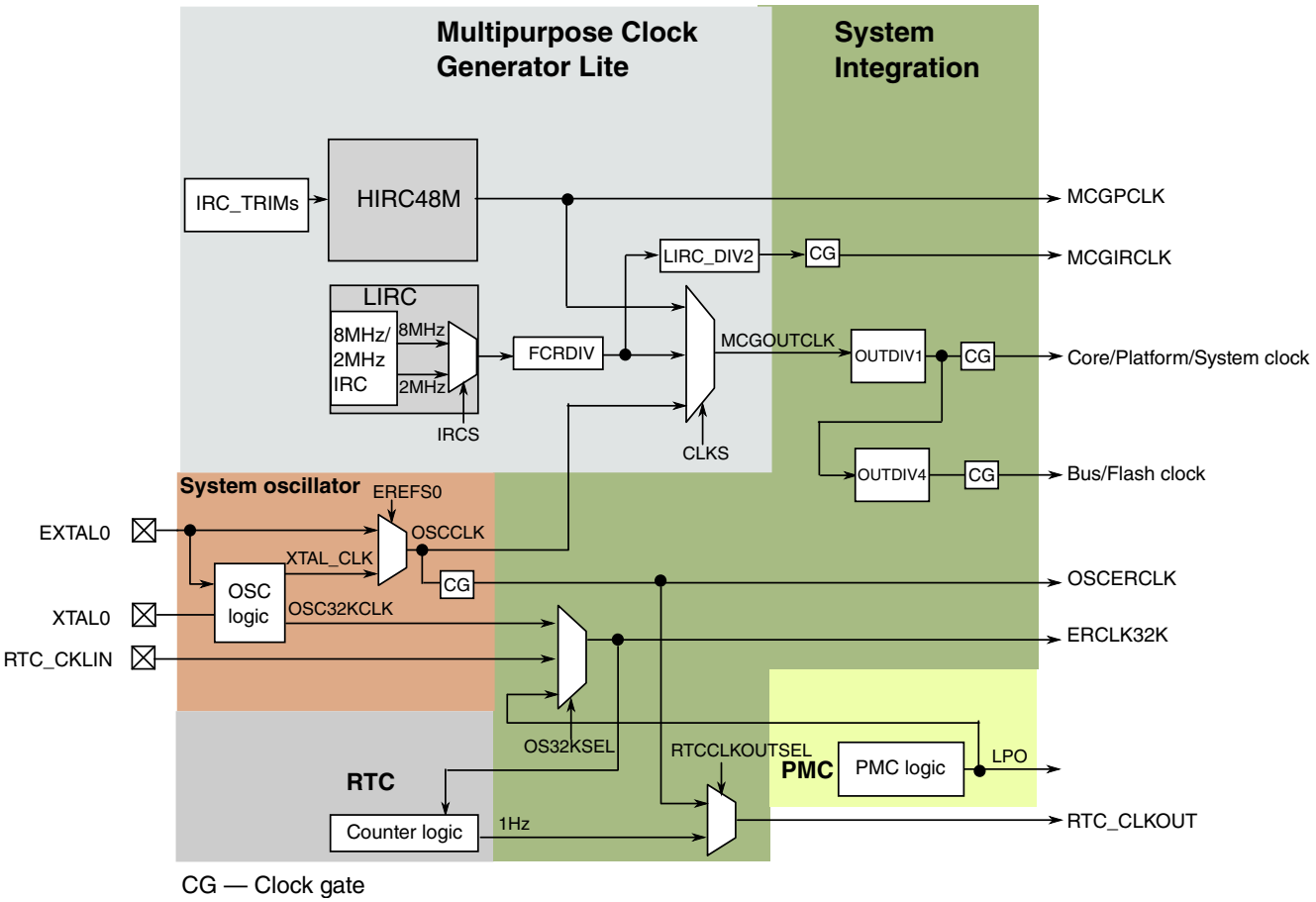


Figure 3. Clock block diagram

In order to provide flexibility, many peripherals can select from multiple clock sources for operation. This enables the peripheral to select a clock that will always be available during operation in various operational modes.

The following table summarizes the clocks associated with each module.

Table 4. Module clocks (continued)

Module	Bus interface clock	Internal clocks	I/O interface clocks
I^2C1	System Clock	—	I2C1_SCL
LPUART0, LPUART1	Bus clock	LPUART0 clock LPUART1 clock	—
UART2	Bus clock	—	—
FlexIO	Bus clock	FlexIO clock	—
Human-machine interfaces			
GPIO	Platform clock	—	—

2.1.7 Security

Security state can be enabled via programming flash configuration field (0x40e). After enabling device security, the SWD port cannot access the memory resources of the MCU, and ROM boot loader is also limited to access flash and not allowed to read out flash information via ROM boot loader commands.

Access interface	Secure state	Unsecure operation
SWD port	Cannot access memory source by SWD interface	The debugger can write to the Flash Mass Erase in Progress field of the MDM-AP Control register to trigger a mass erase (Erase All Blocks) command
ROM boot loader Interface (UART/I2C/SPI)	Limit access to the flash, cannot read out flash content	Send “FlashEraseAllUnsecureh" command or attempt to unlock flash security using the backdoor key

This device features 80-bit unique identification number, which is programmed in factory and loaded to SIM register after power-on reset.

2.1.8 Power management

The Power Management Controller (PMC) expands upon ARM’s operational modes of Run, Sleep, and Deep Sleep, to provide multiple configurable modes. These modes can be used to optimize current consumption for a wide range of applications. The WFI or WFE instruction invokes a Wait or a Stop mode, depending on the current configuration. For more information on ARM’s operational modes, See the ARM® Cortex User Guide.

Table 7. Wakeup source

LLWU pin	Module source or pin name
LLWU_P5	PTB0
LLWU_P6	PTC1
LLWU_P7	PTC3
LLWU_P8	PTC4
LLWU_P9	PTC5
LLWU_P10	PTC6
LLWU_P14	PTD4
LLWU_P15	PTD6
LLWU_M0IF	LPTMR0
LLWU_M1IF	CMP0
LLWU_M2IF	Reserved
LLWU_M3IF	Reserved
LLWU_M4IF	Reserved
LLWU_M5IF	RTC alarm
LLWU_M6IF	Reserved
LLWU_M7IF	RTC seconds

2.1.10 Debug controller

This device supports standard ARM 2-pin SWD debug port. It provides register and memory accessibility from the external debugger interface, basic run/halt control plus 2 breakpoints and 2 watchpoints.

It also supports trace function with the Micro Trace Buffer (MTB), which provides a simple execution trace capability for the Cortex-M0+ processor.

2.1.11 COP

The COP monitors internal system operation and forces a reset in case of failure. It can run from bus clock, LPO, 8/2 MHz internal oscillator or external crystal oscillator. Optional window mode can detect deviations in program flow or system frequency.

The COP has the following features:

- Support multiple clock input, 1 kHz clock(LPO), bus clock, 8/2 MHz internal reference clock, external crystal oscillator
- Can work in Stop/VLPS and Debug mode

- Configurable for short and long timeout values, the longest timeout is up to 262 seconds
- Support window mode

2.2 Peripheral features

The following sections describe the features of each peripherals of the chip.

2.2.1 BME

The Bit Manipulation Engine (BME) provides hardware support for atomic read-modify-write memory operations to the peripheral address space in Cortex-M0+ based microcontrollers. It reduces up to 30% of the code size and up to 9% of the cycles for bit-oriented operations to peripheral registers.

The BME supports unsigned bit field extract, load-and-set 1-bit, load-and-clear 1-bit, bit field insert, logical AND/OR/XOR operations with byte, halfword or word-sized data type.

2.2.2 DMA and DMAMUX

The DMA controller module enables fast transfers of data, which provides an efficient way to move blocks of data with minimal processor interaction. The DMA controller in this device implements four channels which can be routed from up to 63 DMA request sources through DMA MUX module. Some of the peripheral request sources have asynchronous DMA capability which can be used to wake MCU from Stop mode. The peripherals which have such capability include LPUART0, LPUART1, FlexIO, TPM0-TPM2, ADC0, CMP0, PORTA-PORTE. The DMA channel 0 and 1 can be periodically triggered by PIT via DMA MUX.

Main features are listed below:

- Dual-address transfers via 32-bit master connection to the system bus and data transfers in 8-, 16-, or 32-bit blocks
- Supports programmable source and destination address and transfer size, optional modulo addressing from 16 bytes to 256 KB
- Automatic updates of source and destination addresses

64 LQFP	36 XFBGA	32 QFN	48 QFN	64 MAPBGA	Pin name	Driver strength	Default status after POR	Pullup/ pulldown setting after POR	Slew rate after POR	Passive pin filter after POR	Open drain	Pin interrupt
46	B5	24	36	C8	PTC3/ LLWU_P7	HD	Hi-Z	—	FS	N	N	Y
47	—	—	—	E3	VSS	—	—	—	—	—	—	—
48	—	—	—	E4	VDD	—	—	—	—	—	—	—
49	A6	25	37	B8	PTC4/ LLWU_P8	HD	Hi-Z	—	FS	N	N	Y
50	A5	26	38	A8	PTC5/ LLWU_P9	ND	Hi-Z	—	FS	N	N	Y
51	B4	27	39	A7	PTC6/ LLWU_P10	ND	Hi-Z	—	FS	N	N	Y
52	A4	28	40	B6	PTC7	ND	Hi-Z	—	FS	N	N	Y
53	—	—	—	A6	PTC8	ND	Hi-Z	—	SS	N	N	Y
54	—	—	—	B5	PTC9	ND	Hi-Z	—	SS	N	N	Y
55	—	—	—	B4	PTC10	ND	Hi-Z	—	SS	N	N	Y
56	—	—	—	A5	PTC11	ND	Hi-Z	—	SS	N	N	Y
57	—	—	41	C3	PTD0	ND	Hi-Z	—	FS	N	N	Y
58	—	—	42	A4	PTD1	ND	Hi-Z	—	FS	N	N	Y
59	—	—	43	C2	PTD2	ND	Hi-Z	—	FS	N	N	Y
60	—	—	44	B3	PTD3	ND	Hi-Z	—	FS	N	N	Y
61	A3	29	45	A3	PTD4/ LLWU_P14	ND	Hi-Z	—	FS	N	N	Y
62	B3	30	46	C1	PTD5	ND	Hi-Z	—	FS	N	N	Y
63	B2	31	47	B2	PTD6/ LLWU_P15	HD	Hi-Z	—	FS	N	N	Y
64	A2	32	48	A2	PTD7	HD	Hi-Z	—	FS	N	N	Y

Properties	Abbreviation	Descriptions
Driver strength	ND	Normal drive
	HD	High drive
Default status after POR	Hi-Z	High impendence

Table continues on the next page...

4.3.2 System modules

Table 10. System signal descriptions

Chip signal name	Module signal name	Description	I/O
$\overline{\text{NMI}}$	—	Non-maskable interrupt **NOTE:** Driving the $\overline{\text{NMI}}$ signal low forces a non-maskable interrupt, if the $\overline{\text{NMI}}$ function is selected on the corresponding pin.	I
$\overline{\text{RESET}}$	—	Reset bidirectional signal	I/O
VDD	—	MCU power	I
VSS	—	MCU ground	I

Table 11. LLWU signal descriptions

Chip signal name	Module signal name	Description	I/O
LLWU_Pn	LLWU_Pn	Wakeup inputs (n = 5, 6, 7, 8, 9, 10, 14, 15)	I

4.3.3 Clock modules

Table 12. OSC signal descriptions

Chip signal name	Module signal name	Description	I/O
EXTAL0	EXTAL	External clock/Oscillator input	I
XTAL0	XTAL	Oscillator output	O

4.3.4 Analog

This table presents the signal descriptions of the ADC0 module.

Table 13. ADC0 signal descriptions

Chip signal name	Module signal name	Description	I/O
ADC0_DPn	DADP3–DADP0	Differential Analog Channel Inputs	I
ADC0_DMn	DADM3–DADM0	Differential Analog Channel Inputs	I
ADC0_SEn	AD*n*	Single-Ended Analog Channel Inputs	I
VREFH	V_{REFSH}	Voltage Reference Select High	I

Table continues on the next page...

Table 13. ADC0 signal descriptions (continued)

Chip signal name	Module signal name	Description	I/O
VREFL	V_{REFSL}	Voltage Reference Select Low	I
VDDA	V_{DDA}	Analog Power Supply	I
VSSA	V_{SSA}	Analog Ground	I
EXTRG_IN	ADHWT	Hardware trigger	I

This table presents the signal descriptions of the CMP0 module.

Table 14. CMP0 signal descriptions

Chip signal name	Module signal name	Description	I/O
CMP0_IN[5:0]	IN[5:0]	Analog voltage inputs	I
CMP0_OUT	CMPO	Comparator output	O

Table 15. VREF signal descriptions

Chip signal name	Module signal name	Description	I/O
VREF_OUT	VREF_OUT	Internally-generated voltage reference output	O

4.3.5 Timer Modules

Table 16. TPM0 signal descriptions

Chip signal name	Module signal name	Description	I/O
TPM_CLKIN[1:0]	TPM_EXTCLK	External clock. TPM external clock can be selected to increment the TPM counter on every rising edge synchronized to the counter clock.	I
TPM0_CH[5:0]	TPM_CHn	TPM channel (n = 5 to 0). A TPM channel pin is configured as output when configured in an output compare or PWM mode and the TPM counter is enabled, otherwise the TPM channel pin is an input.	I/O

Table 26. LPUART1 signal descriptions

Chip signal name	Module signal name	Description	I/O
LPUART1_TX	TxD	Transmit data	I/O
LPUART1_RX	RxD	Receive data	I

Table 27. UART2 signal descriptions

Chip signal name	Module signal name	Description	I/O
UART2_TX	TxD	Transmit data	O
UART2_RX	RxD	Receive data	I

Table 28. FlexIO signal descriptions

Chip signal name	Module signal name	Description	I/O
FXIO0_Dx	FXIO_Dn (n=0...7)	Bidirectional FlexIO Shifter and Timer pin inputs/outputs	I/O

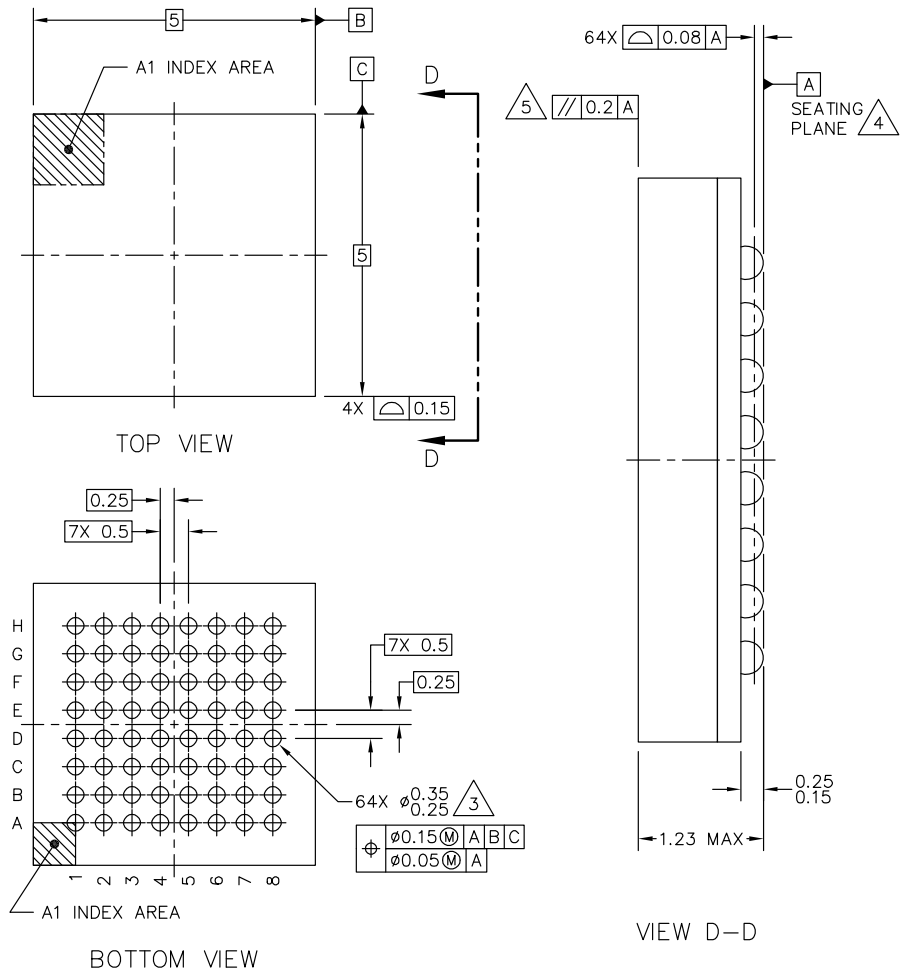
4.3.7 Human-machine interfaces (HMI)

Table 29. GPIO Signal Descriptions

Chip signal name	Module signal name	Description	I/O
PTA[31:0]	PORTA31–PORTA0	General-purpose input/output	I/O
PTB[31:0]	PORTB31–PORTB0	General-purpose input/output	I/O
PTC[11:0]	PORTC11–PORTC0	General-purpose input/output	I/O
PTD[7:0]	PORTD7–PORTD0	General-purpose input/output	I/O
PTE[31:0]	PORTE31–PORTE0	General-purpose input/output	I/O

4.4 KL17 Family Pinouts

The figure below shows the 32 QFN pinouts.



NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM A.
4. DATUM A, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

Figure 13. 64-pin MAPBGA package dimension

Table 38. Power consumption operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	• at 85 °C • at 105 °C					
I_{DD_VLLS3}	Very-low-leakage stop mode 3 current with RTC current, at 3.0 V • at 25 °C and below • at 50 °C • at 70 °C • at 85 °C • at 105 °C	 — — — — —	 1.83 2.47 3.96 6.44 13.84	 1.98 2.93 5.65 8.13 17.56	µA	3
I_{DD_VLLS3}	Very-low-leakage stop mode 3 current with RTC current, at 1.8 V • at 25 °C and below • at 50 °C • at 70 °C • at 85 °C • at 105 °C	 — — — — —	 1.68 2.27 3.66 5.97 12.92	 1.83 2.73 5.35 7.66 16.64	µA	3
I_{DD_VLLS1}	Very-low-leakage stop mode 1 current all peripheral disabled at 3.0 V • at 25 °C and below • at 50°C • at 70°C • at 85°C • at 105 °C	 — — — — —	 0.84 1.19 2.03 3.54 8.53	 1.06 1.33 2.62 4.13 9.98	µA	
I_{DD_VLLS1}	Very-low-leakage stop mode 1 current RTC enabled at 3.0 V • at 25 °C and below • at 50°C • at 70°C • at 85°C • at 105 °C	 — — — — —	 1.26 1.61 2.5 4.07 9	 1.48 1.75 3.09 4.66 10.45	µA	3
I_{DD_VLLS1}	Very-low-leakage stop mode 1 current RTC enabled at 1.8 V • at 25 °C and below • at 50°C • at 70°C • at 85°C • at 105 °C	 — — — — —	 1.08 1.42 2.21 3.59 8.02	 1.30 1.56 2.80 4.18 9.47	µA	3

Table continues on the next page...

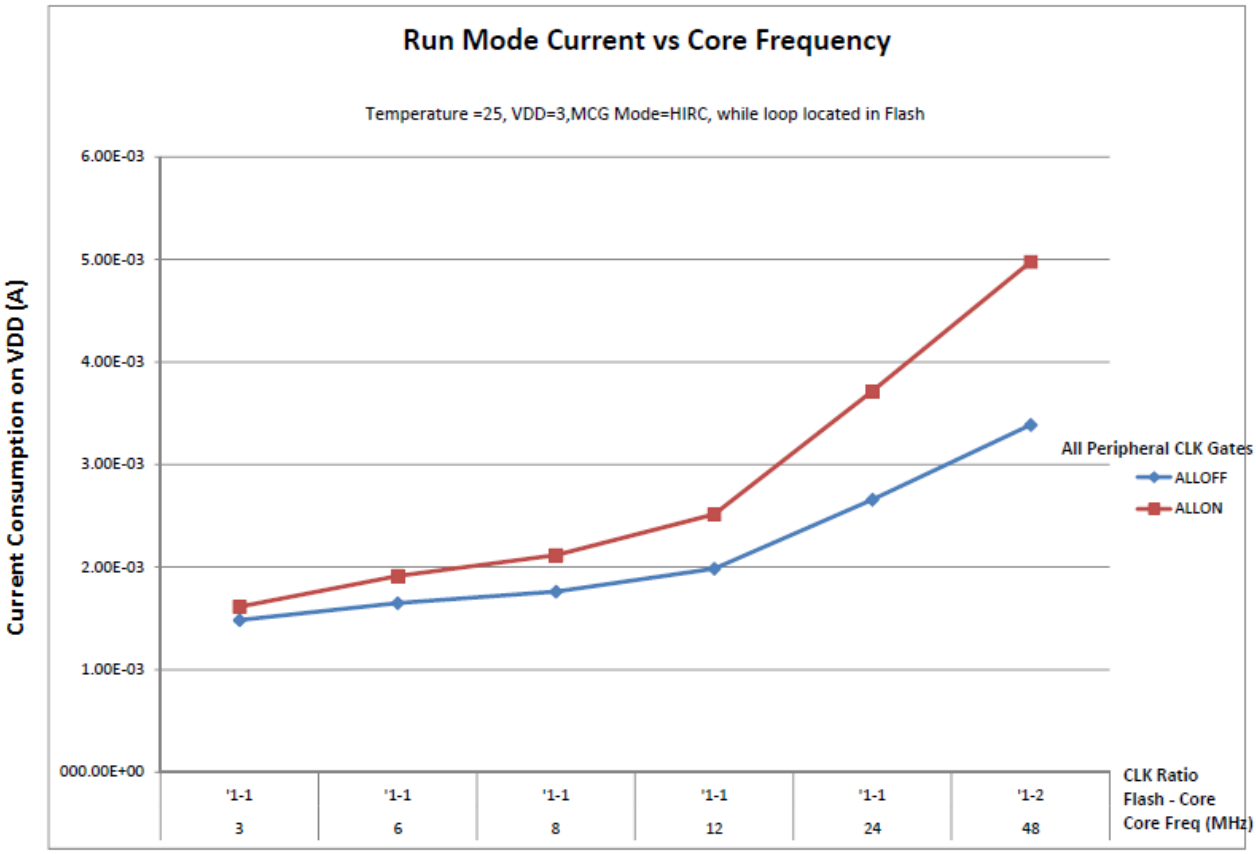


Figure 20. Run mode supply current vs. core frequency

5.2.3.2 General switching specifications

These general-purpose specifications apply to all signals configured for GPIO and UART signals.

Table 42. General switching specifications

Description	Min.	Max.	Unit	Notes
GPIO pin interrupt pulse width (digital glitch filter disabled) — Synchronous path	1.5	—	Bus clock cycles	1
External RESET and NMI pin interrupt pulse width — Asynchronous path	100	—	ns	2
GPIO pin interrupt pulse width — Asynchronous path	16	—	ns	2
Port rise and fall time	—	36	ns	3

1. The synchronous and asynchronous timing must be met.
2. This is the shortest pulse that is guaranteed to be recognized.
3. 75 pF load

5.2.4 Thermal specifications

5.2.4.1 Thermal operating requirements

Table 43. Thermal operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
T_J	Die junction temperature	–40	125	°C	
T_A	Ambient temperature	–40	105	°C	1

1. Maximum T_A can be exceeded only if the user ensures that T_J does not exceed the maximum. The simplest method to determine T_J is: $T_J = T_A + R_{\theta JA} \times$ chip power dissipation.

5.2.4.2 Thermal attributes

NOTE

The 48 QFN and 64 MAPBGA packages for this product are not yet available. However, it is included in Package Your Way program for Kinetis MCUs. Visit freescale.com/KPYW for more details.

5.3.1.1 SWD electricals

Table 45. SWD full voltage range electricals

Symbol	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
J1	SWD_CLK frequency of operation • Serial wire debug	0	25	MHz
J2	SWD_CLK cycle period	1/J1	—	ns
J3	SWD_CLK clock pulse width • Serial wire debug	20	—	ns
J4	SWD_CLK rise and fall times	—	3	ns
J9	SWD_DIO input data setup time to SWD_CLK rise	10	—	ns
J10	SWD_DIO input data hold time after SWD_CLK rise	0	—	ns
J11	SWD_CLK high to SWD_DIO data valid	—	32	ns
J12	SWD_CLK high to SWD_DIO high-Z	5	—	ns

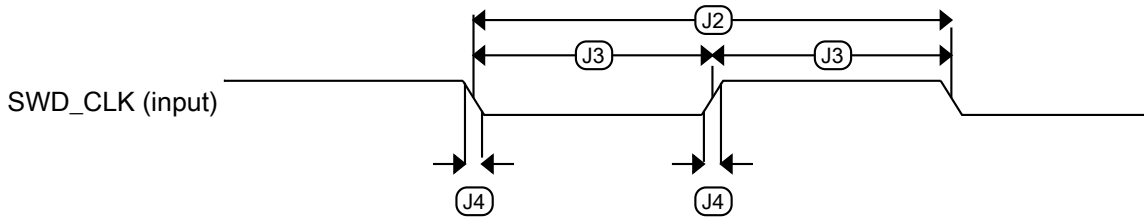


Figure 22. Serial wire clock input timing

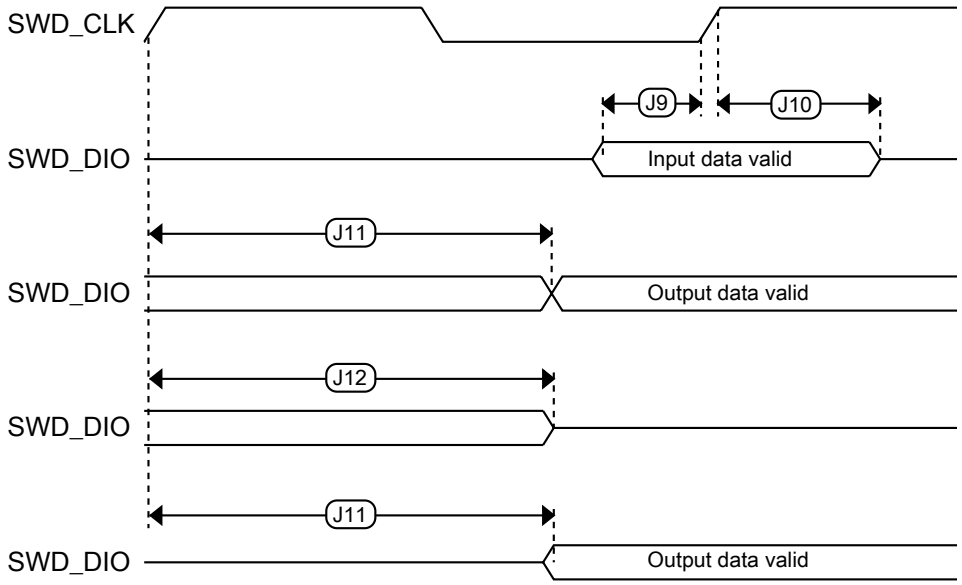


Figure 23. Serial wire data timing

5.3.2 System modules

There are no specifications necessary for the device's system modules.

5.3.3 Clock modules

5.3.3.1 MCG-Lite specifications

Table 46. IRC48M specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I_{DD48M}	Supply current	—	400	500	µA	
f_{irc48m}	Internal reference frequency	—	48	—	MHz	
$\Delta f_{irc48m\_ol\_lv}$	Open loop total deviation of IRC48M frequency at low voltage (VDD=1.71V-1.89V) over temperature	—	± 0.5	± 1.5	$\%f_{irc48m}$	
$\Delta f_{irc48m\_ol\_hv}$	Open loop total deviation of IRC48M frequency at high voltage (VDD=1.89V-3.6V) over temperature	—	± 0.5	± 1.0	$\%f_{irc48m}$	1
J_{cyc_irc48m}	Period Jitter (RMS)	—	35	150	ps	
$t_{irc48mst}$	Startup time	—	2	3	µs	2

1. The maximum value represents characterized results equivalent to the mean plus or minus three times the standard deviation (mean±3 sigma).
2. IRC48M startup time is defined as the time between clock enablement and clock availability for system use. Enable the clock by one of the following settings:
   - MCG operating in an external clocking mode and MCG_C7[OSCSEL]=10, or
   - SIM_SOPT2[PLLFLLSEL]=11

Table 47. IRC8M/2M specification

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I_{DD_2M}	Supply current in 2 MHz mode	—	14	17	µA	—
I_{DD_8M}	Supply current in 8 MHz mode	—	30	35	µA	—
f_{IRC_2M}	Output frequency	—	2	—	MHz	—
f_{IRC_8M}	Output frequency	—	8	—	MHz	—
$f_{IRC\_T\_2M}$	Output frequency range (trimmed)	—	—	±3	$\%f_{IRC}$	—
$f_{IRC\_T\_8M}$	Output frequency range (trimmed)	—	—	±3	$\%f_{IRC}$	—
T_{su_2M}	Startup time	—	—	12.5	µs	—
T_{su_8M}	Startup time	—	—	12.5	µs	—

5.3.3.2 Oscillator electrical specifications

5.3.3.2.1 Oscillator DC electrical specifications

Table 48. Oscillator DC electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{DD}	Supply voltage	1.71	—	3.6	V	
I_{DDOSC}	Supply current — low-power mode (HGO=0)					1
	• 32 kHz	—	500	—	nA	
	• 4 MHz	—	200	—	µA	
	• 8 MHz (RANGE=01)	—	300	—	µA	
	• 16 MHz	—	950	—	µA	
	• 24 MHz	—	1.2	—	mA	
	• 32 MHz	—	1.5	—	mA	
I_{DDOSC}	Supply current — high gain mode (HGO=1)					1
	• 32 kHz	—	25	—	µA	
	• 4 MHz	—	400	—	µA	
	• 8 MHz (RANGE=01)	—	500	—	µA	
	• 16 MHz	—	2.5	—	mA	
	• 24 MHz	—	3	—	mA	
	• 32 MHz	—	4	—	mA	

Table continues on the next page...

Table 53. NVM reliability specifications (continued)

Symbol	Description	Min.	Typ.[1]	Max.	Unit	Notes
$t_{nvmretp10k}$	Data retention after up to 10 K cycles	5	50	—	years	—
$t_{nvmretp1k}$	Data retention after up to 1 K cycles	20	100	—	years	—
$n_{nvmcycp}$	Cycling endurance	10 K	50 K	—	cycles	2

1. Typical data retention values are based on measured response accelerated at high temperature and derated to a constant 25 °C use profile. Engineering Bulletin EB618 does not apply to this technology. Typical endurance defined in Engineering Bulletin EB619.
2. Cycling endurance represents number of program/erase cycles at –40 °C ≤ T_j ≤ 125 °C.

5.3.5 Security and integrity modules

There are no specifications necessary for the device's security and integrity modules.

5.3.6 Analog

5.3.6.1 ADC electrical specifications

Using differential inputs can achieve better system accuracy than using single-end inputs.

5.3.6.1.1 16-bit ADC operating conditions

Table 54. 16-bit ADC operating conditions

Symbol	Description	Conditions	Min.	Typ.[1]	Max.	Unit	Notes
V_{DDA}	Supply voltage	Absolute	1.71	—	3.6	V	—
ΔV_{DDA}	Supply voltage	Delta to V_{DD} (V_{DD} – V_{DDA})	-100	0	+100	mV	2
ΔV_{SSA}	Ground voltage	Delta to V_{SS} (V_{SS} – V_{SSA})	-100	0	+100	mV	2
V_{ADIN}	Input voltage	• 16-bit differential mode • All other modes	VREFL VREFL	— —	31/32 × VREFH VREFH	V	—
C_{ADIN}	Input capacitance	• 16-bit mode • 8-bit / 10-bit / 12-bit modes	— —	8 4	10 5	pF	—
R_{ADIN}	Input series resistance		—	2	5	kΩ	—
R_{AS}	Analog source resistance (external)	13-bit / 12-bit modes f_{ADCK} < 4 MHz	—	—	5	kΩ	3

Table continues on the next page...

Table 62. SPI slave mode timing on slew rate disabled pads (continued)

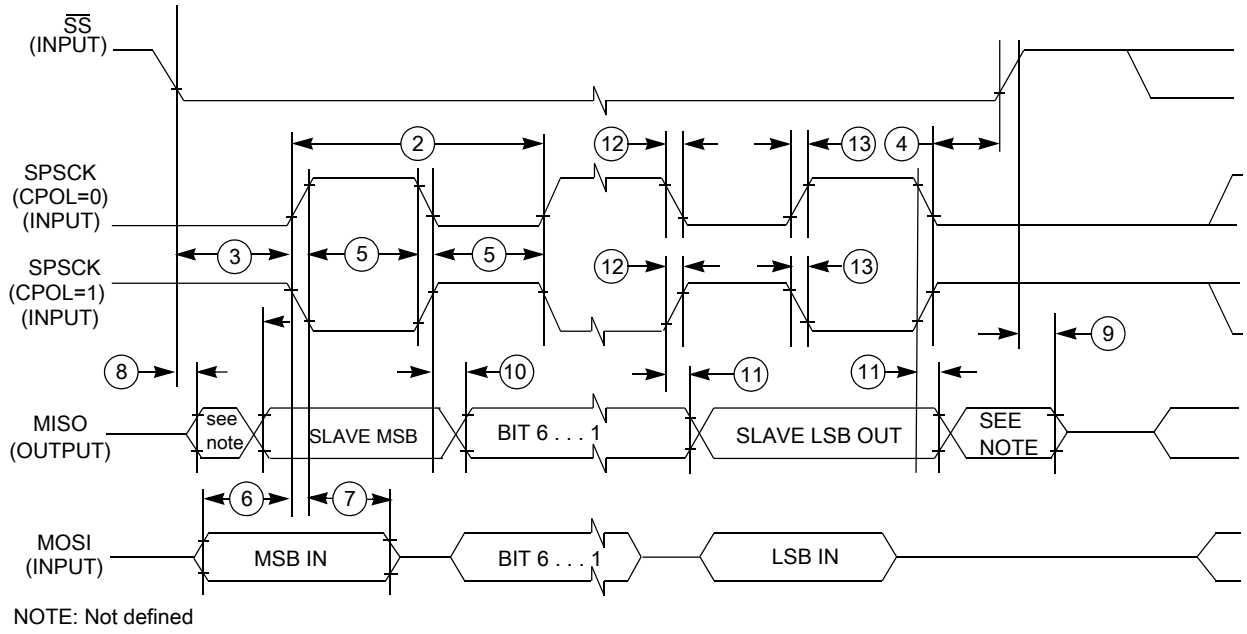
Num.	Symbol	Description	Min.	Max.	Unit	Note
4	t_{Lag}	Enable lag time	1	—	t_{periph}	—
5	t_{WSPSCK}	Clock (SPSCK) high or low time	t_{periph} - 30	—	ns	—
6	t_{SU}	Data setup time (inputs)	2.5	—	ns	—
7	t_{HI}	Data hold time (inputs)	3.5	—	ns	—
8	t_a	Slave access time	—	t_{periph}	ns	3
9	t_{dis}	Slave MISO disable time	—	t_{periph}	ns	4
10	t_v	Data valid (after SPSCK edge)	—	31	ns	—
11	t_{HO}	Data hold time (outputs)	0	—	ns	—
12	t_{RI}	Rise time input	—	t_{periph} - 25	ns	—
	t_{FI}	Fall time input				
13	t_{RO}	Rise time output	—	25	ns	—
	t_{FO}	Fall time output				

1. For SPI0 f_{periph} is the bus clock (f_{BUS}). For SPI1 f_{periph} is the system clock (f_{SYS}).
2. $t_{periph} = 1/f_{periph}$
3. Time to data active from high-impedance state
4. Hold time to high-impedance state

Table 63. SPI slave mode timing on slew rate enabled pads

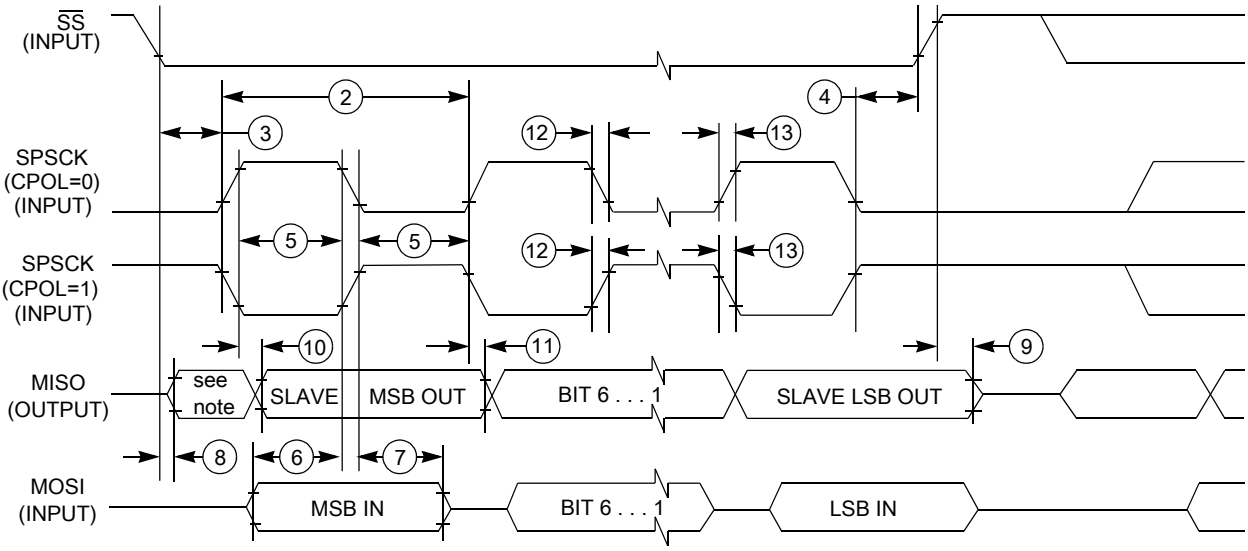
Num.	Symbol	Description	Min.	Max.	Unit	Note
1	f_{op}	Frequency of operation	0	$f_{periph}/4$	Hz	1
2	t_{SPSCK}	SPSCK period	4 x t_{periph}	—	ns	2
3	t_{Lead}	Enable lead time	1	—	t_{periph}	—
4	t_{Lag}	Enable lag time	1	—	t_{periph}	—
5	t_{WSPSCK}	Clock (SPSCK) high or low time	t_{periph} - 30	—	ns	—
6	t_{SU}	Data setup time (inputs)	2	—	ns	—
7	t_{HI}	Data hold time (inputs)	7	—	ns	—
8	t_a	Slave access time	—	t_{periph}	ns	3
9	t_{dis}	Slave MISO disable time	—	t_{periph}	ns	4
10	t_v	Data valid (after SPSCK edge)	—	122	ns	—
11	t_{HO}	Data hold time (outputs)	0	—	ns	—
12	t_{RI}	Rise time input	—	t_{periph} - 25	ns	—
	t_{FI}	Fall time input				
13	t_{RO}	Rise time output	—	36	ns	—
	t_{FO}	Fall time output				

1. For SPI0 f_{periph} is the bus clock (f_{BUS}). For SPI1 f_{periph} is the system clock (f_{SYS}).
2. $t_{periph} = 1/f_{periph}$
3. Time to data active from high-impedance state
4. Hold time to high-impedance state



NOTE: Not defined

Figure 31. SPI slave mode timing (CPHA = 0)



NOTE: Not defined

Figure 32. SPI slave mode timing (CPHA = 1)

5.5.2 Inter-Integrated Circuit Interface (I2C) timing

Table 64. I2C timing

Characteristic	Symbol	Standard Mode		Fast Mode		Unit
		Minimum	Maximum	Minimum	Maximum	
SCL Clock Frequency	f_{SCL}	0	100	0	400[1]	kHz
Hold time (repeated) START condition. After this period, the first clock pulse is generated.	t_{HD}; STA	4	—	0.6	—	µs
LOW period of the SCL clock	t_{LOW}	4.7	—	1.25	—	µs
HIGH period of the SCL clock	t_{HIGH}	4	—	0.6	—	µs
Set-up time for a repeated START condition	t_{SU}; STA	4.7	—	0.6	—	µs
Data hold time for I²C bus devices	t_{HD}; DAT	0[2]	3.45[3]	0[4]	0.9[2]	µs
Data set-up time	t_{SU}; DAT	250[5]	—	100[3, 6]	—	ns
Rise time of SDA and SCL signals	t_r	—	1000	20 +0.1C_b[7]	300	ns
Fall time of SDA and SCL signals	t_f	—	300	20 +0.1C_b[6]	300	ns
Set-up time for STOP condition	t_{SU}; STO	4	—	0.6	—	µs
Bus free time between STOP and START condition	t_{BUF}	4.7	—	1.3	—	µs
Pulse width of spikes that must be suppressed by the input filter	t_{SP}	N/A	N/A	0	50	ns

1. The maximum SCL Clock Frequency in Fast mode with maximum bus loading can be achieved only when using the high drive pins across the full voltage range and when using the normal drive pins and VDD ≥ 2.7 V.
2. The master mode I²C deasserts ACK of an address byte simultaneously with the falling edge of SCL. If no slaves acknowledge this address byte, then a negative hold time can result, depending on the edge rates of the SDA and SCL lines.
3. The maximum tHD; DAT must be met only if the device does not stretch the LOW period (tLOW) of the SCL signal.
4. Input signal Slew = 10 ns and Output Load = 50 pF
5. Set-up time in slave-transmitter mode is 1 IPBus clock period, if the TX FIFO is empty.
6. A Fast mode I²C bus device can be used in a Standard mode I2C bus system, but the requirement $t_{SU;\ DAT} \geq 250$ ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, then it must output the next data bit to the SDA line $t_{rmax} + t_{SU;\ DAT} = 1000 + 250 = 1250$ ns (according to the Standard mode I²C bus specification) before the SCL line is released.
7. C_b = total capacitance of the one bus line in pF.

To achieve 1MHz I2C clock rates, consider the following recommendations:

- To counter the effects of clock stretching, the I2C baud Rate select bits can be configured for faster than desired baud rate.
- Use high drive pad and DSE bit should be set in PORTx_PCRn register.
- Minimize loading on the I2C SDA and SCL pins to ensure fastest rise times for the SCL line to avoid clock stretching.
- Use smaller pull up resistors on SDA and SCL to reduce the RC time constant.

Table 66. External crystal/resonator connections

Oscillator mode	Oscillator mode
Low frequency (32.768kHz), low power	Diagram 1
Low frequency (32.768kHz), high gain	Diagram 2, Diagram 4
High frequency (1-32MHz), low power	Diagram 3
High frequency (1-32MHz), high gain	Diagram 4

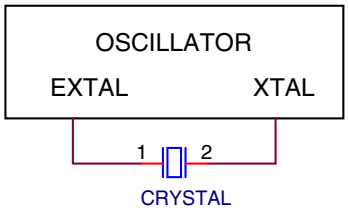


Figure 40. Crystal connection – Diagram 1

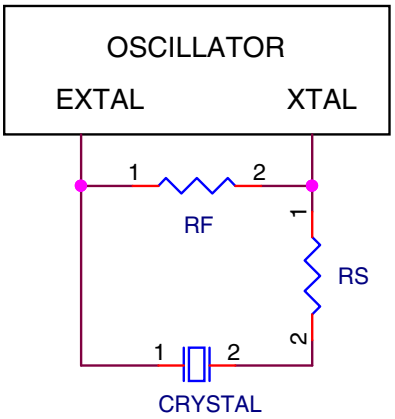


Figure 41. Crystal connection – Diagram 2

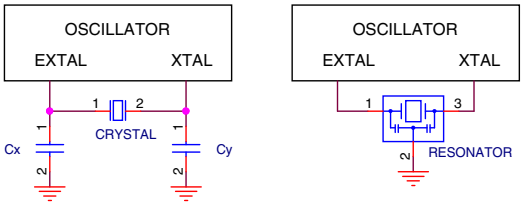


Figure 42. Crystal connection – Diagram 3