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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

| | |
|----------------------------|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-M0+ |
| Core Size | 32-Bit Single-Core |
| Speed | 48MHz |
| Connectivity | I ² C, FlexIO, SPI, UART/USART |
| Peripherals | DMA, I ² S, PWM, WDT |
| Number of I/O | 28 |
| Program Memory Size | 64KB (64K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 16K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.71V ~ 3.6V |
| Data Converters | A/D 11x16b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 105°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 32-UFQFN Exposed Pad |
| Supplier Device Package | 32-QFN (5x5) |
| Purchase URL | https://www.e-xfl.com/product-detail/nxp-semiconductors/mkl17z64vfm4 |

The Flash Option (FOPT) register in the Flash Memory module (FTFA_FOPT) allows the user to customize the operation of the MCU at boot time. The register contains read-only bits that are loaded from the NVM's option byte in the flash configuration field. Below is boot flow chart for this device.

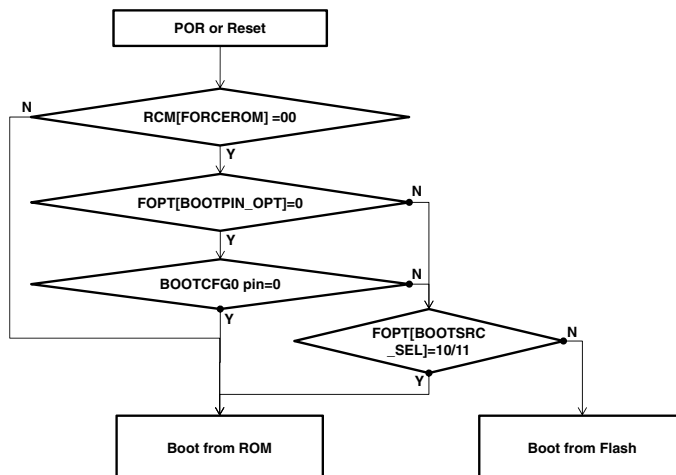


Figure 2. Boot flow chart

The blank chip is default to boot from ROM and remaps the vector table to ROM base address, otherwise, it remaps to flash address.

2.1.6 Clock options

This chip provides a wide range of sources to generate the internal clocks. These sources include internal resistor capacitor (IRC) oscillators, external oscillators, external clock sources, and ceramic resonators. These sources can be configured to provide the required performance and optimize the power consumption.

The IRC oscillators include the high-speed internal resistor capacitor (HIRC) oscillator, the low-speed internal resistor capacitor (LIRC) oscillator, and the low power oscillator (LPO).

The HIRC oscillator generates a 48 MHz clock.

The LIRC oscillator generates an 8 MHz or 2 MHz clock, and default to 8 MHz system clock on reset. The LIRC oscillator cannot be used in any VLLS modes.

The LPO generates a 1 kHz clock and cannot be used in VLLS0 mode.

The system oscillator supports low frequency crystals (32 kHz to 40 kHz), high frequency crystals (1 MHz to 32 MHz), and ceramic resonators (1 MHz to 32 MHz). An external clock source, DC to 48 MHz, can be used as the system clock through the EXTAL0 pin. The external oscillator also supports a low speed external clock (32.768 kHz) on the RTC_CLKIN pin for use with the RTC.

For more details on the clock operations and configurations, see Reference Manual.

The following figure is a high level block diagram of the clock generation.

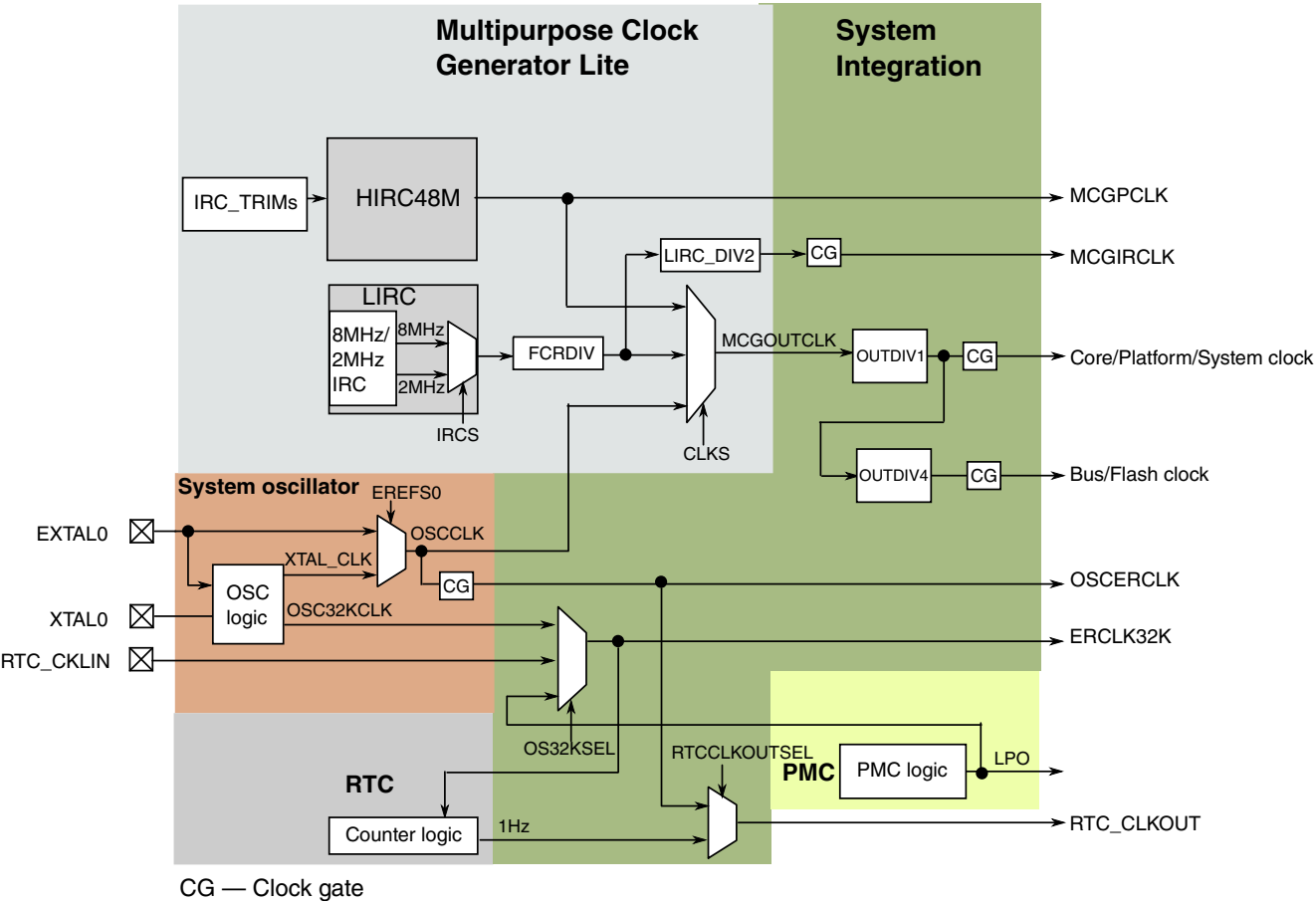


Figure 3. Clock block diagram

In order to provide flexibility, many peripherals can select from multiple clock sources for operation. This enables the peripheral to select a clock that will always be available during operation in various operational modes.

The following table summarizes the clocks associated with each module.

Table 4. Module clocks (continued)

| Module | Bus interface clock | Internal clocks | I/O interface clocks |
|---------------------------------|---------------------|--------------------------------|----------------------|
| I ² C1 | System Clock | — | I2C1_SCL |
| LPUART0, LPUART1 | Bus clock | LPUART0 clock LPUART1 clock | — |
| UART2 | Bus clock | — | — |
| FlexIO | Bus clock | FlexIO clock | — |
| Human-machine interfaces | | | |
| GPIO | Platform clock | — | — |

2.1.7 Security

Security state can be enabled via programming flash configuration field (0x40e). After enabling device security, the SWD port cannot access the memory resources of the MCU, and ROM boot loader is also limited to access flash and not allowed to read out flash information via ROM boot loader commands.

| Access interface | Secure state | Unsecure operation |
|--|--|--|
| SWD port | Cannot access memory source by SWD interface | The debugger can write to the Flash Mass Erase in Progress field of the MDM-AP Control register to trigger a mass erase (Erase All Blocks) command |
| ROM boot loader Interface (UART/I2C/SPI) | Limit access to the flash, cannot read out flash content | Send "FlashEraseAllUnsecureh" command or attempt to unlock flash security using the backdoor key |

This device features 80-bit unique identification number, which is programmed in factory and loaded to SIM register after power-on reset.

2.1.8 Power management

The Power Management Controller (PMC) expands upon ARM's operational modes of Run, Sleep, and Deep Sleep, to provide multiple configurable modes. These modes can be used to optimize current consumption for a wide range of applications. The WFI or WFE instruction invokes a Wait or a Stop mode, depending on the current configuration. For more information on ARM's operational modes, See the ARM® Cortex User Guide.

The PMC provides Run (Run), and Very Low Power Run (VLPR) configurations in ARM's Run operation mode. In these modes, the MCU core is active and can access all peripherals. The difference between the modes is the maximum clock frequency of the system and therefore the power consumption. The configuration that matches the power versus performance requirements of the application can be selected.

The PMC provides Wait (Wait) and Very Low Power Wait (VLPW) configurations in ARM's Sleep operation mode. In these modes, even though the MCU core is inactive, all of the peripherals can be enabled and operate as programmed. The difference between the modes is the maximum clock frequency of the system and therefore the power consumption.

The PMC provides Stop (Stop), Very Low Power Stop (VLPS), Low Leakage Stop (LLS), and Very Low Leakage Stop (VLLS) configurations in ARM's Deep Sleep operational mode. In these modes, the MCU core and most of the peripherals are disabled. Depending on the requirements of the application, different portions of the analog, logic, and memory can be retained or disabled to conserve power.

The Nested Vectored Interrupt Controller (NVIC), the Asynchronous Wake-up Interrupt Controller (AWIC), and the Low Leakage Wake-Up Controller (LLWU) are used to wake up the MCU from low power states. The NVIC is used to wake up the MCU core from WAIT and VLPW modes. The AWIC is used to wake up the MCU core from STOP and VLPS modes. The LLWU is used to wake up the MCU core from LLS and VLLSx modes.

For additional information regarding operational modes, power management, the NVIC, AWIC, or the LLWU, please refer to the Reference Manual.

The following table provides information about the state of the peripherals in the various operational modes and the modules that can wake MCU from low power modes.

Table 6. Peripherals states in different operational modes

| Core mode | Device mode | Descriptions |
|------------|---------------------|---|
| Run mode | Run | In Run mode, all device modules are operational. |
| | Very Low Power Run | In VLPR mode, all device modules are operational at a reduced frequency except the Low Voltage Detect (LVD) monitor, which is disabled. |
| Sleep mode | Wait | In Wait mode, all peripheral modules are operational. The MCU core is placed into Sleep mode. |
| | Very Low Power Wait | In VLPW mode, all peripheral modules are operational at a reduced frequency except the Low Voltage Detect (LVD) monitor, which is disabled. The MCU core is placed into Sleep mode. |

Table continues on the next page...

2.2.6 CMP

The device contains one high-speed comparator and two 8-input multiplexers for both the inverting and non-inverting inputs of the comparator. Each CMP input channel connects to both muxes.

The CMP includes one 6-bit DAC, which provides a selectable voltage reference for various user application cases. Besides, the CMP also has several module-to-module interconnects in order to facilitate ADC triggering, TPM triggering, and interfaces.

The CMP has the following features:

- Inputs may range from rail to rail
- Programmable hysteresis control
- Selectable interrupt on rising-edge, falling-edge, or both rising or falling edges of the comparator output
- Selectable inversion on comparator output
- Capability to produce a wide range of outputs such as sampled, digitally filtered
- External hysteresis can be used at the same time that the output filter is used for internal functions
- Two software selectable performance levels: shorter propagation delay at the expense of higher power and Low power with longer propagation delay
- DMA transfer support
- Functional in all modes of operation except in VLLS0 mode
- The filter functions are not available in Stop, VLPS, LLS, or VLLSx modes
- Integrated 6-bit DAC with selectable supply reference source and can be power down to conserve power
- Two 8-to-1 channel mux

2.2.7 RTC

The RTC is an always powered-on block that remains active in all low power modes. The time counter within the RTC is clocked by a 32.768 kHz clock sourced from an external crystal using the oscillator or clock directly from RTC_CLKIN pin.

RTC is reset on power-on reset, and a software reset bit in RTC can also initialize all RTC registers.

The RTC module has the following features

- 32-bit seconds counter with roll-over protection and 32-bit alarm

| 64 LQFP | 36 XFB GA | 32 QFN | 48 QFN | 64 MAP BGA | Pin Name | Default | ALT0 | ALT1 | ALT2 | ALT3 | ALT4 | ALT5 | ALT6 | ALT7 |
|------------|-----------------|-----------|-----------|------------------|--------------------------------|-----------|-----------|--------------------------------|-----------|-------------|------------|-----------|----------|------|
| 37 | — | — | 29 | E7 | PTB2 | ADC0_SE12 | ADC0_SE12 | PTB2 | I2C0_SCL | TPM2_CH0 | | | | |
| 38 | — | — | 30 | E8 | PTB3 | ADC0_SE13 | ADC0_SE13 | PTB3 | I2C0_SDA | TPM2_CH1 | | | | |
| 39 | — | — | 31 | E6 | PTB16 | DISABLED | | PTB16 | SPI1_MOSI | LPUART0_RX | TPM_CLKIN0 | SPI1_MISO | | |
| 40 | — | — | 32 | D7 | PTB17 | DISABLED | | PTB17 | SPI1_MISO | LPUART0_TX | TPM_CLKIN1 | SPI1_MOSI | | |
| 41 | — | — | — | D6 | PTB18 | DISABLED | | PTB18 | | TPM2_CH0 | | | | |
| 42 | — | — | — | C7 | PTB19 | DISABLED | | PTB19 | | TPM2_CH1 | | | | |
| 43 | — | — | 33 | D8 | PTC0 | ADC0_SE14 | ADC0_SE14 | PTC0 | | EXTRG_IN | | CMP0_OUT | | |
| 44 | C5 | 22 | 34 | C6 | PTC1/ LLWU_P6/ RTC_CLKIN | ADC0_SE15 | ADC0_SE15 | PTC1/ LLWU_P6/ RTC_CLKIN | I2C1_SCL | | TPM0_CH0 | | | |
| 45 | B6 | 23 | 35 | B7 | PTC2 | ADC0_SE11 | ADC0_SE11 | PTC2 | I2C1_SDA | | TPM0_CH1 | | | |
| 46 | B5 | 24 | 36 | C8 | PTC3/ LLWU_P7 | DISABLED | | PTC3/ LLWU_P7 | SPI1_SCK | LPUART1_RX | TPM0_CH2 | CLKOUT | | |
| 47 | — | — | — | E3 | VSS | VSS | VSS | | | | | | | |
| 48 | — | — | — | E4 | VDD | VDD | VDD | | | | | | | |
| 49 | A6 | 25 | 37 | B8 | PTC4/ LLWU_P8 | DISABLED | | PTC4/ LLWU_P8 | SPI0_PCS0 | LPUART1_TX | TPM0_CH3 | SPI1_PCS0 | | |
| 50 | A5 | 26 | 38 | A8 | PTC5/ LLWU_P9 | DISABLED | | PTC5/ LLWU_P9 | SPI0_SCK | LPTMR0_ALT2 | | | CMP0_OUT | |
| 51 | B4 | 27 | 39 | A7 | PTC6/ LLWU_P10 | CMP0_IN0 | CMP0_IN0 | PTC6/ LLWU_P10 | SPI0_MOSI | EXTRG_IN | | SPI0_MISO | | |
| 52 | A4 | 28 | 40 | B6 | PTC7 | CMP0_IN1 | CMP0_IN1 | PTC7 | SPI0_MISO | | | SPI0_MOSI | | |
| 53 | — | — | — | A6 | PTC8 | CMP0_IN2 | CMP0_IN2 | PTC8 | I2C0_SCL | TPM0_CH4 | | | | |
| 54 | — | — | — | B5 | PTC9 | CMP0_IN3 | CMP0_IN3 | PTC9 | I2C0_SDA | TPM0_CH5 | | | | |
| 55 | — | — | — | B4 | PTC10 | DISABLED | | PTC10 | I2C1_SCL | | | | | |
| 56 | — | — | — | A5 | PTC11 | DISABLED | | PTC11 | I2C1_SDA | | | | | |
| 57 | — | — | 41 | C3 | PTD0 | DISABLED | | PTD0 | SPI0_PCS0 | | TPM0_CH0 | | FXIO0_D0 | |
| 58 | — | — | 42 | A4 | PTD1 | ADC0_SE5b | ADC0_SE5b | PTD1 | SPI0_SCK | | TPM0_CH1 | | FXIO0_D1 | |
| 59 | — | — | 43 | C2 | PTD2 | DISABLED | | PTD2 | SPI0_MOSI | UART2_RX | TPM0_CH2 | SPI0_MISO | FXIO0_D2 | |
| 60 | — | — | 44 | B3 | PTD3 | DISABLED | | PTD3 | SPI0_MISO | UART2_TX | TPM0_CH3 | SPI0_MOSI | FXIO0_D3 | |
| 61 | A3 | 29 | 45 | A3 | PTD4/ LLWU_P14 | DISABLED | | PTD4/ LLWU_P14 | SPI1_PCS0 | UART2_RX | TPM0_CH4 | | FXIO0_D4 | |
| 62 | B3 | 30 | 46 | C1 | PTD5 | ADC0_SE6b | ADC0_SE6b | PTD5 | SPI1_SCK | UART2_TX | TPM0_CH5 | | FXIO0_D5 | |
| 63 | B2 | 31 | 47 | B2 | PTD6/ LLWU_P15 | ADC0_SE7b | ADC0_SE7b | PTD6/ LLWU_P15 | SPI1_MOSI | LPUART0_RX | I2C1_SDA | SPI1_MISO | FXIO0_D6 | |

| 64 LQFP | 36 XFBGA | 32 QFN | 48 QFN | 64 MAPBGA | Pin name | Driver strength | Default status after POR | Pullup/ pulldown setting after POR | Slew rate after POR | Passive pin filter after POR | Open drain | Pin interrupt |
|---------|----------|--------|--------|-----------|--------------------------------|-----------------|--------------------------|------------------------------------|---------------------|------------------------------|------------|---------------|
| 18 | F2 | 9 | 14 | H2 | PTE30 | ND | Hi-Z | — | SS | N | N | Y |
| 19 | — | — | — | H3 | PTE31 | ND | Hi-Z | — | SS | N | N | Y |
| 20 | — | — | 15 | H4 | PTE24 | ND | Hi-Z | — | SS | N | N | Y |
| 21 | — | — | 16 | H5 | PTE25 | ND | Hi-Z | — | SS | N | N | Y |
| 22 | F3 | 10 | 17 | D3 | PTA0 | ND | L | PD | SS | N | N | Y |
| 23 | F4 | 11 | 18 | D4 | PTA1 | ND | Hi-Z | — | SS | N | N | Y |
| 24 | E4 | 12 | 19 | E5 | PTA2 | ND | Hi-Z | — | SS | N | N | Y |
| 25 | E5 | 13 | 20 | D5 | PTA3 | ND | H | PU | FS | N | N | Y |
| 26 | F5 | 14 | 21 | G5 | PTA4 | ND | H | PU | SS | Y | N | Y |
| 27 | — | — | — | F5 | PTA5 | ND | Hi-Z | — | SS | N | N | Y |
| 28 | — | — | — | H6 | PTA12 | ND | Hi-Z | — | SS | N | N | Y |
| 29 | — | — | — | G6 | PTA13 | ND | Hi-Z | — | SS | N | N | Y |
| 30 | C3 | 15 | 22 | G7 | VDD | ND | — | — | — | — | — | — |
| 31 | C4 | 16 | 23 | H7 | VSS | ND | — | — | — | — | — | — |
| 32 | F6 | 17 | 24 | H8 | PTA18 | ND | Hi-Z | — | SS | N | N | Y |
| 33 | E6 | 18 | 25 | G8 | PTA19 | ND | Hi-Z | — | SS | N | N | Y |
| 34 | D5 | 19 | 26 | F8 | PTA20 | ND | H | PU | SS | N | Y | Y |
| 35 | D6 | 20 | 27 | F7 | PTB0/LLWU_P5 | HD | Hi-Z | — | FS | N | N | Y |
| 36 | C6 | 21 | 28 | F6 | PTB1 | HD | Hi-Z | — | FS | N | N | Y |
| 37 | — | — | 29 | E7 | PTB2 | ND | Hi-Z | — | SS | N | N | Y |
| 38 | — | — | 30 | E8 | PTB3 | ND | Hi-Z | — | SS | N | N | Y |
| 39 | — | — | 31 | E6 | PTB16 | ND | Hi-Z | — | FS | N | N | Y |
| 40 | — | — | 32 | D7 | PTB17 | ND | Hi-Z | — | FS | N | N | Y |
| 41 | — | — | — | D6 | PTB18 | ND | Hi-Z | — | SS | N | N | Y |
| 42 | — | — | — | C7 | PTB19 | ND | Hi-Z | — | SS | N | N | Y |
| 43 | — | — | 33 | D8 | PTC0 | ND | Hi-Z | — | SS | N | N | Y |
| 44 | C5 | 22 | 34 | C6 | PTC1/ LLWU_P6/ RTC_CLKIN | ND | Hi-Z | — | SS | N | N | Y |
| 45 | B6 | 23 | 35 | B7 | PTC2 | ND | Hi-Z | — | SS | N | N | Y |

Table continues on the next page...

| Properties | Abbreviation | Descriptions |
|------------------------------------|--------------|-----------------------|
| | H | High level |
| | L | Low level |
| Pullup/ pulldown setting after POR | PD | Pullup |
| | PU | Pulldown |
| Slew rate after POR | FS | Fast slew rate |
| | SS | Slow slew rate |
| Passive Pin Filter after POR | N | Disabled |
| | Y | Enabled |
| Open drain | N | Disabled ¹ |
| | Y | Enabled ² |
| Pin interrupt | Y | Yes |

1. When I2C module is enabled and a pin is functional for I2C, this pin is (pseudo-) open drain enabled. When UART or LPUART module is enabled and a pin is functional for UART or LPUART, this pin is (pseudo-) open drain configurable.
2. PTA20 is a true open drain pin that must never be pulled above VDD.

4.3 Module Signal Description Tables

The following sections correlate the chip-level signal name with the signal name used in the module's chapter. They also briefly describe the signal function and direction.

4.3.1 Core modules

Table 9. SWD signal descriptions

| Chip signal name | Module signal name | Description | I/O |
|------------------|--------------------|--|----------------|
| SWD_DIO | SWD_DIO | Serial Wire Debug Data Input/Output The SWD_DIO pin is used by an external debug tool for communication and device control. This pin is pulled up internally. | Input / Output |
| SWD_CLK | SWD_CLK | Serial Wire Clock This pin is the clock for debug logic when in the Serial Wire Debug mode. This pin is pulled down internally. | Input |

4.3.2 System modules

Table 10. System signal descriptions

| Chip signal name | Module signal name | Description | I/O |
|---------------------------|--------------------|--|-----|
| NMI | — | Non-maskable interrupt NOTE: Driving the $\overline{\text{NMI}}$ signal low forces a non-maskable interrupt, if the $\overline{\text{NMI}}$ function is selected on the corresponding pin. | I |
| $\overline{\text{RESET}}$ | — | Reset bidirectional signal | I/O |
| VDD | — | MCU power | I |
| VSS | — | MCU ground | I |

Table 11. LLWU signal descriptions

| Chip signal name | Module signal name | Description | I/O |
|------------------|--------------------|---|-----|
| LLWU_Pn | LLWU_Pn | Wakeup inputs (n = 5, 6, 7, 8, 9, 10, 14, 15) | I |

4.3.3 Clock modules

Table 12. OSC signal descriptions

| Chip signal name | Module signal name | Description | I/O |
|------------------|--------------------|---------------------------------|-----|
| EXTAL0 | EXTAL | External clock/Oscillator input | I |
| XTAL0 | XTAL | Oscillator output | O |

4.3.4 Analog

This table presents the signal descriptions of the ADC0 module.

Table 13. ADC0 signal descriptions

| Chip signal name | Module signal name | Description | I/O |
|------------------|--------------------|------------------------------------|-----|
| ADC0_DPn | DADP3–DADP0 | Differential Analog Channel Inputs | I |
| ADC0_DMn | DADM3–DADM0 | Differential Analog Channel Inputs | I |
| ADC0_SEn | ADn | Single-Ended Analog Channel Inputs | I |
| VREFH | V _{REFSH} | Voltage Reference Select High | I |

Table continues on the next page...

Table 17. TPM1 signal descriptions

| Chip signal name | Module signal name | Description | I/O |
|------------------|--------------------|---|-----|
| TPM_CLKIN[1:0] | TPM_EXTCLK | External clock. TPM external clock can be selected to increment the TPM counter on every rising edge synchronized to the counter clock. | I |
| TPM1_CH[1:0] | TPM_CHn | TPM channel (n = 1 to 0). A TPM channel pin is configured as output when configured in an output compare or PWM mode and the TPM counter is enabled, otherwise the TPM channel pin is an input. | I/O |

Table 18. TPM2 signal descriptions

| Chip signal name | Module signal name | Description | I/O |
|------------------|--------------------|---|-----|
| TPM_CLKIN[1:0] | TPM_EXTCLK | External clock. TPM external clock can be selected to increment the TPM counter on every rising edge synchronized to the counter clock. | I |
| TPM2_CH[1:0] | TPM_CHn | TPM channel (n = 1 to 0). A TPM channel pin is configured as output when configured in an output compare or PWM mode and the TPM counter is enabled, otherwise the TPM channel pin is an input. | I/O |

Table 19. LPTMR0 signal descriptions

| Chip signal name | Module signal name | Description | I/O |
|------------------|--------------------|-------------------------|-----|
| LPTMR0_ALT[3:1] | LPTMR0_ALTN | Pulse Counter Input pin | I |

Table 20. RTC signal descriptions

| Chip signal name | Module signal name | Description | I/O |
|-------------------------|--------------------|-------------------------------------|-----|
| RTC_CLKOUT ¹ | RTC_CLKOUT | 1 Hz square-wave output or OSCERCLK | O |

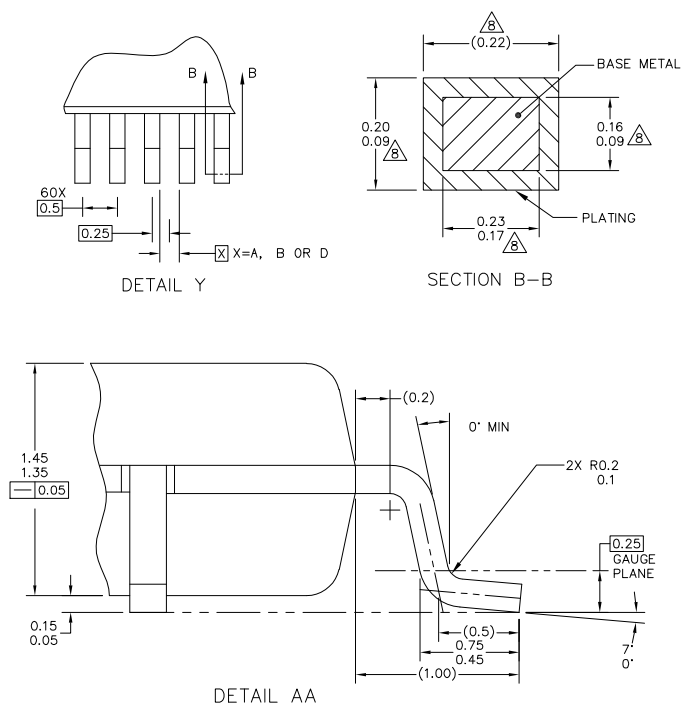
1. RTC_CLKOUT can also be driven with OSCERCLK via SIM control bit SIM_SOPT[RCTCLKOUTSEL]

4.3.6 Communication interfaces

Table 21. SPI0 signal descriptions

| Chip signal name | Module signal name | Description | I/O |
|------------------|--------------------|--------------------------------|-----|
| SPI0_MISO | MISO | Master Data In, Slave Data Out | I/O |

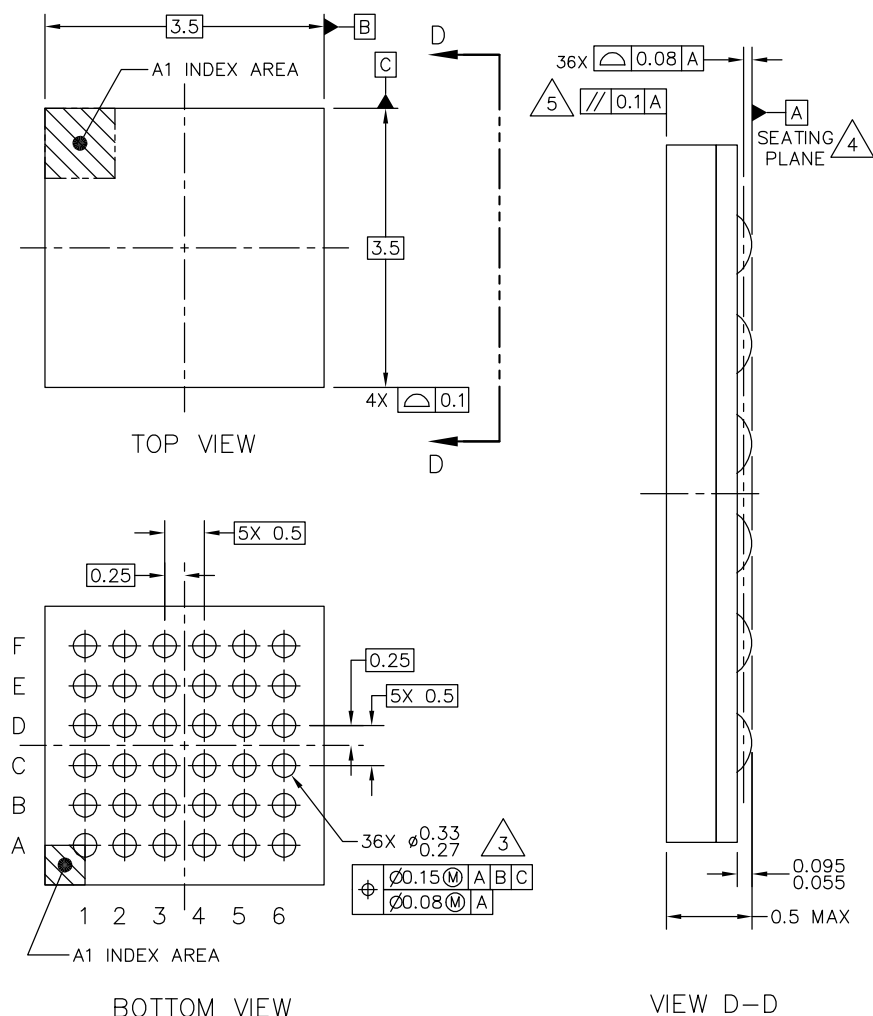
Table continues on the next page...



NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. DATUMS A, B AND D TO BE DETERMINED AT DATUM PLANE H.
4. DIMENSIONS TO BE DETERMINED AT SEATING PLANE C.
5. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE UPPER LIMIT BY MORE THAN 0.08 MM AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD SHALL NOT BE LESS THAN 0.07 MM.
6. THIS DIMENSION DOES NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 MM PER SIDE. THIS DIMENSION IS MAXIMUM PLASTIC BODY SIZE INCLUDING MOLD MISMATCH.
7. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.1 MM AND 0.25 MM FROM THE LEAD TIP.

Figure 12. 64-pin LQFP package dimensions 2



NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM A.
4. DATUM A, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

Figure 16. 36-pin XFBGA package dimension

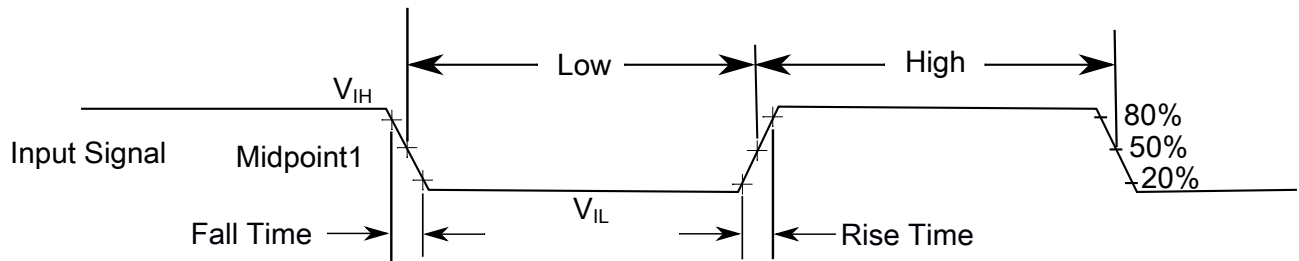
Table 33. Voltage and current absolute operating ratings (continued)

| Symbol | Description | Min. | Max. | Unit |
|-----------|---|----------------|----------------|------|
| V_{IO} | IO pin input voltage | -0.3 | $V_{DD} + 0.3$ | V |
| I_D | Instantaneous maximum current single pin limit (applies to all port pins) | -25 | 25 | mA |
| V_{DDA} | Analog supply voltage | $V_{DD} - 0.3$ | $V_{DD} + 0.3$ | V |

5.2 General

5.2.1 AC electrical characteristics

Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured at the 20% and 80% points, as shown in the following figure.



The midpoint is $V_{IL} + (V_{IH} - V_{IL}) / 2$

Figure 19. Input signal measurement reference

All digital I/O switching characteristics, unless otherwise specified, assume that the output pins have the following characteristics.

- $C_L=30$ pF loads
- Slew rate disabled
- Normal drive strength

5.2.2 Nonswitching electrical specifications

Table 38. Power consumption operating behaviors (continued)

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|------------------|---|------|--------------|--------------|------|-------|
| I_{DD_RUN} | Run mode current—48M HIRC mode, running While(1) loop in flash all peripheral clock disable, 48 MHz core/24 MHz flash, $V_{DD} = 3.0$ V <ul style="list-style-type: none"> at 25 °C at 105 °C | — | 3.39 3.57 | 3.53 3.71 | mA | |
| I_{DD_RUN} | Run mode current—48M HIRC mode, running While(1) loop in Flash all peripheral clock disable, 24 MHz core/12 MHz flash, $V_{DD} = 3.0$ V <ul style="list-style-type: none"> at 25 °C at 105 °C | — | 2.36 2.53 | 2.48 2.66 | mA | |
| I_{DD_RUN} | Run mode current—48M HIRC mode, Running While(1) loop in Flash all peripheral clock disable, 12 MHz core/6 MHz flash, $V_{DD} = 3.0$ V <ul style="list-style-type: none"> at 25 °C at 105 °C | — | 1.84 2 | 1.93 2.10 | mA | |
| I_{DD_RUN} | Run mode current—48M HIRC mode, Running While(1) loop in Flash all peripheral clock enable, 48 MHz core/24 MHz flash, $V_{DD} = 3.0$ V <ul style="list-style-type: none"> at 25 °C at 105 °C | — | 4.98 5.16 | 5.18 5.37 | mA | |
| I_{DD_VLPRCO} | Very-low-power run core mark in flash in compute operation mode— 8 MHz LIRC mode, 4 MHz core/1 MHz flash, $V_{DD} = 3.0$ V <ul style="list-style-type: none"> at 25 °C | — | 710 | 752.6 | μA | |
| I_{DD_VLPRCO} | Very-low-power-run While(1) loop in SRAM in compute operation mode— 8 MHz LIRC mode, 4 MHz core / 1 MHz flash, $V_{DD} = 3.0$ V <ul style="list-style-type: none"> at 25 °C | — | 251 | 376.5 | μA | |
| I_{DD_VLPRCO} | Very-low-power run While(1) loop in SRAM in compute operation mode:—2 MHz LIRC mode, 2 MHz core / 0.5 MHz flash, $V_{DD} = 3.0$ V <ul style="list-style-type: none"> at 25 °C | — | 115 | 143.75 | μA | |
| I_{DD_VLPR} | Very-low-power run mode current— 2 MHz LIRC mode, While(1) loop in flash all peripheral clock disable, 2 MHz core / 0.5 MHz flash, $V_{DD} = 3.0$ V <ul style="list-style-type: none"> at 25 °C | — | 91 | 136.5 | μA | |
| I_{DD_VLPR} | Very-low-power run mode current— 2 MHz LIRC mode, While(1) loop in flash all peripheral clock disable, 125 kHz core / 31.25 kHz flash, $V_{DD} = 3.0$ V <ul style="list-style-type: none"> at 25 °C | — | 34 | 51 | μA | |

Table continues on the next page...

Table 38. Power consumption operating behaviors (continued)

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|------------------|---|------------------|--------------------------------|--------------------------------------|---------------|-------|
| I_{DD_VLPR} | Very-low-power run mode current— 8 MHz LIRC mode, While(1) loop in flash all peripheral clock disable, 4 MHz core / 1 MHz flash, $V_{DD} = 3.0\text{ V}$ • at 25 °C | — | 212 | 318 | μA | |
| I_{DD_VLPR} | Very-low-power run mode current—8 MHz LIRC mode, While(1) loop in flash all peripheral clock enable, 4 MHz core / 1 MHz flash, $V_{DD} = 3.0\text{ V}$ • at 25 °C | — | 302 | 392.6 | μA | |
| I_{DD_WAIT} | Wait mode current—core disabled, 48 MHz system/24 MHz bus, flash disabled (flash doze enabled), all peripheral clocks disabled, MCG_Lite under HIRC mode, $V_{DD} = 3.0\text{ V}$ • at 25 °C | — | 1.81 | 2.12 | mA | |
| I_{DD_WAIT} | Wait mode current—core disabled, 24 MHz system/12 MHz bus, flash disabled (flash doze enabled), all peripheral clocks disabled, MCG_Lite under HIRC mode, $V_{DD} = 3.0\text{ V}$ • at 25 °C | — | 1.27 | 1.46 | mA | |
| I_{DD_VLPW} | Very-low-power wait mode current, core disabled, 4 MHz system/ 1 MHz bus and flash, all peripheral clocks disabled, $V_{DD} = 3.0\text{ V}$ • at 25 °C | — | 156 | 193.2 | μA | |
| I_{DD_VLPW} | Very-low-power wait mode current, core disabled, 2 MHz system/ 0.5 MHz bus and flash, all peripheral clocks disabled, $V_{DD} = 3.0\text{ V}$ • at 25 °C | — | 63 | 100.8 | μA | |
| I_{DD_VLPW} | Very-low-power wait mode current, core disabled, 125 kHz system/ 31.25 kHz bus and flash, all peripheral clocks disabled, $V_{DD} = 3.0\text{ V}$ • at 25 °C | — | 32 | 48 | μA | |
| I_{DD_PSTOP2} | Partial Stop 2, core and system clock disabled, 12 MHz bus and flash, $V_{DD} = 3.0\text{ V}$ • at 25 °C | — | 1.68 | 2.05 | mA | |
| I_{DD_PSTOP2} | Partial Stop 2, core and system clock disabled, flash doze enabled, 12 MHz bus, $V_{DD} = 3.0\text{ V}$ • at 25 °C | — | 1.05 | 1.26 | mA | |
| I_{DD_STOP} | Stop mode current at 3.0 V • at 25 °C and below • at 50 °C • at 85 °C • at 105 °C | — — — — | 158.1 171 203.8 251.7 | 175.81 180.24 228.64 300.06 | μA | |

Table continues on the next page...

Table 39. Low power mode peripheral adders — typical value (continued)

| Symbol | Description | Temperature (°C) | | | | | | Unit |
|--------------------|--|------------------|-----|-----|-----|-----|-----|------|
| | | -40 | 25 | 50 | 70 | 85 | 105 | |
| | entering all modes with the crystal enabled. <ul style="list-style-type: none"> VLLS1 VLLS3 LLS VLPS STOP | 440 | 490 | 540 | 560 | 570 | 580 | nA |
| | | 490 | 490 | 540 | 560 | 570 | 680 | |
| | | 510 | 560 | 560 | 560 | 610 | 680 | |
| | | 510 | 560 | 560 | 560 | 610 | 680 | |
| I _{LPTMR} | LPTMR peripheral adder measured by placing the device in VLLS1 mode with LPTMR enabled using LPO. | 30 | 30 | 30 | 85 | 100 | 200 | nA |
| I _{CMP} | CMP peripheral adder measured by placing the device in VLLS1 mode with CMP enabled using the 6-bit DAC and a single external input for compare. Includes 6-bit DAC power consumption. | 16 | 16 | 16 | 16 | 16 | 16 | μA |
| I _{RTC} | RTC peripheral adder measured by placing the device in VLLS1 mode with external 32 kHz crystal enabled by means of the RTC_CR[OSCE] bit and the RTC ALARM set for 1 minute. Includes ERCLK32K (32 kHz external crystal) power consumption. | 430 | 500 | 500 | 530 | 530 | 760 | nA |
| I _{UART} | UART peripheral adder measured by placing the device in STOP or VLPS mode with selected clock source waiting for RX data at 115200 baud rate. Includes selected clock source power consumption. | | | | | | | μA |
| | <ul style="list-style-type: none"> IRC8M (8 MHz internal reference clock) | 96 | 96 | 96 | 96 | 96 | 96 | |
| | <ul style="list-style-type: none"> IRC2M (2 MHz internal reference clock) | 31 | 31 | 31 | 31 | 31 | 31 | |
| I _{TPM} | TPM peripheral adder measured by placing the device in STOP or VLPS mode with selected clock source configured for output compare generating 100 Hz clock signal. No load is placed on the I/O generating the clock signal. Includes selected clock source and I/O switching currents. | | | | | | | μA |
| | <ul style="list-style-type: none"> IRC8M (8 MHz internal reference clock) IRC2M (2 MHz internal reference clock) | 130 | 130 | 130 | 130 | 130 | 130 | |

Table continues on the next page...

5.3.6.1.2 16-bit ADC electrical characteristics

Table 55. 16-bit ADC characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$)

| Symbol | Description | Conditions ¹ | Min. | Typ. ² | Max. | Unit | Notes |
|----------------|---------------------------------|---|----------------------------------|------------------------------|------------------------------|------------------------------|-----------------------------------|
| I_{DDA_ADC} | Supply current | | 0.215 | — | 1.7 | mA | 3 |
| f_{ADACK} | ADC asynchronous clock source | <ul style="list-style-type: none"> • ADLPC = 1, ADHSC = 0 • ADLPC = 1, ADHSC = 1 • ADLPC = 0, ADHSC = 0 • ADLPC = 0, ADHSC = 1 | 1.2 2.4 3.0 4.4 | 2.4 4.0 5.2 6.2 | 3.9 6.1 7.3 9.5 | MHz MHz MHz MHz | $t_{ADACK} = 1/f_{ADACK}$ |
| | Sample Time | See Reference Manual chapter for sample times | | | | | |
| TUE | Total unadjusted error | <ul style="list-style-type: none"> • 12-bit modes • <12-bit modes | — — | ± 2 ± 1.4 | ± 6.8 ± 2.1 | LSB ⁴ | 5 |
| DNL | Differential non-linearity | <ul style="list-style-type: none"> • 12-bit modes • <12-bit modes | — — | ± 0.7 ± 0.2 | –1.1 to +1.9 –0.3 to 0.5 | LSB ⁴ | 5 |
| INL | Integral non-linearity | <ul style="list-style-type: none"> • 12-bit modes • <12-bit modes | — — | ± 0.9 ± 0.4 | –2.7 to +1.9 –0.7 to +0.5 | LSB ⁴ | 5 |
| E_{FS} | Full-scale error | <ul style="list-style-type: none"> • 12-bit modes • <12-bit modes | — — | –4 –1.4 | –5.4 –1.8 | LSB ⁴ | $V_{ADIN} = V_{DDA}$ ⁵ |
| E_Q | Quantization error | <ul style="list-style-type: none"> • 16-bit modes • ≤ 13-bit modes | — — | –1 to 0 — | — ± 0.5 | LSB ⁴ | |
| ENOB | Effective number of bits | 16-bit differential mode <ul style="list-style-type: none"> • Avg = 32 • Avg = 4 16-bit single-ended mode <ul style="list-style-type: none"> • Avg = 32 • Avg = 4 | 12.8 11.9 12.2 11.4 | 14.5 13.8 13.9 13.1 | — — — — | bits bits bits bits | 6 |
| SINAD | Signal-to-noise plus distortion | See ENOB | $6.02 \times \text{ENOB} + 1.76$ | | | dB | |
| THD | Total harmonic distortion | 16-bit differential mode <ul style="list-style-type: none"> • Avg = 32 16-bit single-ended mode | — — | –94 –85 | — — | dB dB | 7 |

Table continues on the next page...

Table 62. SPI slave mode timing on slew rate disabled pads (continued)

| Num. | Symbol | Description | Min. | Max. | Unit | Note |
|------|--------------|--------------------------------|-------------------|-------------------|--------------|------|
| 4 | t_{Lag} | Enable lag time | 1 | — | t_{periph} | — |
| 5 | t_{WSPSCK} | Clock (SPSCK) high or low time | $t_{periph} - 30$ | — | ns | — |
| 6 | t_{SU} | Data setup time (inputs) | 2.5 | — | ns | — |
| 7 | t_{HI} | Data hold time (inputs) | 3.5 | — | ns | — |
| 8 | t_a | Slave access time | — | t_{periph} | ns | 3 |
| 9 | t_{dis} | Slave MISO disable time | — | t_{periph} | ns | 4 |
| 10 | t_v | Data valid (after SPSCK edge) | — | 31 | ns | — |
| 11 | t_{HO} | Data hold time (outputs) | 0 | — | ns | — |
| 12 | t_{RI} | Rise time input | — | $t_{periph} - 25$ | ns | — |
| | t_{FI} | Fall time input | | | | |
| 13 | t_{RO} | Rise time output | — | 25 | ns | — |
| | t_{FO} | Fall time output | | | | |

1. For SPI0 f_{periph} is the bus clock (f_{BUS}). For SPI1 f_{periph} is the system clock (f_{SYS}).

2. $t_{periph} = 1/f_{periph}$

3. Time to data active from high-impedance state

4. Hold time to high-impedance state

Table 63. SPI slave mode timing on slew rate enabled pads

| Num. | Symbol | Description | Min. | Max. | Unit | Note |
|------|--------------|--------------------------------|-----------------------|-------------------|--------------|------|
| 1 | f_{op} | Frequency of operation | 0 | $f_{periph}/4$ | Hz | 1 |
| 2 | t_{SPSCK} | SPSCK period | $4 \times t_{periph}$ | — | ns | 2 |
| 3 | t_{Lead} | Enable lead time | 1 | — | t_{periph} | — |
| 4 | t_{Lag} | Enable lag time | 1 | — | t_{periph} | — |
| 5 | t_{WSPSCK} | Clock (SPSCK) high or low time | $t_{periph} - 30$ | — | ns | — |
| 6 | t_{SU} | Data setup time (inputs) | 2 | — | ns | — |
| 7 | t_{HI} | Data hold time (inputs) | 7 | — | ns | — |
| 8 | t_a | Slave access time | — | t_{periph} | ns | 3 |
| 9 | t_{dis} | Slave MISO disable time | — | t_{periph} | ns | 4 |
| 10 | t_v | Data valid (after SPSCK edge) | — | 122 | ns | — |
| 11 | t_{HO} | Data hold time (outputs) | 0 | — | ns | — |
| 12 | t_{RI} | Rise time input | — | $t_{periph} - 25$ | ns | — |
| | t_{FI} | Fall time input | | | | |
| 13 | t_{RO} | Rise time output | — | 36 | ns | — |
| | t_{FO} | Fall time output | | | | |

1. For SPI0 f_{periph} is the bus clock (f_{BUS}). For SPI1 f_{periph} is the system clock (f_{SYS}).

2. $t_{periph} = 1/f_{periph}$

3. Time to data active from high-impedance state

4. Hold time to high-impedance state

For all other partner-developed software and tools, visit <http://www.freescale.com/partners>.

7 Part identification

7.1 Description

Part numbers for the chip have fields that identify the specific part. You can use the values of these fields to determine the specific part you have received.

7.2 Format

Part numbers for this device have the following format:

Q KL## A FFF R T PP CC N

7.3 Fields

This table lists the possible values for each field in the part number (not all combinations are valid):

Table 67. Part number fields description

| Field | Description | Values |
|-------|-----------------------------|---|
| Q | Qualification status | <ul style="list-style-type: none"> M = Fully qualified, general market flow P = Prequalification |
| KL## | Kinetis family | <ul style="list-style-type: none"> KL17 |
| A | Key attribute | <ul style="list-style-type: none"> Z = Cortex-M0+ |
| FFF | Program flash memory size | <ul style="list-style-type: none"> 32 = 32 KB 64 = 64 KB |
| R | Silicon revision | <ul style="list-style-type: none"> (Blank) = Main A = Revision after main |
| T | Temperature range (°C) | <ul style="list-style-type: none"> V = -40 to 105 |
| PP | Package identifier | <ul style="list-style-type: none"> FM = 32 QFN (5 mm x 5 mm) FT = 48 QFN (7 mm x 7 mm)¹ LH = 64 LQFP (10 mm x 10 mm) MP = 64 MAPBGA (5 mm x 5 mm)¹ DA = 36 XFBGA (3.5 mm x 3.5 mm) |
| CC | Maximum CPU frequency (MHz) | <ul style="list-style-type: none"> 4 = 48 MHz |

Table continues on the next page...

Table 67. Part number fields description (continued)

| Field | Description | Values |
|-------|----------------|--|
| N | Packaging type | <ul style="list-style-type: none"> R = Tape and reel (Blank) = Trays |

1. This package for this product is not yet available. However, it is included in Package Your Way program for Kinetis MCUs. Visit freescale.com/KPYW for more details.

7.4 Example

This is an example part number:

MKL17Z64VLH4

8 Revision history

The following table provides a revision history for this document.

Table 68. Revision history

| Rev. No. | Date | Substantial Changes |
|----------|-----------------|---|
| 4 | 28 January/2015 | Initial public release <ul style="list-style-type: none"> Updated the features and completed the ordering information. Updated Table 9 - Power consumption operating behaviors with Max. values. Added a note before Table 9. Updated Table 17 - IRC48M specifications. Updated Table 28. VREF full-range (-40 – 105 °C) operating behaviors with Min., Max., and Typical values. Added Table 36 - I²C 1Mbit/s timing. |
| 4.1 | 2 February/2015 | <ul style="list-style-type: none"> Moved the ordering information out of the front page to be a separate chapter. Added Module signal description table and Package dimension sections. |
| 5 | 21 April/2015 | <ul style="list-style-type: none"> 32-pin QFN package is now standard part, added Marking information and thermal attributes of this package Added Overview chapter Added Memory map chapter Added Pin properties Added a note to the t_{rd1all} in Flash timing specifications — commands Added a note to the Maximum of f_{SCL} in the fast mode in Inter-Integrated Circuit Interface (I2C) timing Added a footnote to the Δfirc48m_ol_hv in MCG-Lite specifications Added Design considerations chapter |