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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I²C, FlexIO, SPI, UART/USART
Peripherals	DMA, I²S, PWM, WDT
Number of I/O	28
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 11x16b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	32-UFQFN Exposed Pad
Supplier Device Package	32-QFN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mkl17z64vfm4r

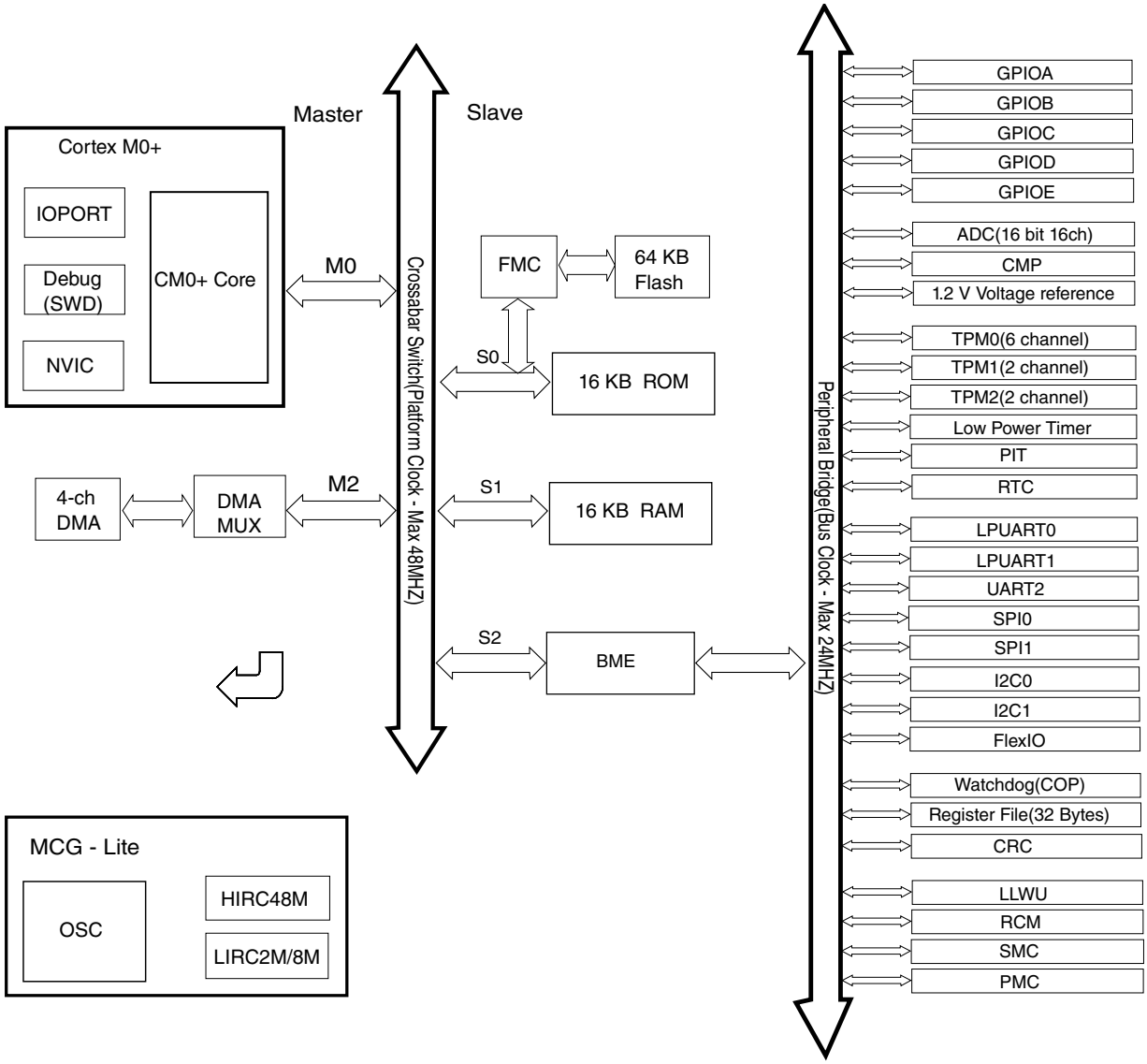


Figure 1. System diagram

The crossbar switch connects bus masters and slaves using a crossbar switch structure. This structure allows up to four bus masters to access different bus slaves simultaneously, while providing arbitration among the bus masters when they access the same slave.

2.1 System features

The following sections describe the high-level system features.

2.1.5 Reset and boot

The following table lists all the reset sources supported by this device.

NOTE

In the following table, Y means the specific module, except for the registers, bits or conditions mentioned in the footnote, is reset by the corresponding Reset source. N means the specific module is not reset by the corresponding Reset source.

Table 3. Reset source

Reset sources	Descriptions	Modules								
		PMC	SIM	SMC	RCM	LLWU	Reset pin is negated	RTC	LPTMR	Others
POR reset	Power-on reset (POR)	Y	Y	Y	Y	Y	Y	Y	Y	Y
System resets	Low-voltage detect (LVD)	Y[1]	Y	Y	Y	Y	Y	N	Y	Y
	Low leakage wakeup (LLWU) reset	N	Y[2]	N	Y	N	Y[3]	N	N	Y
	External pin reset ($\overline{\text{RESET}}$)	Y[1]	Y[2]	Y[4]	Y	Y	Y	N	N	Y
	Computer operating properly (COP) watchdog reset	Y[1]	Y[2]	Y[4]	Y[5]	Y	Y	N	N	Y
	Stop mode acknowledge error (SACKERR)	Y[1]	Y[2]	Y[4]	Y[5]	Y	Y	N	N	Y
	Software reset (SW)	Y[1]	Y[2]	Y[4]	Y[5]	Y	Y	N	N	Y
	Lockup reset (LOCKUP)	Y[1]	Y[2]	Y[4]	Y[5]	Y	Y	N	N	Y
	MDM DAP system reset	Y[1]	Y[2]	Y[4]	Y[5]	Y	Y	N	N	Y
Debug reset	Debug reset	Y[1]	Y[2]	Y[4]	Y[5]	Y	Y	N	N	Y

1. Except PMC_LVDSC1[LVDV] and PMC_LVDSC2[LVWV]
2. Except SIM_SOPT1
3. Only if $\overline{\text{RESET}}$ is used to wake from VLLS mode.
4. Except SMC_PMCTRL, SMC_STOPCTRL, SMC_PMSTAT
5. Except RCM_RPFC, RCM_RPFW, RCM_FM

The CM0+ core adds support for a programmable Vector Table Offset Register (VTOR) to relocate the exception vector table after reset. This device supports booting from:

- internal flash
- boot ROM

Table 4. Module clocks (continued)

Module	Bus interface clock	Internal clocks	I/O interface clocks
I^2C1	System Clock	—	I2C1_SCL
LPUART0, LPUART1	Bus clock	LPUART0 clock LPUART1 clock	—
UART2	Bus clock	—	—
FlexIO	Bus clock	FlexIO clock	—
Human-machine interfaces			
GPIO	Platform clock	—	—

2.1.7 Security

Security state can be enabled via programming flash configuration field (0x40e). After enabling device security, the SWD port cannot access the memory resources of the MCU, and ROM boot loader is also limited to access flash and not allowed to read out flash information via ROM boot loader commands.

Access interface	Secure state	Unsecure operation
SWD port	Cannot access memory source by SWD interface	The debugger can write to the Flash Mass Erase in Progress field of the MDM-AP Control register to trigger a mass erase (Erase All Blocks) command
ROM boot loader Interface (UART/I2C/SPI)	Limit access to the flash, cannot read out flash content	Send “FlashEraseAllUnsecureh" command or attempt to unlock flash security using the backdoor key

This device features 80-bit unique identification number, which is programmed in factory and loaded to SIM register after power-on reset.

2.1.8 Power management

The Power Management Controller (PMC) expands upon ARM’s operational modes of Run, Sleep, and Deep Sleep, to provide multiple configurable modes. These modes can be used to optimize current consumption for a wide range of applications. The WFI or WFE instruction invokes a Wait or a Stop mode, depending on the current configuration. For more information on ARM’s operational modes, See the ARM® Cortex User Guide.

Table 6. Peripherals states in different operational modes (continued)

Core mode	Device mode	Descriptions
Deep sleep	Stop	In Stop mode, most peripheral clocks are disabled and placed in a static state. Stop mode retains all registers and SRAMs while maintaining Low Voltage Detection protection. In Stop mode, the ADC, CMP, LPTimer, RTC, and pin interrupts are operational. The NVIC is disabled, but the AWIC can be used to wake up from an interrupt.
	Very Low Power Stop	In VLPS mode, the contents of the SRAM are retained. The CMP (low speed), ADC, OSC, RTC, LPTMR, TPM, FlexIO, LPUART, and DMA are operational, LVD and NVIC are disabled, AWIC is used to wake up from interrupt.
	Low Leakage Stop	In LLS mode, the contents of the SRAM and the 32-byte system register file are retained. The CMP (low speed), LLWU, LPTMR, and RTC are operational. The ADC, CRC, DMA, FlexIO, I2C, LPUART, MCG-Lite, NVIC, PIT, SPI, TPM, UART, and COP are static, but retain their programming. The GPIO, and VREF are static, retain their programming, and continue to drive their previous values.
	Very Low Leakage Stop	In VLLS modes, most peripherals are powered off and will resume operation from their reset state when the device wakes up. The LLWU, LPTMR, and RTC are operational in all VLLS modes. In VLLS3, the contents of the SRAM and the 32-byte system register file are retained. The CMP (low speed), and PMC are operational. The GPIO, and VREF are not operational but continue driving. In VLLS1, the contents of the 32-byte system register file are retained. The CMP (low speed), and PMC are operational. The GPIO, and VREF are not operational but continue driving. In VLLS0, the contents of the 32-byte system register file are retained. The PMC is operational. The GPIO is not operational but continues driving. The POR detection circuit can be enabled or disabled.

2.1.9 LLWU

The LLWU module is used to wake MCU from low leakage power mode (LLS and VLLSx) and functional only on entry into a low-leakage power mode. After recovery from LLS, the LLWU is immediately disabled. After recovery from VLLSx, the LLWU continues to detect wake-up events until the user has acknowledged the wake-up event.

This device uses 8 external wakeup pin inputs and 4 internal modules as wakeup sources to the LLWU module.

The following is internal peripheral and external pin inputs as wakeup sources to the LLWU module.

- Auto-alignment feature for source or destination accesses allows block transfers to occur at the optimal size based on the address, byte count,and programmed size, which significantly improves the speed of block transfer
- Automatic single or double channel linking allows the current DMA channel to automatically trigger a DMA request to the linked channels without CPU intervention

For more information on asynchronous DMA, see AN4631.

2.2.3 TPM

This device contains three low power TPM modules (TPM). All TPM modules are functional in Stop/VLPS mode if the clock source is enabled.

The TPM features include:

- TPM clock mode is selectable from external clock input or internal clock source, HIRC48M clock, external crystal input clock or LIRC2M/8M clock.
- Prescaler divide-by 1, 2, 4, 8, 16, 32, 64, or 128
- TPM includes a 16-bit counter
- Includes 6 channels that can be configured for input capture, output compare, edge-aligned PWM mode, or center-aligned PWM mode
- Support the generation of an interrupt and/or DMA request per channel or counter overflow
- Support selectable trigger input to optionally reset or cause the counter to start or stop incrementing
- Support the generation of hardware triggers when the counter overflows and per channel

2.2.4 ADC

this device contains one ADC module. This ADC module supports hardware triggers from TPM, LPTMR, PIT, RTC, external trigger pin and CMP output. It supports wakeup of MCU in low power mode when using internal clock source or external crystal clock.

ADC module has the following features:

- Linear successive approximation algorithm with up to 16-bit resolution
- Up to four pairs of differential and 17 single-ended external analog inputs
- Support selectable 16-bit, 13-bit, 11-bit, and 9-bit differential output mode, or 16-bit, 12-bit, 10-bit, and 8-bit single-ended output modes

- 1/16 bit-time noise detection
- DMA interface

2.2.12 LPUART

This product contains two Low-Power UART modules, both of their clock sources are selectable from IRC48M, IRC8M/2M or external crystal clock, and can work in Stop and VLPS modes. They also support 4× to 32× data oversampling rate to meet different applications.

The LPUART module has the following features:

- Programmable baud rates (13-bit modulo divider) with configurable oversampling ratio from 4× to 32×
- Transmit and receive baud rate can operate asynchronous to the bus clock and can be configured independently of the bus clock frequency, support operation in Stop mode
- Interrupt, DMA or polled operation
- Hardware parity generation and checking
- Programmable 8-bit, 9-bit or 10-bit character length
- Programmable 1-bit or 2-bit stop bits
- Three receiver wakeup methods
  - Idle line wakeup
  - Address mark wakeup
  - Receive data match
- Automatic address matching to reduce ISR overhead:
  - Address mark matching
  - Idle line address matching
  - Address match start, address match end
- Optional 13-bit break character generation / 11-bit break character detection
- Configurable idle length detection supporting 1, 2, 4, 8, 16, 32, 64 or 128 idle characters
- Selectable transmitter output and receiver input polarity

2.2.13 SPI

This device contains two SPI modules. SPI modules support 8-bit and 16-bit modes. FIFO function is available only on SPI1 module.

The SPI modules have the following features:

4.3.2 System modules

Table 10. System signal descriptions

Chip signal name	Module signal name	Description	I/O
$\overline{\text{NMI}}$	—	Non-maskable interrupt **NOTE:** Driving the $\overline{\text{NMI}}$ signal low forces a non-maskable interrupt, if the $\overline{\text{NMI}}$ function is selected on the corresponding pin.	I
$\overline{\text{RESET}}$	—	Reset bidirectional signal	I/O
VDD	—	MCU power	I
VSS	—	MCU ground	I

Table 11. LLWU signal descriptions

Chip signal name	Module signal name	Description	I/O
LLWU_Pn	LLWU_Pn	Wakeup inputs (n = 5, 6, 7, 8, 9, 10, 14, 15)	I

4.3.3 Clock modules

Table 12. OSC signal descriptions

Chip signal name	Module signal name	Description	I/O
EXTAL0	EXTAL	External clock/Oscillator input	I
XTAL0	XTAL	Oscillator output	O

4.3.4 Analog

This table presents the signal descriptions of the ADC0 module.

Table 13. ADC0 signal descriptions

Chip signal name	Module signal name	Description	I/O
ADC0_DPn	DADP3–DADP0	Differential Analog Channel Inputs	I
ADC0_DMn	DADM3–DADM0	Differential Analog Channel Inputs	I
ADC0_SEn	AD*n*	Single-Ended Analog Channel Inputs	I
VREFH	V_{REFSH}	Voltage Reference Select High	I

Table continues on the next page...

Table 17. TPM1 signal descriptions

Chip signal name	Module signal name	Description	I/O
TPM_CLKIN[1:0]	TPM_EXTCLK	External clock. TPM external clock can be selected to increment the TPM counter on every rising edge synchronized to the counter clock.	I
TPM1_CH[1:0]	TPM_CHn	TPM channel (n = 1 to 0). A TPM channel pin is configured as output when configured in an output compare or PWM mode and the TPM counter is enabled, otherwise the TPM channel pin is an input.	I/O

Table 18. TPM2 signal descriptions

Chip signal name	Module signal name	Description	I/O
TPM_CLKIN[1:0]	TPM_EXTCLK	External clock. TPM external clock can be selected to increment the TPM counter on every rising edge synchronized to the counter clock.	I
TPM2_CH[1:0]	TPM_CHn	TPM channel (n = 1 to 0). A TPM channel pin is configured as output when configured in an output compare or PWM mode and the TPM counter is enabled, otherwise the TPM channel pin is an input.	I/O

Table 19. LPTMR0 signal descriptions

Chip signal name	Module signal name	Description	I/O
LPTMR0_ALT[3:1]	LPTMR0_ALT*n*	Pulse Counter Input pin	I

Table 20. RTC signal descriptions

Chip signal name	Module signal name	Description	I/O
RTC_CLKOUT[1]	RTC_CLKOUT	1 Hz square-wave output or OSCERCLK	O

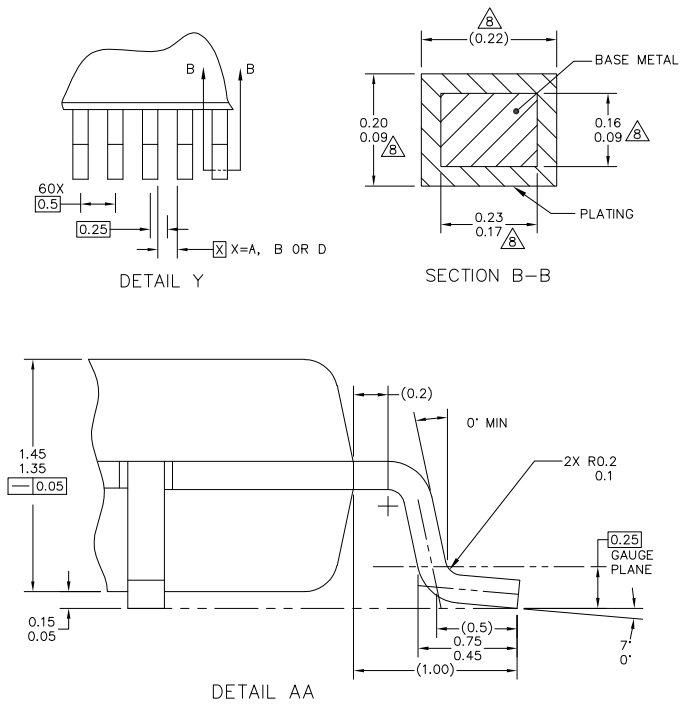
1. RTC_CLKOUT can also be driven with OSCERCLK via SIM control bit SIM_SOPT[RCTCLKOUTSEL]

4.3.6 Communication interfaces

Table 21. SPI0 signal descriptions

Chip signal name	Module signal name	Description	I/O
SPI0_MISO	MISO	Master Data In, Slave Data Out	I/O

Table continues on the next page...



NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. DATUMS A, B AND D TO BE DETERMINED AT DATUM PLANE H.
4. DIMENSIONS TO BE DETERMINED AT SEATING PLANE C.
5. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE UPPER LIMIT BY MORE THAN 0.08 MM AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD SHALL NOT BE LESS THAN 0.07 MM.
6. THIS DIMENSION DOES NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 MM PER SIDE. THIS DIMENSION IS MAXIMUM PLASTIC BODY SIZE DIMENSION INCLUDING MOLD MISMATCH.
7. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.1 MM AND 0.25 MM FROM THE LEAD TIP.

Figure 12. 64-pin LQFP package dimensions 2

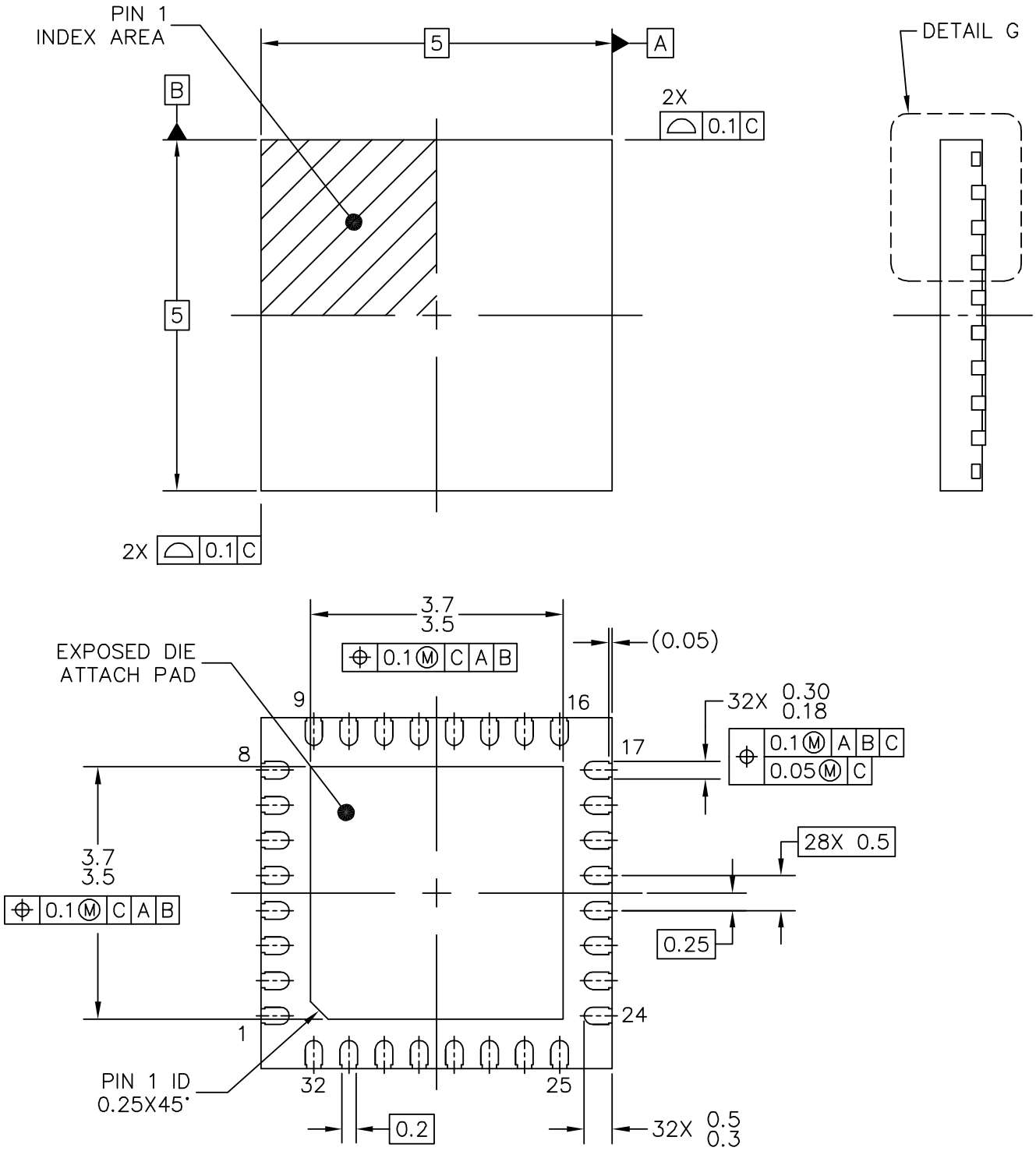
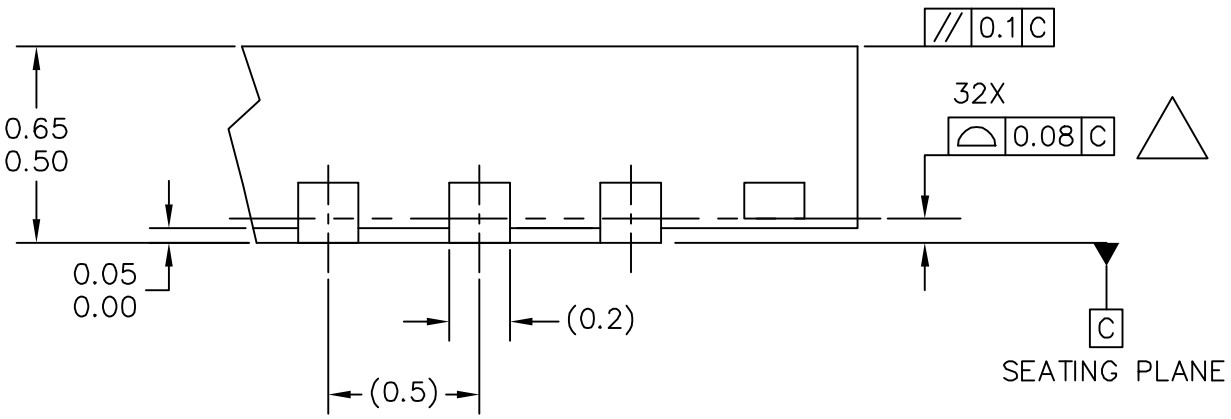


Figure 17. 32-pin QFN package dimension 1



DETAIL G
VIEW ROTATED 90°CW

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. THIS IS A NON–JEDEC REGISTERED PACKAGE.
4. COPLANARITY APPLIES TO LEADS AND DIE ATTACH FLAG.
5. MIN. METAL GAP SHOULD BE 0.2 MM.

Figure 18. 32-pin QFN package dimension 2

5 Electrical characteristics

5.1 Ratings

Table 39. Low power mode peripheral adders — typical value (continued)

Symbol	Description	Temperature (°C)						Unit
		-40	25	50	70	85	105	
	entering all modes with the crystal enabled. • VLLS1 • VLLS3 • LLS • VLPS • STOP	440 490 510 510	490 490 560 560	540 540 560 560	560 560 560 560	570 570 610 610	580 680 680 680	nA
I_{LPTMR}	LPTMR peripheral adder measured by placing the device in VLLS1 mode with LPTMR enabled using LPO.	30	30	30	85	100	200	nA
I_{CMP}	CMP peripheral adder measured by placing the device in VLLS1 mode with CMP enabled using the 6-bit DAC and a single external input for compare. Includes 6-bit DAC power consumption.	16	16	16	16	16	16	µA
I_{RTC}	RTC peripheral adder measured by placing the device in VLLS1 mode with external 32 kHz crystal enabled by means of the RTC_CR[OSCE] bit and the RTC ALARM set for 1 minute. Includes ERCLK32K (32 kHz external crystal) power consumption.	430	500	500	530	530	760	nA
I_{UART}	UART peripheral adder measured by placing the device in STOP or VLPS mode with selected clock source waiting for RX data at 115200 baud rate. Includes selected clock source power consumption. • IRC8M (8 MHz internal reference clock) • IRC2M (2 MHz internal reference clock)	96 31	96 31	96 31	96 31	96 31	96 31	µA
I_{TPM}	TPM peripheral adder measured by placing the device in STOP or VLPS mode with selected clock source configured for output compare generating 100 Hz clock signal. No load is placed on the I/O generating the clock signal. Includes selected clock source and I/O switching currents. • IRC8M (8 MHz internal reference clock) • IRC2M (2 MHz internal reference clock)	130	130	130	130	130	130	µA

Table continues on the next page...

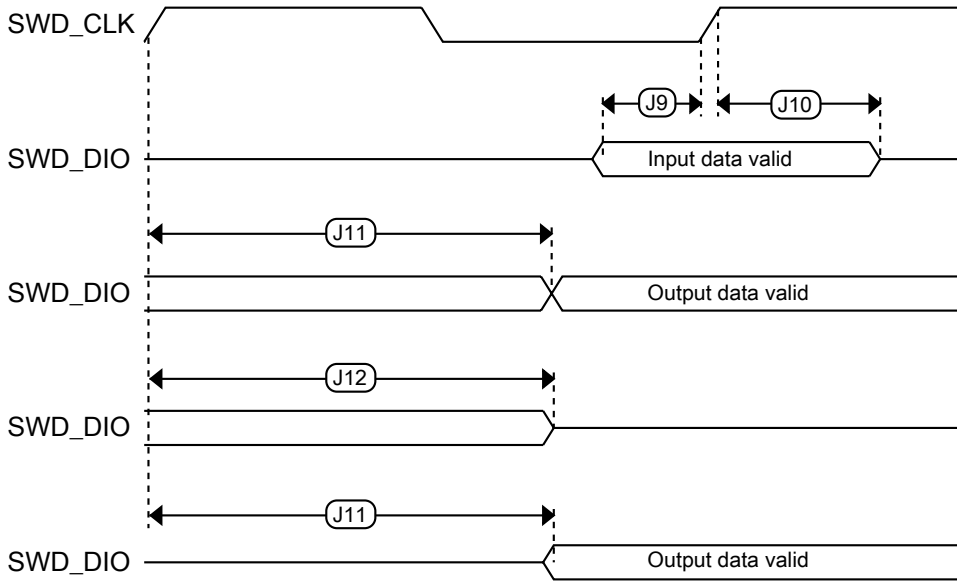


Figure 23. Serial wire data timing

5.3.2 System modules

There are no specifications necessary for the device's system modules.

5.3.3 Clock modules

5.3.3.1 MCG-Lite specifications

Table 46. IRC48M specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I_{DD48M}	Supply current	—	400	500	µA	
f_{irc48m}	Internal reference frequency	—	48	—	MHz	
$\Delta f_{irc48m\_ol\_lv}$	Open loop total deviation of IRC48M frequency at low voltage (VDD=1.71V-1.89V) over temperature	—	± 0.5	± 1.5	$\%f_{irc48m}$	
$\Delta f_{irc48m\_ol\_hv}$	Open loop total deviation of IRC48M frequency at high voltage (VDD=1.89V-3.6V) over temperature	—	± 0.5	± 1.0	$\%f_{irc48m}$	1
J_{cyc_irc48m}	Period Jitter (RMS)	—	35	150	ps	
$t_{irc48mst}$	Startup time	—	2	3	µs	2

1. The maximum value represents characterized results equivalent to the mean plus or minus three times the standard deviation (mean±3 sigma).
2. IRC48M startup time is defined as the time between clock enablement and clock availability for system use. Enable the clock by one of the following settings:
   - MCG operating in an external clocking mode and MCG_C7[OSCSEL]=10, or
   - SIM_SOPT2[PLLFLLSEL]=11

Table 47. IRC8M/2M specification

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I_{DD_2M}	Supply current in 2 MHz mode	—	14	17	µA	—
I_{DD_8M}	Supply current in 8 MHz mode	—	30	35	µA	—
f_{IRC_2M}	Output frequency	—	2	—	MHz	—
f_{IRC_8M}	Output frequency	—	8	—	MHz	—
$f_{IRC\_T\_2M}$	Output frequency range (trimmed)	—	—	±3	$\%f_{IRC}$	—
$f_{IRC\_T\_8M}$	Output frequency range (trimmed)	—	—	±3	$\%f_{IRC}$	—
T_{su_2M}	Startup time	—	—	12.5	µs	—
T_{su_8M}	Startup time	—	—	12.5	µs	—

5.3.3.2 Oscillator electrical specifications

5.3.3.2.1 Oscillator DC electrical specifications

Table 48. Oscillator DC electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{DD}	Supply voltage	1.71	—	3.6	V	
I_{DDOSC}	Supply current — low-power mode (HGO=0)					1
	• 32 kHz	—	500	—	nA	
	• 4 MHz	—	200	—	µA	
	• 8 MHz (RANGE=01)	—	300	—	µA	
	• 16 MHz	—	950	—	µA	
	• 24 MHz	—	1.2	—	mA	
	• 32 MHz	—	1.5	—	mA	
I_{DDOSC}	Supply current — high gain mode (HGO=1)					1
	• 32 kHz	—	25	—	µA	
	• 4 MHz	—	400	—	µA	
	• 8 MHz (RANGE=01)	—	500	—	µA	
	• 16 MHz	—	2.5	—	mA	
	• 24 MHz	—	3	—	mA	
	• 32 MHz	—	4	—	mA	

Table continues on the next page...

Table 53. NVM reliability specifications (continued)

Symbol	Description	Min.	Typ.[1]	Max.	Unit	Notes
$t_{nvmretp10k}$	Data retention after up to 10 K cycles	5	50	—	years	—
$t_{nvmretp1k}$	Data retention after up to 1 K cycles	20	100	—	years	—
$n_{nvmcycp}$	Cycling endurance	10 K	50 K	—	cycles	2

1. Typical data retention values are based on measured response accelerated at high temperature and derated to a constant 25 °C use profile. Engineering Bulletin EB618 does not apply to this technology. Typical endurance defined in Engineering Bulletin EB619.
2. Cycling endurance represents number of program/erase cycles at –40 °C ≤ T_j ≤ 125 °C.

5.3.5 Security and integrity modules

There are no specifications necessary for the device's security and integrity modules.

5.3.6 Analog

5.3.6.1 ADC electrical specifications

Using differential inputs can achieve better system accuracy than using single-end inputs.

5.3.6.1.1 16-bit ADC operating conditions

Table 54. 16-bit ADC operating conditions

Symbol	Description	Conditions	Min.	Typ.[1]	Max.	Unit	Notes
V_{DDA}	Supply voltage	Absolute	1.71	—	3.6	V	—
ΔV_{DDA}	Supply voltage	Delta to V_{DD} (V_{DD} – V_{DDA})	-100	0	+100	mV	2
ΔV_{SSA}	Ground voltage	Delta to V_{SS} (V_{SS} – V_{SSA})	-100	0	+100	mV	2
V_{ADIN}	Input voltage	• 16-bit differential mode • All other modes	VREFL VREFL	— —	31/32 × VREFH VREFH	V	—
C_{ADIN}	Input capacitance	• 16-bit mode • 8-bit / 10-bit / 12-bit modes	— —	8 4	10 5	pF	—
R_{ADIN}	Input series resistance		—	2	5	kΩ	—
R_{AS}	Analog source resistance (external)	13-bit / 12-bit modes f_{ADCK} < 4 MHz	—	—	5	kΩ	3

Table continues on the next page...

5.3.6.1.2 16-bit ADC electrical characteristics

Table 55. 16-bit ADC characteristics (V_{REFH} = V_{DDA}, V_{REFL} = V_{SSA})

Symbol	Description	Conditions[1]	Min.	Typ.[2]	Max.	Unit	Notes
I_{DDA_ADC}	Supply current		0.215	—	1.7	mA	3
f_{ADACK}	ADC asynchronous clock source	• ADLPC = 1, ADHSC = 0 • ADLPC = 1, ADHSC = 1 • ADLPC = 0, ADHSC = 0 • ADLPC = 0, ADHSC = 1	1.2 2.4 3.0 4.4	2.4 4.0 5.2 6.2	3.9 6.1 7.3 9.5	MHz MHz MHz MHz	t_{ADACK} = $1/f_{ADACK}$
	Sample Time	See Reference Manual chapter for sample times					
TUE	Total unadjusted error	• 12-bit modes • <12-bit modes	— —	±2 ±1.4	±6.8 ±2.1	LSB[4]	5
DNL	Differential non-linearity	• 12-bit modes • <12-bit modes	— —	±0.7 ±0.2	–1.1 to +1.9 –0.3 to 0.5	LSB[4]	5
INL	Integral non-linearity	• 12-bit modes • <12-bit modes	— —	±0.9 ±0.4	–2.7 to +1.9 –0.7 to +0.5	LSB[4]	5
E_{FS}	Full-scale error	• 12-bit modes • <12-bit modes	— —	–4 –1.4	–5.4 –1.8	LSB[4]	V_{ADIN} = V_{DDA}[5]
E_Q	Quantization error	• 16-bit modes • ≤13-bit modes	— —	–1 to 0 —	— ±0.5	LSB[4]	
ENOB	Effective number of bits	16-bit differential mode • Avg = 32 • Avg = 4 16-bit single-ended mode • Avg = 32 • Avg = 4	 12.8 11.9 12.2 11.4	 14.5 13.8 13.9 13.1	 — — — —	 bits bits bits bits	6
SINAD	Signal-to-noise plus distortion	See ENOB	6.02 × ENOB + 1.76			dB	
THD	Total harmonic distortion	16-bit differential mode • Avg = 32 16-bit single-ended mode	 — —	 –94 –85	 — —	 dB dB	7

Table continues on the next page...

All timing is shown with respect to 20% V_{DD} and 80% V_{DD} thresholds, unless noted, as well as input signal transitions of 3 ns and a 30 pF maximum load on all SPI pins.

Table 60. SPI master mode timing on slew rate disabled pads

Num.	Symbol	Description	Min.	Max.	Unit	Note
1	f_{op}	Frequency of operation	$f_{periph}/2048$	$f_{periph}/2$	Hz	1
2	t_{SPSCK}	SPSCK period	2 x t_{periph}	2048 x t_{periph}	ns	2
3	t_{Lead}	Enable lead time	1/2	—	t_{SPSCK}	—
4	t_{Lag}	Enable lag time	1/2	—	t_{SPSCK}	—
5	t_{WSPSCK}	Clock (SPSCK) high or low time	t_{periph} - 30	1024 x t_{periph}	ns	—
6	t_{SU}	Data setup time (inputs)	18	—	ns	—
7	t_{HI}	Data hold time (inputs)	0	—	ns	—
8	t_{v}	Data valid (after SPSCK edge)	—	15	ns	—
9	t_{HO}	Data hold time (outputs)	0	—	ns	—
10	t_{RI}	Rise time input	—	t_{periph} - 25	ns	—
	t_{FI}	Fall time input				
11	t_{RO}	Rise time output	—	25	ns	—
	t_{FO}	Fall time output				

1. For SPI0 f_{periph} is the bus clock (f_{BUS}). For SPI1 f_{periph} is the system clock (f_{SYS}).
2. $t_{periph} = 1/f_{periph}$

Table 61. SPI master mode timing on slew rate enabled pads

Num.	Symbol	Description	Min.	Max.	Unit	Note
1	f_{op}	Frequency of operation	$f_{periph}/2048$	$f_{periph}/2$	Hz	1
2	t_{SPSCK}	SPSCK period	2 x t_{periph}	2048 x t_{periph}	ns	2
3	t_{Lead}	Enable lead time	1/2	—	t_{SPSCK}	—
4	t_{Lag}	Enable lag time	1/2	—	t_{SPSCK}	—
5	t_{WSPSCK}	Clock (SPSCK) high or low time	t_{periph} - 30	1024 x t_{periph}	ns	—
6	t_{SU}	Data setup time (inputs)	96	—	ns	—
7	t_{HI}	Data hold time (inputs)	0	—	ns	—
8	t_{v}	Data valid (after SPSCK edge)	—	52	ns	—
9	t_{HO}	Data hold time (outputs)	0	—	ns	—
10	t_{RI}	Rise time input	—	t_{periph} - 25	ns	—
	t_{FI}	Fall time input				
11	t_{RO}	Rise time output	—	36	ns	—
	t_{FO}	Fall time output				

1. For SPI0 f_{periph} is the bus clock (f_{BUS}). For SPI1 f_{periph} is the system clock (f_{SYS}).
2. $t_{periph} = 1/f_{periph}$

Table 65. I²C 1Mbit/s timing

Characteristic	Symbol	Minimum	Maximum	Unit
SCL Clock Frequency	f_{SCL}	0	1[1]	MHz
Hold time (repeated) START condition. After this period, the first clock pulse is generated.	t_{HD}; STA	0.26	—	µs
LOW period of the SCL clock	t_{LOW}	0.5	—	µs
HIGH period of the SCL clock	t_{HIGH}	0.26	—	µs
Set-up time for a repeated START condition	t_{SU}; STA	0.26	—	µs
Data hold time for I_2C bus devices	t_{HD}; DAT	0	—	µs
Data set-up time	t_{SU}; DAT	50	—	ns
Rise time of SDA and SCL signals	t_r	20 +0.1C_b	120	ns
Fall time of SDA and SCL signals	t_f	20 +0.1C_b[2]	120	ns
Set-up time for STOP condition	t_{SU}; STO	0.26	—	µs
Bus free time between STOP and START condition	t_{BUF}	0.5	—	µs
Pulse width of spikes that must be suppressed by the input filter	t_{SP}	0	50	ns

1. The maximum SCL clock frequency of 1 Mbit/s can support maximum bus loading when using the high drive pins across the full voltage range.
2. C_b = total capacitance of the one bus line in pF.

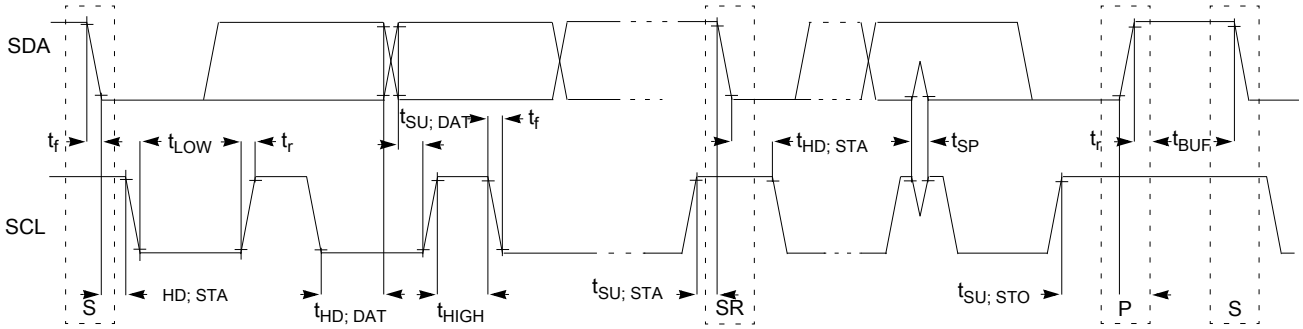


Figure 33. Timing definition for devices on the I²C bus

5.5.3 UART

See General switching specifications.

6 Design considerations

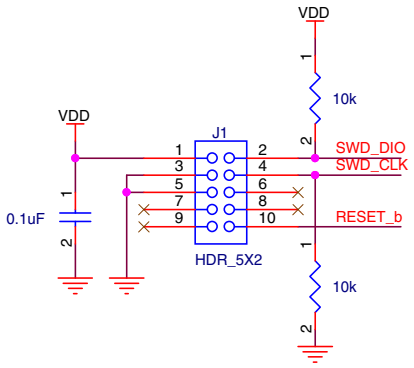


Figure 39. SWD debug interface

- Low leakage stop mode wakeup

  Select low leakage wakeup pins (LLWU_Px) to wake the MCU from one of the low leakage stop modes (LLS/VLLSx). See KL17 Signal Multiplexing and Pin Assignments for pin selection.

- Unused pin

  Unused GPIO pins must be left floating (no electrical connections) with the MUX field of the pin's PORTx_PCRn register equal to 0:0:0. This disables the digital input path to the MCU.

6.1.5 Crystal oscillator

When using an external crystal or ceramic resonator as the frequency reference for the MCU clock system, refer to the following table and diagrams.

The feedback resistor, RF, is incorporated internally with the low power oscillators. An external feedback is required when using high gain (HGO=1) mode.

The series resistor, RS, is required in high gain (HGO=1) mode when the crystal or resonator frequency is below 2MHz. Otherwise, the low power oscillator (HGO=0) must not have any series resistance; and the high frequency, high gain oscillator with a frequency above 2MHz does not require any series resistance.

Internal load capacitors (Cx, Cy) are provided in the low frequency (32.786kHz) mode. Use the SCxP bits in the OSC0_CR register to adjust the load capacitance for the crystal. Typically, values of 10pf to 16pF are sufficient for 32.768kHz crystals that have a 12.5pF CL specification. The internal load capacitor selection must not be used for high frequency crystals and resonators.

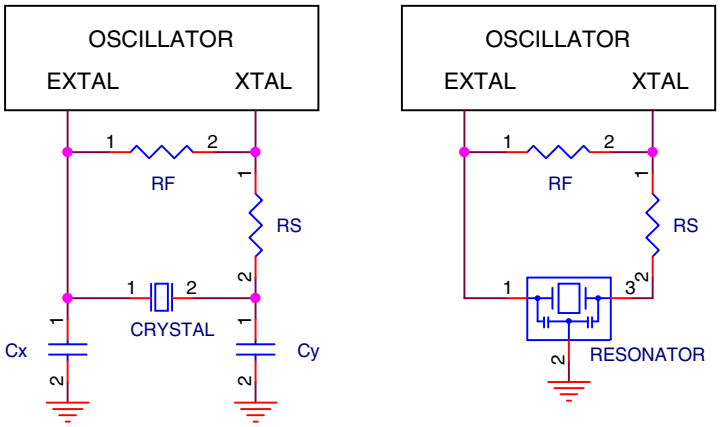


Figure 43. Crystal connection – Diagram 4

6.2 Software considerations

All Kinetis MCUs are supported by comprehensive Freescale and third-party hardware and software enablement solutions, which can reduce development costs and time to market. Featured software and tools are listed below. Visit http://www.freescale.com/kinetis/sw for more information and supporting collateral.

Evaluation and Prototyping Hardware

- Freescale Freedom Development Platform: http://www.freescale.com/freedom
- Tower System Development Platform: http://www.freescale.com/tower

IDEs for Kinetis MCUs

- Kinetis Design Studio IDE: http://www.freescale.com/kds
- Partner IDEs: http://www.freescale.com/kide

Development Tools

- PEG Graphics Software: http://www.freescale.com/peg
- Processor Expert Software and Embedded Components: http://www.freescale.com/processorexpert)

Run-time Software

- Kinetis SDK: http://www.freescale.com/ksdk
- Kinetis Bootloader: http://www.freescale.com/kboot
- ARM mbed Development Platform: http://www.freescale.com/mbed
- MQX RTOS: http://www.freescale.com/mqx