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Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I ² C, FlexIO, SPI, UART/USART
Peripherals	DMA, I ² S, PWM, WDT
Number of I/O	54
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 20x16b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mkl17z64vlh4

Table 2. AWIC stop wake-up sources (continued)

Wake-up source	Description
I ² Cx	Address match wakeup
LPUART0 , LPUART1	Any enabled interrupt can be a source as long as the module remains clocked
UART2	Active edge on RXD
RTC	Alarm or seconds interrupt
NMI	NMI pin
TPMx	Any enabled interrupt can be a source as long as the module remains clocked
LPTMR	Any enabled interrupt can be a source as long as the module remains clocked
SPIx	Slave mode interrupt
FlexIO	Any enabled interrupt can be a source as long as the module remains clocked

2.1.4 Memory

This device has the following features:

- 8/16 KB of embedded RAM accessible (read/write) at CPU clock speed with 0 wait states.
- The non-volatile memory is divided into two arrays
 - 32/64 KB of embedded program memory
 - 16 KB ROM (built-in bootloader to support UART, I2C, and SPI interfaces)

The program flash memory contains a 16-byte flash configuration field that stores default protection settings and security information. The page size of program flash is 1 KB.

The protection setting can protect 32 regions of the program flash memory from unintended erase or program operations.

The security circuitry prevents unauthorized access to RAM or flash contents from debug port.

- System register file

This device contains a 32-byte register file that is powered in all power modes.

Also, it retains contents during low power modes and is reset only during a power-on reset.

2.1.5 Reset and boot

The following table lists all the reset sources supported by this device.

NOTE

In the following table, Y means the specific module, except for the registers, bits or conditions mentioned in the footnote, is reset by the corresponding Reset source. N means the specific module is not reset by the corresponding Reset source.

Table 3. Reset source

Reset sources	Descriptions	Modules								
		PMC	SIM	SMC	RCM	LLWU	Reset pin is negated	RTC	LPTMR	Others
POR reset	Power-on reset (POR)	Y	Y	Y	Y	Y	Y	Y	Y	Y
System resets	Low-voltage detect (LVD)	Y ¹	Y	Y	Y	Y	Y	N	Y	Y
	Low leakage wakeup (LLWU) reset	N	Y ²	N	Y	N	Y ³	N	N	Y
	External pin reset (RESET)	Y ¹	Y ²	Y ⁴	Y	Y	Y	N	N	Y
	Computer operating properly (COP) watchdog reset	Y ¹	Y ²	Y ⁴	Y ⁵	Y	Y	N	N	Y
	Stop mode acknowledge error (SACKERR)	Y ¹	Y ²	Y ⁴	Y ⁵	Y	Y	N	N	Y
	Software reset (SW)	Y ¹	Y ²	Y ⁴	Y ⁵	Y	Y	N	N	Y
	Lockup reset (LOCKUP)	Y ¹	Y ²	Y ⁴	Y ⁵	Y	Y	N	N	Y
	MDM DAP system reset	Y ¹	Y ²	Y ⁴	Y ⁵	Y	Y	N	N	Y
Debug reset	Debug reset	Y ¹	Y ²	Y ⁴	Y ⁵	Y	Y	N	N	Y

1. Except PMC_LVDSC1[LVDV] and PMC_LVDSC2[LVWV]
2. Except SIM_SOPT1
3. Only if RESET is used to wake from VLLS mode.
4. Except SMC_PMCTRL, SMC_STOPCTRL, SMC_PMSTAT
5. Except RCM_RPFC, RCM_RPFW, RCM_FM

The CM0+ core adds support for a programmable Vector Table Offset Register (VTOR) to relocate the exception vector table after reset. This device supports booting from:

- internal flash
- boot ROM

The system oscillator supports low frequency crystals (32 kHz to 40 kHz), high frequency crystals (1 MHz to 32 MHz), and ceramic resonators (1 MHz to 32 MHz). An external clock source, DC to 48 MHz, can be used as the system clock through the EXTAL0 pin. The external oscillator also supports a low speed external clock (32.768 kHz) on the RTC_CLKIN pin for use with the RTC.

For more details on the clock operations and configurations, see Reference Manual.

The following figure is a high level block diagram of the clock generation.

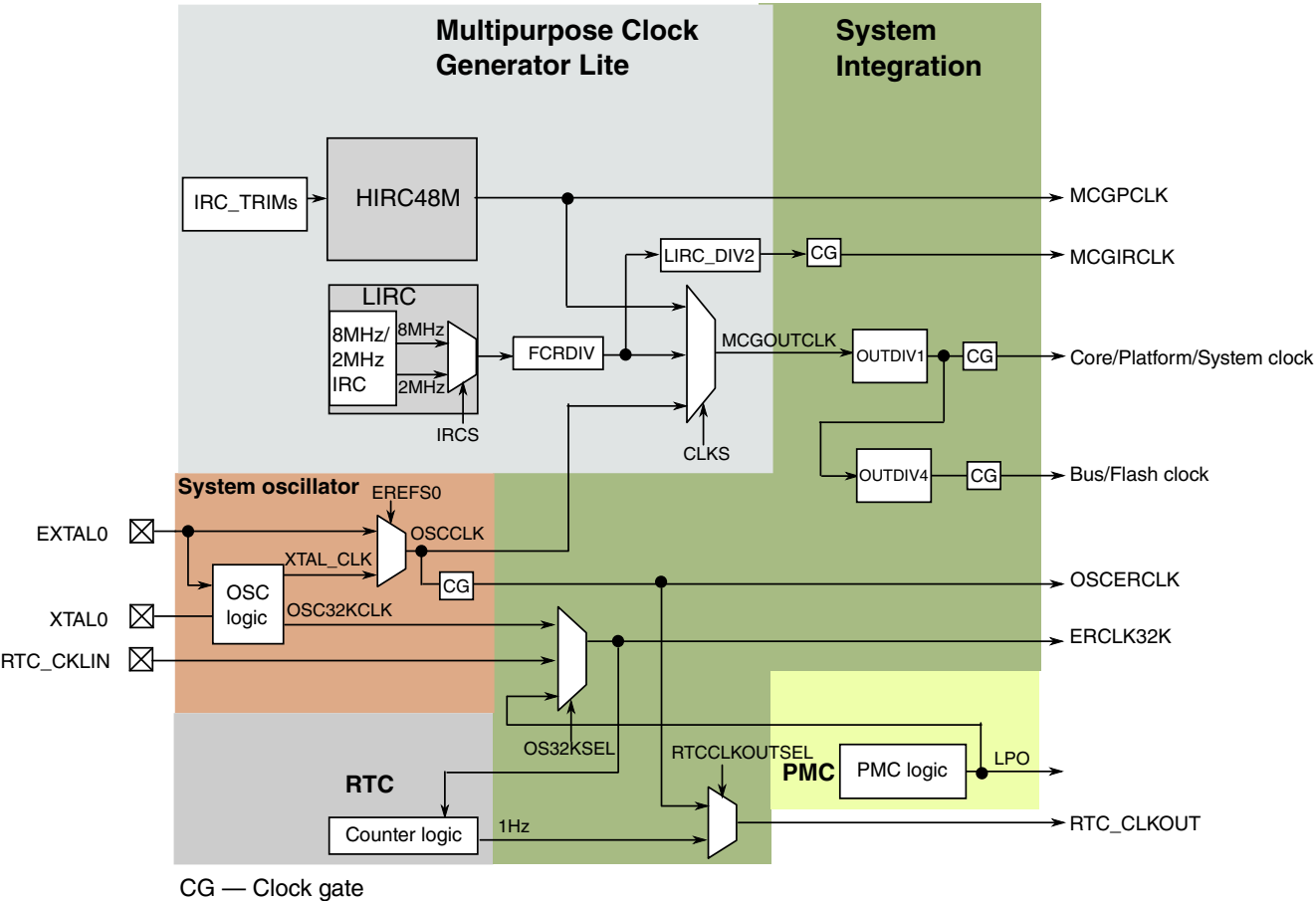


Figure 3. Clock block diagram

In order to provide flexibility, many peripherals can select from multiple clock sources for operation. This enables the peripheral to select a clock that will always be available during operation in various operational modes.

The following table summarizes the clocks associated with each module.

The PMC provides Run (Run), and Very Low Power Run (VLPR) configurations in ARM's Run operation mode. In these modes, the MCU core is active and can access all peripherals. The difference between the modes is the maximum clock frequency of the system and therefore the power consumption. The configuration that matches the power versus performance requirements of the application can be selected.

The PMC provides Wait (Wait) and Very Low Power Wait (VLPW) configurations in ARM's Sleep operation mode. In these modes, even though the MCU core is inactive, all of the peripherals can be enabled and operate as programmed. The difference between the modes is the maximum clock frequency of the system and therefore the power consumption.

The PMC provides Stop (Stop), Very Low Power Stop (VLPS), Low Leakage Stop (LLS), and Very Low Leakage Stop (VLLS) configurations in ARM's Deep Sleep operational mode. In these modes, the MCU core and most of the peripherals are disabled. Depending on the requirements of the application, different portions of the analog, logic, and memory can be retained or disabled to conserve power.

The Nested Vectored Interrupt Controller (NVIC), the Asynchronous Wake-up Interrupt Controller (AWIC), and the Low Leakage Wake-Up Controller (LLWU) are used to wake up the MCU from low power states. The NVIC is used to wake up the MCU core from WAIT and VLPW modes. The AWIC is used to wake up the MCU core from STOP and VLPS modes. The LLWU is used to wake up the MCU core from LLS and VLLSx modes.

For additional information regarding operational modes, power management, the NVIC, AWIC, or the LLWU, please refer to the Reference Manual.

The following table provides information about the state of the peripherals in the various operational modes and the modules that can wake MCU from low power modes.

Table 6. Peripherals states in different operational modes

Core mode	Device mode	Descriptions
Run mode	Run	In Run mode, all device modules are operational.
	Very Low Power Run	In VLPR mode, all device modules are operational at a reduced frequency except the Low Voltage Detect (LVD) monitor, which is disabled.
Sleep mode	Wait	In Wait mode, all peripheral modules are operational. The MCU core is placed into Sleep mode.
	Very Low Power Wait	In VLPW mode, all peripheral modules are operational at a reduced frequency except the Low Voltage Detect (LVD) monitor, which is disabled. The MCU core is placed into Sleep mode.

Table continues on the next page...

- 16-bit prescaler with compensation that can correct errors between 0.12 ppm and 3906 ppm
- Register write protection with register lock mechanism
- 1 Hz square wave or second pulse output with optional interrupt

2.2.8 PIT

The Periodic Interrupt Timer (PIT) is used to generate periodic interrupt to the CPU. It has two independent channels and each channel has a 32-bit counter. Both channels can be chained together to form a 64-bit counter.

Channel 0 can be used to periodically trigger DMA channel 0, and channel 1 can be used to periodically trigger DMA channel 1. Either channel can be programmed as an ADC trigger source, or TPM trigger source. Channel 0 can be programmed to trigger DAC.

The PIT module has the following features:

- Each 32-bit timers is able to generate DMA trigger
- Each 32-bit timers is able to generate timeout interrupts
- Two timers can be cascaded to form a 64-bit timer
- Each timer can be programmed as ADC/TPM trigger source
- Timer 0 is able to trigger DAC

2.2.9 LPTMR

The low-power timer (LPTMR) can be configured to operate as a time counter with optional prescaler, or as a pulse counter with optional glitch filter, across all power modes, including the low-leakage modes. It can also continue operating through most system reset events, allowing it to be used as a time of day counter.

The LPTMR module has the following features:

- 16-bit time counter or pulse counter with compare
 - Optional interrupt can generate asynchronous wakeup from any low-power mode
 - Hardware trigger output
 - Counter supports free-running mode or reset on compare
- Configurable clock source for prescaler/glitch filter
- Configurable input source for pulse counter

2.2.10 CRC

This device contains one cyclic redundancy check (CRC) module which can generate 16/32-bit CRC code for error detection.

The CRC module provides a programmable polynomial, WAS, and other parameters required to implement a 16-bit or 32-bit CRC standard.

The CRC module has the following features:

- Hardware CRC generator circuit using a 16-bit or 32-bit programmable shift register
- Programmable initial seed value and polynomial
- Option to transpose input data or output data (the CRC result) bitwise or byte-wise.
- Option for inversion of final CRC result
- 32-bit CPU register programming interface

2.2.11 UART

This device contains a basic universal asynchronous receiver/transmitter (UART) module with DMA function supported. Generally, this module is used in RS-232, RS-485, and other communications and supports LIN slave operation and ISO7816.

The UART module has the following features:

- Full-duplex operation
- 13-bit baud rate selection with /32 fractional divide, based on the module clock frequency
- Programmable 8-bit or 9-bit data format
- Programmable transmitter output polarity
- Programmable receive input polarity
- Up to 14-bit break character transmission.
- 11-bit break character detection option
- Two receiver wakeup methods with idle line or address mark wakeup
- Address match feature in the receiver to reduce address mark wakeup ISR overhead
- Ability to select MSB or LSB to be first bit on wire
- Support for ISO 7816 protocol to interface with SIM cards and smart cards
- Receiver framing error detection
- Hardware parity generation and checking

- 1/16 bit-time noise detection
- DMA interface

2.2.12 LPUART

This product contains two Low-Power UART modules, both of their clock sources are selectable from IRC48M, IRC8M/2M or external crystal clock, and can work in Stop and VLPS modes. They also support 4× to 32× data oversampling rate to meet different applications.

The LPUART module has the following features:

- Programmable baud rates (13-bit modulo divider) with configurable oversampling ratio from 4× to 32×
- Transmit and receive baud rate can operate asynchronous to the bus clock and can be configured independently of the bus clock frequency, support operation in Stop mode
- Interrupt, DMA or polled operation
- Hardware parity generation and checking
- Programmable 8-bit, 9-bit or 10-bit character length
- Programmable 1-bit or 2-bit stop bits
- Three receiver wakeup methods
 - Idle line wakeup
 - Address mark wakeup
 - Receive data match
- Automatic address matching to reduce ISR overhead:
 - Address mark matching
 - Idle line address matching
 - Address match start, address match end
- Optional 13-bit break character generation / 11-bit break character detection
- Configurable idle length detection supporting 1, 2, 4, 8, 16, 32, 64 or 128 idle characters
- Selectable transmitter output and receiver input polarity

2.2.13 SPI

This device contains two SPI modules. SPI modules support 8-bit and 16-bit modes. FIFO function is available only on SPI1 module.

The SPI modules have the following features:

Pinouts

64 LQFP	36 XFB GA	32 QFN	48 QFN	64 MAP BGA	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
						ADC0_SE4a	ADC0_SE4a							
11	E1	—	—	G2	PTE22	ADC0_DP3/ ADC0_SE3	ADC0_DP3/ ADC0_SE3	PTE22		TPM2_CH0	UART2_TX		FXIO0_D6	
12	F1	—	—	F2	PTE23	ADC0_DM3/ ADC0_SE7a	ADC0_DM3/ ADC0_SE7a	PTE23		TPM2_CH1	UART2_RX		FXIO0_D7	
13	D3	7	9	F4	VDDA	VDDA	VDDA							
14	D3	7	10	G4	VREFH	VREFH	VREFH							
14	—	—	10	G4	VREFO	VREFO_A	VREFO_A							
15	D4	8	11	G3	VREFL	VREFL	VREFL							
16	D4	8	12	F3	VSSA	VSSA	VSSA							
17	—	—	13	H1	PTE29	CMP0_IN5/ ADC0_SE4b	CMP0_IN5/ ADC0_SE4b	PTE29		TPM0_CH2	TPM_CLKIN0			
18	F2	9	14	H2	PTE30	ADC0_SE23/ CMP0_IN4	ADC0_SE23/ CMP0_IN4	PTE30		TPM0_CH3	TPM_CLKIN1	LPUART1_TX	LPTMR0_ALT1	
19	—	—	—	H3	PTE31	DISABLED		PTE31		TPM0_CH4				
20	—	—	15	H4	PTE24	DISABLED		PTE24		TPM0_CH0		I2C0_SCL		
21	—	—	16	H5	PTE25	DISABLED		PTE25		TPM0_CH1		I2C0_SDA		
22	F3	10	17	D3	PTA0	SWD_CLK		PTA0		TPM0_CH5				SWD_CLK
23	F4	11	18	D4	PTA1	DISABLED		PTA1	LPUART0_RX	TPM2_CH0				
24	E4	12	19	E5	PTA2	DISABLED		PTA2	LPUART0_TX	TPM2_CH1				
25	E5	13	20	D5	PTA3	SWD_DIO		PTA3	I2C1_SCL	TPM0_CH0				SWD_DIO
26	F5	14	21	G5	PTA4	NMI_b		PTA4	I2C1_SDA	TPM0_CH1				NMI_b
27	—	—	—	F5	PTA5	DISABLED		PTA5		TPM0_CH2				
28	—	—	—	H6	PTA12	DISABLED		PTA12		TPM1_CH0				
29	—	—	—	G6	PTA13	DISABLED		PTA13		TPM1_CH1				
30	C3	15	22	G7	VDD	VDD	VDD							
31	C4	16	23	H7	VSS	VSS	VSS							
32	F6	17	24	H8	PTA18	EXTAL0	EXTAL0	PTA18		LPUART1_RX	TPM_CLKIN0			
33	E6	18	25	G8	PTA19	XTAL0	XTAL0	PTA19		LPUART1_TX	TPM_CLKIN1		LPTMR0_ALT1	
34	D5	19	26	F8	PTA20	RESET_b		PTA20						RESET_b
35	D6	20	27	F7	PTB0/ LLWU_P5	ADC0_SE8	ADC0_SE8	PTB0/ LLWU_P5	I2C0_SCL	TPM1_CH0	SPI1_MOSI	SPI1_MISO		
36	C6	21	28	F6	PTB1	ADC0_SE9	ADC0_SE9	PTB1	I2C0_SDA	TPM1_CH1	SPI1_MISO	SPI1_MOSI		

Pinouts

64 LQFP	36 XFBGA	32 QFN	48 QFN	64 MAPBGA	Pin name	Driver strength	Default status after POR	Pullup/ pulldown setting after POR	Slew rate after POR	Passive pin filter after POR	Open drain	Pin interrupt
46	B5	24	36	C8	PTC3/ LLWU_P7	HD	Hi-Z	—	FS	N	N	Y
47	—	—	—	E3	VSS	—	—	—	—	—	—	—
48	—	—	—	E4	VDD	—	—	—	—	—	—	—
49	A6	25	37	B8	PTC4/ LLWU_P8	HD	Hi-Z	—	FS	N	N	Y
50	A5	26	38	A8	PTC5/ LLWU_P9	ND	Hi-Z	—	FS	N	N	Y
51	B4	27	39	A7	PTC6/ LLWU_P10	ND	Hi-Z	—	FS	N	N	Y
52	A4	28	40	B6	PTC7	ND	Hi-Z	—	FS	N	N	Y
53	—	—	—	A6	PTC8	ND	Hi-Z	—	SS	N	N	Y
54	—	—	—	B5	PTC9	ND	Hi-Z	—	SS	N	N	Y
55	—	—	—	B4	PTC10	ND	Hi-Z	—	SS	N	N	Y
56	—	—	—	A5	PTC11	ND	Hi-Z	—	SS	N	N	Y
57	—	—	41	C3	PTD0	ND	Hi-Z	—	FS	N	N	Y
58	—	—	42	A4	PTD1	ND	Hi-Z	—	FS	N	N	Y
59	—	—	43	C2	PTD2	ND	Hi-Z	—	FS	N	N	Y
60	—	—	44	B3	PTD3	ND	Hi-Z	—	FS	N	N	Y
61	A3	29	45	A3	PTD4/ LLWU_P14	ND	Hi-Z	—	FS	N	N	Y
62	B3	30	46	C1	PTD5	ND	Hi-Z	—	FS	N	N	Y
63	B2	31	47	B2	PTD6/ LLWU_P15	HD	Hi-Z	—	FS	N	N	Y
64	A2	32	48	A2	PTD7	HD	Hi-Z	—	FS	N	N	Y

Properties	Abbreviation	Descriptions
Driver strength	ND	Normal drive
	HD	High drive
Default status after POR	Hi-Z	High impedance

Table continues on the next page...

	1	2	3	4	5	6	
A	PTE0	PTD7	PTD4/ LLWU_P14	PTC7	PTC5/ LLWU_P9	PTC4/ LLWU_P8	A
B	PTE1	PTD6/ LLWU_P15	PTD5	PTC6/ LLWU_P10	PTC3/ LLWU_P7	PTC2	B
C	PTE17	PTE16	VDD	VSS	PTC1/ LLWU_P6/ RTC_CLKIN	PTB1	C
D	PTE18	PTE19	VDDA/ VREFH	VREFL/ VSSA	PTA20	PTB0/ LLWU_P5	D
E	PTE22	PTE21	PTE20	PTA2	PTA3	PTA19	E
F	PTE23	VREF0/ PTE30	PTA0	PTA1	PTA4	PTA18	F
	1	2	3	4	5	6	

Figure 10. 36 XFBGA Pinout diagram (transparent top view)

4.5 Package dimensions

The following figures show the dimensions of the package options for the devices supported by this document.



1. ALL DIMENSIONS IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM A.
4. DATUM A, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

Figure 13. 64-pin MAPBGA package dimension

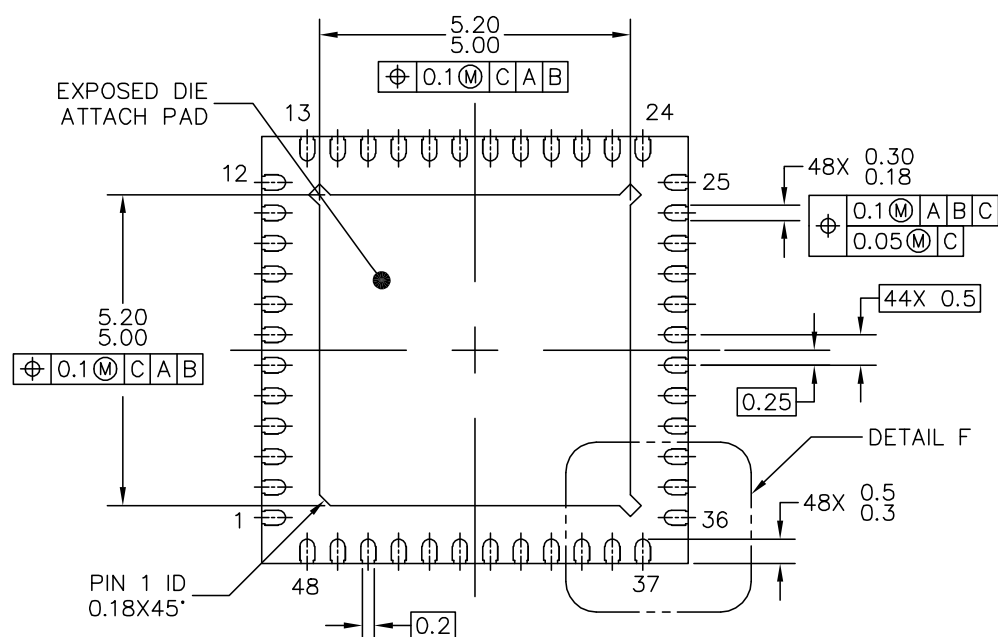
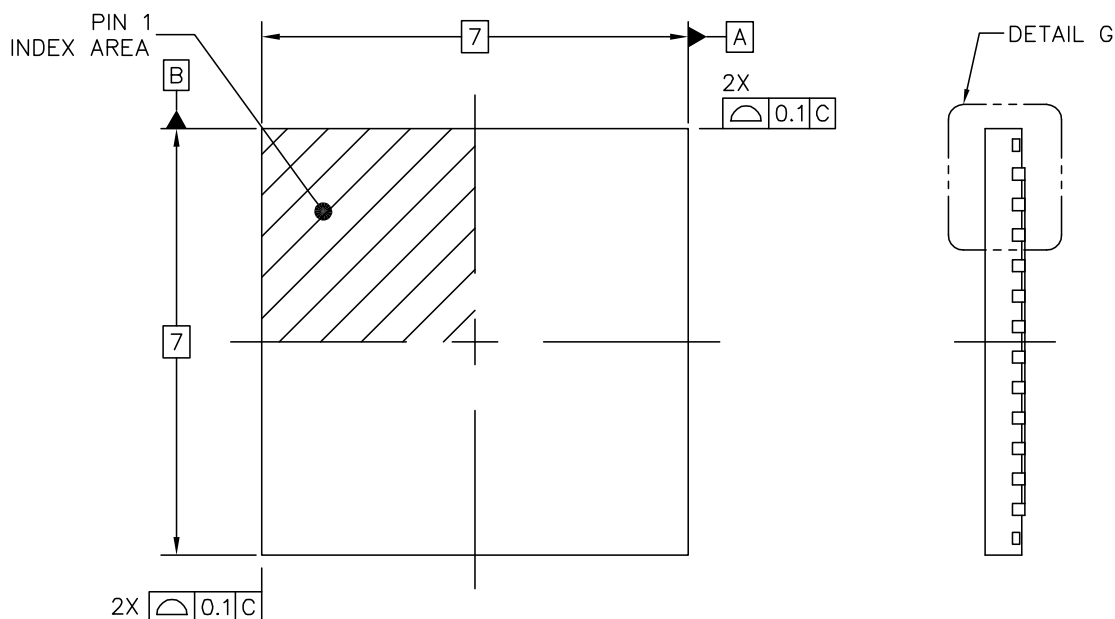


Figure 14. 48-pin QFN package dimension 1

5.2.2.5 Power consumption operating behaviors

The maximum values stated in the following table represent the characterized results equivalent to the mean plus three times the standard deviation (mean + 3 sigma).

NOTE

The while(1) test is executed with flash cache enabled.

Table 38. Power consumption operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I_{DDA}	Analog supply current	—	—	See note	mA	1
I_{DD_RUNCO}	Running CoreMark in flash in compute operation mode—48M HIRC mode, 48 MHz core / 24 MHz flash, $V_{DD} = 3.0$ V <ul style="list-style-type: none"> at 25 °C at 105 °C 	—	4.79 4.94	4.98 5.14	mA	2
I_{DD_RUNCO}	Running While(1) loop in flash in compute operation mode—48M HIRC mode, 48 MHz core / 24 MHz flash, $V_{DD} = 3.0$ V <ul style="list-style-type: none"> at 25 °C at 105 °C 	—	2.73 2.9	2.87 3.05	mA	
I_{DD_RUN}	Run mode current—48M HIRC mode, running CoreMark in Flash all peripheral clock disable 48 MHz core/24 MHz flash, $V_{DD} = 3.0$ V <ul style="list-style-type: none"> at 25 °C at 105 °C 	— —	5.45 5.6	5.67 5.82	mA	2
I_{DD_RUN}	Run mode current—48M HIRC mode, running CoreMark in flash all peripheral clock disable, 24 MHz core/12 MHz flash, $V_{DD} = 3.0$ V <ul style="list-style-type: none"> at 25 °C at 105 °C 	— —	3.41 3.56	3.55 3.70	mA mA	2
I_{DD_RUN}	Run mode current—48M HIRC mode, running CoreMark in Flash all peripheral clock disable 12 MHz core/6 MHz flash, $V_{DD} = 3.0$ V <ul style="list-style-type: none"> at 25 °C at 105 °C 	—	2.37 2.52	2.49 2.65	mA	2
I_{DD_RUN}	Run mode current—48M HIRC mode, running CoreMark in Flash all peripheral clock enable 48 MHz core/24 MHz flash, $V_{DD} = 3.0$ V <ul style="list-style-type: none"> at 25 °C at 105 °C 	—	7.05 7.2	7.33 7.49	mA	2

Table continues on the next page...

5.2.3.2 General switching specifications

These general-purpose specifications apply to all signals configured for GPIO and UART signals.

Table 42. General switching specifications

Description	Min.	Max.	Unit	Notes
GPIO pin interrupt pulse width (digital glitch filter disabled) — Synchronous path	1.5	—	Bus clock cycles	1
External RESET and NMI pin interrupt pulse width — Asynchronous path	100	—	ns	2
GPIO pin interrupt pulse width — Asynchronous path	16	—	ns	2
Port rise and fall time	—	36	ns	3

1. The synchronous and asynchronous timing must be met.
2. This is the shortest pulse that is guaranteed to be recognized.
3. 75 pF load

5.2.4 Thermal specifications

5.2.4.1 Thermal operating requirements

Table 43. Thermal operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
T _J	Die junction temperature	−40	125	°C	
T _A	Ambient temperature	−40	105	°C	1

1. Maximum T_A can be exceeded only if the user ensures that T_J does not exceed the maximum. The simplest method to determine T_J is: $T_J = T_A + R_{\theta JA} \times \text{chip power dissipation}$.

5.2.4.2 Thermal attributes

NOTE

The 48 QFN and 64 MAPBGA packages for this product are not yet available. However, it is included in Package Your Way program for Kinetis MCUs. Visit freescale.com/KPYW for more details.

5.3.3.2.2 Oscillator frequency specifications

Table 49. Oscillator frequency specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
f_{osc_lo}	Oscillator crystal or resonator frequency — low-frequency mode (MCG_C2[RANGE]=00)	32	—	40	kHz	
$f_{osc_hi_1}$	Oscillator crystal or resonator frequency — high-frequency mode (low range) (MCG_C2[RANGE]=01)	3	—	8	MHz	
$f_{osc_hi_2}$	Oscillator crystal or resonator frequency — high frequency mode (high range) (MCG_C2[RANGE]=1x)	8	—	32	MHz	
f_{ec_extal}	Input clock frequency (external clock mode)	—	—	48	MHz	1, 2
t_{dc_extal}	Input clock duty cycle (external clock mode)	40	50	60	%	
t_{cst}	Crystal startup time — 32 kHz low-frequency, low-power mode (HGO=0)	—	750	—	ms	3, 4
	Crystal startup time — 32 kHz low-frequency, high-gain mode (HGO=1)	—	250	—	ms	
	Crystal startup time — 8 MHz high-frequency (MCG_C2[RANGE]=01), low-power mode (HGO=0)	—	0.6	—	ms	
	Crystal startup time — 8 MHz high-frequency (MCG_C2[RANGE]=01), high-gain mode (HGO=1)	—	1	—	ms	

1. Other frequency limits may apply when external clock is being used as a reference for the FLL
2. When transitioning from FEI or FBI to FBE mode, restrict the frequency of the input clock so that, when it is divided by FRDIV, it remains within the limits of the DCO input clock frequency.
3. Proper PC board layout procedures must be followed to achieve specifications.
4. Crystal startup time is defined as the time between the oscillator being enabled and the OSCINIT bit in the MCG_S register being set.

5.3.4 Memories and memory interfaces

5.3.4.1 Flash electrical specifications

This section describes the electrical characteristics of the flash memory module.

5.3.4.1.1 Flash timing specifications — program and erase

The following specifications represent the amount of time the internal charge pumps are active and do not include command overhead.

Table 50. NVM program/erase timing specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$t_{hvp\text{gm}4}$	Longword Program high-voltage time	—	7.5	18	μs	—
$t_{h\text{versscr}}$	Sector Erase high-voltage time	—	13	113	ms	1
$t_{h\text{versall}}$	Erase All high-voltage time	—	52	452	ms	1

1. Maximum time based on expectations at cycling end-of-life.

5.3.4.1.2 Flash timing specifications — commands

Table 51. Flash command timing specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$t_{rd1\text{sec}1k}$	Read 1s Section execution time (flash sector)	—	—	60	μs	1
t_{pgmchk}	Program Check execution time	—	—	45	μs	1
$t_{rd\text{rsrc}}$	Read Resource execution time	—	—	30	μs	1
t_{pgm4}	Program Longword execution time	—	65	145	μs	—
t_{ersscr}	Erase Flash Sector execution time	—	14	114	ms	2
$t_{rd1\text{all}}$	Read 1s All Blocks execution time	—	—	0.9	ms	1
t_{rdonce}	Read Once execution time	—	—	25	μs	1
$t_{pgmonce}$	Program Once execution time	—	65	—	μs	—
t_{ersall}	Erase All Blocks execution time	—	70	575	ms	2
t_{vfykey}	Verify Backdoor Access Key execution time	—	—	30	μs	1
$t_{ersallu}$	Erase All Blocks Unsecure execution time	—	70	575	ms	2

1. Assumes 25 MHz flash clock frequency.

2. Maximum times for erase parameters based on expectations at cycling end-of-life.

5.3.4.1.3 Flash high voltage current behaviors

Table 52. Flash high voltage current behaviors

Symbol	Description	Min.	Typ.	Max.	Unit
I_{DD_PGM}	Average current adder during high voltage flash programming operation	—	2.5	6.0	mA
I_{DD_ERS}	Average current adder during high voltage flash erase operation	—	1.5	4.0	mA

5.3.4.1.4 Reliability specifications

Table 53. NVM reliability specifications

Symbol	Description	Min.	Typ. ¹	Max.	Unit	Notes
Program Flash						

Table continues on the next page...

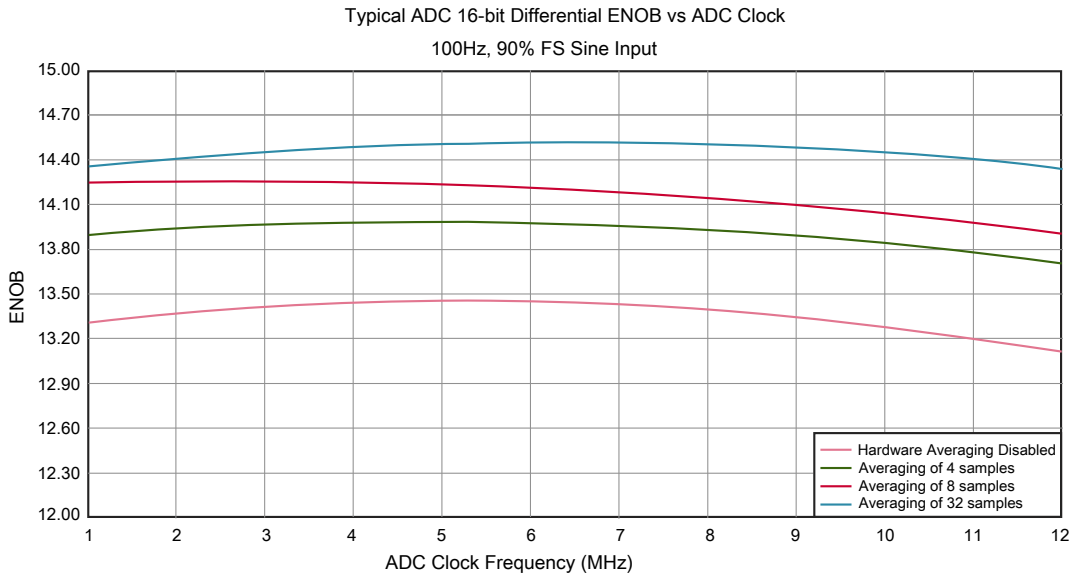


Figure 25. Typical ENOB vs. ADC_CLK for 16-bit differential mode

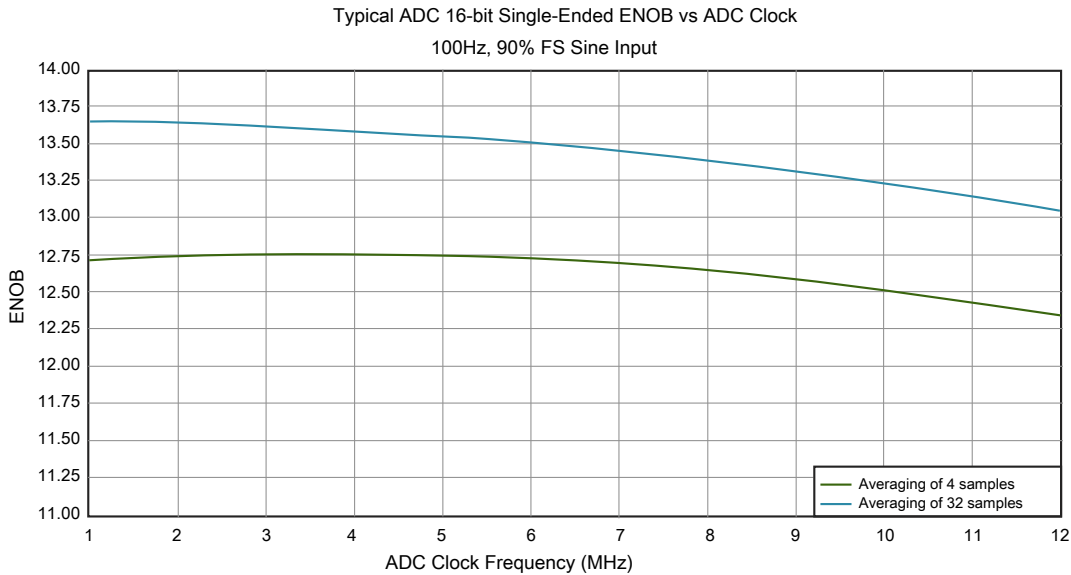


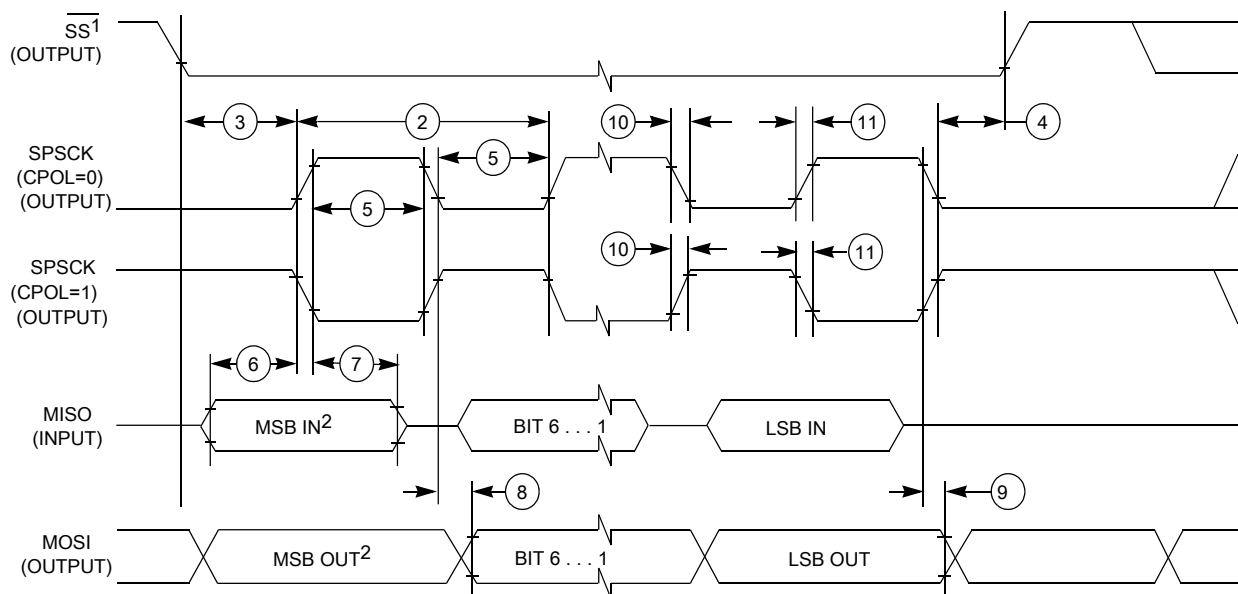
Figure 26. Typical ENOB vs. ADC_CLK for 16-bit single-ended mode

5.3.6.1.3 Voltage reference electrical specifications

Table 56. VREF full-range operating requirements

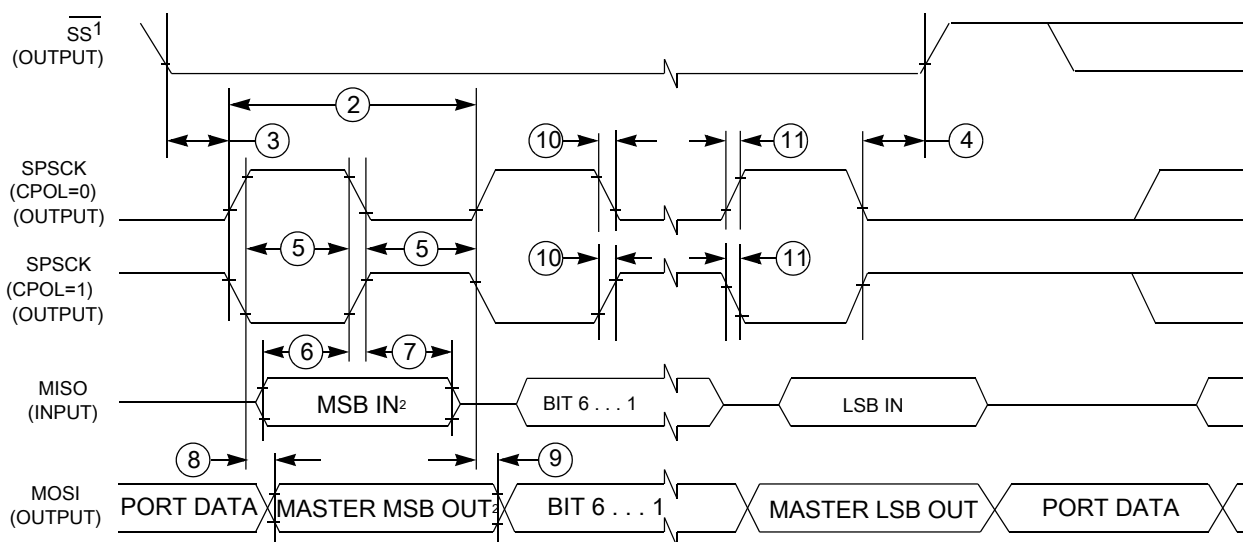
Symbol	Description	Min.	Max.	Unit	Notes
V _{DDA}	Supply voltage		3.6	V	

Table continues on the next page...



1. If configured as an output.
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 29. SPI master mode timing (CPHA = 0)



1. If configured as output
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 30. SPI master mode timing (CPHA = 1)

Table 62. SPI slave mode timing on slew rate disabled pads

Num.	Symbol	Description	Min.	Max.	Unit	Note
1	f_{op}	Frequency of operation	0	$f_{periph}/4$	Hz	1
2	t_{SPSCCK}	SPSCCK period	$4 \times t_{periph}$	—	ns	2
3	t_{Lead}	Enable lead time	1	—	t_{periph}	—

Table continues on the next page...

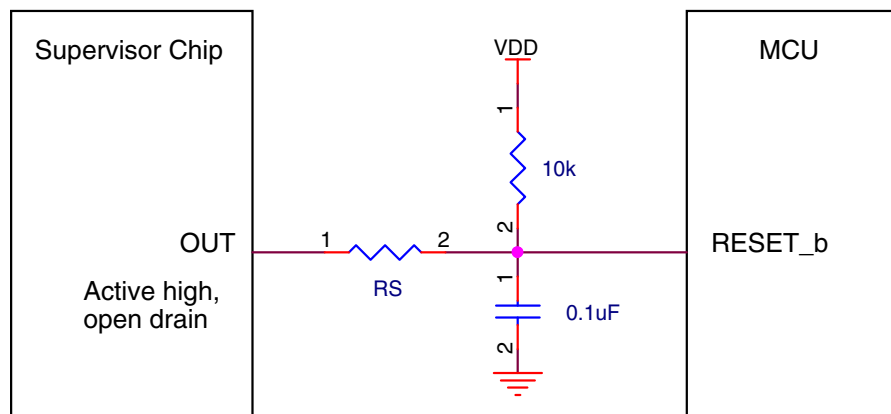


Figure 37. Reset signal connection to external reset chip

- NMI pin

Do not add a pull-down resistor or capacitor on the NMI_b pin, because a low level on this pin will trigger non-maskable interrupt. When this pin is enabled as the NMI function, an external pull-up resistor (10 kΩ) as shown in the following figure is recommended for robustness.

If the NMI_b pin is used as an I/O pin, the non-maskable interrupt handler is required to disable the NMI function by remapping to another function. The NMI function is disabled by programming the FOPT[NMI_DIS] bit to zero.

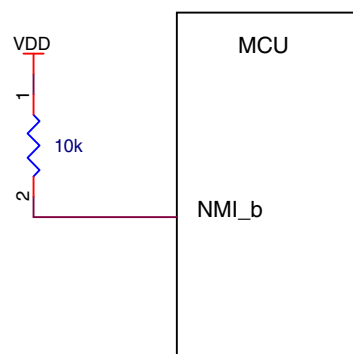


Figure 38. NMI pin biasing

- Debug interface

This MCU uses the standard ARM SWD interface protocol as shown in the following figure. While pull-up or pull-down resistors are not required (SWD_DIO has an internal pull-up and SWD_CLK has an internal pull-down), external 10 kΩ pull resistors are recommended for system robustness. The RESET_b pin recommendations mentioned above must also be considered.

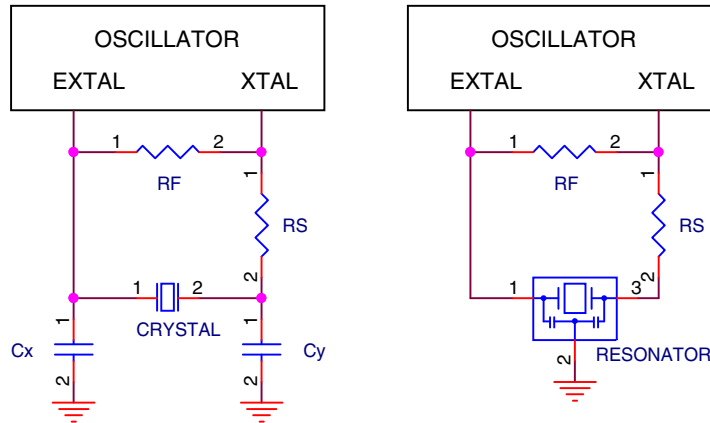


Figure 43. Crystal connection – Diagram 4

6.2 Software considerations

All Kinetis MCUs are supported by comprehensive Freescale and third-party hardware and software enablement solutions, which can reduce development costs and time to market. Featured software and tools are listed below. Visit <http://www.freescale.com/kinetis/sw> for more information and supporting collateral.

Evaluation and Prototyping Hardware

- Freescale Freedom Development Platform: <http://www.freescale.com/freedom>
- Tower System Development Platform: <http://www.freescale.com/tower>

IDEs for Kinetis MCUs

- Kinetis Design Studio IDE: <http://www.freescale.com/kds>
- Partner IDEs: <http://www.freescale.com/kide>

Development Tools

- PEG Graphics Software: <http://www.freescale.com/peg>
- Processor Expert Software and Embedded Components: <http://www.freescale.com/processorexpert>)

Run-time Software

- Kinetis SDK: <http://www.freescale.com/ksdk>
- Kinetis Bootloader: <http://www.freescale.com/kboot>
- ARM mbed Development Platform: <http://www.freescale.com/mbed>
- MQX RTOS: <http://www.freescale.com/mqx>