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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I²C, FlexIO, SPI, UART/USART
Peripherals	DMA, I²S, PWM, WDT
Number of I/O	54
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 20x16b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mkl17z64vlh4r

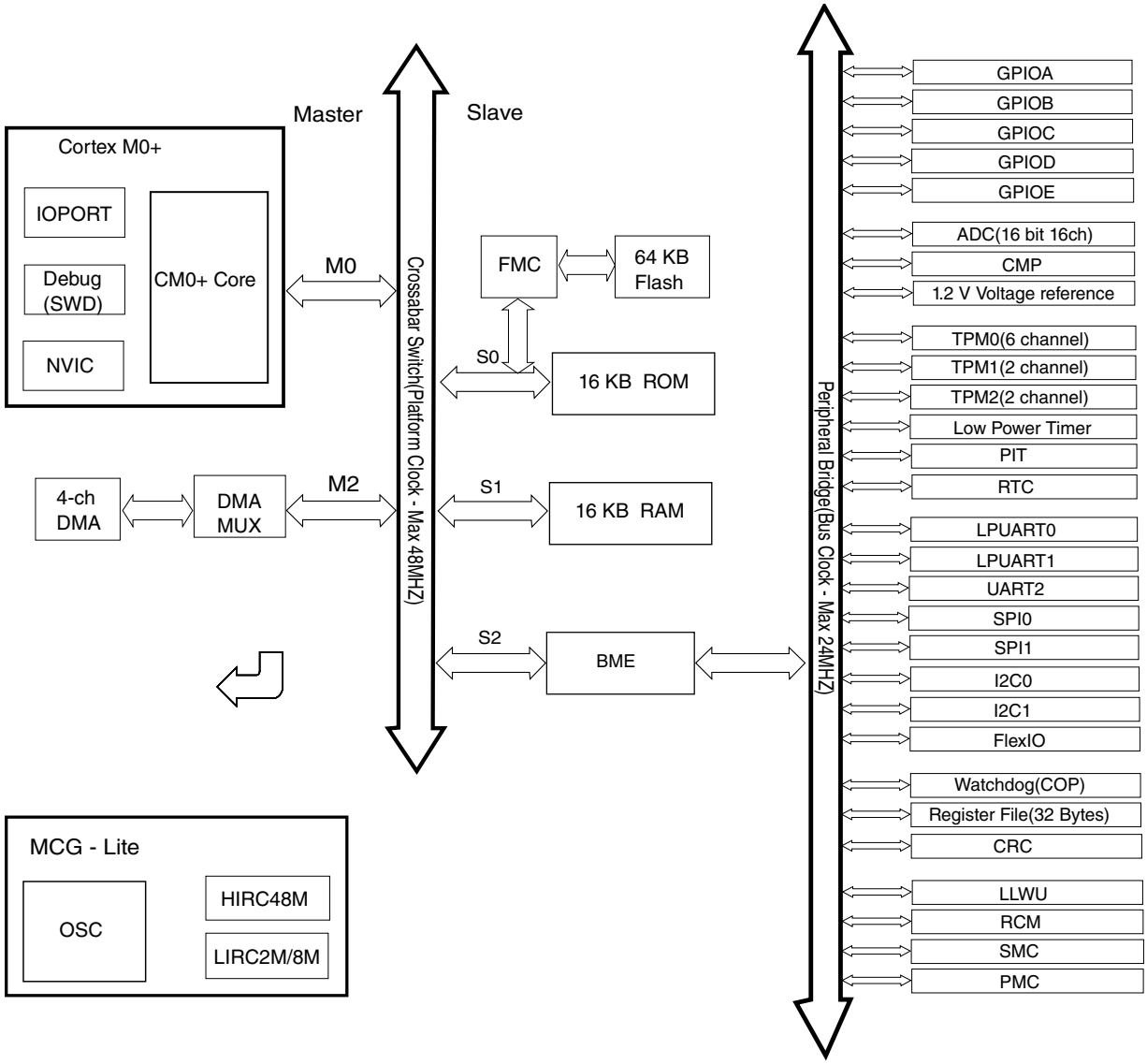

Figure 1. System diagram

The crossbar switch connects bus masters and slaves using a crossbar switch structure. This structure allows up to four bus masters to access different bus slaves simultaneously, while providing arbitration among the bus masters when they access the same slave.

2.1 System features

The following sections describe the high-level system features.

- Auto-alignment feature for source or destination accesses allows block transfers to occur at the optimal size based on the address, byte count,and programmed size, which significantly improves the speed of block transfer
- Automatic single or double channel linking allows the current DMA channel to automatically trigger a DMA request to the linked channels without CPU intervention

For more information on asynchronous DMA, see AN4631.

2.2.3 TPM

This device contains three low power TPM modules (TPM). All TPM modules are functional in Stop/VLPS mode if the clock source is enabled.

The TPM features include:

- TPM clock mode is selectable from external clock input or internal clock source, HIRC48M clock, external crystal input clock or LIRC2M/8M clock.
- Prescaler divide-by 1, 2, 4, 8, 16, 32, 64, or 128
- TPM includes a 16-bit counter
- Includes 6 channels that can be configured for input capture, output compare, edge-aligned PWM mode, or center-aligned PWM mode
- Support the generation of an interrupt and/or DMA request per channel or counter overflow
- Support selectable trigger input to optionally reset or cause the counter to start or stop incrementing
- Support the generation of hardware triggers when the counter overflows and per channel

2.2.4 ADC

this device contains one ADC module. This ADC module supports hardware triggers from TPM, LPTMR, PIT, RTC, external trigger pin and CMP output. It supports wakeup of MCU in low power mode when using internal clock source or external crystal clock.

ADC module has the following features:

- Linear successive approximation algorithm with up to 16-bit resolution
- Up to four pairs of differential and 17 single-ended external analog inputs
- Support selectable 16-bit, 13-bit, 11-bit, and 9-bit differential output mode, or 16-bit, 12-bit, 10-bit, and 8-bit single-ended output modes

2.2.6 CMP

The device contains one high-speed comparator and two 8-input multiplexers for both the inverting and non-inverting inputs of the comparator. Each CMP input channel connects to both muxes.

The CMP includes one 6-bit DAC, which provides a selectable voltage reference for various user application cases. Besides, the CMP also has several module-to-module interconnects in order to facilitate ADC triggering, TPM triggering, and interfaces.

The CMP has the following features:

- Inputs may range from rail to rail
- Programmable hysteresis control
- Selectable interrupt on rising-edge, falling-edge, or both rising or falling edges of the comparator output
- Selectable inversion on comparator output
- Capability to produce a wide range of outputs such as sampled, digitally filtered
- External hysteresis can be used at the same time that the output filter is used for internal functions
- Two software selectable performance levels: shorter propagation delay at the expense of higher power and Low power with longer propagation delay
- DMA transfer support
- Functional in all modes of operation except in VLLS0 mode
- The filter functions are not available in Stop, VLPS, LLS, or VLLSx modes
- Integrated 6-bit DAC with selectable supply reference source and can be power down to conserve power
- Two 8-to-1 channel mux

2.2.7 RTC

The RTC is an always powered-on block that remains active in all low power modes. The time counter within the RTC is clocked by a 32.768 kHz clock sourced from an external crystal using the oscillator or clock directly from RTC_CLKIN pin.

RTC is reset on power-on reset, and a software reset bit in RTC can also initialize all RTC registers.

The RTC module has the following features

- 32-bit seconds counter with roll-over protection and 32-bit alarm

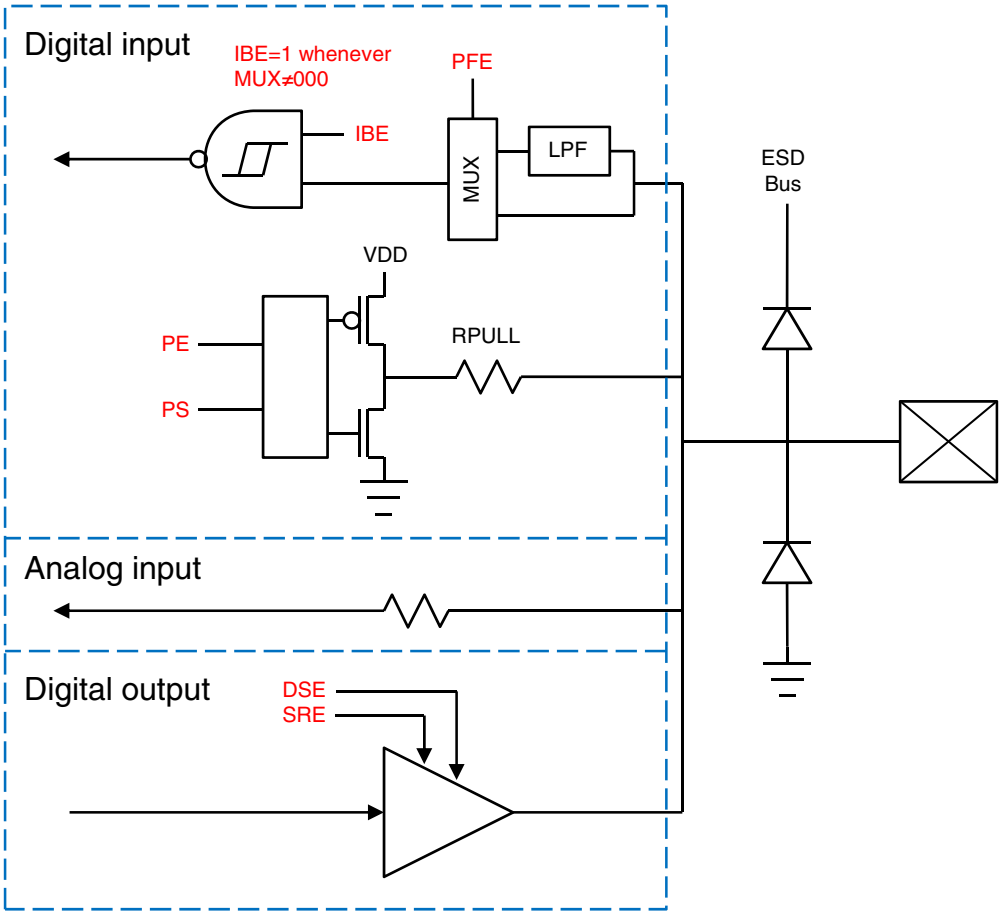

Figure 4. I/O simplified block diagram

The PORT module has the following features:

- all PIN support interrupt enable .
- Configurable edge(rising,falling,both) or level sensitive interrupt type
- Support DMA request
- Asynchronous wake-up in low-power modes
- Configurable pullup, pulldown, and pull-disable on select pins
- Configurable high and low drive strength on selected pins
- Configurable fast and slow slew rates on selected pins
- Configurable passive filter on selected pins
- Individual mux control field supporting analog or pin disabled, GPIO, and up to chip-specific digital functions
- Pad configuration fields are functional in all digital pin muxing modes.

The GPIO module has the following features:

- Port Data Input register visible in all digital pin-multiplexing modes
- Port Data Output register with corresponding set/clear/toggle registers

64 LQFP	36 XFBGA	32 QFN	48 QFN	64 MAPBGA	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
37	—	—	29	E7	PTB2	ADC0_SE12	ADC0_SE12	PTB2	I2C0_SCL	TPM2_CH0				
38	—	—	30	E8	PTB3	ADC0_SE13	ADC0_SE13	PTB3	I2C0_SDA	TPM2_CH1				
39	—	—	31	E6	PTB16	DISABLED		PTB16	SPI1_MOSI	LPUART0_RX	TPM_CLKIN0	SPI1_MISO		
40	—	—	32	D7	PTB17	DISABLED		PTB17	SPI1_MISO	LPUART0_TX	TPM_CLKIN1	SPI1_MOSI		
41	—	—	—	D6	PTB18	DISABLED		PTB18		TPM2_CH0				
42	—	—	—	C7	PTB19	DISABLED		PTB19		TPM2_CH1				
43	—	—	33	D8	PTC0	ADC0_SE14	ADC0_SE14	PTC0		EXTRG_IN		CMP0_OUT		
44	C5	22	34	C6	PTC1/LLWU_P6/RTC_CLKIN	ADC0_SE15	ADC0_SE15	PTC1/LLWU_P6/RTC_CLKIN	I2C1_SCL		TPM0_CH0			
45	B6	23	35	B7	PTC2	ADC0_SE11	ADC0_SE11	PTC2	I2C1_SDA		TPM0_CH1			
46	B5	24	36	C8	PTC3/LLWU_P7	DISABLED		PTC3/LLWU_P7	SPI1_SCK	LPUART1_RX	TPM0_CH2	CLKOUT		
47	—	—	—	E3	VSS	VSS	VSS							
48	—	—	—	E4	VDD	VDD	VDD							
49	A6	25	37	B8	PTC4/LLWU_P8	DISABLED		PTC4/LLWU_P8	SPI0_PCS0	LPUART1_TX	TPM0_CH3	SPI1_PCS0		
50	A5	26	38	A8	PTC5/LLWU_P9	DISABLED		PTC5/LLWU_P9	SPI0_SCK	LPTMR0_ALT2			CMP0_OUT	
51	B4	27	39	A7	PTC6/LLWU_P10	CMP0_IN0	CMP0_IN0	PTC6/LLWU_P10	SPI0_MOSI	EXTRG_IN		SPI0_MISO		
52	A4	28	40	B6	PTC7	CMP0_IN1	CMP0_IN1	PTC7	SPI0_MISO			SPI0_MOSI		
53	—	—	—	A6	PTC8	CMP0_IN2	CMP0_IN2	PTC8	I2C0_SCL	TPM0_CH4				
54	—	—	—	B5	PTC9	CMP0_IN3	CMP0_IN3	PTC9	I2C0_SDA	TPM0_CH5				
55	—	—	—	B4	PTC10	DISABLED		PTC10	I2C1_SCL					
56	—	—	—	A5	PTC11	DISABLED		PTC11	I2C1_SDA					
57	—	—	41	C3	PTD0	DISABLED		PTD0	SPI0_PCS0		TPM0_CH0		FXIO0_D0	
58	—	—	42	A4	PTD1	ADC0_SE5b	ADC0_SE5b	PTD1	SPI0_SCK		TPM0_CH1		FXIO0_D1	
59	—	—	43	C2	PTD2	DISABLED		PTD2	SPI0_MOSI	UART2_RX	TPM0_CH2	SPI0_MISO	FXIO0_D2	
60	—	—	44	B3	PTD3	DISABLED		PTD3	SPI0_MISO	UART2_TX	TPM0_CH3	SPI0_MOSI	FXIO0_D3	
61	A3	29	45	A3	PTD4/LLWU_P14	DISABLED		PTD4/LLWU_P14	SPI1_PCS0	UART2_RX	TPM0_CH4		FXIO0_D4	
62	B3	30	46	C1	PTD5	ADC0_SE6b	ADC0_SE6b	PTD5	SPI1_SCK	UART2_TX	TPM0_CH5		FXIO0_D5	
63	B2	31	47	B2	PTD6/LLWU_P15	ADC0_SE7b	ADC0_SE7b	PTD6/LLWU_P15	SPI1_MOSI	LPUART0_RX	I2C1_SDA	SPI1_MISO	FXIO0_D6	

64 LQFP	36 XFBGA	32 QFN	48 QFN	64 MAPBGA	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
64	A2	32	48	A2	PTD7	DISABLED		PTD7	SPI1_MISO	LPUART0_TX	I2C1_SCL	SPI1_MOSI	FXIO0_D7	

4.2 Pin properties

The following table lists the pin properties.

64 LQFP	36 XFBGA	32 QFN	48 QFN	64 MAPBGA	Pin name	Driver strength	Default status after POR	Pullup/ pulldown setting after POR	Slew rate after POR	Passive pin filter after POR	Open drain	Pin interrupt
—	F2	9	—	—	VREF0	—	—	—	—	—	—	—
—	—	—	—	C5	NC	—	—	—	—	—	—	—
1	A1	1	—	A1	PTE0	ND	Hi-Z	—	FS	N	N	Y
2	B1	2	—	B1	PTE1	ND	Hi-Z	—	FS	N	N	Y
3	—	—	1	—	VDD	—	—	—	—	—	—	—
4	C4	—	2	C4	VSS	—	—	—	—	—	—	—
5	C2	3	3	E1	PTE16	ND	Hi-Z	—	FS	N	N	Y
6	C1	4	4	D1	PTE17	ND	HI-Z	—	FS	N	N	Y
7	D1	5	5	E2	PTE18	ND	Hi-Z	—	FS	N	N	Y
8	D2	6	6	D2	PTE19	ND	HI-Z	—	FS	N	N	Y
9	E3	—	7	G1	PTE20	ND	Hi-Z	—	SS	N	N	Y
10	E2	—	8	F1	PTE21	ND	Hi-Z	—	SS	N	N	Y
11	E1	—	—	G2	PTE22	ND	Hi-Z	—	SS	N	N	Y
12	F1	—	—	F2	PTE23	ND	Hi-Z	—	SS	N	N	Y
13	D3	7	9	F4	VDDA	—	—	—	—	—	—	—
14	D3	7	10	G4	VREFH	—	—	—	—	—	—	—
14	—	—	10	G4	VREFO	—	—	—	—	—	—	—
15	D4	8	11	G3	VREFL	—	—	—	—	—	—	—
16	D4	8	12	F3	VSSA	—	—	—	—	—	—	—
17	—	—	13	H1	PTE29	ND	Hi-Z	—	SS	N	N	Y

Table continues on the next page...

64 LQFP	36 XFBGA	32 QFN	48 QFN	64 MAPBGA	Pin name	Driver strength	Default status after POR	Pullup/ pulldown setting after POR	Slew rate after POR	Passive pin filter after POR	Open drain	Pin interrupt
18	F2	9	14	H2	PTE30	ND	Hi-Z	—	SS	N	N	Y
19	—	—	—	H3	PTE31	ND	Hi-Z	—	SS	N	N	Y
20	—	—	15	H4	PTE24	ND	Hi-Z	—	SS	N	N	Y
21	—	—	16	H5	PTE25	ND	Hi-Z	—	SS	N	N	Y
22	F3	10	17	D3	PTA0	ND	L	PD	SS	N	N	Y
23	F4	11	18	D4	PTA1	ND	Hi-Z	—	SS	N	N	Y
24	E4	12	19	E5	PTA2	ND	Hi-Z	—	SS	N	N	Y
25	E5	13	20	D5	PTA3	ND	H	PU	FS	N	N	Y
26	F5	14	21	G5	PTA4	ND	H	PU	SS	Y	N	Y
27	—	—	—	F5	PTA5	ND	Hi-Z	—	SS	N	N	Y
28	—	—	—	H6	PTA12	ND	Hi-Z	—	SS	N	N	Y
29	—	—	—	G6	PTA13	ND	Hi-Z	—	SS	N	N	Y
30	C3	15	22	G7	VDD	ND	—	—	—	—	—	—
31	C4	16	23	H7	VSS	ND	—	—	—	—	—	—
32	F6	17	24	H8	PTA18	ND	Hi-Z	—	SS	N	N	Y
33	E6	18	25	G8	PTA19	ND	Hi-Z	—	SS	N	N	Y
34	D5	19	26	F8	PTA20	ND	H	PU	SS	N	Y	Y
35	D6	20	27	F7	PTB0/LLWU_P5	HD	Hi-Z	—	FS	N	N	Y
36	C6	21	28	F6	PTB1	HD	Hi-Z	—	FS	N	N	Y
37	—	—	29	E7	PTB2	ND	Hi-Z	—	SS	N	N	Y
38	—	—	30	E8	PTB3	ND	Hi-Z	—	SS	N	N	Y
39	—	—	31	E6	PTB16	ND	Hi-Z	—	FS	N	N	Y
40	—	—	32	D7	PTB17	ND	Hi-Z	—	FS	N	N	Y
41	—	—	—	D6	PTB18	ND	Hi-Z	—	SS	N	N	Y
42	—	—	—	C7	PTB19	ND	Hi-Z	—	SS	N	N	Y
43	—	—	33	D8	PTC0	ND	Hi-Z	—	SS	N	N	Y
44	C5	22	34	C6	PTC1/ LLWU_P6/ RTC_CLKIN	ND	Hi-Z	—	SS	N	N	Y
45	B6	23	35	B7	PTC2	ND	Hi-Z	—	SS	N	N	Y

Table continues on the next page...

Table 26. LPUART1 signal descriptions

Chip signal name	Module signal name	Description	I/O
LPUART1_TX	TxD	Transmit data	I/O
LPUART1_RX	RxD	Receive data	I

Table 27. UART2 signal descriptions

Chip signal name	Module signal name	Description	I/O
UART2_TX	TxD	Transmit data	O
UART2_RX	RxD	Receive data	I

Table 28. FlexIO signal descriptions

Chip signal name	Module signal name	Description	I/O
FXIO0_Dx	FXIO_Dn (n=0...7)	Bidirectional FlexIO Shifter and Timer pin inputs/outputs	I/O

4.3.7 Human-machine interfaces (HMI)

Table 29. GPIO Signal Descriptions

Chip signal name	Module signal name	Description	I/O
PTA[31:0]	PORTA31–PORTA0	General-purpose input/output	I/O
PTB[31:0]	PORTB31–PORTB0	General-purpose input/output	I/O
PTC[11:0]	PORTC11–PORTC0	General-purpose input/output	I/O
PTD[7:0]	PORTD7–PORTD0	General-purpose input/output	I/O
PTE[31:0]	PORTE31–PORTE0	General-purpose input/output	I/O

4.4 KL17 Family Pinouts

The figure below shows the 32 QFN pinouts.

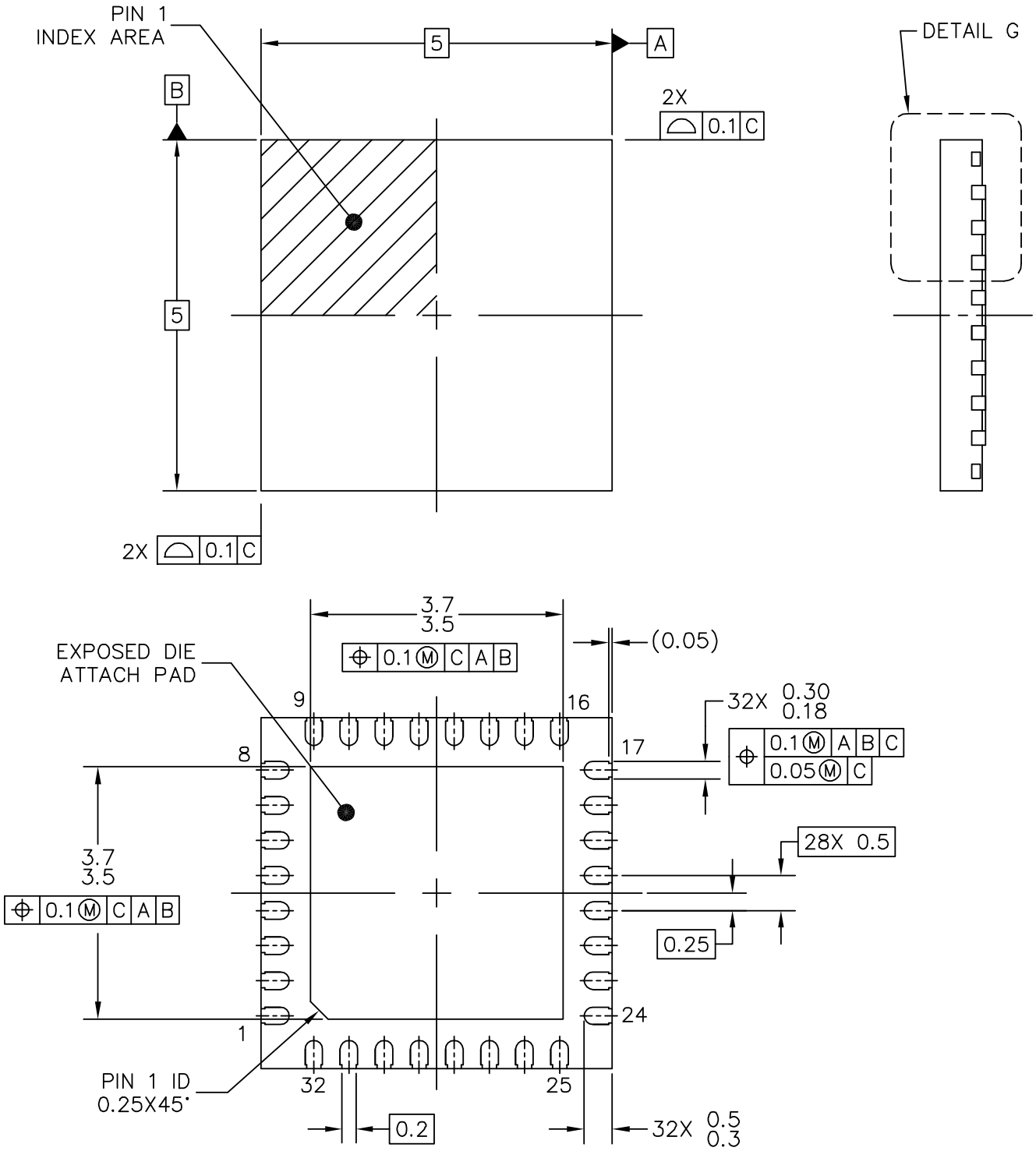

Figure 17. 32-pin QFN package dimension 1

5.2.2.5 Power consumption operating behaviors

The maximum values stated in the following table represent the characterized results equivalent to the mean plus three times the standard deviation (mean + 3 sigma).

NOTE

The while(1) test is executed with flash cache enabled.

Table 38. Power consumption operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I_{DDA}	Analog supply current	—	—	See note	mA	1
I_{DD_RUNCO}	Running CoreMark in flash in compute operation mode—48M HIRC mode, 48 MHz core / 24 MHz flash, V_{DD} = 3.0 V • at 25 °C • at 105 °C	—	4.79 4.94	4.98 5.14	mA	2
I_{DD_RUNCO}	Running While(1) loop in flash in compute operation mode—48M HIRC mode, 48 MHz core / 24 MHz flash, V_{DD} = 3.0 V • at 25 °C • at 105 °C	—	2.73 2.9	2.87 3.05	mA	
I_{DD_RUN}	Run mode current—48M HIRC mode, running CoreMark in Flash all peripheral clock disable 48 MHz core/24 MHz flash, V_{DD} = 3.0 V • at 25 °C • at 105 °C	— —	5.45 5.6	5.67 5.82	mA	2
I_{DD_RUN}	Run mode current—48M HIRC mode, running CoreMark in flash all peripheral clock disable, 24 MHz core/12 MHz flash, V_{DD} = 3.0 V • at 25 °C • at 105 °C	— —	3.41 3.56	3.55 3.70	mA mA	2
I_{DD_RUN}	Run mode current—48M HIRC mode, running CoreMark in Flash all peripheral clock disable 12 MHz core/6 MHz flash, V_{DD} = 3.0 V • at 25 °C • at 105 °C	—	2.37 2.52	2.49 2.65	mA	2
I_{DD_RUN}	Run mode current—48M HIRC mode, running CoreMark in Flash all peripheral clock enable 48 MHz core/24 MHz flash, V_{DD} = 3.0 V • at 25 °C • at 105 °C	—	7.05 7.2	7.33 7.49	mA	2

Table continues on the next page...

Table 38. Power consumption operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	• at 85 °C • at 105 °C					
I_{DD_VLLS3}	Very-low-leakage stop mode 3 current with RTC current, at 3.0 V • at 25 °C and below • at 50 °C • at 70 °C • at 85 °C • at 105 °C	 — — — — —	 1.83 2.47 3.96 6.44 13.84	 1.98 2.93 5.65 8.13 17.56	µA	3
I_{DD_VLLS3}	Very-low-leakage stop mode 3 current with RTC current, at 1.8 V • at 25 °C and below • at 50 °C • at 70 °C • at 85 °C • at 105 °C	 — — — — —	 1.68 2.27 3.66 5.97 12.92	 1.83 2.73 5.35 7.66 16.64	µA	3
I_{DD_VLLS1}	Very-low-leakage stop mode 1 current all peripheral disabled at 3.0 V • at 25 °C and below • at 50°C • at 70°C • at 85°C • at 105 °C	 — — — — —	 0.84 1.19 2.03 3.54 8.53	 1.06 1.33 2.62 4.13 9.98	µA	
I_{DD_VLLS1}	Very-low-leakage stop mode 1 current RTC enabled at 3.0 V • at 25 °C and below • at 50°C • at 70°C • at 85°C • at 105 °C	 — — — — —	 1.26 1.61 2.5 4.07 9	 1.48 1.75 3.09 4.66 10.45	µA	3
I_{DD_VLLS1}	Very-low-leakage stop mode 1 current RTC enabled at 1.8 V • at 25 °C and below • at 50°C • at 70°C • at 85°C • at 105 °C	 — — — — —	 1.08 1.42 2.21 3.59 8.02	 1.30 1.56 2.80 4.18 9.47	µA	3

Table continues on the next page...

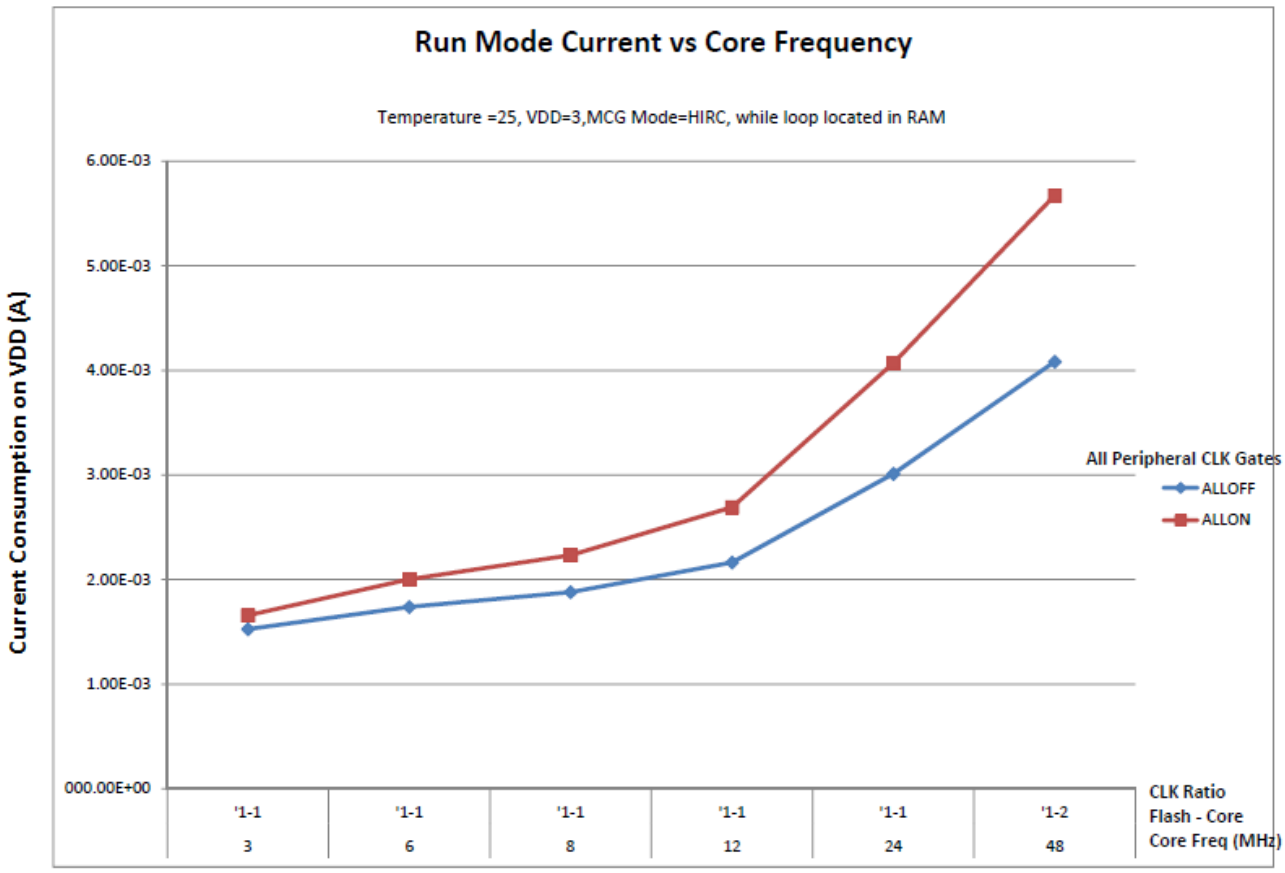
Run Mode Current vs Core Frequency
Temperature =25, VDD=3,MCG Mode=HIRC, while loop located in RAM
Current Consumption on VDD (A)
6.00E-03
5.00E-03
4.00E-03
3.00E-03
2.00E-03
1.00E-03
000.00E+00
All Peripheral CLK Gates
ALLOFF
ALLON
'1-1
3
'1-1
6
'1-1
8
'1-1
12
'1-1
24
'1-2
48
CLK Ratio
Flash - Core
Core Freq (MHz)

Table 53. NVM reliability specifications (continued)

Symbol	Description	Min.	Typ.[1]	Max.	Unit	Notes
$t_{nvmretp10k}$	Data retention after up to 10 K cycles	5	50	—	years	—
$t_{nvmretp1k}$	Data retention after up to 1 K cycles	20	100	—	years	—
$n_{nvmcycp}$	Cycling endurance	10 K	50 K	—	cycles	2

1. Typical data retention values are based on measured response accelerated at high temperature and derated to a constant 25 °C use profile. Engineering Bulletin EB618 does not apply to this technology. Typical endurance defined in Engineering Bulletin EB619.
2. Cycling endurance represents number of program/erase cycles at –40 °C ≤ T_j ≤ 125 °C.

5.3.5 Security and integrity modules

There are no specifications necessary for the device's security and integrity modules.

5.3.6 Analog

5.3.6.1 ADC electrical specifications

Using differential inputs can achieve better system accuracy than using single-end inputs.

5.3.6.1.1 16-bit ADC operating conditions

Table 54. 16-bit ADC operating conditions

Symbol	Description	Conditions	Min.	Typ.[1]	Max.	Unit	Notes
V_{DDA}	Supply voltage	Absolute	1.71	—	3.6	V	—
ΔV_{DDA}	Supply voltage	Delta to V_{DD} (V_{DD} – V_{DDA})	-100	0	+100	mV	2
ΔV_{SSA}	Ground voltage	Delta to V_{SS} (V_{SS} – V_{SSA})	-100	0	+100	mV	2
V_{ADIN}	Input voltage	• 16-bit differential mode • All other modes	VREFL VREFL	— —	31/32 × VREFH VREFH	V	—
C_{ADIN}	Input capacitance	• 16-bit mode • 8-bit / 10-bit / 12-bit modes	— —	8 4	10 5	pF	—
R_{ADIN}	Input series resistance		—	2	5	kΩ	—
R_{AS}	Analog source resistance (external)	13-bit / 12-bit modes f_{ADCK} < 4 MHz	—	—	5	kΩ	3

Table continues on the next page...

5.3.6.1.2 16-bit ADC electrical characteristics

Table 55. 16-bit ADC characteristics (V_{REFH} = V_{DDA}, V_{REFL} = V_{SSA})

Symbol	Description	Conditions[1]	Min.	Typ.[2]	Max.	Unit	Notes
I_{DDA_ADC}	Supply current		0.215	—	1.7	mA	3
f_{ADACK}	ADC asynchronous clock source	• ADLPC = 1, ADHSC = 0 • ADLPC = 1, ADHSC = 1 • ADLPC = 0, ADHSC = 0 • ADLPC = 0, ADHSC = 1	1.2 2.4 3.0 4.4	2.4 4.0 5.2 6.2	3.9 6.1 7.3 9.5	MHz MHz MHz MHz	t_{ADACK} = $1/f_{ADACK}$
	Sample Time	See Reference Manual chapter for sample times					
TUE	Total unadjusted error	• 12-bit modes • <12-bit modes	— —	±2 ±1.4	±6.8 ±2.1	LSB[4]	5
DNL	Differential non-linearity	• 12-bit modes • <12-bit modes	— —	±0.7 ±0.2	–1.1 to +1.9 –0.3 to 0.5	LSB[4]	5
INL	Integral non-linearity	• 12-bit modes • <12-bit modes	— —	±0.9 ±0.4	–2.7 to +1.9 –0.7 to +0.5	LSB[4]	5
E_{FS}	Full-scale error	• 12-bit modes • <12-bit modes	— —	–4 –1.4	–5.4 –1.8	LSB[4]	V_{ADIN} = V_{DDA}[5]
E_Q	Quantization error	• 16-bit modes • ≤13-bit modes	— —	–1 to 0 —	— ±0.5	LSB[4]	
ENOB	Effective number of bits	16-bit differential mode • Avg = 32 • Avg = 4 16-bit single-ended mode • Avg = 32 • Avg = 4	 12.8 11.9 12.2 11.4	 14.5 13.8 13.9 13.1	 — — — —	 bits bits bits bits	6
SINAD	Signal-to-noise plus distortion	See ENOB	6.02 × ENOB + 1.76			dB	
THD	Total harmonic distortion	16-bit differential mode • Avg = 32 16-bit single-ended mode	 — —	 –94 –85	 — —	 dB dB	7

Table continues on the next page...

is required as a filter. Do not connect any other supply voltage to the pin that has VREFO activated.

6.1.3 Analog design

Each ADC input must have an RC filter as shown in the following figure. The maximum value of R must be RAS max if fast sampling and high resolution are required. The value of C must be chosen to ensure that the RC time constant is very small compared to the sample period.

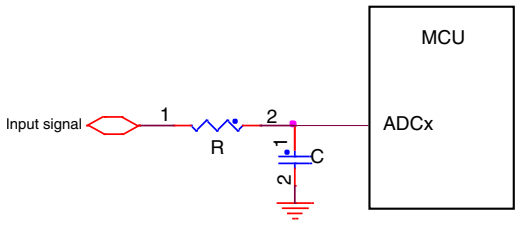

Figure 34. RC circuit for ADC input

High voltage measurement circuits require voltage division, current limiting, and over-voltage protection as shown the following figure. The voltage divider formed by R1 – R4 must yield a voltage less than or equal to VREFH. The current must be limited to less than the injection current limit. Since the ADC pins do not have diodes to VDD, external clamp diodes must be included to protect against transient over-voltages.

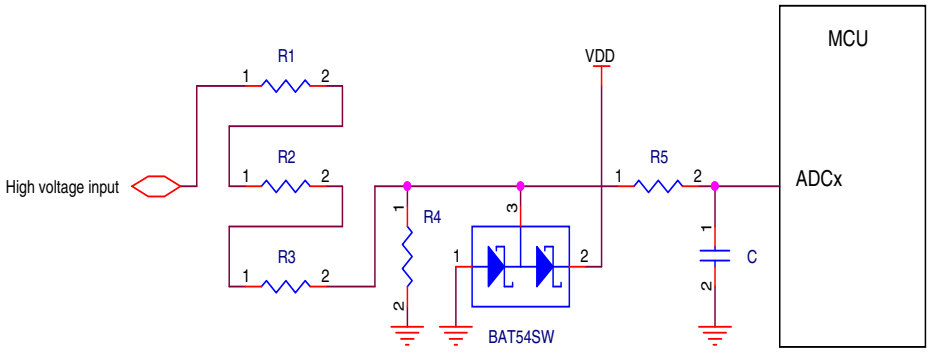

Figure 35. High voltage measurement with an ADC input

6.1.4 Digital design

Ensure that all I/O pins cannot get pulled above VDD (Max I/O is VDD+0.3V).

CAUTION

Do not provide power to I/O pins prior to VDD, especially the RESET_b pin.

- RESET_b pin

  The RESET_b pin is an open-drain I/O pin that has an internal pullup resistor. An external RC circuit is recommended to filter noise as shown in the following figure. The resistor value must be in the range of 4.7 kΩ to 10 kΩ; the recommended capacitance value is 0.1 µF. The RESET_b pin also has a selectable digital filter to reject spurious noise.

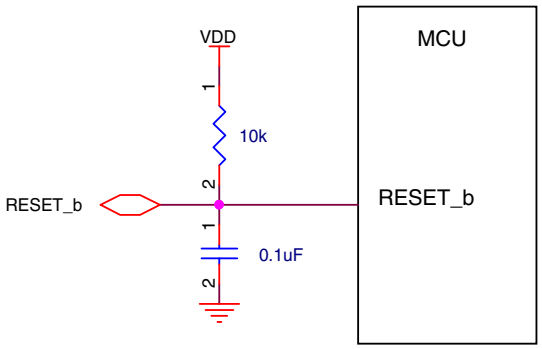

Figure 36. Reset circuit

When an external supervisor chip is connected to the RESET_b pin, a series resistor must be used to avoid damaging the supervisor chip or the RESET_b pin, as shown in the following figure. The series resistor value (RS below) must be in the range of 100 Ω to 1 kΩ depending on the external reset chip drive strength. The supervisor chip must have an active high, open-drain output.

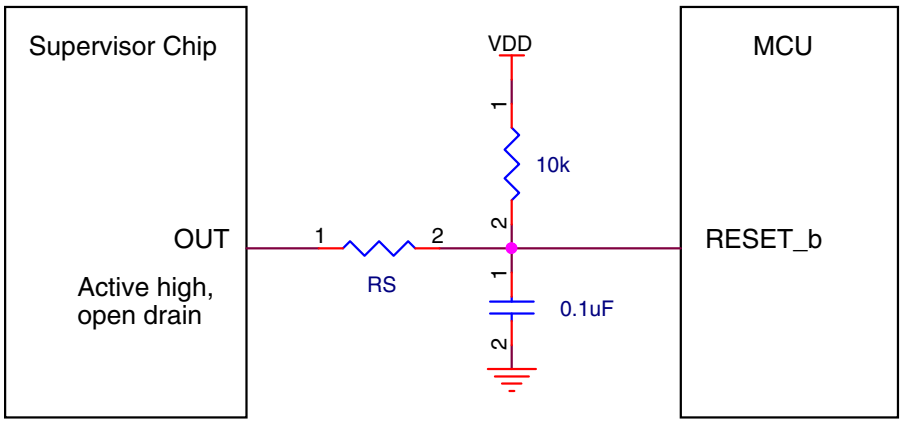

Figure 37. Reset signal connection to external reset chip

- NMI pin

  Do not add a pull-down resistor or capacitor on the NMI_b pin, because a low level on this pin will trigger non-maskable interrupt. When this pin is enabled as the NMI function, an external pull-up resistor (10 kΩ) as shown in the following figure is recommended for robustness.

  If the NMI_b pin is used as an I/O pin, the non-maskable interrupt handler is required to disable the NMI function by remapping to another function. The NMI function is disabled by programming the FOPT[NMI_DIS] bit to zero.

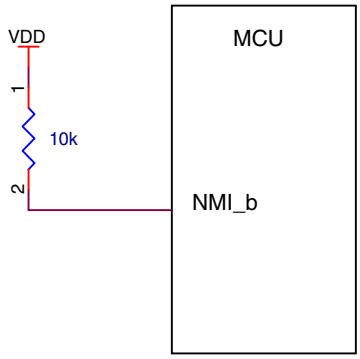

Figure 38. NMI pin biasing

- Debug interface

  This MCU uses the standard ARM SWD interface protocol as shown in the following figure. While pull-up or pull-down resistors are not required (SWD_DIO has an internal pull-up and SWD_CLK has an internal pull-down), external 10 kΩ pull resistors are recommended for system robustness. The RESET_b pin recommendations mentioned above must also be considered.

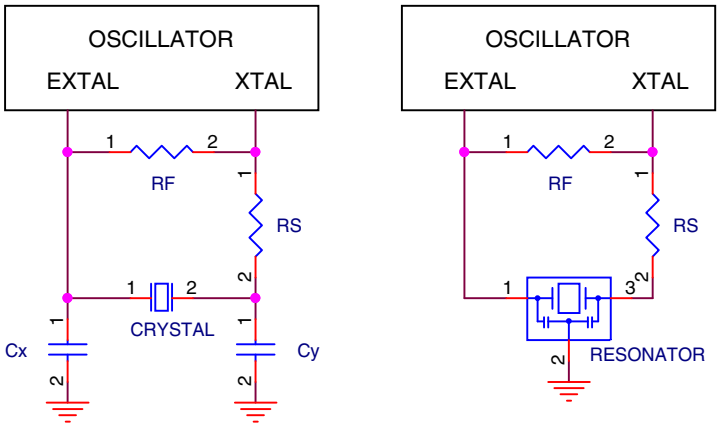

Figure 43. Crystal connection – Diagram 4

6.2 Software considerations

All Kinetis MCUs are supported by comprehensive Freescale and third-party hardware and software enablement solutions, which can reduce development costs and time to market. Featured software and tools are listed below. Visit http://www.freescale.com/kinetis/sw for more information and supporting collateral.

Evaluation and Prototyping Hardware

- Freescale Freedom Development Platform: http://www.freescale.com/freedom
- Tower System Development Platform: http://www.freescale.com/tower

IDEs for Kinetis MCUs

- Kinetis Design Studio IDE: http://www.freescale.com/kds
- Partner IDEs: http://www.freescale.com/kide

Development Tools

- PEG Graphics Software: http://www.freescale.com/peg
- Processor Expert Software and Embedded Components: http://www.freescale.com/processorexpert)

Run-time Software

- Kinetis SDK: http://www.freescale.com/ksdk
- Kinetis Bootloader: http://www.freescale.com/kboot
- ARM mbed Development Platform: http://www.freescale.com/mbed
- MQX RTOS: http://www.freescale.com/mqx

For all other partner-developed software and tools, visit http://www.freescale.com/partners.

7 Part identification

7.1 Description

Part numbers for the chip have fields that identify the specific part. You can use the values of these fields to determine the specific part you have received.

7.2 Format

Part numbers for this device have the following format:

Q KL## A FFF R T PP CC N

7.3 Fields

This table lists the possible values for each field in the part number (not all combinations are valid):

Table 67. Part number fields description

Field	Description	Values
Q	Qualification status	• M = Fully qualified, general market flow • P = Prequalification
KL##	Kinetis family	• KL17
A	Key attribute	• Z = Cortex-M0+
FFF	Program flash memory size	• 32 = 32 KB • 64 = 64 KB
R	Silicon revision	• (Blank) = Main • A = Revision after main
T	Temperature range (°C)	• V = –40 to 105
PP	Package identifier	• FM = 32 QFN (5 mm x 5 mm) • FT = 48 QFN (7 mm x 7 mm)[1] • LH = 64 LQFP (10 mm x 10 mm) • MP = 64 MAPBGA (5 mm x 5 mm)[1] • DA = 36 XFBGA (3.5 mm x 3.5 mm)
CC	Maximum CPU frequency (MHz)	• 4 = 48 MHz

Table continues on the next page...

Table 67. Part number fields description (continued)

Field	Description	Values
N	Packaging type	• R = Tape and reel • (Blank) = Trays

1. This package for this product is not yet available. However, it is included in Package Your Way program for Kinetis MCUs. Visit freescale.com/KPYW for more details.

7.4 Example

This is an example part number:

MKL17Z64VLH4

8 Revision history

The following table provides a revision history for this document.

Table 68. Revision history

Rev. No.	Date	Substantial Changes
4	28 January/ 2015	Initial public release • Updated the features and completed the ordering information. • Updated Table 9 - Power consumption operating behaviors with Max. values. • Added a note before Table 9. • Updated Table 17 - IRC48M specifications. • Updated Table 28. VREF full-range (-40 – 105 °C) operating behaviors with Min., Max., and Typical values. • Added Table 36 - I^2C 1Mbit/s timing.
4.1	2 February/ 2015	• Moved the ordering information out of the front page to be a separate chapter. • Added Module signal description table and Package dimension sections.
5	21 April/2015	• 32-pin QFN package is now standard part, added Marking information and thermal attributes of this package • Added Overview chapter • Added Memory map chapter • Added Pin properties • Added a note to the t_{rd1all} in Flash timing specifications — commands • Added a note to the Maximum of f_{SCL} in the fast mode in Inter-Integrated Circuit Interface (I2C) timing • Added a footnote to the Δfirc48m_ol_hv in MCG-Lite specifications • Added Design considerations chapter