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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, IrDA, SD, SPI, UART/USART, USB, USB OTG
Peripherals	DMA, I²S, LVD, POR, PWM, WDT
Number of I/O	100
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 41x16b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mk63fn1m0vlq12r

Symbol	Description	Min.	Max.	Unit
V_{DD}	Digital supply voltage	–0.3	3.8	V
I_{DD}	Digital supply current	—	185	mA
V_{DIO}	Digital input voltage (except $\overline{\text{RESET}}$, EXTAL, and XTAL)	–0.3	5.5	V
V_{AIO}	Analog[1], $\overline{\text{RESET}}$, EXTAL, and XTAL input voltage	–0.3	V_{DD} + 0.3	V
I_D	Maximum current single pin limit (applies to all digital pins)	–25	25	mA
V_{DDA}	Analog supply voltage	V_{DD} – 0.3	V_{DD} + 0.3	V
V_{USB0_DP}	USB0_DP input voltage	–0.3	3.63	V
V_{USB0_DM}	USB0_DM input voltage	–0.3	3.63	V
V_{REGIN}	USB regulator input	–0.3	6.0	V
V_{BAT}	RTC battery supply voltage	–0.3	3.8	V

1. Analog pins are defined as pins that do not have an associated general purpose I/O port function.

2 General

2.1 AC electrical characteristics

Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured at the 20% and 80% points, as shown in the following figure.

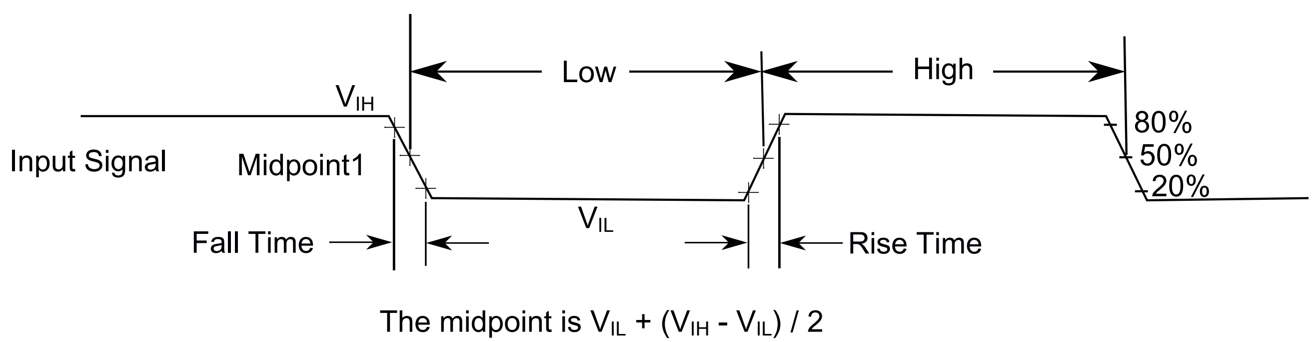

Figure 2. Input signal measurement reference

2.2 Nonswitching electrical specifications

Table 6. Power consumption operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	• @ 70°C • @ 105°C	—	114.9	196.49	μA	
I_{DD_VLLS3}	Very low-leakage stop mode 3 current at 3.0 V • @ –40 to 25°C • @ 70°C • @ 105°C	— — —	4.4 21 90.2	5.54 36.46 150.17	μA μA μA	
I_{DD_VLLS2}	Very low-leakage stop mode 2 current at 3.0 V • @ –40 to 25°C • @ 70°C • @ 105°C	— — —	2.1 6.84 29.4	2.34 10.36 46.74	μA μA μA	
I_{DD_VLLS1}	Very low-leakage stop mode 1 current at 3.0 V • @ –40 to 25°C • @ 70°C • @ 105°C	— — —	0.817 3.97 21.3	0.86 5.77 33.99	μA μA μA	
I_{DD_VLLS0}	Very low-leakage stop mode 0 current at 3.0 V with POR detect circuit enabled • @ –40 to 25°C • @ 70°C • @ 105°C	— — —	0.52 3.67 21.20	0.62 5.7 34.9	μA μA μA	
I_{DD_VLLS0}	Very low-leakage stop mode 0 current at 3.0 V with POR detect circuit disabled • @ –40 to 25°C • @ 70°C • @ 105°C	— — —	0.339 3.36 20.3	0.412 4.2 29.9	μA μA μA	

I_{DD_VBAT}	Average current with RTC and 32 kHz disabled
	• @ 1.8 V
	  • @ –40 to 25°C
	  • @ 70°C
	  • @ 105°C
	• @ 3.0 V
	  • @ –40 to 25°C
	  • @ 70°C
	  • @ 105°C
		—
		—
		—
		—
		—
		—
			0.16
			0.55
			2.5
			0.18
			0.66
			2.92
				0.19
				0.72
				3.68
				0.21
				0.86
				4.30
					μA
					μA
					μA
					μA
					μA
					μA	

I_{DD_VBAT}	Average current when CPU is not accessing RTC registers					10

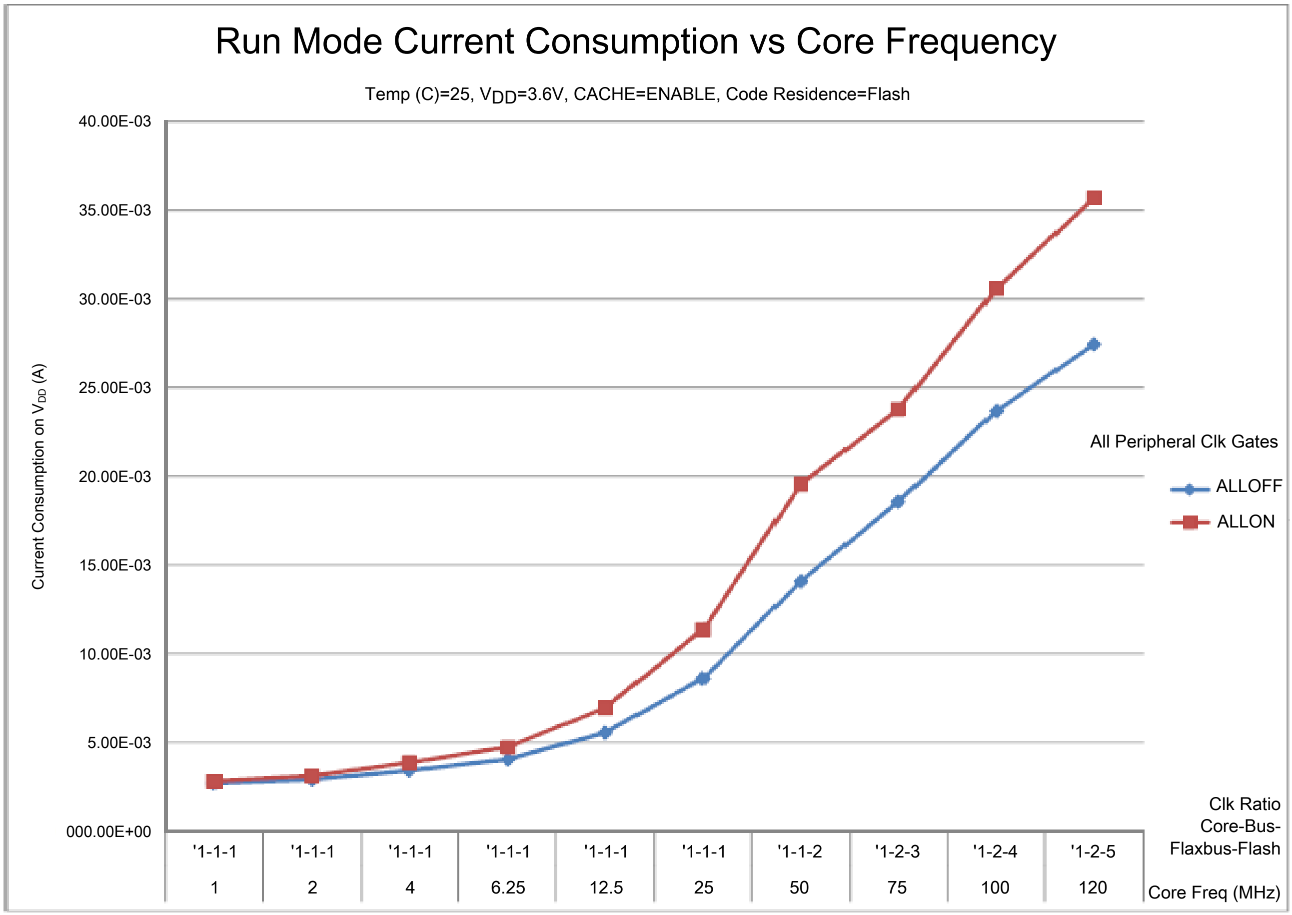

Figure 3. Run mode supply current vs. core frequency

Table 13. Thermal attributes

Board type	Symbol	Description	144 LQFP	144 MAPBGA	Unit	Notes
		outside center (natural convection)				

1. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air)*, or EIA/JEDEC Standard JESD51-6, *Integrated Circuit Thermal Test Method Environmental Conditions—Forced Convection (Moving Air)*.
2. Determined according to JEDEC Standard JESD51-8, *Integrated Circuit Thermal Test Method Environmental Conditions—Junction-to-Board*.
3. Determined according to Method 1012.1 of MIL-STD 883, *Test Method Standard, Microcircuits*, with the cold plate temperature used for the case temperature. The value includes the thermal resistance of the interface material between the top of the package and the cold plate.
4. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air)*.

3 Peripheral operating requirements and behaviors

3.1 Core modules

3.1.1 Debug trace timing specifications

Table 14. Debug trace operating behaviors

Symbol	Description	Min.	Max.	Unit
T_{cyc}	Clock period	Frequency dependent		MHz
T_{wl}	Low pulse width	2	—	ns
T_{wh}	High pulse width	2	—	ns
T_r	Clock and data rise time	—	3	ns
T_f	Clock and data fall time	—	3	ns
T_s	Data setup	1.5	—	ns
T_h	Data hold	1	—	ns

Table 15. JTAG limited voltage range electricals (continued)

Symbol	Description	Min.	Max.	Unit
J11	TCLK low to TDO data valid	—	17	ns
J12	TCLK low to TDO high-Z	—	17	ns
J13	$\overline{\text{TRST}}$ assert time	100	—	ns
J14	$\overline{\text{TRST}}$ setup time (negation) to TCLK high	8	—	ns

Table 16. JTAG full voltage range electricals

Symbol	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
J1	TCLK frequency of operation • Boundary Scan • JTAG and CJTAG • Serial Wire Debug	 0 0 0	 10 20 40	MHz
J2	TCLK cycle period	1/J1	—	ns
J3	TCLK clock pulse width • Boundary Scan • JTAG and CJTAG • Serial Wire Debug	 50 25 12.5	 — — —	 ns ns ns
J4	TCLK rise and fall times	—	3	ns
J5	Boundary scan input data setup time to TCLK rise	20	—	ns
J6	Boundary scan input data hold time after TCLK rise	0	—	ns
J7	TCLK low to boundary scan output data valid	—	25	ns
J8	TCLK low to boundary scan output high-Z	—	25	ns
J9	TMS, TDI input data setup time to TCLK rise	8	—	ns
J10	TMS, TDI input data hold time after TCLK rise	2.9	—	ns
J11	TCLK low to TDO data valid	—	22.1	ns
J12	TCLK low to TDO high-Z	—	22.1	ns
J13	$\overline{\text{TRST}}$ assert time	100	—	ns
J14	$\overline{\text{TRST}}$ setup time (negation) to TCLK high	8	—	ns

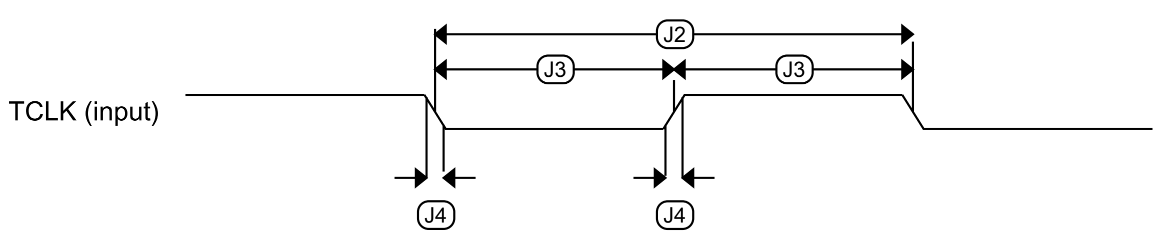

Figure 7. Test clock input timing

Table 17. MCG specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	• f_{vco} = 48 MHz	—	1350	—	ps	
	• f_{vco} = 120 MHz	—	600	—	ps	
D_{lock}	Lock entry frequency tolerance	± 1.49	—	± 2.98	%	
D_{unl}	Lock exit frequency tolerance	± 4.47	—	± 5.97	%	
t_{pll_lock}	Lock detector detection time	—	—	$150 \times 10^{-6} + 1075(1/f_{pll\_ref})$	s	10

1. This parameter is measured with the internal reference (slow clock) being used as a reference to the FLL (FEI clock mode).
2. 2 V <= VDD <= 3.6 V.
3. These typical values listed are with the slow internal reference clock (FEI) using factory trim and DMX32=0.
4. The resulting system clock frequencies should not exceed their maximum specified values. The DCO frequency deviation (Δf_{dco_t}) over voltage and temperature should be considered.
5. These typical values listed are with the slow internal reference clock (FEI) using factory trim and DMX32=1.
6. The resulting clock frequency must not exceed the maximum specified clock frequency of the device.
7. This specification applies to any time the FLL reference source or reference divider is changed, trim value is changed, DMX32 bit is changed, DRS bits are changed, or changing from FLL disabled (BLPE, BLPI) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.
8. Excludes any oscillator currents that are also consuming power while PLL is in operation.
9. This specification was obtained using a NXP developed PCB. PLL jitter is dependent on the noise characteristics of each PCB and results will vary.
10. This specification applies to any time the PLL VCO divider or reference divider is changed, or changing from PLL disabled (BLPE, BLPI) to PLL enabled (PBE, PEE). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

3.3.2 IRC48M specifications

Table 18. IRC48M specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{DD}	Supply voltage	1.71	—	3.6	V	
I_{DD48M}	Supply current	—	400	500	μA	
f_{irc48m}	Internal reference frequency	—	48	—	MHz	
$\Delta f_{irc48m\_ol\_lv}$	Open loop total deviation of IRC48M frequency at low voltage (VDD=1.71V-1.89V) over full temperature				$\%f_{irc48m}$	1
	• Regulator disable (USB_CLK_RECOVER_IRC_EN[REG_EN]=0)	—	± 0.5	± 1.5		
	• Regulator enable (USB_CLK_RECOVER_IRC_EN[REG_EN]=1)	—	± 0.5	± 2.0		
$\Delta f_{irc48m\_ol\_hv}$	Open loop total deviation of IRC48M frequency at high voltage (VDD=1.89V-3.6V) over full temperature				$\%f_{irc48m}$	1
	• Regulator enable (USB_CLK_RECOVER_IRC_EN[REG_EN]=1)	—	± 0.5	± 1.5		

Table continues on the next page...

Table 18. IRC48M specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$\Delta f_{irc48m\_ol\_hv}$	Open loop total deviation of IRC48M frequency at high voltage (VDD=1.89V-3.6V) over 0 to 85 °C • Regulator enable (USB_CLK_RECOVER_IRC_EN[REG_EN]=1)	—	± 0.5	± 1.0	$\%f_{irc48m}$	1
Δf_{irc48m_cl}	Closed loop total deviation of IRC48M frequency over voltage and temperature	—	—	± 0.1	$\%f_{host}$	2
J_{cyc_irc48m}	Period Jitter (RMS)	—	35	150	ps	
$t_{irc48mst}$	Startup time	—	2	3	μs	3

1. The maximum value represents characterized results equivalent to the mean plus or minus three times the standard deviation (mean ± 3 sigma)
2. Closed loop operation of the IRC48M is only feasible for USB device operation; it is not usable for USB host operation. It is enabled by configuring for USB Device, selecting IRC48M as USB clock source, and enabling the clock recover function (USB_CLK_RECOVER_IRC_CTRL[CLOCK_RECOVER_EN]=1, USB_CLK_RECOVER_IRC_EN[IRC_EN]=1).
3. IRC48M startup time is defined as the time between clock enablement and clock availability for system use. Enable the clock by setting USB_CLK_RECOVER_IRC_EN[IRC_EN]=1.

3.3.3 Oscillator electrical specifications

3.3.3.1 Oscillator DC electrical specifications

Table 19. Oscillator DC electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{DD}	Supply voltage	1.71	—	3.6	V	
I_{DDOSC}	Supply current — low-power mode (HGO=0)					1
	• 32 kHz	—	500	—	nA	
	• 4 MHz	—	200	—	μA	
	• 8 MHz (RANGE=01)	—	300	—	μA	
	• 16 MHz	—	950	—	μA	
	• 24 MHz	—	1.2	—	mA	
	• 32 MHz	—	1.5	—	mA	
I_{DDOSC}	Supply current — high-gain mode (HGO=1)					1
	• 32 kHz	—	25	—	μA	
	• 4 MHz	—	400	—	μA	
	• 8 MHz (RANGE=01)	—	500	—	μA	
	• 16 MHz	—	2.5	—	mA	
	• 24 MHz	—	3	—	mA	
	• 32 MHz	—	4	—	mA	

Table continues on the next page...

Table 19. Oscillator DC electrical specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
C_x	EXTAL load capacitance	—	—	—		2, 3
C_y	XTAL load capacitance	—	—	—		2, 3
R_F	Feedback resistor — low-frequency, low-power mode (HGO=0)	—	—	—	MΩ	2, 4
	Feedback resistor — low-frequency, high-gain mode (HGO=1)	—	10	—	MΩ	
	Feedback resistor — high-frequency, low-power mode (HGO=0)	—	—	—	MΩ	
	Feedback resistor — high-frequency, high-gain mode (HGO=1)	—	1	—	MΩ	
R_S	Series resistor — low-frequency, low-power mode (HGO=0)	—	—	—	kΩ	
	Series resistor — low-frequency, high-gain mode (HGO=1)	—	200	—	kΩ	
	Series resistor — high-frequency, low-power mode (HGO=0)	—	—	—	kΩ	
	Series resistor — high-frequency, high-gain mode (HGO=1)	—	0	—	kΩ	
V_{pp}[5]	Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, low-power mode (HGO=0)	—	0.6	—	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, high-gain mode (HGO=1)	—	V_{DD}	—	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, low-power mode (HGO=0)	—	0.6	—	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, high-gain mode (HGO=1)	—	V_{DD}	—	V	

1. V_{DD}=3.3 V, Temperature =25 °C
2. See crystal or resonator manufacturer's recommendation
3. C_x and C_y can be provided by using either integrated capacitors or external components.
4. When low-power mode is selected, R_F is integrated and must not be attached externally.
5. The EXTAL and XTAL pins should only be connected to required oscillator components and must not be connected to any other device.

Table 21. 32kHz oscillator DC electrical specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit
C_{para}	Parasitical capacitance of EXTAL32 and XTAL32	—	5	7	pF
V_{pp}[1]	Peak-to-peak amplitude of oscillation	—	0.6	—	V

1. When a crystal is being used with the 32 kHz oscillator, the EXTAL32 and XTAL32 pins should only be connected to required oscillator components and must not be connected to any other devices.

3.3.4.2 32 kHz oscillator frequency specifications

Table 22. 32 kHz oscillator frequency specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
f_{osc_lo}	Oscillator crystal	—	32.768	—	kHz	
t_{start}	Crystal start-up time	—	1000	—	ms	1
$f_{ec\_extal32}$	Externally provided input clock frequency	—	32.768	—	kHz	2
$v_{ec\_extal32}$	Externally provided input clock amplitude	700	—	V_{BAT}	mV	2, 3

1. Proper PC board layout procedures must be followed to achieve specifications.
2. This specification is for an externally supplied clock driven to EXTAL32 and does not apply to any other clock input. The oscillator remains enabled and XTAL32 must be left unconnected.
3. The parameter specified is a peak-to-peak value and V_{IH} and V_{IL} specifications do not apply. The voltage of the applied clock must be within the range of V_{SS} to V_{BAT}.

3.4 Memories and memory interfaces

3.4.1 Flash (FTFE) electrical specifications

This section describes the electrical characteristics of the FTFE module.

3.4.1.1 Flash timing specifications — program and erase

The following specifications represent the amount of time the internal charge pumps are active and do not include command overhead.

Table 23. NVM program/erase timing specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
t_{hvpgm8}	Program Phrase high-voltage time	—	7.5	18	μs	
$t_{hversscr}$	Erase Flash Sector high-voltage time	—	13	113	ms	1
$t_{hversblk512k}$	Erase Flash Block high-voltage time for 512 KB	—	416	3616	ms	1

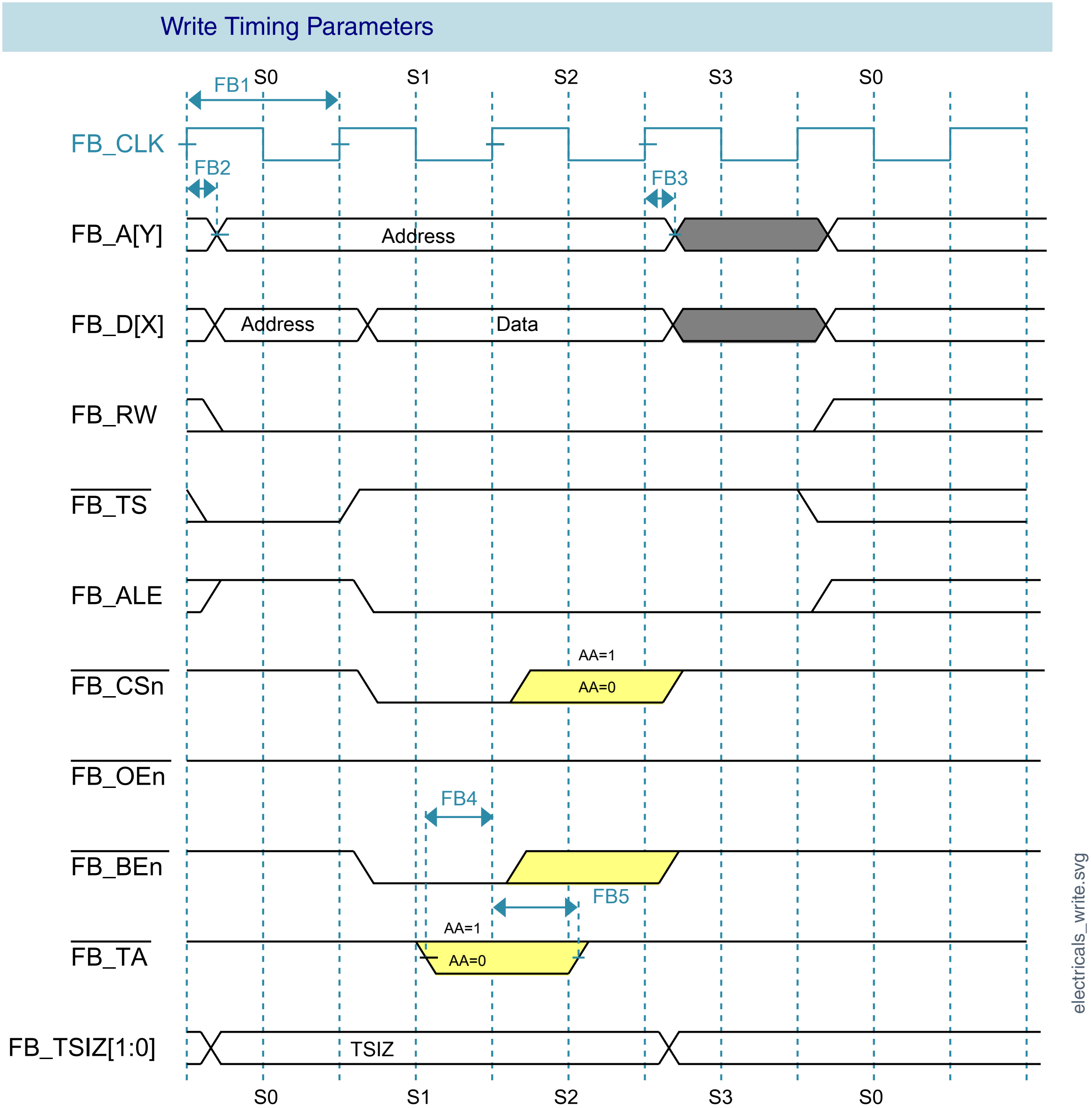

Figure 13. FlexBus write timing diagram

3.5 Security and integrity modules

3.5.1 DryIce Tamper Electrical Specifications

Information about security-related modules is not included in this document and is available only after a nondisclosure agreement (NDA) has been signed. To request an NDA, please contact your local NXP sales representative.

3.6 Analog

3.6.1 ADC electrical specifications

The 16-bit accuracy specifications listed in Table 30 and Table 31 are achievable on the differential pins ADCx_DP0, ADCx_DM0.

All other ADC channels meet the 13-bit differential/12-bit single-ended accuracy specifications.

3.6.1.1 16-bit ADC operating conditions

Table 30. 16-bit ADC operating conditions

Symbol	Description	Conditions	Min.	Typ.[1]	Max.	Unit	Notes
V_{DDA}	Supply voltage	Absolute	1.71	—	3.6	V	
ΔV_{DDA}	Supply voltage	Delta to V_{DD} ($V_{DD} - V_{DDA}$)	-100	0	+100	mV	2
ΔV_{SSA}	Ground voltage	Delta to V_{SS} ($V_{SS} - V_{SSA}$)	-100	0	+100	mV	2
V_{REFH}	ADC reference voltage high		1.13	V_{DDA}	V_{DDA}	V	
V_{REFL}	ADC reference voltage low		V_{SSA}	V_{SSA}	V_{SSA}	V	
V_{ADIN}	Input voltage		V_{REFL}	—	V_{REFH}	V	
C_{ADIN}	Input capacitance	• 16-bit mode • 8-bit / 10-bit / 12-bit modes	— —	8 4	10 5	pF	
R_{ADIN}	Input series resistance		—	2	5	kΩ	
R_{AS}	Analog source resistance (external)	13-bit / 12-bit modes f_{ADCK} < 4 MHz	—	—	5	kΩ	3
f_{ADCK}	ADC conversion clock frequency	≤ 13-bit mode	1.0	—	18.0	MHz	4
f_{ADCK}	ADC conversion clock frequency	16-bit mode	2.0	—	12.0	MHz	4
C_{rate}	ADC conversion rate	≤ 13-bit modes No ADC hardware averaging Continuous conversions enabled, subsequent conversion time	20.000	—	818.330	ksps	5

Table continues on the next page...

Table 30. 16-bit ADC operating conditions (continued)

Symbol	Description	Conditions	Min.	Typ.[1]	Max.	Unit	Notes
C_{rate}	ADC conversion rate	16-bit mode No ADC hardware averaging Continuous conversions enabled, subsequent conversion time	37.037	—	461.467	ksps	5

1. Typical values assume V_{DDA} = 3.0 V, Temp = 25 °C, f_{ADCK} = 1.0 MHz, unless otherwise stated. Typical values are for reference only, and are not tested in production.
2. DC potential difference.
3. This resistance is external to MCU. To achieve the best results, the analog source resistance must be kept as low as possible. The results in this data sheet were derived from a system that had < 8 Ω analog source resistance. The R_{AS}/C_{AS} time constant should be kept to < 1 ns.
4. To use the maximum ADC conversion clock frequency, CFG2[ADHSC] must be set and CFG1[ADLPC] must be clear.
5. For guidelines and examples of conversion rate calculation, download the ADC calculator tool.

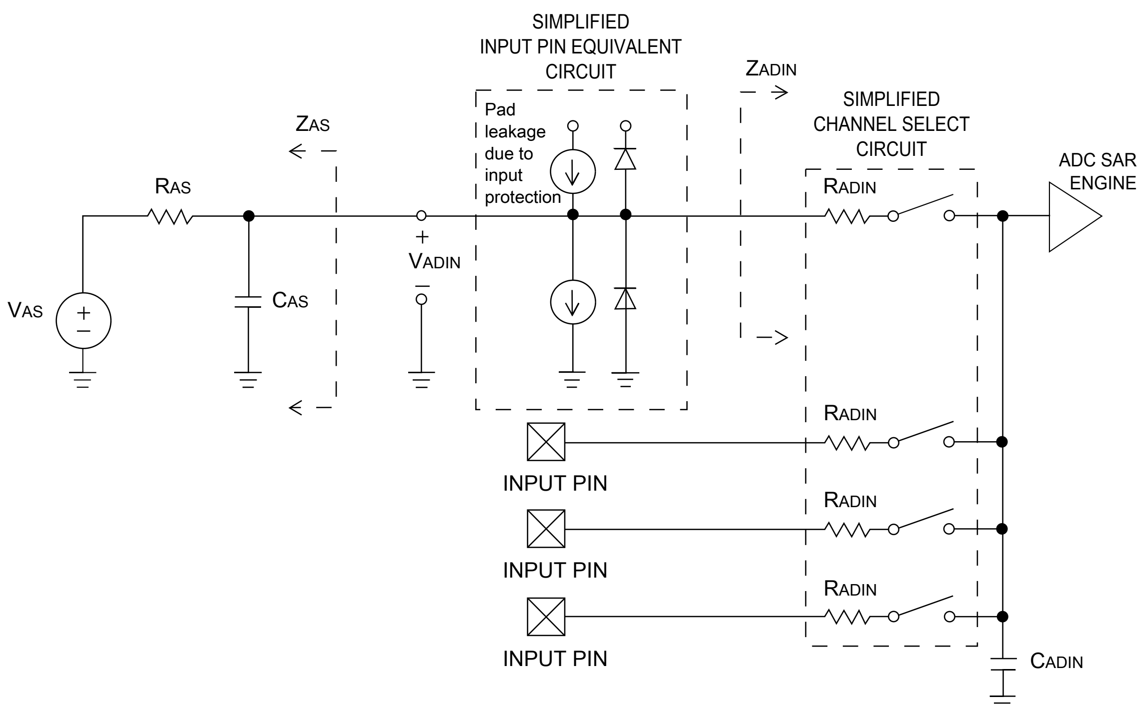

Figure 14. ADC input impedance equivalency diagram

3.6.1.2 16-bit ADC electrical characteristics

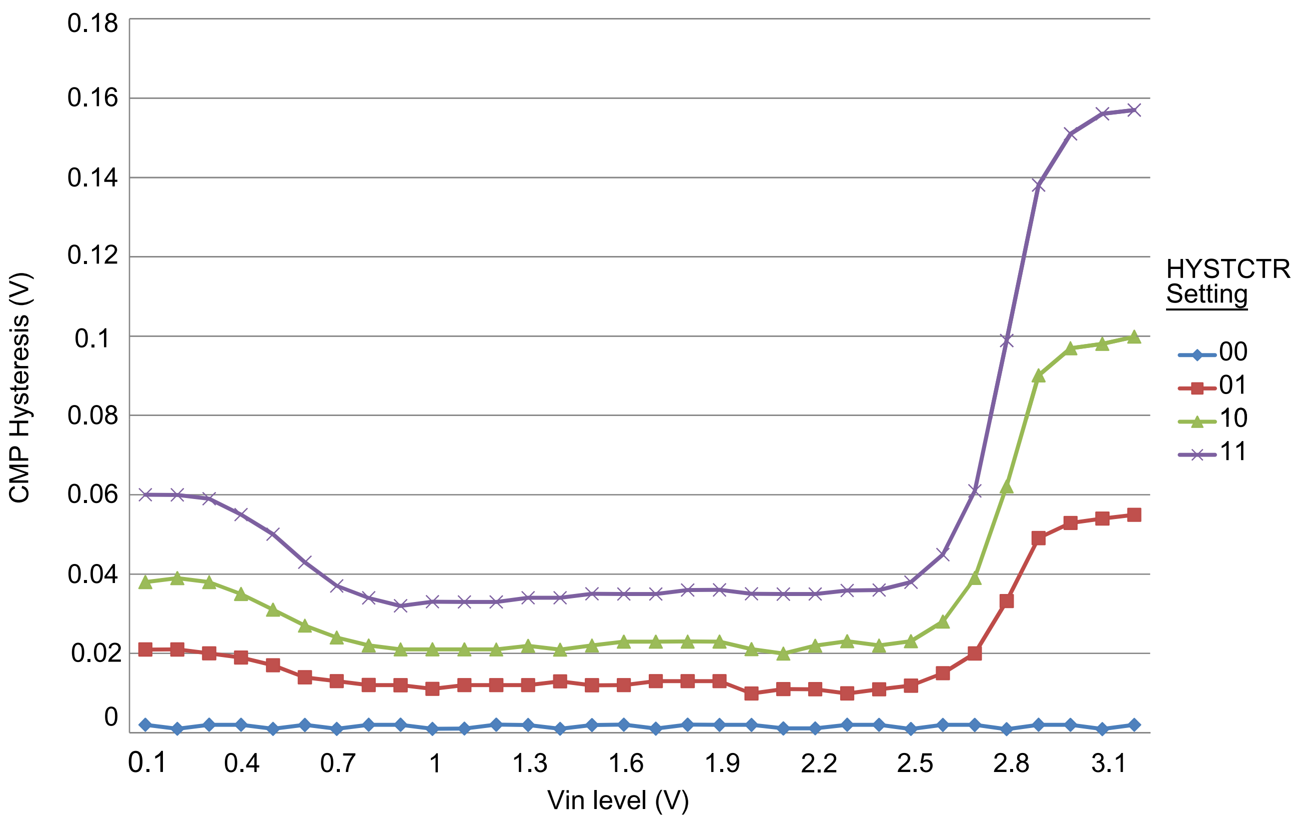

Figure 18. Typical hysteresis vs. Vin level (VDD = 3.3 V, PMODE = 1)

3.6.3 12-bit DAC electrical characteristics

3.6.3.1 12-bit DAC operating requirements

Table 33. 12-bit DAC operating requirements

Symbol	Desciption	Min.	Max.	Unit	Notes
V_{DDA}	Supply voltage	1.71	3.6	V	
V_{DACR}	Reference voltage	1.13	3.6	V	1
C_L	Output load capacitance	—	100	pF	2
I_L	Output load current	—	1	mA	

1. The DAC reference can be selected to be V_{DDA} or V_{REFH}.
2. A small load capacitance (47 pF) can improve the bandwidth performance of the DAC.

6. V_{DDA} = 3.0 V, reference select set for V_{DDA} (DACx_CO:DACRFS = 1), high power mode (DACx_C0:LPEN = 0), DAC set to 0x800, temperature range is across the full range of the device

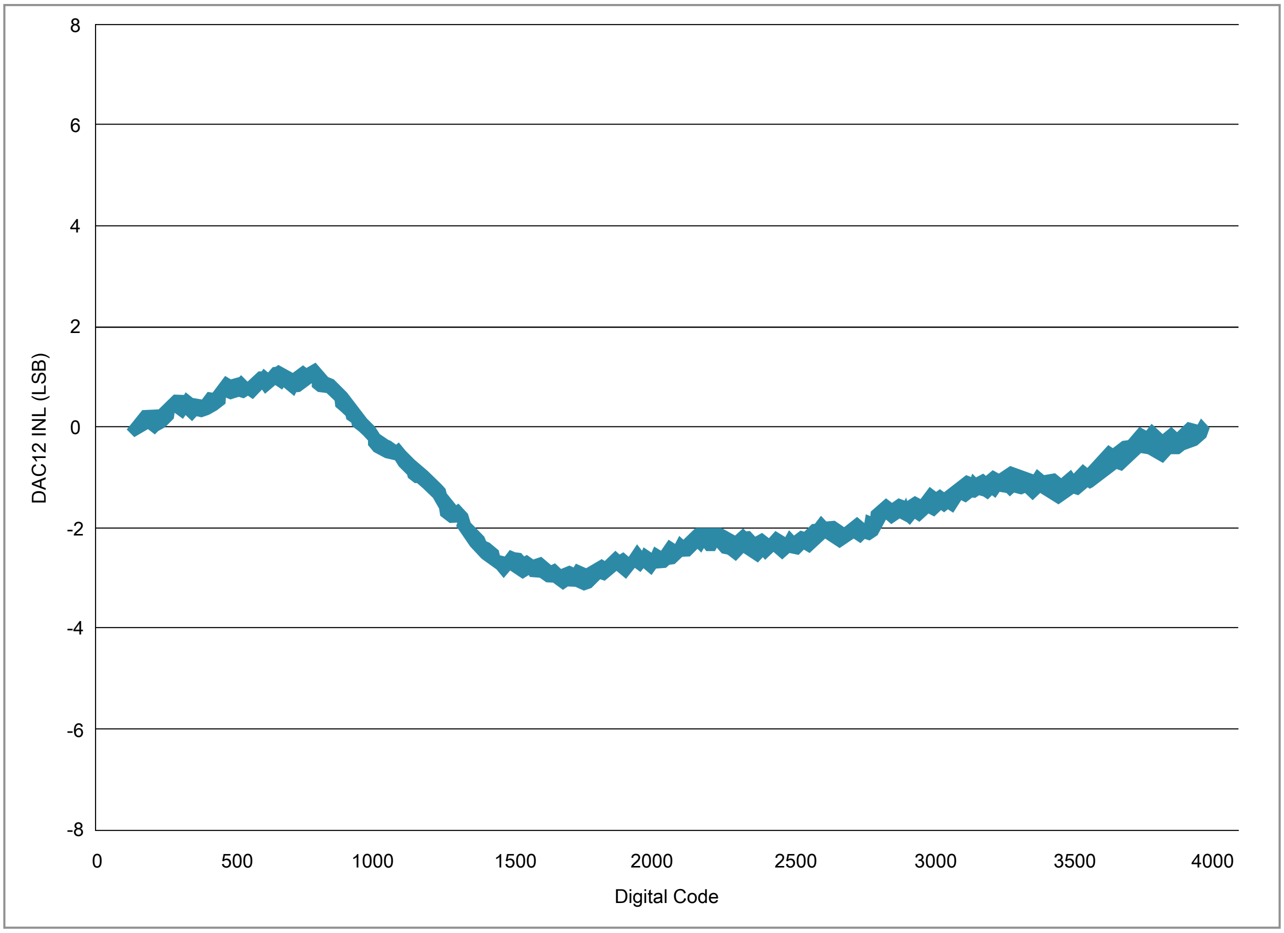

Figure 19. Typical INL error vs. digital code

3.8.6 DSPI switching specifications (limited voltage range)

The DMA Serial Peripheral Interface (DSPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The tables below provide DSPI timing characteristics for classic SPI timing modes. Refer to the DSPI chapter of the Reference Manual for information on the modified transfer formats used for communicating with slower peripheral devices.

Table 44. Master mode DSPI timing (limited voltage range)

Num	Description	Min.	Max.	Unit	Notes
	Operating voltage	2.7	3.6	V	
	Frequency of operation	—	30	MHz	
DS1	DSPI_SCK output cycle time	2 x t_{BUS}	—	ns	
DS2	DSPI_SCK output high/low time	(t_{SCK}/2) − 2	(t_{SCK}/2) + 2	ns	
DS3	DSPI_PCS*n* valid to DSPI_SCK delay	(t_{BUS} x 2) − 2	—	ns	1
DS4	DSPI_SCK to DSPI_PCS*n* invalid delay	(t_{BUS} x 2) − 2	—	ns	2
DS5	DSPI_SCK to DSPI_SOUT valid	—	8.5	ns	
DS6	DSPI_SCK to DSPI_SOUT invalid	−2	—	ns	
DS7	DSPI_SIN to DSPI_SCK input setup	15	—	ns	
DS8	DSPI_SCK to DSPI_SIN input hold	0	—	ns	

1. The delay is programmable in SPIx_CTARn[PSSCK] and SPIx_CTARn[CSSCK].
2. The delay is programmable in SPIx_CTARn[PASC] and SPIx_CTARn[ASC].

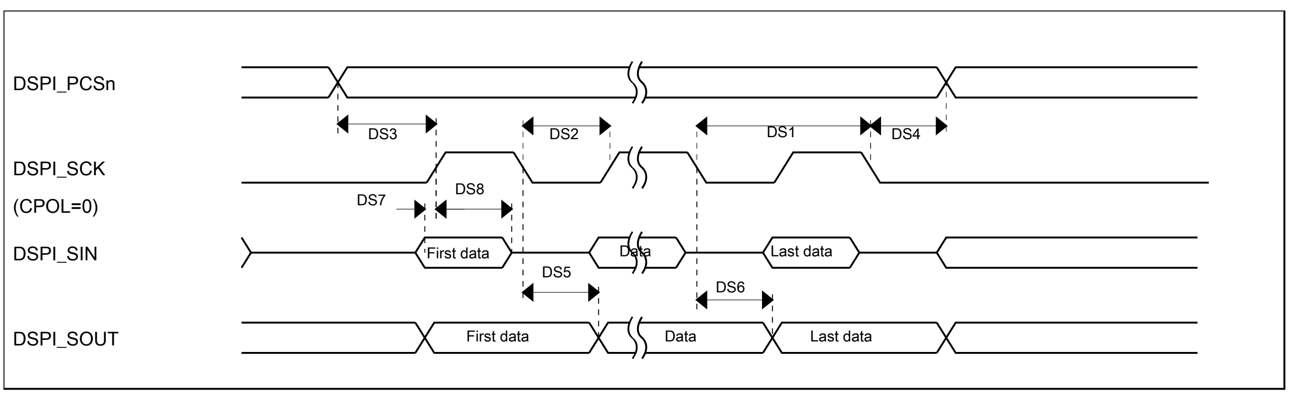

Figure 24. DSPI classic SPI timing — master mode

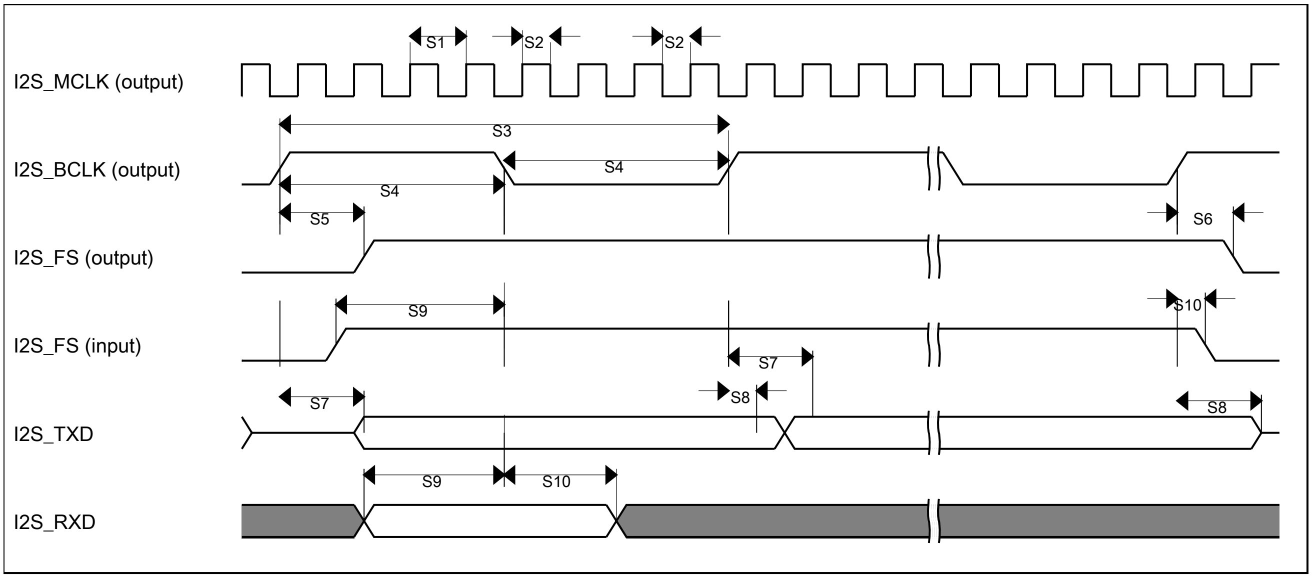

Figure 30. I²S timing — master mode

Table 52. I²S slave mode timing

Num	Description	Min.	Max.	Unit
	Operating voltage	2.7	3.6	V
S11	I2S_BCLK cycle time (input)	80	—	ns
S12	I2S_BCLK pulse width high/low (input)	45%	55%	MCLK period
S13	I2S_FS input setup before I2S_BCLK	5	—	ns
S14	I2S_FS input hold after I2S_BCLK	2	—	ns
S15	I2S_BCLK to I2S_TXD/I2S_FS output valid	—	19.5	ns
S16	I2S_BCLK to I2S_TXD/I2S_FS output invalid	0	—	ns
S17	I2S_RXD setup before I2S_BCLK	5	—	ns
S18	I2S_RXD hold after I2S_BCLK	2	—	ns
S19	I2S_TX_FS input assertion to I2S_TXD output valid[1]		21	ns

1. Applies to first bit in each frame and only if the TCR4[FSE] bit is clear

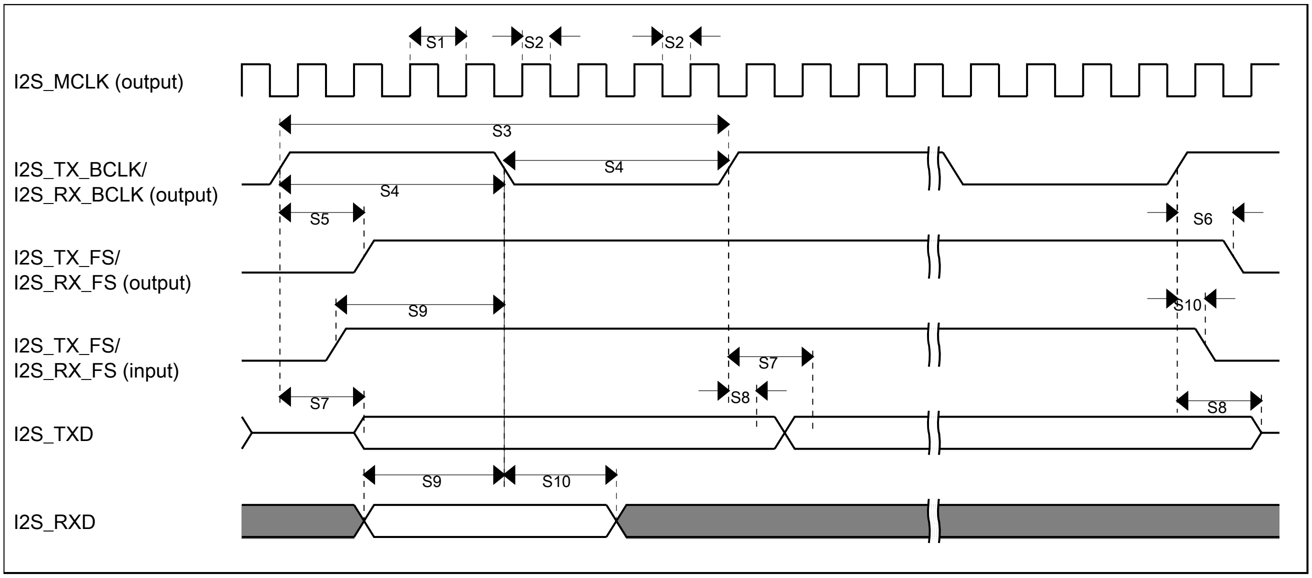

Figure 34. I2S/SAI timing — master modes

Table 56. I2S/SAI slave mode timing in VLPR, VLPW, and VLPS modes (full voltage range)

Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
S11	I2S_TX_BCLK/I2S_RX_BCLK cycle time (input)	250	—	ns
S12	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low (input)	45%	55%	MCLK period
S13	I2S_TX_FS/I2S_RX_FS input setup before I2S_TX_BCLK/I2S_RX_BCLK	30	—	ns
S14	I2S_TX_FS/I2S_RX_FS input hold after I2S_TX_BCLK/I2S_RX_BCLK	11	—	ns
S15	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output valid	—		ns
S16	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output invalid	0	—	ns
S17	I2S_RXD setup before I2S_RX_BCLK	30	—	ns
S18	I2S_RXD hold after I2S_RX_BCLK	11	—	ns
S19	I2S_TX_FS input assertion to I2S_TXD output valid[1]	—	72	ns

1. Applies to first bit in each frame and only if the TCR4[FSE] bit is clear

144 LQFP	144 MAP BGA	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
47	—	PTE26	DISABLED		PTE26	ENET_1588_ CLKIN	UART4_ CTS_b			RTC_ CLKOUT	USB_CLKIN	
48	—	PTE27	DISABLED		PTE27		UART4_ RTS_b					
49	—	PTE28	DISABLED		PTE28							
50	J5	PTA0	JTAG_TCLK/ SWD_CLK/ EZP_CLK		PTA0	UART0_ CTS_b/ UART0_ COL_b	FTM0_CH5				JTAG_TCLK/ SWD_CLK	EZP_CLK
51	J6	PTA1	JTAG_TDI/ EZP_DI		PTA1	UART0_RX	FTM0_CH6				JTAG_TDI	EZP_DI
52	K6	PTA2	JTAG_TDO/ TRACE_ SWO/ EZP_DO		PTA2	UART0_TX	FTM0_CH7				JTAG_TDO/ TRACE_ SWO	EZP_DO
53	K7	PTA3	JTAG_TMS/ SWD_DIO		PTA3	UART0_ RTS_b	FTM0_CH0				JTAG_TMS/ SWD_DIO	
54	L7	PTA4/ LLWU_P3	NMI_b/ EZP_CS_b		PTA4/ LLWU_P3		FTM0_CH1				NMI_b	EZP_CS_b
55	M8	PTA5	DISABLED		PTA5	USB_CLKIN	FTM0_CH2	RMII0_ RXER/ MII0_RXER	CMP2_OUT	I2S0_TX_ BCLK	JTAG_ TRST_b	
56	E7	VDD	VDD	VDD								
57	G7	VSS	VSS	VSS								
58	J7	PTA6	DISABLED		PTA6		FTM0_CH3				TRACE_ CLKOUT	
59	J8	PTA7	ADC0_SE10	ADC0_SE10	PTA7		FTM0_CH4				TRACE_D3	
60	K8	PTA8	ADC0_SE11	ADC0_SE11	PTA8		FTM1_CH0			FTM1_QD_ PHA	TRACE_D2	
61	L8	PTA9	DISABLED		PTA9		FTM1_CH1	MII0_RXD3		FTM1_QD_ PHB	TRACE_D1	
62	M9	PTA10	DISABLED		PTA10		FTM2_CH0	MII0_RXD2		FTM2_QD_ PHA	TRACE_D0	
63	L9	PTA11	DISABLED		PTA11		FTM2_CH1	MII0_RXCLK	I2C2_SDA	FTM2_QD_ PHB		
64	K9	PTA12	CMP2_IN0	CMP2_IN0	PTA12	CAN0_TX	FTM1_CH0	RMII0_ RXD1/ MII0_RXD1	I2C2_SCL	I2S0_TXD0	FTM1_QD_ PHA	
65	J9	PTA13/ LLWU_P4	CMP2_IN1	CMP2_IN1	PTA13/ LLWU_P4	CAN0_RX	FTM1_CH1	RMII0_ RXD0/ MII0_RXD0	I2C2_SDA	I2S0_TX_FS	FTM1_QD_ PHB	
66	L10	PTA14	DISABLED		PTA14	SPI0_PCS0	UART0_TX	RMII0_CRS_ DV/ MII0_RXDV	I2C2_SCL	I2S0_RX_ BCLK	I2S0_TXD1	

144 LQFP	144 MAP BGA	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
94	F5	VDD	VDD	VDD								
95	E10	PTB16	DISABLED		PTB16	SPI1_SOUT	UART0_RX	FTM_CLKIN0	FB_AD17	EWM_IN		
96	E9	PTB17	DISABLED		PTB17	SPI1_SIN	UART0_TX	FTM_CLKIN1	FB_AD16	EWM_OUT_b		
97	D12	PTB18	DISABLED		PTB18	CAN0_TX	FTM2_CH0	I2S0_TX_BCLK	FB_AD15	FTM2_QD_PHA		
98	D11	PTB19	DISABLED		PTB19	CAN0_RX	FTM2_CH1	I2S0_TX_FS	FB_OE_b	FTM2_QD_PHB		
99	D10	PTB20	DISABLED		PTB20	SPI2_PCS0			FB_AD31	CMP0_OUT		
100	D9	PTB21	DISABLED		PTB21	SPI2_SCK			FB_AD30	CMP1_OUT		
101	C12	PTB22	DISABLED		PTB22	SPI2_SOUT			FB_AD29	CMP2_OUT		
102	C11	PTB23	DISABLED		PTB23	SPI2_SIN	SPI0_PCS5		FB_AD28			
103	B12	PTC0	ADC0_SE14	ADC0_SE14	PTC0	SPI0_PCS4	PDB0_EXTRG	USB_SOF_OUT	FB_AD14	I2S0_TXD1		
104	B11	PTC1/LLWU_P6	ADC0_SE15	ADC0_SE15	PTC1/LLWU_P6	SPI0_PCS3	UART1_RTS_b	FTM0_CH0	FB_AD13	I2S0_TXD0		
105	A12	PTC2	ADC0_SE4b/CMP1_IN0	ADC0_SE4b/CMP1_IN0	PTC2	SPI0_PCS2	UART1_CTS_b	FTM0_CH1	FB_AD12	I2S0_TX_FS		
106	A11	PTC3/LLWU_P7	CMP1_IN1	CMP1_IN1	PTC3/LLWU_P7	SPI0_PCS1	UART1_RX	FTM0_CH2	CLKOUT	I2S0_TX_BCLK		
107	H8	VSS	VSS	VSS								
108	—	VDD	VDD	VDD								
109	A9	PTC4/LLWU_P8	DISABLED		PTC4/LLWU_P8	SPI0_PCS0	UART1_TX	FTM0_CH3	FB_AD11	CMP1_OUT		
110	D8	PTC5/LLWU_P9	DISABLED		PTC5/LLWU_P9	SPI0_SCK	LPTMR0_ALT2	I2S0_RXD0	FB_AD10	CMP0_OUT	FTM0_CH2	
111	C8	PTC6/LLWU_P10	CMP0_IN0	CMP0_IN0	PTC6/LLWU_P10	SPI0_SOUT	PDB0_EXTRG	I2S0_RX_BCLK	FB_AD9	I2S0_MCLK		
112	B8	PTC7	CMP0_IN1	CMP0_IN1	PTC7	SPI0_SIN	USB_SOF_OUT	I2S0_RX_FS	FB_AD8			
113	A8	PTC8	ADC1_SE4b/CMP0_IN2	ADC1_SE4b/CMP0_IN2	PTC8		FTM3_CH4	I2S0_MCLK	FB_AD7			
114	D7	PTC9	ADC1_SE5b/CMP0_IN3	ADC1_SE5b/CMP0_IN3	PTC9		FTM3_CH5	I2S0_RX_BCLK	FB_AD6	FTM2_FLT0		
115	C7	PTC10	ADC1_SE6b	ADC1_SE6b	PTC10	I2C1_SCL	FTM3_CH6	I2S0_RX_FS	FB_AD5			
116	B7	PTC11/LLWU_P11	ADC1_SE7b	ADC1_SE7b	PTC11/LLWU_P11	I2C1_SDA	FTM3_CH7	I2S0_RXD1	FB_RW_b			
117	A7	PTC12	DISABLED		PTC12		UART4_RTS_b		FB_AD27	FTM3_FLT0		
118	D6	PTC13	DISABLED		PTC13		UART4_CTS_b		FB_AD26			
119	C6	PTC14	DISABLED		PTC14		UART4_RX		FB_AD25			
120	B6	PTC15	DISABLED		PTC15		UART4_TX		FB_AD24			
121	—	VSS	VSS	VSS								

144 LQFP	144 MAP BGA	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
144	C1	PTD15	DISABLED		PTD15	SPI2_PCS1		SDHC0_D7		FB_A23		

5.2 Unused analog interfaces

Table 57. Unused analog interfaces

Module name	Pins	Recommendation if unused
ADC	ADC0_DP1, ADC0_DM1, ADC1_DP1, ADC1_DM1, ADC0_DP0/ADC1_DP3, ADC0_DM0/ADC1_DM3, ADC1_DP0/ADC0_DP3, ADC1_DM0/ADC0_DM3, ADC1_SE16/ADC0_SE22, ADC0_SE16/ADC0_SE21, ADC1_SE18	Ground
DAC [1]	DAC0_OUT, DAC1_OUT	Float
USB	VREGIN, USB0_GND, VOUT33[2]	Connect VREGIN and VOUT33 together and tie to ground through a 10 kΩ resistor. Do not tie directly to ground, as this causes a latch-up risk.
	USB0_DM, USB0_DP	Float

1. Unused DAC signals do not apply to all parts. See the Pinout section for details.
2. USB0_VBUS and USB0_GND are board level signals

5.3 K63 Pinouts

The below figure shows the pinout diagram for the devices supported by this document. Many signals may be multiplexed onto a single pin. To determine what signals can be used on which pin, see the previous section.